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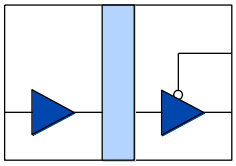
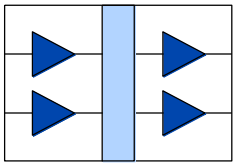
DC-Correct High Speed Digital Isolators

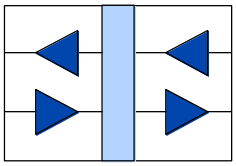
Functional Diagrams



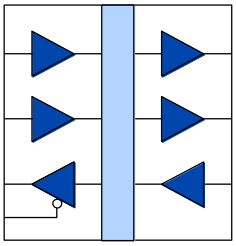
IL810



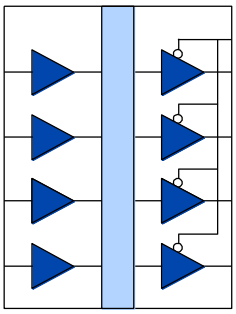
IL811



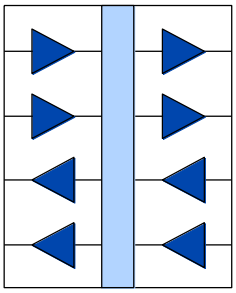
IL821



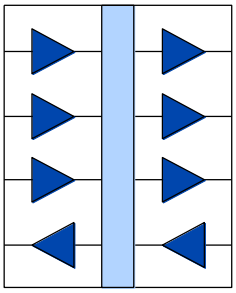
IL814



IL815



IL816



IL817

Features

- DC-correct
- −40ºC to 125ºC operating temperature
- 110 Mbps
- 10 ns propagation delay
- 1.3 mA/channel typical quiescent current
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- 600 V_{RMS} working voltage per VDE V 0884-10
- 44000 year barrier life
- 3 V to 5 V power supplies
- Low EMC footprint
- 8-pin MSOP and SOIC packages for one and two channels
- 16-pin QSOP, 0.15" SOIC, and 0.3" True 8™ SOIC for 3 and 4 channels
- IEC 60747-5-5 (VDE 0884) certified; UL 1577 recognized

Applications

- ADCs and DACs
- Digital Fieldbus
- RS-485 and RS-422
- Multiplexed data transmission
- Data interfaces
- Board-to-board communication
- Digital noise reduction
- Ground loop elimination
- Peripheral interfaces
- Parallel bus
- Logic level shifting

Description

IL800-Series isolators are high-speed, high temperature dc-correct isolators. An internal refresh clock ensures the outputs respond to dc states on inputs within a maximum of 9 µs.

The devices use NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

Absolute Maximum Ratings(1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	−55		150	°C	
Ambient Operating Temperature	T_A	−40		125	°C	
Supply Voltage	V_{DD1}, V_{DD2}	−0.5		7	V	
Input Voltage	V_I	−0.5		V_{DD}+0.5	V	
Output Voltage	V_O	−0.5		V_{DD}+0.5	V	
Output Current Drive	I_O			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	T_A	−40		125	°C	
Supply Voltage	V_{DD1}, V_{DD2}	3.0		5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times(10)	t_{IR}, t_{IF}	DC-Correct				

Insulation Specifications

Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)	MSOP QSOP 0.15" SOIC (8 or 16 pin) 0.3" SOIC		3.0 4.03 4.03 8.03	 8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)			0.012	0.013		mm	
Leakage Current				0.2		µA	240 V_{RMS}, 60 Hz
Barrier Resistance		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance		C_{IO}		4		pF	f = 1 MHz
Comparative Tracking Index		CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC DC	V_{IO}	1000 1500			V_{RMS} V_{DC}	At maximum operating temperature
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	QSOP 0.15" SOIC 0.3" SOIC	θ_{JA}		60 60 60		°C/W	Soldered to double-sided board; free air
Junction–Case (Top) Thermal Resistance	QSOP 0.15" SOIC 0.3" SOIC	Ψ_{JT}		10 10 20		°C/W	
Power Dissipation	QSOP 0.15" SOIC 0.3" SOIC	P_D			675 700 800	mW	

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Safety and Approvals

VDE V 0884-10 (VDE V 0884-11 pending; Basic Isolation; VDE File Number 5016933-4880-0001)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}) 4000 V_{PK}
- Surge rating 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)
Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-1	MSOP/QSOP	150 V_{RMS}
-3	SOIC	150 V_{RMS}
None	Wide-body SOIC/True 8™	300 V_{RMS}

UL 1577 (Component Recognition Program File Number E207481)
Each part tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

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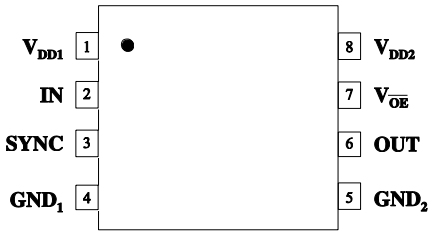
IL810-1/IL810-3 Pin Connections

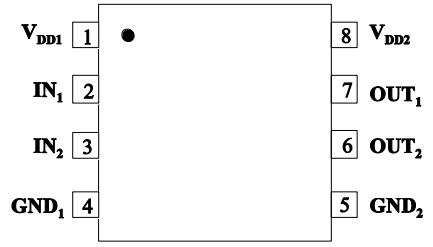
1	V_{DD1}	Supply voltage
2	IN	Data in
3	SYNC	Internal refresh clock disable (normally enabled and internally held low with 10 kΩ)
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT	Data out
7	$V_{\overline{OE}}$	Output enable (internally held low with 100 kΩ)
8	V_{DD2}	Supply voltage



IL810-1/IL810-3

IL811-1/IL811-3 Pin Connections

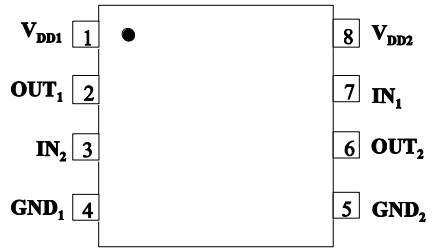
1	V_{DD1}	Supply voltage
2	IN_1	Data in, channel 1
3	IN_2	Data in, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT_2	Data out, channel 2
7	OUT_1	Data out, channel 1
8	V_{DD2}	Supply voltage



IL811-1/IL811-3

IL821-3 Pin Connections

1	V_{DD1}	Supply voltage
2	OUT_1	Data out, channel 1
3	IN_2	Data in, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT_2	Data out, channel 2
7	IN_1	Data in, channel 1
8	V_{DD2}	Supply voltage



IL821-3

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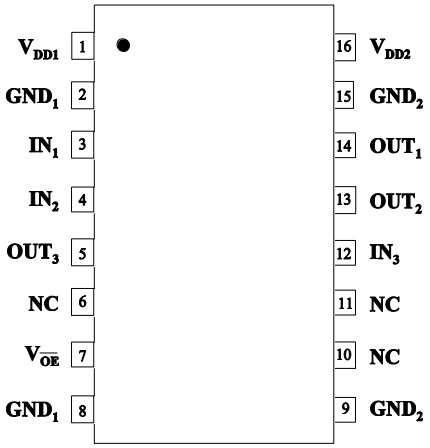
IL814-1/IL814-3/IL814 Pin Connections

1	V_{DD1}	Supply voltage 1
2	GND_1	Ground return for V_{DD1} (pin 2 internally connected to pin 8)
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	OUT_3	Data out, channel 3
6	NC	No connection
7	$V_{\overline{OE}}$	Output enable, channel 3 (internally held low with 100 kΩ)
8	GND_1	Ground return for V_{DD1} (pin 8 internally connected to pin 2)
9	GND_2	Ground return for V_{DD2} (pin 9 internally connected to pin 15)
10	NC	No connection
11	NC	No connection
12	IN_3	Data in, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2} (pin 15 internally connected to pin 9)
16	V_{DD2}	Supply voltage

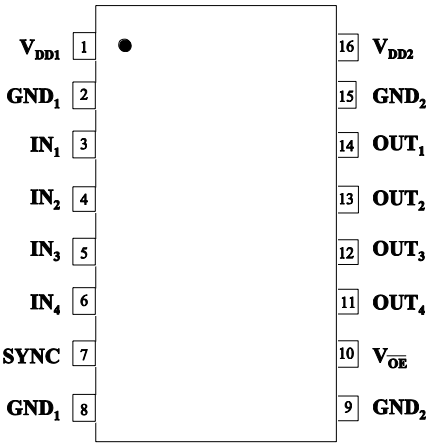


IL814-1/IL814-3/IL814

IL815-1/IL815-3/IL815 Pin Connections

1	V_{DD1}	Supply voltage
2	GND_1	Ground return for V_{DD1} (pin 2 internally connected to pin 8)
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	IN_3	Data in, channel 3
6	IN_4	Data in, channel 4
7	SYNC*	Internal refresh clock disable (normally enabled and internally held low with 10 kΩ)
8	GND_1	Ground return for V_{DD1} (pin 8 internally connected to pin 2)
9	GND_2	Ground return for V_{DD2} (pin 9 internally connected to pin 15)
10	$V_{\overline{OE}}$*	Output enable for all outputs (internally held low with 100 kΩ)
11	OUT_4	Data out, channel 4
12	OUT_3	Data out, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2} (pin 15 internally connected to pin 9)
16	V_{DD2}	Supply voltage

*Wide-body version (IL815TE) only.
No internal connections to pins 7 or 10
in QSOP or narrow-body (IL815T-1E or IL815T-3E) versions.



IL815-1/IL815-3/IL815

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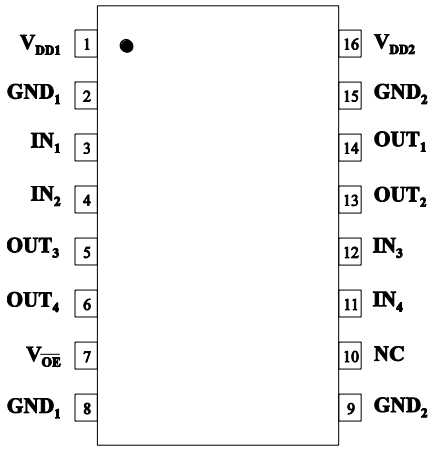
IL816-1/IL816-3/IL816 Pin Connections

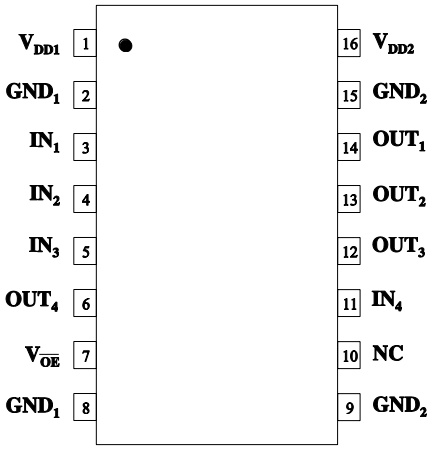
1	V_{DD1}	Supply voltage
2	GND_1	Ground return for V_{DD1} (pin 2 internally connected to pin 8)
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	OUT_3	Data out, channel 3
6	OUT_4	Data out, channel 4
7	$V_{\overline{OE}}$	Output enable, channels 3 and 4 (internally held low with 100 kΩ)
8	GND_1	Ground return for V_{DD1} (pin 8 internally connected to pin 2)
9	GND_2	Ground return for V_{DD2} (pin 9 internally connected to pin 15)
10	NC	No connection
11	IN_4	Data in, channel 4
12	IN_3	Data in, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2} (pin 15 internally connected to pin 9)
16	V_{DD2}	Supply voltage



IL816-1/IL816-3/IL816

IL817-3/IL817 Pin Connections

1	V_{DD1}	Supply voltage
2	GND_1	Ground return for V_{DD1} (pin 2 internally connected to pin 8)
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	IN_3	Data in, channel 3
6	OUT_4	Data out, channel 4
7	$V_{\overline{OE}}$	Output enable, channel 4 (internally held low with 100 kΩ)
8	GND_1	Ground return for V_{DD1} (pin 8 internally connected to pin 2)
9	GND_2	Ground return for V_{DD2} (pin 9 internally connected to pin 15)
10	NC	No connection
11	IN_4	Data in, channel 4
12	OUT_3	Data out, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2} (pin 15 internally connected to pin 9)
16	V_{DD2}	Supply voltage



IL817-3/IL817

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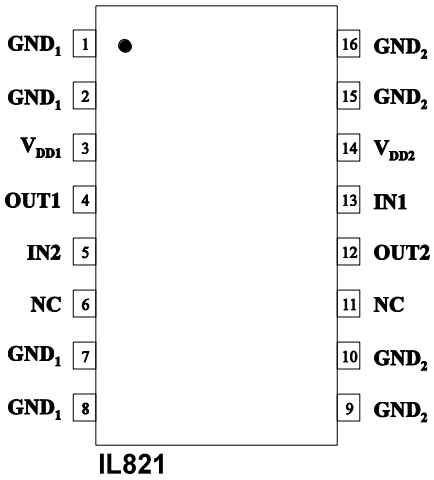
IL821 Pin Connections

1 2	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
3	V_{DD1}	Supply voltage
4	OUT_1	Data out, channel 1
5	IN_2	Data in, channel 2
6	NC	No connection
7 8	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
9 10	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)
11	NC	No connection
12	OUT_2	Data out, channel 2
13	IN_1	Data in, channel 1
14	V_{DD2}	Supply voltage
15 16	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)



IL821

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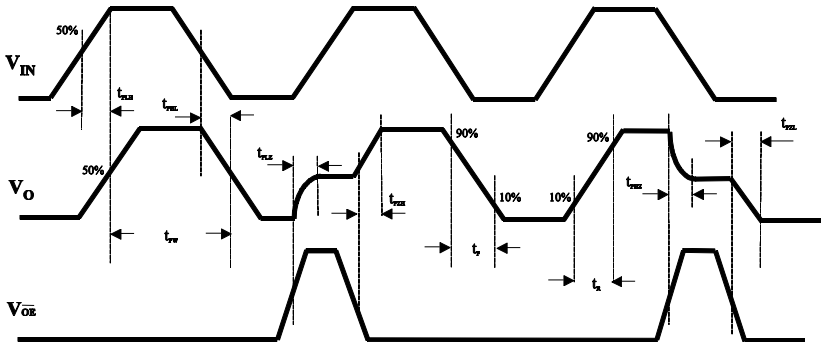
Timing Diagrams



Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_{PLZ}	Propagation Delay, Low to High Impedance
t_{PZH}	Propagation Delay, High Impedance to High
t_{PHZ}	Propagation Delay, High to High Impedance
t_{PZL}	Propagation Delay, High Impedance to Low
t_R	Rise Time
t_F	Fall Time

Truth Tables

Output Enable

V_I	$V_{\overline{OE}}$	V_O
L	L	L
H	L	H
L	H	Z
H	H	Z

SYNC

SYNC	Internal Refresh Clock
0	Enabled
1	Disabled

Note: SYNC should be left open or connected to GND to enable the internal refresh clock, or connected to V_{DD} to disable the internal clock.

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3.3 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current						
IL810, IL811, IL815	I_{DD1}		15	30	µA	
IL812, IL814, IL817, IL821			1.3	1.8	mA	
IL816			2.6	3.6	mA	
Output Quiescent Supply Current						
IL810, IL812, IL821	I_{DD2}		1.3	1.8	mA	
IL811, IL814, IL816			2.6	3.6	mA	
IL815			5.2	7.2	mA	
IL817			3.9	5.4	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} − 0.1	V_{DD}		V	I_O = −20 µA, V_I = V_{IH}
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.5	0.8		I_O = 4 mA, V_I = V_{IL}

Switching Specifications (V_{DD} = 3.3 V)						
Maximum Data Rate		100	110		Mbps	C_L = 15 pF
Pulse Width[7]	PW	10			ns	V_O 50% points;
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	C_L = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t_{PHZ}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t_{PLZ}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t_{PZH}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t_{PZL}			5	ns	C_L = 15 pF
Pulse Width Distortion[2]	PWD		2	3	ns	C_L = 15 pF
Propagation Delay Skew[3]	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		2	4	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		2	4	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	$\|CM_H\|$,$\|CM_L\|$	30	50		kV/µs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns
Channel-to-Channel Skew	t_{CSK}		2	3	ns	C_L = 15 pF
SYNC Internal Clock Off Time[11]	t_{OFF}			5	ns	
Dynamic Power Consumption[6]			140	240	µA/Mbps	per channel

Magnetic Field Immunity[8] (V_{DD2}= 3V, 3V<V_{DD1}<5.5V)						
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

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5 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current						
IL810, IL811, IL815	I_{DD1}		24	40	µA	
IL814, IL817, IL821			1.8	2.5	mA	
IL816			3.6	5	mA	
Output Quiescent Supply Current						
IL810, IL821	I_{DD2}		1.8	2.5	mA	
IL811, IL814, IL816			3.6	5	mA	
IL815			7.2	10	mA	
IL817			5.4	7.5	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} − 0.1	V_{DD}		V	I_O = −20 µA, V_I = V_{IH}
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.5	0.8		I_O = 4 mA, V_I = V_{IL}

Switching Specifications						
Maximum Data Rate		100	110		Mbps	C_L = 15 pF
Pulse Width[7]	PW	10			ns	V_O 50% points
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	C_L = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t_{PHZ}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t_{PLZ}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t_{PZH}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t_{PZL}			5	ns	C_L = 15 pF
Pulse Width Distortion[2]	PWD		2	3	ns	C_L = 15 pF
Propagation Delay Skew[3]	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	$\|CM_H\|$,$\|CM_L\|$	30	50		kV/µs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns
Channel-to-Channel Skew	t_{CSK}		3	5	ns	C_L = 15 pF
SYNC Internal Clock Off Time[11]	t_{OFF}			5	ns	
Dynamic Power Consumption[6]			200	340	µA/Mbps	per channel

Magnetic Field Immunity[8] (V_{DD2}= 5V, 3V<V_{DD1}<5.5V)						
Power Frequency Magnetic Immunity	H_{PF}		3,500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		4,500		A/m	t_p = 8 µs
Damped Oscillatory Magnetic Field	H_{OSC}		4,500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

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Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins on each side of the package are shorted.
6. Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 12.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 12).
10. If internal clock is used, devices will respond to DC states on inputs within a maximum of 9 µs. Outputs may oscillate if the SYNC input slew rate is less than 1 V/ms.
11. t_{off} is the maximum time for the internal refresh clock to shut down.

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Application Information

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

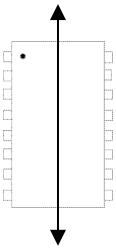
IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

Additionally, on the IL810 and IL815, the internal clock can be disabled for even better EMC performance.

These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

EN50081-1
Residential, Commercial & Light Industrial
Methods EN55022, EN55014
EN50082-2: Industrial Environment
Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)
ENV50204
Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR ceramic capacitors of at least 47 nF. Capacitors must be located as close as possible to the V_{DD} pins.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. A magnetic field is created around the GMR Wheatstone bridge by detecting the edge transitions of the input logic signal and converting them to narrow current pulses. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

DC Correctness, EMC, and the SYNC Function

NVE digital isolators have the lowest EMC noise signature of any high-speed digital isolator on the market today because of the dc nature of the GMR sensors used. It is perhaps fair to include opto-couplers in that dc category too, but their limited parametric performance, physically large size, and wear-out problems effectively limit side by side comparisons between NVE's isolators and isolators coupled with RF, matched capacitors, or transformers.

IL800-Series isolators has an internal refresh clock which ensure the synchronization of input and output within 9 µs of the supply passing the 1.5 V threshold. The IL810 and IL815 allow external control of the refresh clock through the SYNC pin thereby further lowering the EMC footprint. This can be advantageous in applications such as hi-fi, motor control and power conversion.

The isolators can be used with Power on Reset (POR) circuits common in microcontroller applications, as the means of ensuring the output of the device is in the same state as the input a short time after power up. Figure 1 shows a practical Power on Reset circuit:

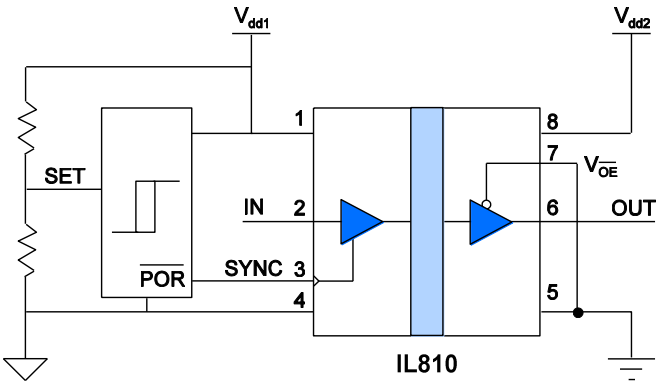
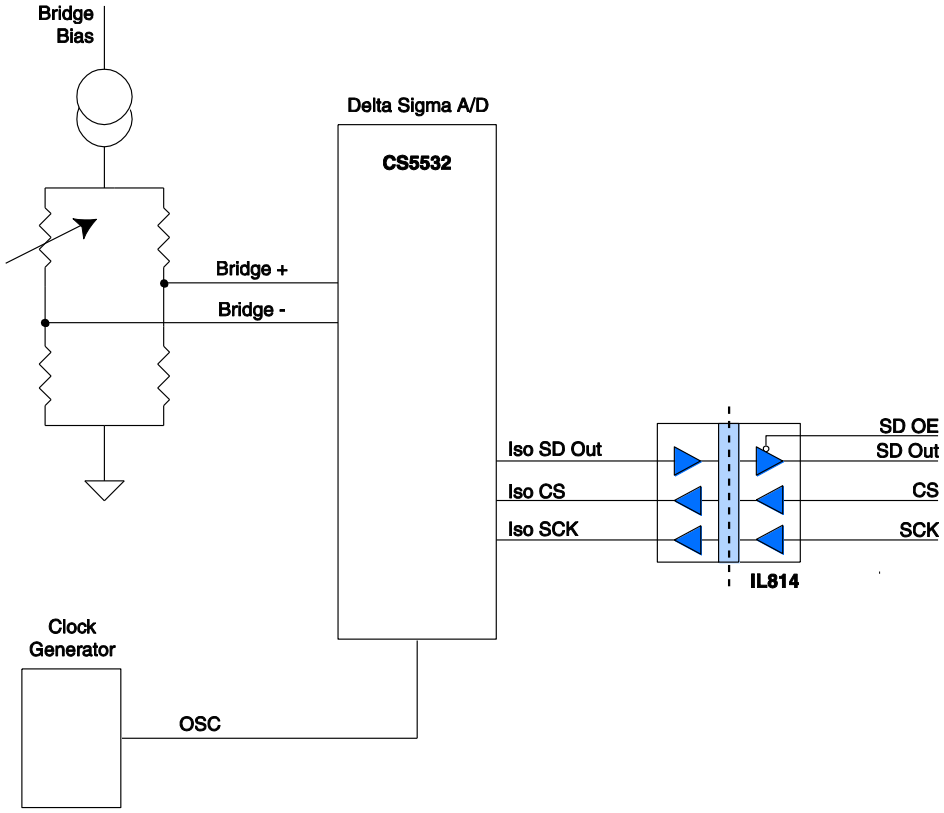


Fig. 1. Typical Power On Reset Circuit for IL810

After POR, the SYNC line goes high, the internal clock is disabled, and the EMC signature is optimized. Decoupling capacitors are omitted for clarity.

Illustrative Applications

Isolated A/D Converter



A delta-sigma A-D converter interfaced with the three-channel IL814. Multiple channels can easily be combined using the IL814's output enable function.

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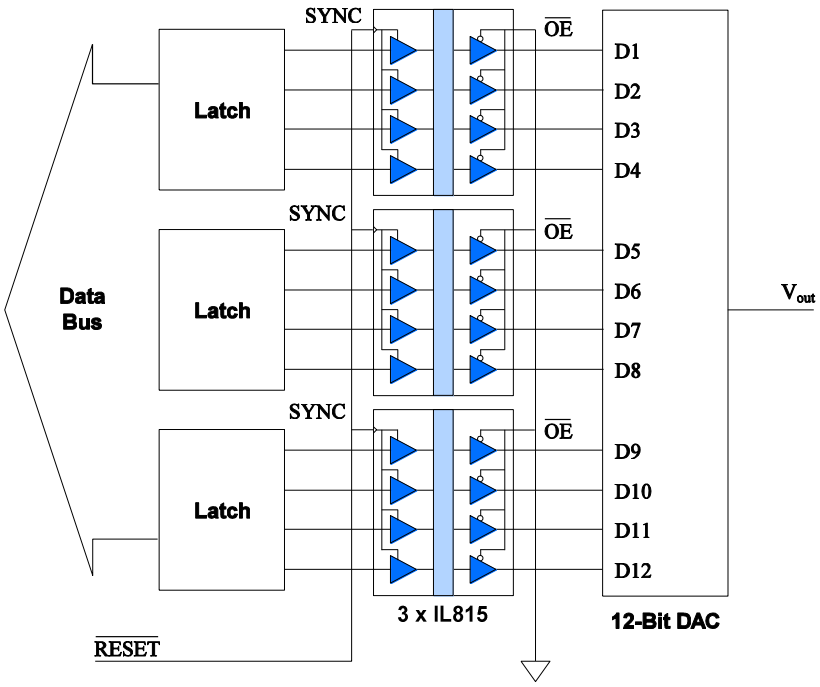
12-Bit D/A Converter Isolation



The IL815 four-channel isolator is ideally suited for parallel bus isolation. The circuit above uses three IL815s to isolate a 12-bit DAC. The SYNC function automatically synchronizes the outputs to the inputs, ensuring correct data on the isolator outputs. After the reset pulse goes high, data transfer from input to output is initiated by the leading edge of each changing data bit.

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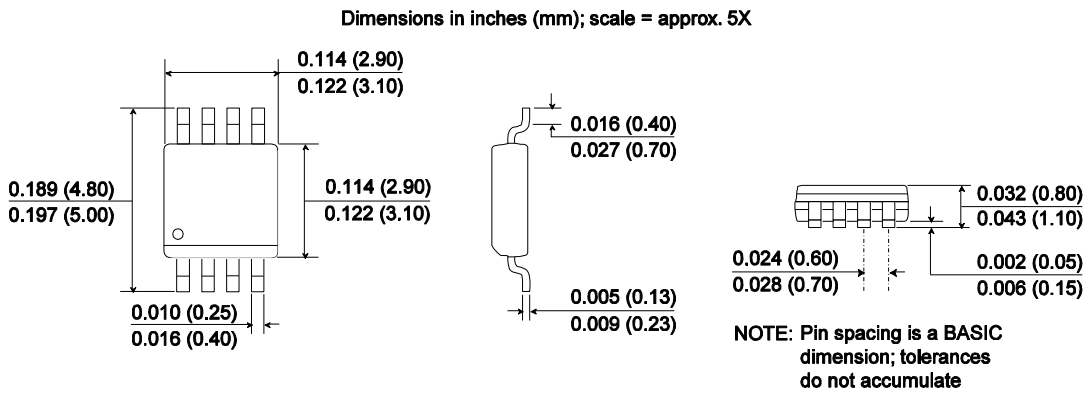
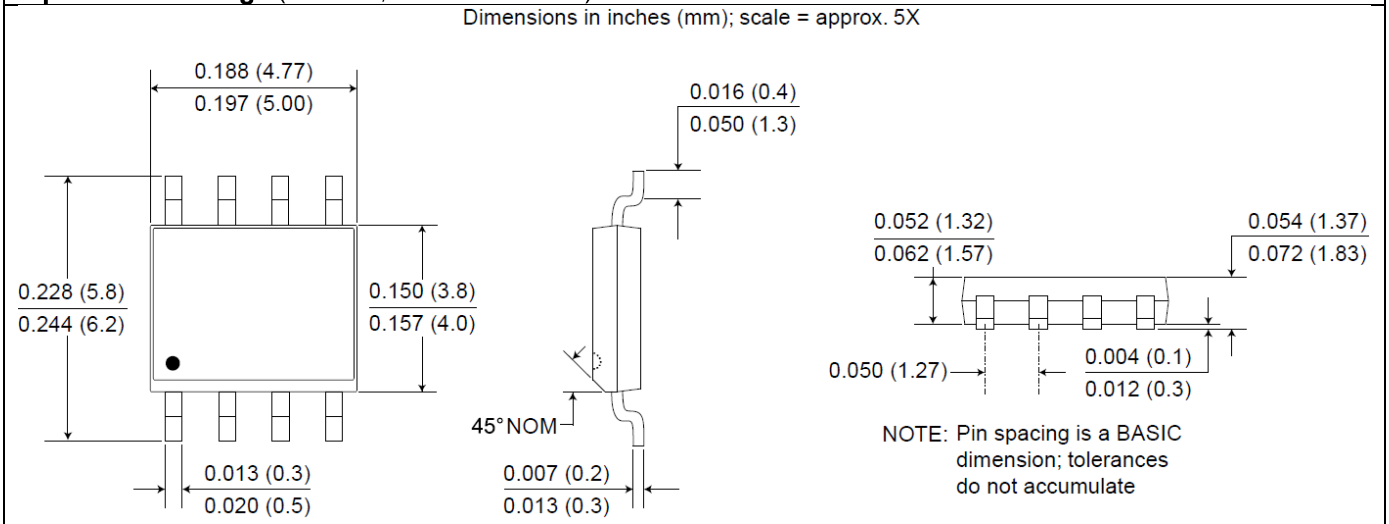
Package Drawings

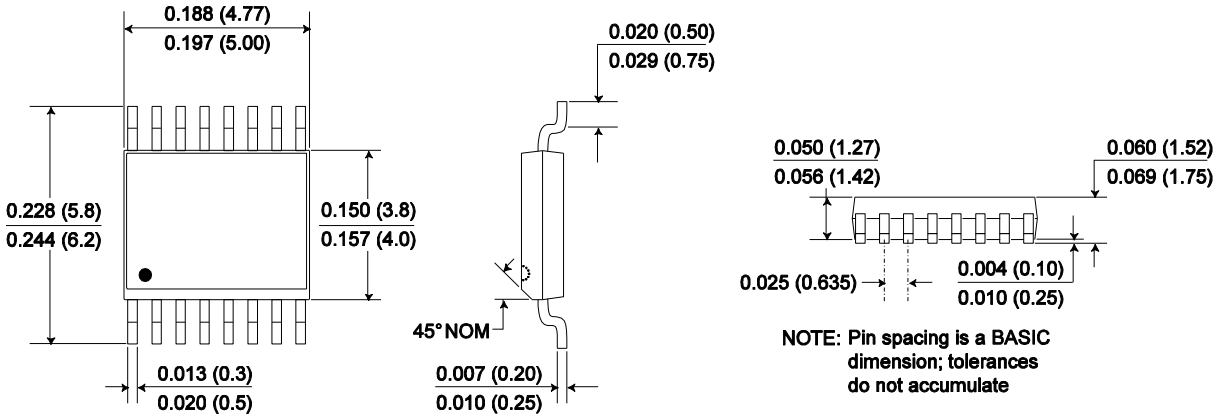
8-pin MSOP (-1 suffix; 1 and 2 channel)



8-pin SOIC Package (-3 suffix; 1 and 2 channel)

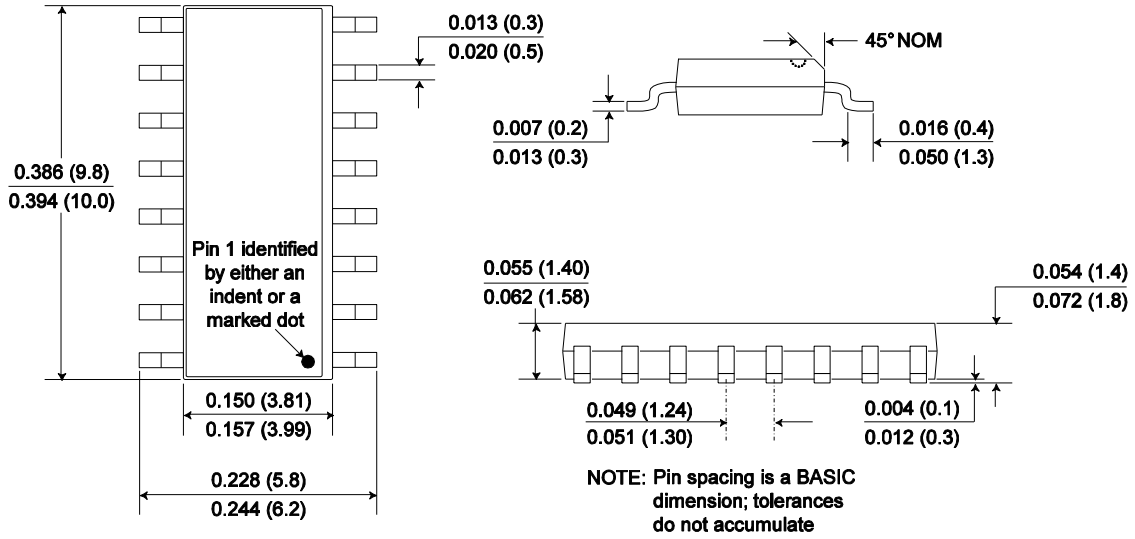


Ultraminiature 16-pin QSOP Package (-1 suffix; 3 and 4 channel)



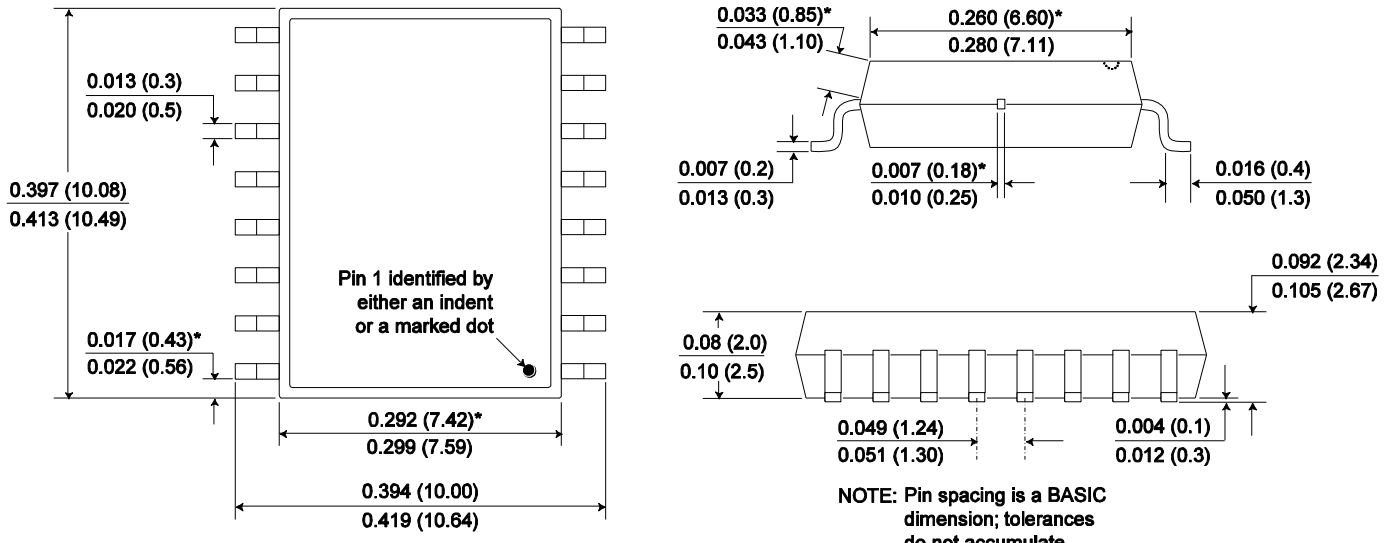
0.15" 16-pin SOIC Package (-3 suffix; 3 and 4 channel)

Dimensions in inches (mm); scale = approx. 5X



True8™ 0.3" 16-pin SOIC Package (no suffix; 2, 3, and 4 channel)

Dimensions in inches (mm); scale = approx. 5X



*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

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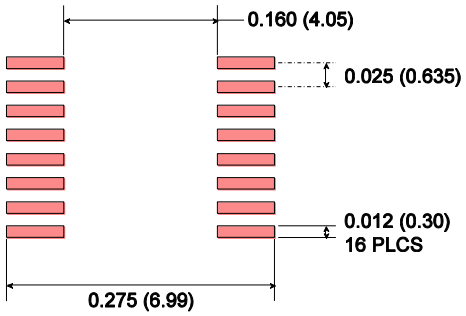
Recommended Pad Layouts

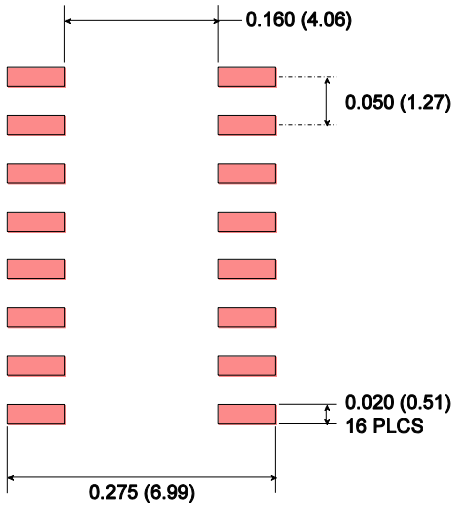
4 mm x 5 mm 16-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



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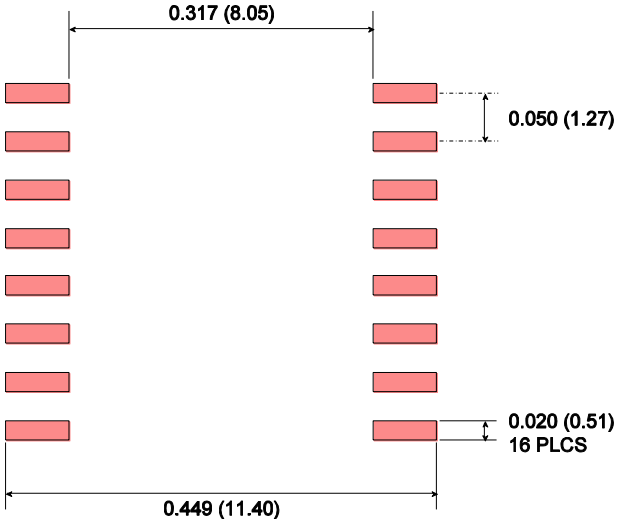
0.3" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



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Ordering Information

IL 8 16 - 3 T E TR13

Bulk Packaging
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Package
E = RoHS Compliant

Temperature Range
T = -40°C to 125°C

Package Type
-1 = 8-pin MSOP or 16-pin QSOP
-3 = 0.15" 8-pin or 16-pin SOIC
Blank = True8™ 0.3" 16-pin SOIC

Channels
10 = 1 Transmit Channel
11 = 2 Transmit Channels
21 = 1 Transmit Channel
1 Receive Channel
14 = 2 Transmit Channels;
1 Receive Channel
15 = 4 Transmit Channels
16 = 2 Transmit Channels;
2 Receive Channels
17 = 3 Transmit Channels;
1 Receive Channels

Base Part Number
8 = 110 Mbps, DC-Correct

Product Family
IL = Isolators

Available Parts	Xmit Ch.	Rcv. Ch.	Package
IL810T-1E	1	0	MSOP-8
IL810T-3E	1	0	SOIC-8
IL811T-1E	2	0	MSOP-8
IL811T-3E	2	0	SOIC-8
IL814T-1E	2	1	QSOP-16
IL814T-3E	2	1	0.15" SOIC-16
IL814TE	2	1	True8
IL815T-1E	4	0	QSOP-16
IL815T-3E	4	0	0.15" SOIC-16
IL815TE	4	0	True8
IL816T-1E	2	2	QSOP
IL816T-3E	2	2	0.15" SOIC-16
IL816TE	2	2	True8
IL817T-3E	3	1	0.15" SOIC-16
IL817TE	3	1	True8
IL821T-3E	1	1	SOIC-8
IL821TE	1	1	True8

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ISB-DS-001-IL800-H
March 2017

Changes:
- Corrected 8-pin SOC Package outline dimensions.
- Removed minimum Magnetic Field Immunity specification.

ISB-DS-001-IL800-G
November 2016

Changes:
- Updated IEC 60747-5-5 (VDE 0884) certification to VDE V 0884-10.

ISB-DS-001-IL800-F
June 2014

Changes:
- Added IL814T-1, IL815T-1, and IL816T-1 QSOP versions.
- Dropped IL812 configuration in favor of IL821 two-channel bidirectional configuration.
- Updated thermal characteristics.
- Added recommended pad layouts.

ISB-DS-001-IL800-E
November 2013

Changes:
- Added IL821TE part type (16-pin True8 wide-body package).
- Added output enables to IL816 and IL817.
- Clarified pinouts for different package types.
- IEC 60747-5-5 (VDE 0884) certification.
- Upgraded from MSL 2 to MSL 1.

ISB-DS-001-IL800-D
August 2013

Changes:
- Tighter quiescent current specifications.
- Added IL817 part types.

ISB-DS-001-IL800-C
July 2013

Changes:
- Added IL812-3 and IL821-3 part types (8-pin SOIC packages).

ISB-DS-001-IL800-B
June 2013

Changes:
- Increased transient immunity specifications based on additional data.

ISB-DS-001-IL800-A
May 27, 2013

Changes:
- Added “T” to full part numbers to indicate 125°C max. operating temperature.
- Added two-channel bidirectional versions (IL812 and IL821).
- Added list of available part types.

ISB-DS-001-IL800-PREVIEW
May 3, 2013

Changes:
- Released product preview.

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ISB-DS-001-IL800T-H

March 2017