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Never stop thinking

ILD1151

Multitopology High Power LED DC/DC Controller for Industrial Applications

Datasheet

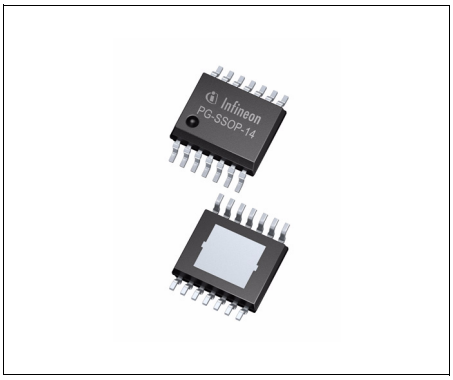
Rev. 1.1, 2012-04-11

Table of Contents

ILD1151

RoHS

1 Overview



PG-SSOP-14

Features

- Wide Input Voltage Range from 4.5 V to 45 V
- Constant Current or Constant Voltage Regulation
- Drives LEDs in Boost, Buck, Buck-Boost, SEPIC and Flyback Topology
- Very Low Shutdown Current: I_{q_OFF} < 10 µA
- Flexible Switching Frequency Range, 100 kHz to 500 kHz
- Synchronization with external clock source
- PWM Dimming
- Analog Dimming feature to adjust average LED current
- Internal 5 V Low Drop Out Voltage Regulator
- Open Circuit Detection
- Short to GND Protection
- Output Overvoltage Protection
- Internal Soft Start
- Over Temperature Shutdown
- Wide LED current range via simple adaptation of external components
- 300mV High Side Current Sense to ensure highest flexibility and LED current accuracy
- Available in a small thermally enhanced PG-SSOP-14 package
- Green Product (RoHS) Compliant

Description

The ILD1151 is a Multitopology High Power DC/DC Controller IC with built in protection features. The main function of this device is to regulate a constant LED current. The constant current regulation is especially beneficial for LED color accuracy and longer lifetime. The controller concept of the ILD1151 allows multiple configurations such as Boost, Buck, Buck-Boost, SEPIC and Flyback by simply adjusting the external components. The ILD1151 offers the most flexible dimming options. Dimming can be achieved with analog or PWM input.The switching frequency is adjustable in the range of 100 kHz to 500 kHz and can be synchronized to an external clock source. The ILD1151 features an enable function reducing the shut-down current consumption to I_{q_OFF} < 10 µA. The current mode regulation scheme of this device provides a stable regulation loop maintained by small external compensation components. The integrated soft start feature limits the current peak as well as voltage overshoot at start-up. This IC provides output overvoltage protection, device overtemperature shutdown and short circuit to GND protection.

Type	Package	Marking
ILD1151	PG-SSOP-14	ILD1151

Applications

- LED Controller for Industrial Applications
- Universal Constant Current and Voltage Source
- General Illumination e.g. Halogen Replacement
- Residential Architectural and Industrial Commercial Lighting for in- and outdoor
- Signal and Marker Lights for Orientation or Navigation (e.g. steps, exit ways, etc.)

For automotive and transportation applications, please refer to the Infineon® Auto LED products.

2 Block Diagram

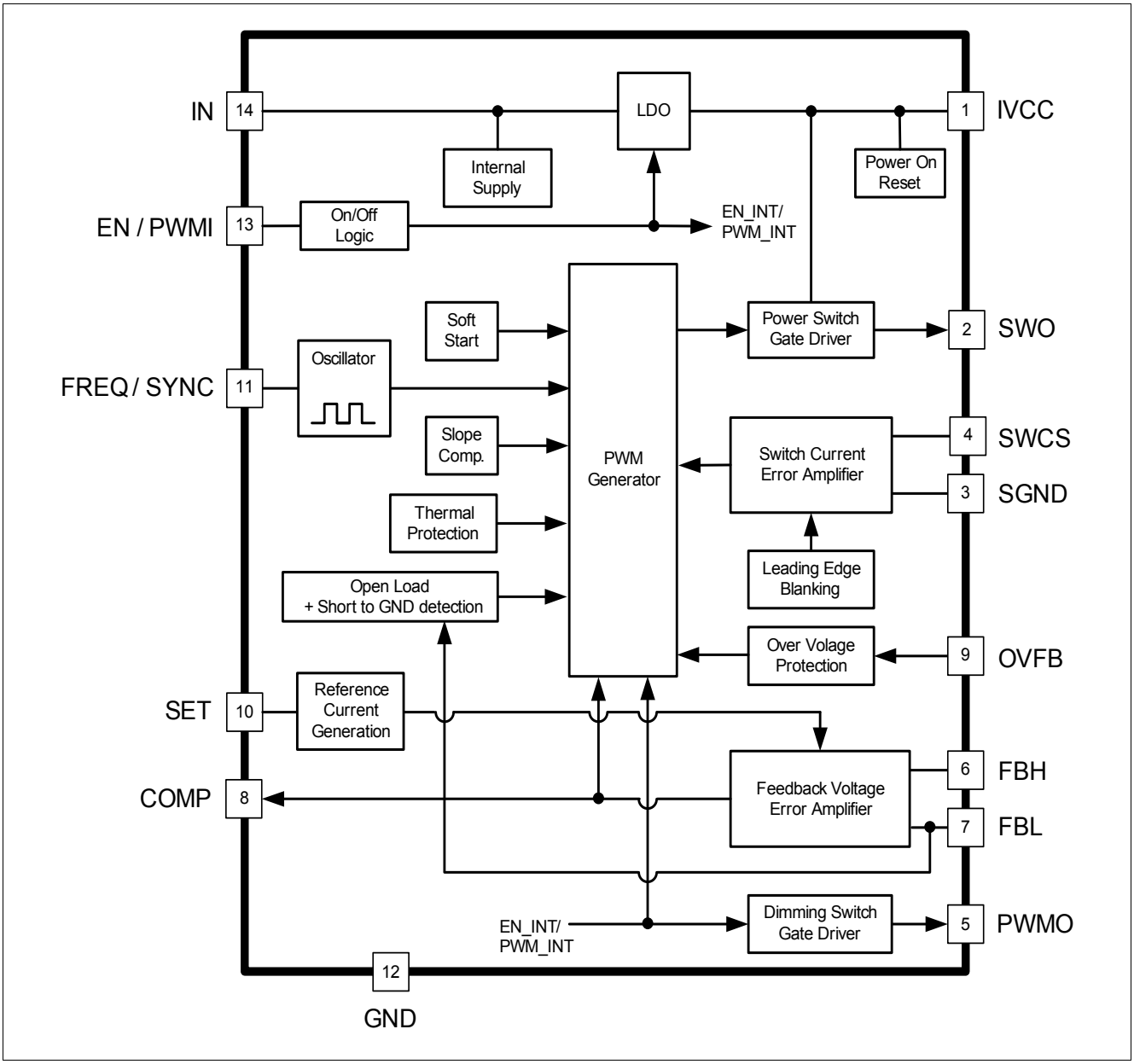


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

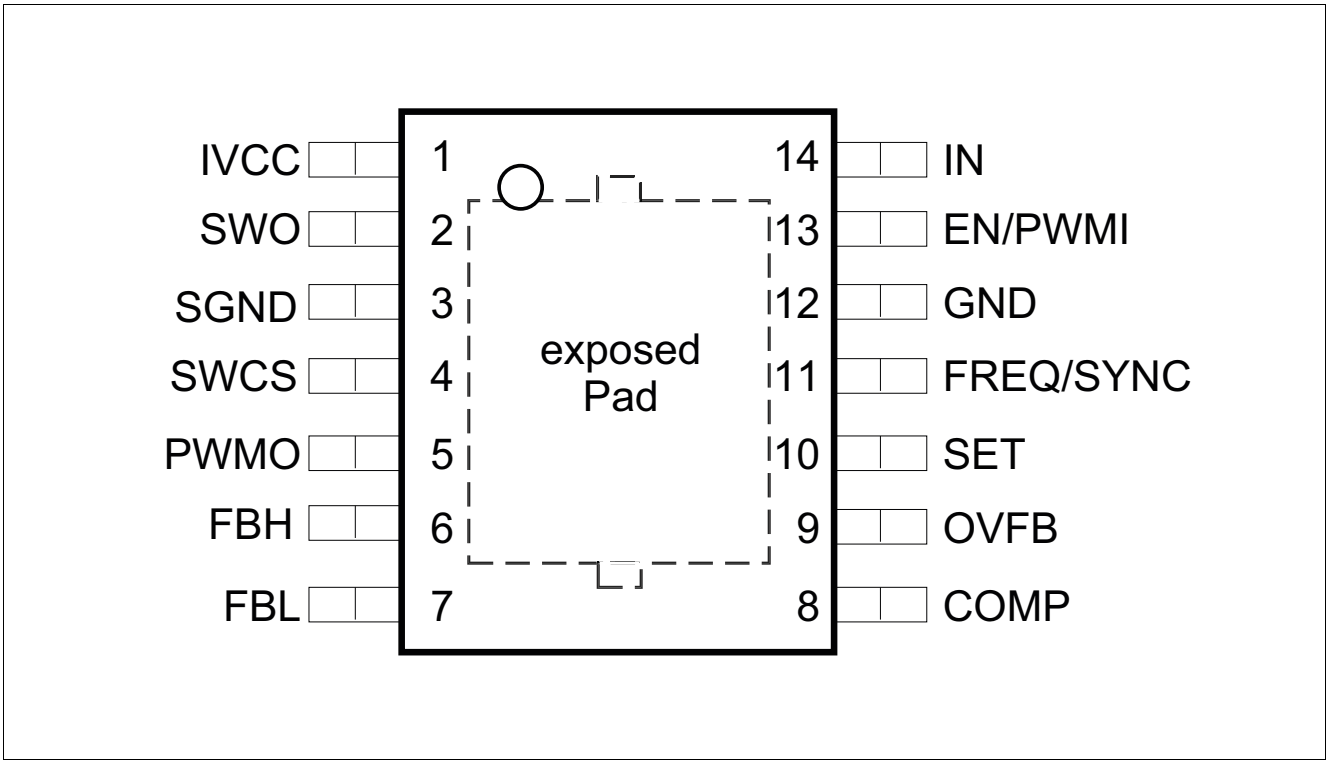


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	IVCC	**Internal LDO Output;** Used for internal biasing and gate drive. Bypass with external capacitor close to the pin. Pin must not be left open.
2	SWO	**Switch Output;** Connect to gate of external switching MOSFET
3	SGND	**Current Sense Ground;** Ground return for current sense switch
4	SWCS	**Current Sense Input;** Detects the peak current through switch
5	PWMO	**PWM Dimming Output;** Connect to gate of external MOSFET
6	FBH	**Voltage Feedback Positive;** Non inverting Input (+)
7	FBL	**Voltage Feedback Negative;** Inverting Input (-)
8	COMP	**Compensation Input;** Connect R and C network to pin for stability

Pin	Symbol	Function
9	OVFB	**Output Overvoltage Protection Feedback;** Connect to resistive voltage divider to set overvoltage threshold.
10	SET	**Analog Dimming Input;** Load current adjustment Pin. Pin must not be left open. If analog dimming feature is not used connect to IVCC pin.
11	FREQ / SYNC	**Frequency Select or Synchronization Input;** Connect external resistor to GND to set frequency. Or apply external clock signal for synchronization within frequency capture range.
12	GND	**Ground;** Connect to system ground.
13	EN / PWMI	**Enable or PWM Input;** Apply logic HIGH signal to enable device or PWM signal for dimming LED.
14	IN	**Supply Input;** Supply for internal biasing.
EP		**Exposed Pad;** Connect to external heatspreading GND Cu area (e.g. inner GND layer of multilayer PCB with thermal vias).

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]

T_j = -40 °C to +125 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	IN Supply Input	V_{IN}	-0.3	45	V	–
4.1.2	EN / PWMI Enable or PWM Input	V_{EN}	-40	45	V	–
4.1.3	FBH-FBL Feedback Error Amplifier Differential	V_{FBH}-V_{FBL}	-40	61	V	The maximum delta must not exceed 61V
4.1.4	FBH Feedback Error Amplifier Positive Input	V_{FBH}	-40	61	V	The difference between V_{FBH} and V_{FBL} must not exceed 61V, refer to Parameter 4.1.3
4.1.5	FBL Feedback Error Amplifier Negative Input	V_{FBL}	-40	61	V	The difference between V_{FBH} and V_{FBL} must not exceed 61V, refer to Parameter 4.1.3
4.1.6	FBH and FBL current	$I_{FBL,FBH}$	–	1	mA	t < 100ms, V_{FBH} - V_{FBL} = 0.3V
4.1.7	OVFB Over Voltage Feedback Input	V_{OVP}	-0.3	5.5	V	–
4.1.8			-0.3	6.2	V	t < 10s
4.1.9	SWCS Switch Current Sense Input	V_{SWCS}	-0.3	5.5	V	–
4.1.10			-0.3	6.2	V	t < 10s
4.1.11	SWO Switch Gate Drive Output	V_{SWO}	-0.3	5.5	V	–
4.1.12			-0.3	6.2	V	t < 10s
4.1.13	SGND Current Sense Switch GND	V_{SGND}	-0.3	0.3	V	–
4.1.14	COMP Compensation Input	V_{COMP}	-0.3	5.5	V	–
4.1.15			-0.3	6.2	V	t < 10s
4.1.16	FREQ / SYNC; Frequency and Synchronization Input	$V_{FREQ / SYNC}$	-0.3	5.5	V	–
4.1.17			-0.3	6.2	V	t < 10s
4.1.18	PWMO PWM Dimming Output	V_{PWMO}	-0.3	5.5	V	–
4.1.19			-0.3	6.2	V	t < 10s
4.1.20	SET	V_{SET}	-0.3	45	V	–
4.1.21	IVCC Internal Linear Voltage Regulator Output	V_{IVCC}	-0.3	5.5	V	–
4.1.22			-0.3	6.2	V	t < 10s
Temperatures						
4.1.23	Junction Temperature	T_j	-40	150	°C	–

Absolute Maximum Ratings[1)]

T_j = -40 °C to +125 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.24	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.25	ESD Resistivity of all Pins	$V_{ESD,HBM}$	-2	2	kV	HBM[2)]
4.1.26	ESD Resistivity of IN, EN/PWMI, FBH, FBL and SET pin to GND	$V_{ESD,HBM}$	-4	4	kV	HBM[2)]

1) Not subject to production test, specified by design.

2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001 (1.5kΩ, 100pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range	V_{IN}	4.5	45[1)]	V	$V_{IVCC} > V_{IVCC,RTH,d}$
4.2.2	Feedback Voltage Input	V_{FBH}; V_{FBL}	3	60	V	–
4.2.3	Junction Temperature	T_j	-40	125	°C	–

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1) 2)]	R_{thJC}	–	10	–	K/W	–
4.3.2	Junction to Ambient[1) 3)]	R_{thJA}	–	47	–	K/W	2s2p
4.3.3		R_{thJA}	–	54	–	K/W	1s0p + 600 mm^2
4.3.4		R_{thJA}	–	64	–	K/W	1s0p + 300 mm^2

1) Not subject to production test, specified by design.

2) Specified RthJC value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). Ta=25°C; The IC is dissipating 1W.

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70µm Cu) and 2 inner copper layers (2 x 35µm Cu). A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. Ta=25°C; The IC is dissipating 1W.

5 Switching Regulator

5.1 Description

The ILD1151 regulator is suitable for Boost, Buck, Buck-Boost, SEPIC and Flyback configurations. The constant output current is especially useful for light emitting diode (LED) applications. The regulator function is implemented by a pulse width modulated (PWM) current mode controller.

The PWM current mode controller uses the peak current through the external power switch and error in the output current to determine the appropriate pulse width duty cycle (on time) for constant output current. The current mode controller provides a PWM signal to an internal gate driver which then outputs to an external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch.

The current mode controller also has built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty).

An additional built-in feature is an integrated soft start that limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over t_{SS} (Parameter **5.2.8**) to minimize potential overvoltage at the output.

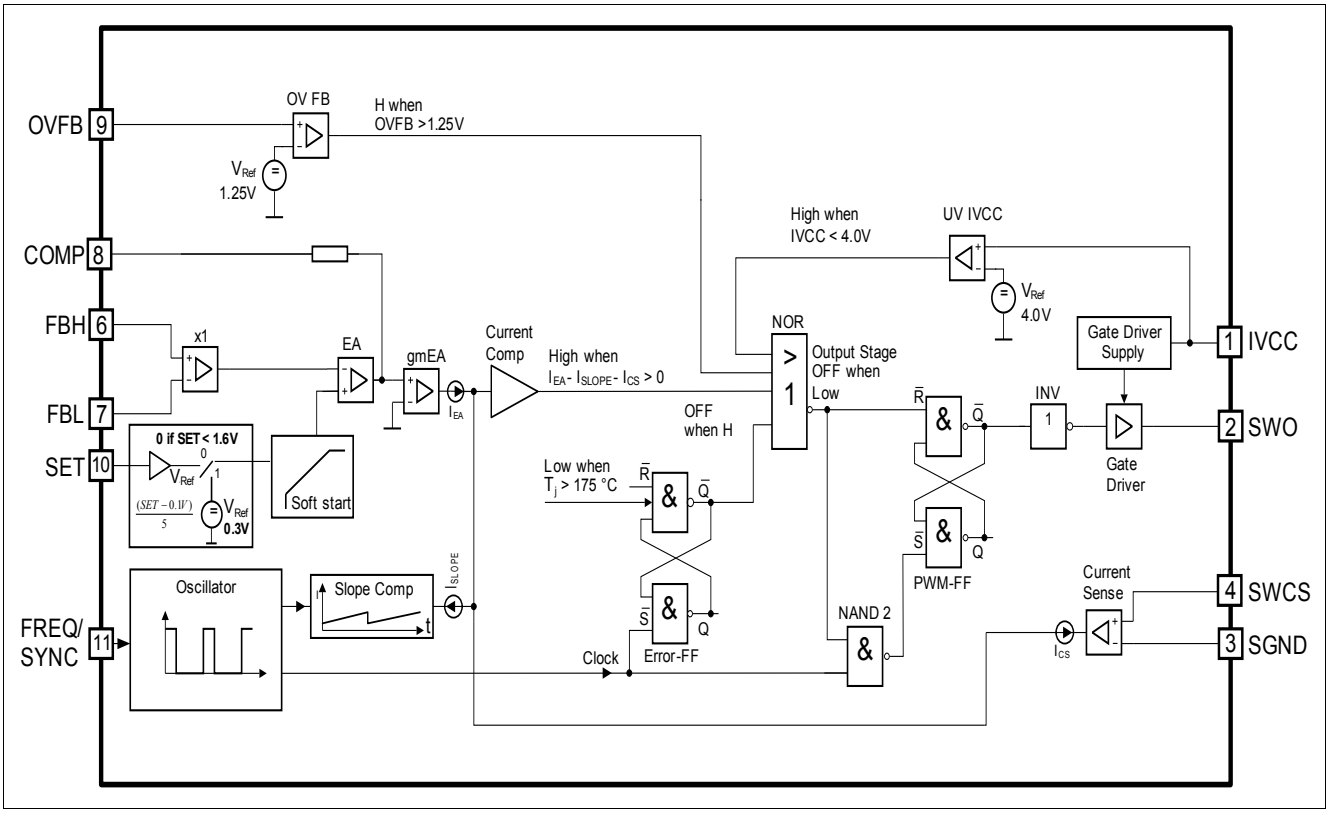


Figure 3 Switching Regulator Block Diagram

5.2 Electrical Characteristics

All parameters have been tested at 25°C, unless otherwise specified.

Table 1 EC Switching Regulator

V_{IN} = 24V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Regulator:							
5.2.1	Feedback Reference Voltage	V_{REF}	0.29	0.30	0.31	V	refer to **Figure 29** $V_{REF} = V_{FBH} - V_{FBL}$ V_{SET} = 5V I_{LED} = 350 mA
5.2.2	Feedback Reference Voltage	V_{REF}	0.057	0.06	0.063	V	refer to **Figure 29** $V_{REF} = V_{FBH} - V_{FBL}$ V_{SET} = 0.4V I_{LED} = 70mA
5.2.3	Feedback Reference Voltage Offset	V_{REF_offset}	–	–	5	mV	refer to **Figure 17** and **Figure 29** $V_{REF} = V_{FBH} - V_{FBL}$ V_{SET} = 0.1V $V_{OUT} > V_{IN}$
5.2.4	Voltage Load Regulation	$(\Delta V_{REF} / V_{REF}) / \Delta I_{BO}$	–	–	5	%/A	refer to **Figure 29** V_{SET} = 5V; I_{LED} = 100 to 500mA
5.2.5	Switch Peak Over Current Threshold	V_{SWCS}	130	150	170	mV	V_{FBH} = V_{FBL} = 5V V_{COMP} = 3.5V
5.2.6	Maximum Duty Cycle	$D_{MAX,fixed}$	91	93	95	%	Fixed frequency mode
5.2.7	Maximum Duty Cycle	$D_{MAX,sync}$	88	–	–	%	Synchronization mode
5.2.8	Soft Start Ramp	t_{SS}	350	1000	1500	µs	V_{FB} rising from 5% to 95% of V_{FB}, typ.
5.2.9	IFBH Feedback High Input Current	I_{FBH}	38	46	54	µA	V_{FBH} - V_{FBL} = 0.3V
5.2.10	IFBL Feedback Low Input Current	I_{FBL}	15	21	27	µA	V_{FBH} - V_{FBL} = 0.3V
5.2.11	Switch Current Sense Input Current	I_{SWCS}	10	50	100	µA	V_{SWCS} = 150mV
5.2.12	Input Undervoltage Shutdown	$V_{IN,off}$	3.5	–	4.5	V	V_{IN} decreasing
5.2.13	Input Voltage Startup	$V_{IN,on}$	–	–	4.85	V	V_{IN} increasing

1) Not subject to production test, specified by design

Table 1 EC Switching Regulator

V_{IN} = 24V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Gate Driver for external Switch							
5.2.14	Gate Driver Peak Sourcing Current	$I_{SWO,SRC}$	–	380	–	mA	1) V_{SWO} = 1V to 4V
5.2.15	Gate Driver Peak Sinking Current	$I_{SWO,SNK}$	–	550	–	mA	1) V_{SWO} = 4V to 1V
5.2.16	Gate Driver Output Rise Time	$t_{R,SWO}$	–	30	60	ns	1) $C_{L,SWO}$ = 3.3nF; V_{SWO} = 1V to 4V
5.2.17	Gate Driver Output Fall Time	$t_{F,SWO}$	–	20	40	ns	1) $C_{L,SWO}$ = 3.3nF; V_{SWO} = 4V to 1V
5.2.18	Gate Driver Output Voltage	V_{SWO}	4.5	–	5.5	V	1) $C_{L,SWO}$ = 3.3nF;

1) Not subject to production test, specified by design

6 Oscillator and Synchronization

6.1 Description

The internal oscillator is used to determine the switching frequency of the boost regulator. The switching frequency can be selected from 100 kHz to 500 kHz with an external resistor to GND. To set the switching frequency with an external resistor the following formula can be applied.

$$R_{FREQ} = \frac{1}{\left(141 \times 10^{-12}\left[\frac{s}{\Omega}\right]\right) \times \left(f_{FREQ}\left[\frac{1}{s}\right]\right)} - \left(3.5 \times 10^{3}\left[\Omega\right]\right)\left[\Omega\right]$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin FREQ/SYNC, then the internal oscillator synchronizes to this external clock frequency and the boost regulator switches at the synchronized frequency. The synchronization frequency capture range is 250 kHz to 500 kHz.

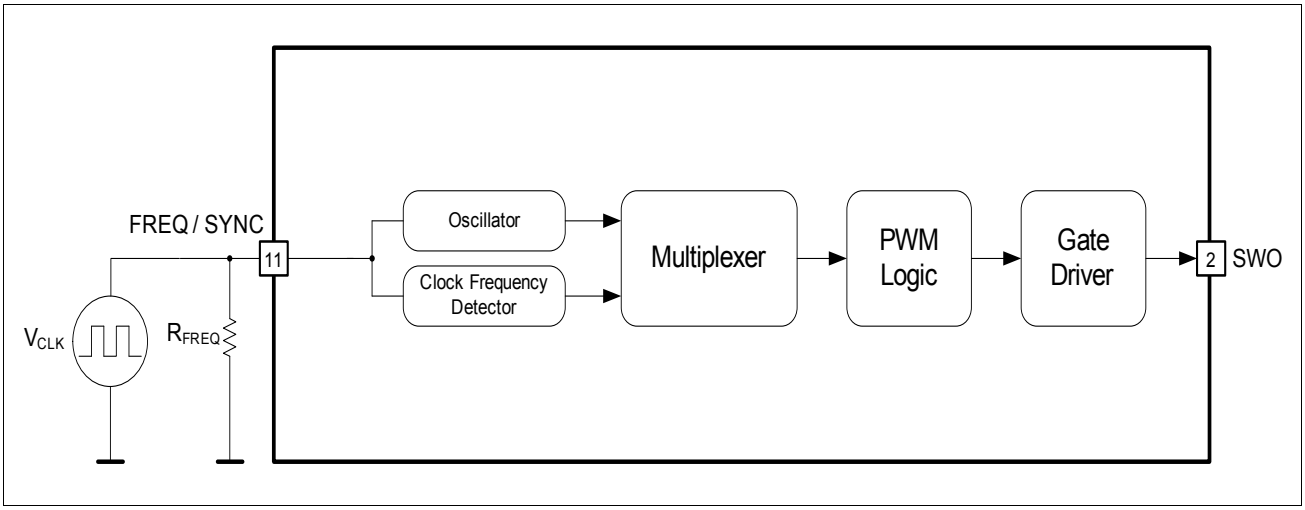


Figure 4 Oscillator and Synchronization Block Diagram and Simplified Application Circuit

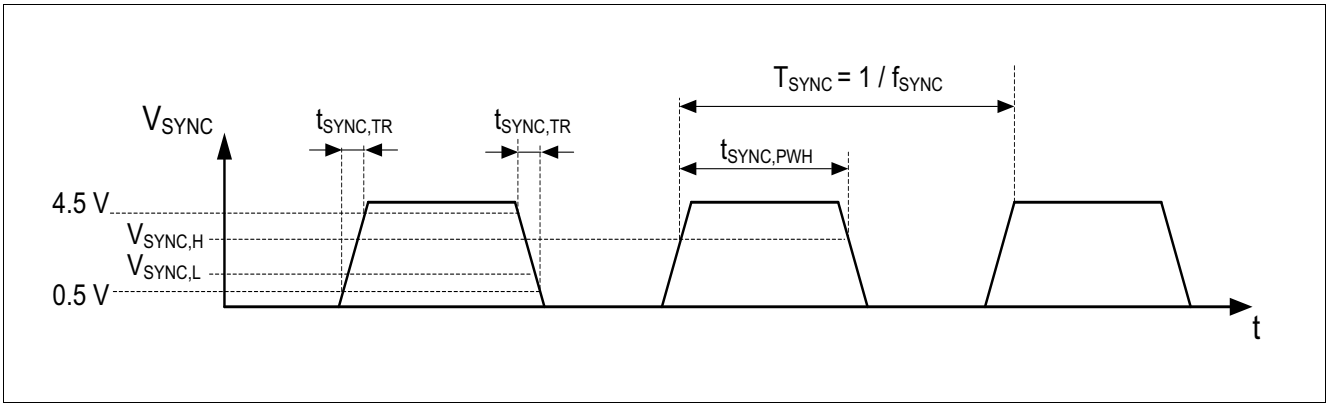


Figure 5 Synchronization Timing Diagram

6.2 Electrical Characteristics

All parameters have been tested at 25°C, unless otherwise specified.

Table 2 EC Oscillator and Synchronization

V_{IN} = 24V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

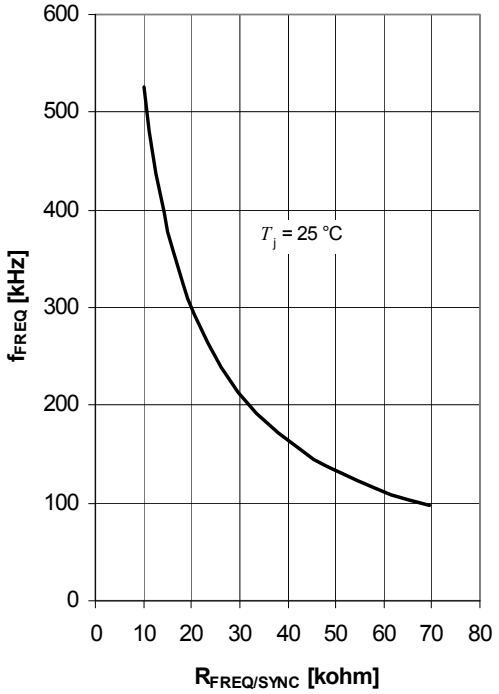
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Oscillator:							
6.2.1	Oscillator Frequency	f_{FREQ}	250	300	350	kHz	R_{FREQ} = 20kΩ
6.2.2	Oscillator Frequency Adjustment Range	f_{FREQ}	100	–	500	kHz	
6.2.3	FREQ / SYNC Supply Current	I_{FREQ}	–	–	-700	µA	V_{FREQ} = 0V
6.2.4	Frequency Voltage	V_{FREQ}	1.16	1.24	1.32	V	f_{FREQ} = 100kHz
Synchronization							
6.2.5	Synchronization Frequency Capture Range	f_{SYNC}	250	–	500	kHz	–
6.2.6	Synchronization Signal High Logic Level Valid	$V_{SYNC,H}$	3.0	–	–	V	1) 2)
6.2.7	Synchronization Signal Low Logic Level Valid	$V_{SYNC,L}$	–	–	0.8	V	1) 2)
6.2.8	Synchronization Signal Logic High Pulse Width	$t_{SYNC,PWH}$	200	–	–	ns	1) 2)

1) Synchronization of external PWM ON signal to falling edge

2) Not subject to production test, specified by design

Typical Performance Characteristics of Oscillator

Switching Frequency f_{SW} versus Frequency Select Resistor to GND $R_{FREQ/SYNC}$



7 Enable and Dimming Function

7.1 Description

The enable function powers ON or OFF the device. A valid logic LOW signal on enable pin EN/PWMI powers OFF the device and current consumption is less than I_{q_OFF} (Parameter **7.2.14**). A valid logic HIGH enable signal on enable pin EN/PWMI powers on the device. The enable function features an integrated pull down resistor which ensures that the IC is shut down and the power switch is OFF in case the enable pin EN is left open.

In addition to the enable function described above, the EN/PWMI pin detects a pulse width modulated (PWM) input signal that is fed through to an internal gate driver. The internal gate driver outputs the same PWM signal on the PWMO pin to an external N-channel enhancement mode MOSFET for PWM dimming an LED load. PWM dimming an LED is a commonly practiced dimming method and can prevent color shift in an LED light source. Moreover the PWM output function may also be used to drive other types of loads besides LED.

The enable and PWM input function share the same pin. Therefore a valid logic LOW signal at the EN/PWMI pin needs to differentiate between an enable power OFF or an PWM dimming LOW signal. The device differentiates between enable OFF and PWM dimming signal by requiring the enable OFF at the EN/PWMI pin to stay LOW for the Enable Turn OFF Delay Time ($t_{EN,OFF,DEL}$ Parameter **7.2.6**).

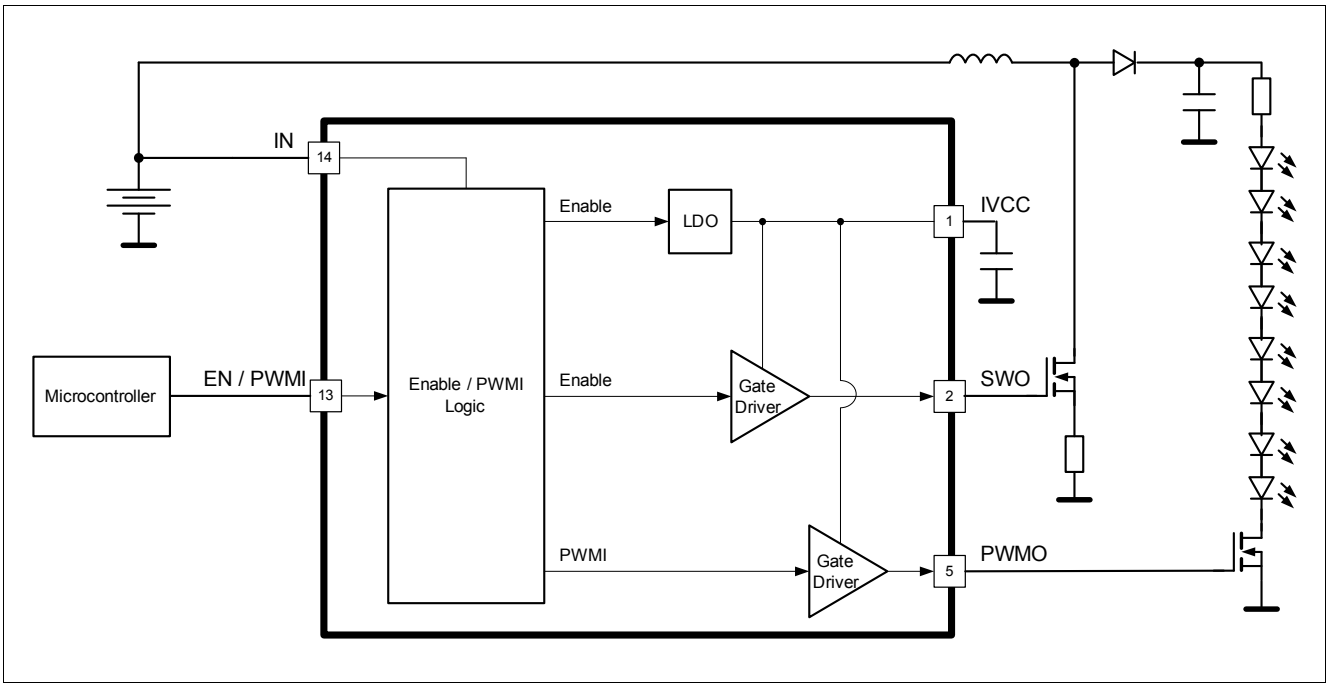


Figure 6 Block Diagram and Simplified Application Circuit Enable and LED Dimming

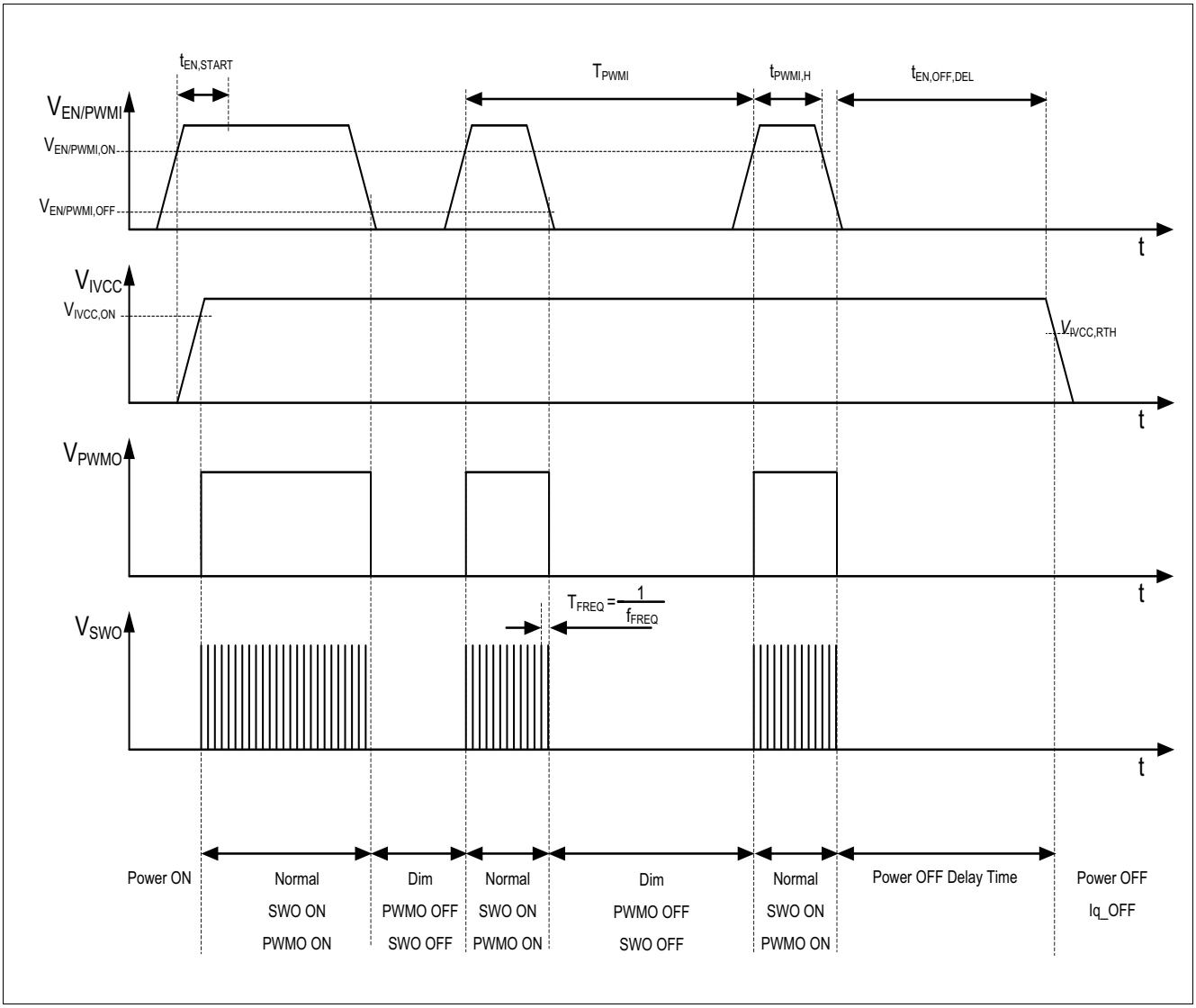


Figure 7 Timing Diagram Enable and LED Dimming

7.2 Electrical Characteristics

All parameters have been tested at 25°C, unless otherwise specified.

Table 3 EC Enable and Dimming

V_{IN} = 24V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Enable/PWM Input:							
7.2.1	Enable/PWMI Turn On Threshold	$V_{EN/PWMI,ON}$	3.0	–		V	–
7.2.2	Enable/PWMI Turn Off Threshold	$V_{EN/PWMI,OFF}$	–	–	0.8	V	–

Table 3 EC Enable and Dimming

V_{IN} = 24V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.2.3	Enable/PWMI Hysteresis	$V_{EN/PWMI,HYS}$	50	200	400	mV	1)
7.2.4	Enable/PWMI High Input Current	$I_{EN/PWMI,H}$	–	–	30	µA	$V_{EN/PWMI}$ = 16.0V
7.2.5	Enable/PWMI Low Input Current	$I_{EN/PWMI,L}$	–	0.1	1	µA	$V_{EN/PWMI}$ = 0.5V
7.2.6	Enable Turn Off Delay Time	$t_{EN,OFF,DEL}$	8	10	12	ms	–
7.2.7	PWMI Min Duty Time	$t_{PWMI,H}$	4	–	–	µs	–
7.2.8	Enable Startup Time	$t_{EN,START}$	100	–	–	µs	1)
Gate Driver for Dimming Switch:							
7.2.9	PWMO Gate Driver Peak Sourcing Current	$I_{PWMO,SRC}$	–	230	–	mA	1) V_{PWMO} = 1V to 4V
7.2.10	PWMO Gate Driver Peak Sinking Current	$I_{PWMO,SNK}$	–	370	–	mA	1) V_{PWMO} = 4V to 1V
7.2.11	PWMO Gate Driver Output Rise Time	$t_{R,PWMO}$	–	50	100	ns	1) $C_{L,PWMO}$ = 3.3nF; V_{PWMO} = 1V to 4V
7.2.12	PWMO Gate Driver Output Fall Time	$t_{F,PWMO}$	–	30	60	ns	1) $C_{L,PWMO}$ = 3.3nF; V_{PWMO} = 4V to 1V
7.2.13	PWMO Gate Driver Output Voltage	V_{PWMO}	4.5	–	5.5	V	1) $C_{L,PWMO}$ = 3.3nF;
Current Consumption							
7.2.14	Current Consumption, Shutdown Mode	I_{q_OFF}	–	–	10	µA	$V_{EN/PWMI}$ = 0.8 V; $T_j \leq$ 105C; V_{IN} = 16V
7.2.15	Current Consumption, Active Mode[2)]	I_{q_ON}	–	–	7	mA	$V_{EN/PWMI} \geq$ 4.75V; I_{BO} = 0mA; V_{SWO} = 0% Duty Cycle

1) Not subject to production test, specified by design

2) Dependency on switching frequency and gate charge of boost and dimming switch.

8 Linear Regulator

8.1 Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5V and current up to $I_{LIM,min}$ (Parameter **8.2.2**). An external output capacitor with ESR lower than $R_{IVCC,ESR}$ (Parameter **8.2.5**) is required on pin IVCC for stability and buffering transient load currents. During normal operation the external boost and dimming MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches.

Integrated undervoltage protection for the external switching MOSFET:

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage (V_{IVCC}) and resets the device in case the output voltage falls below the IVCC Undervoltage Reset switch OFF Threshold ($V_{IVCC,RTH,d}$ Parameter **8.2.7**). The Undervoltage Reset threshold for the IVCC pin helps to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level N-channel MOSFET.

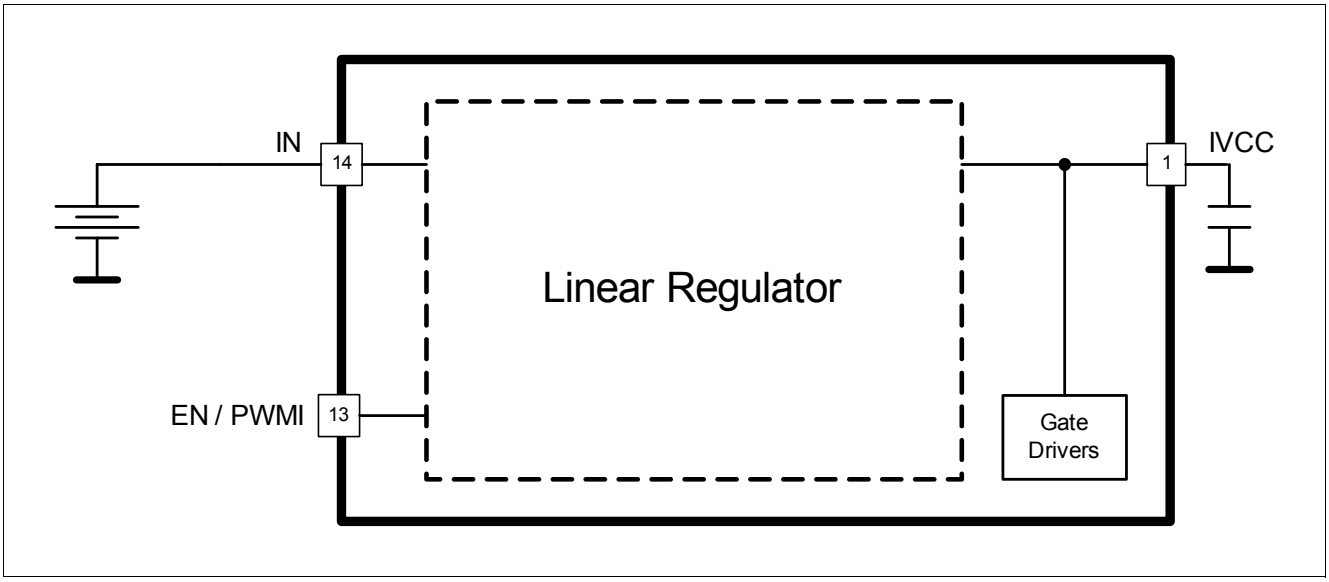


Figure 8 Voltage Regulator Block Diagram and Simplified Application Circuit

8.2 Electrical Characteristics

All parameters have been tested at 25°C, unless otherwise specified.

Table 4 EC Line Regulator

V_{IN} = 24V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.2.1	Output Voltage	V_{IVCC}	4.85	5	5.15	V	$6V \le V_{IN} \le 45V$ $0.1mA \le I_{IVCC} \le 50mA$
8.2.2	Output Current Limitation	I_{LIM}	51	–	90	mA	V_{IN} = 13.5V V_{IVCC} = 4.5V
8.2.3	Drop out Voltage	V_{DR}	–	–	0.5	V	V_{IN} = 4.5V I_{IVCC} = 25mA
8.2.4	IVCC Buffer Capacitor	C_{IVCC}	0.47	1	100	µF	1) 2)
8.2.5	IVCC Buffer Capacitor ESR	$R_{IVCC,ESR}$	–	–	0.5	Ω	1)
8.2.6	Undervoltage Reset Headroom	$V_{IVCC,HDRM}$	100	–	–	mV	V_{IVCC} decreasing V_{IVCC} - $V_{IVCC,RTH,d}$
8.2.7	IVCC Undervoltage Reset switch OFF Threshold	$V_{IVCC,RTH,d}$	3.6	–	4.0	V	3) V_{IVCC} decreasing.
8.2.8	IVCC Undervoltage Reset switch ON Threshold	$V_{IVCC,RTH,i}$	–	–	4.5	V	V_{IVCC} increasing

1) Not subject to production test, specified by design

2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.

3) Selection of external switching MOSFET is crucial and the $V_{IVCC,RTH,d}$ min. as worst case V_{GS} must be considered.

9 Protection and Diagnostic Functions

9.1 Description

The ILD1151 has integrated circuits to diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. Additionally the FBH and FBL potential is monitored and in case the LED load short circuits to GND (see description **Figure 15**) the regulator stops the operation and protects the system. In case any of the six fault conditions occur the PWMO and IVCC signal will change to an active logic LOW signal to communicate that a fault has occurred (detailed overview in **Figure 9** and **Figure 10** below). **Figure 11** illustrates the various open load and open feedback conditions. In case of an overtemperature condition the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator. The typical junction shutdown temperature is 175°C ($T_{j,SD}$ Parameter **9.2.2**). After cooling down the IC will automatically restart. Thermal shutdown is an integrated protection function designed to prevent IC destruction and is not intended for continuous use in normal operation (**Figure 13**). To calculate the proper overvoltage protection resistor values an example is given in **Figure 14**.

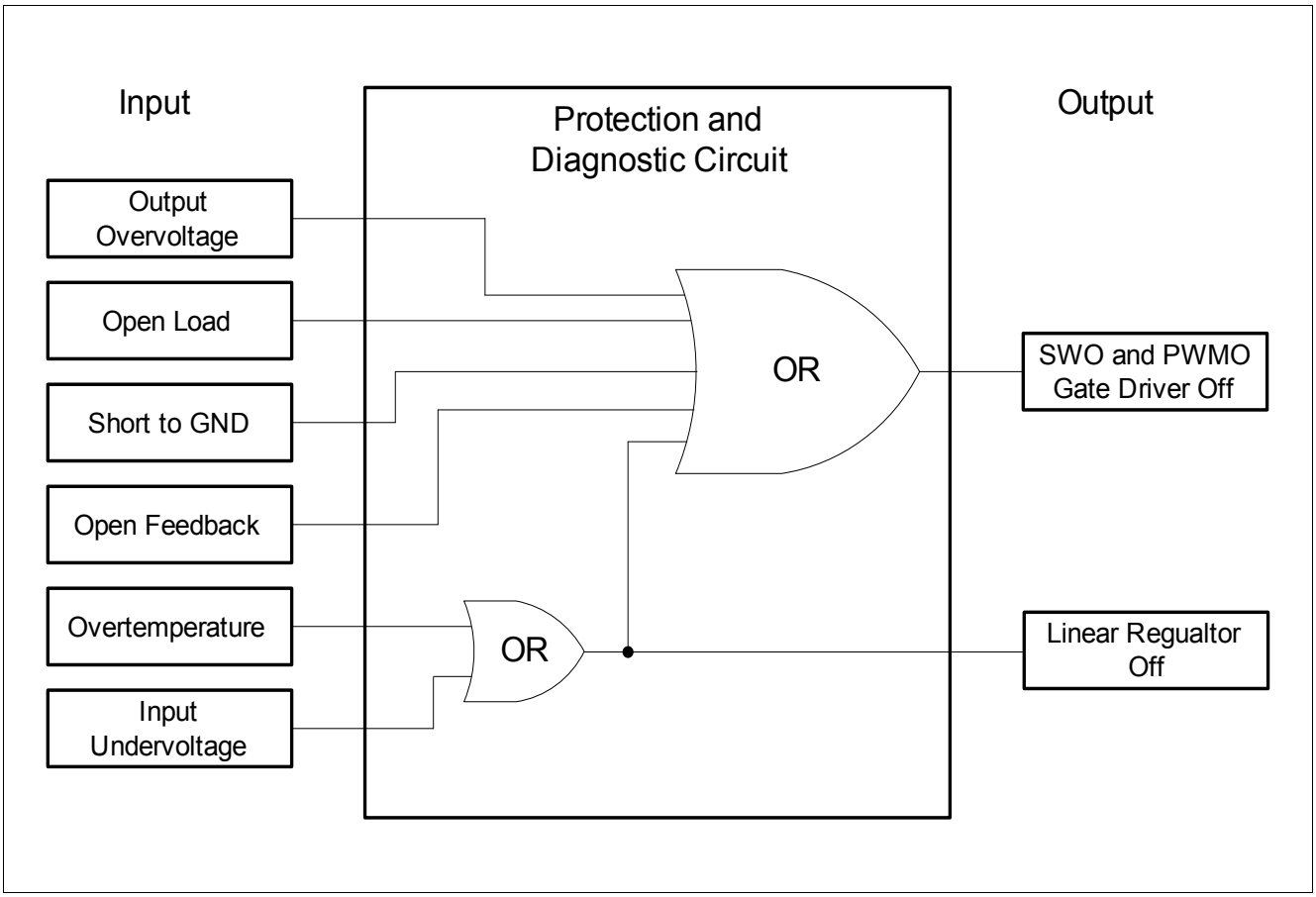
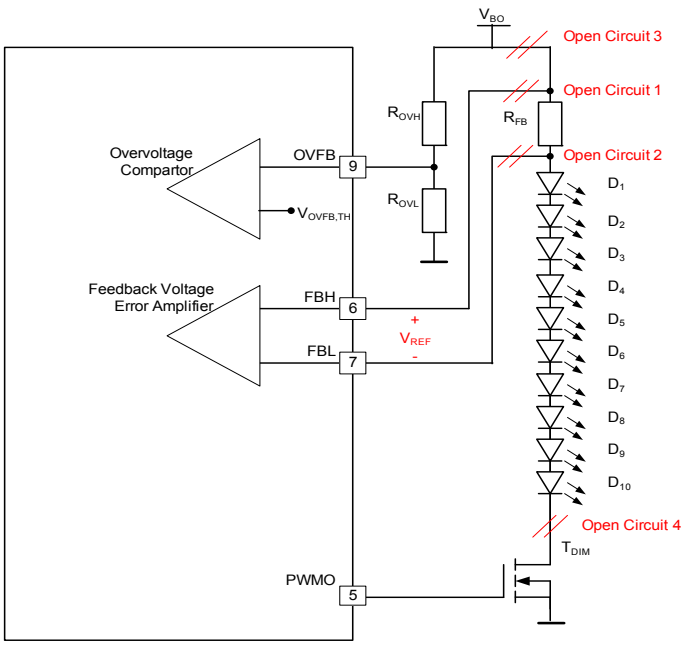


Figure 9 Protection and Diagnostic Function Block Diagram

Input		Output		
Condition	Level*	SWO	PWMO	IVCC
Overvoltage @ Output	False	Sw*	H or Sw*	Active
	True	L	L	Active
Open Load	False	Sw*	H or Sw*	Active
	True	L	L	Active
Short to GND @ LED chain	False	Sw*	H or Sw*	Active
	True	L	L	Active
Open Feedback	False	Sw*	H or Sw*	Active
	True	L	L	Active
Overtemperature	False	Sw*	H or Sw*	Active
	True	L	L	Shutdown
Undervoltage @ Input	False	Sw*	H or Sw*	Active
	True	L	L	Shutdown

*Note:
Sw = Switching
False = Condition does not exist
True = Condition does exist

Figure 10 Diagnosis Truth Table



Output Open Circuit Conditions

Open Circuit Condition	Fault Condition	Fault Threshold Voltage V_{REF}
1	Open FBH	-20 to -100 mV
2	Open FBL	0.5 to 1.0 V
3	Open VBO	-20 to -100 mV
4	Open PWMO	Detected by overvoltage

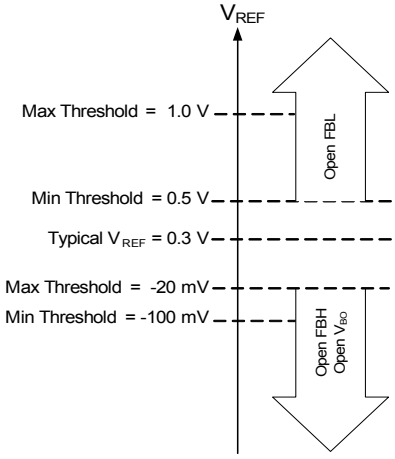


Figure 11 Open Load and Open Feedback Conditions

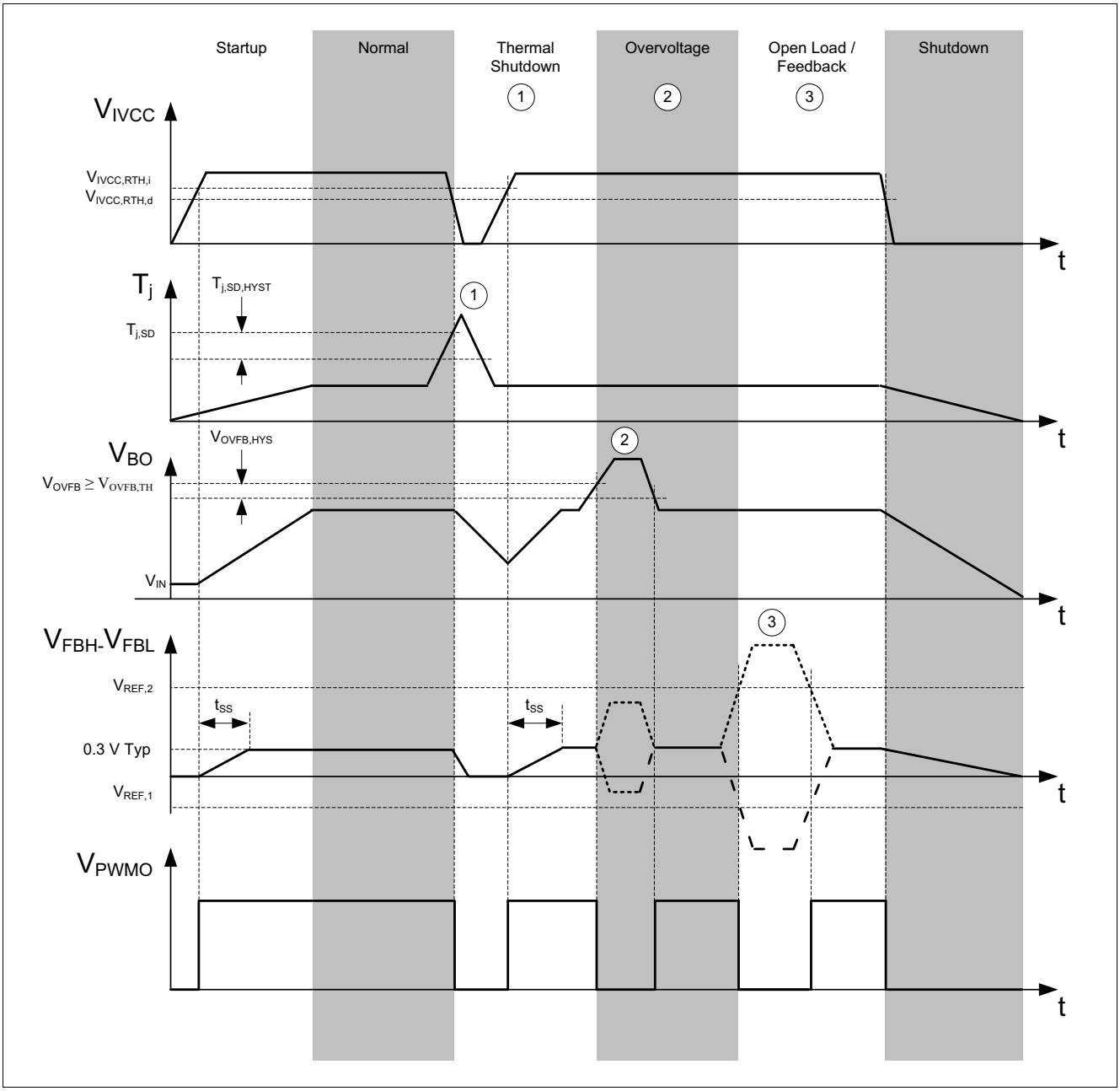


Figure 12 Open load, Overvoltage and Overtemperature Timing Diagram

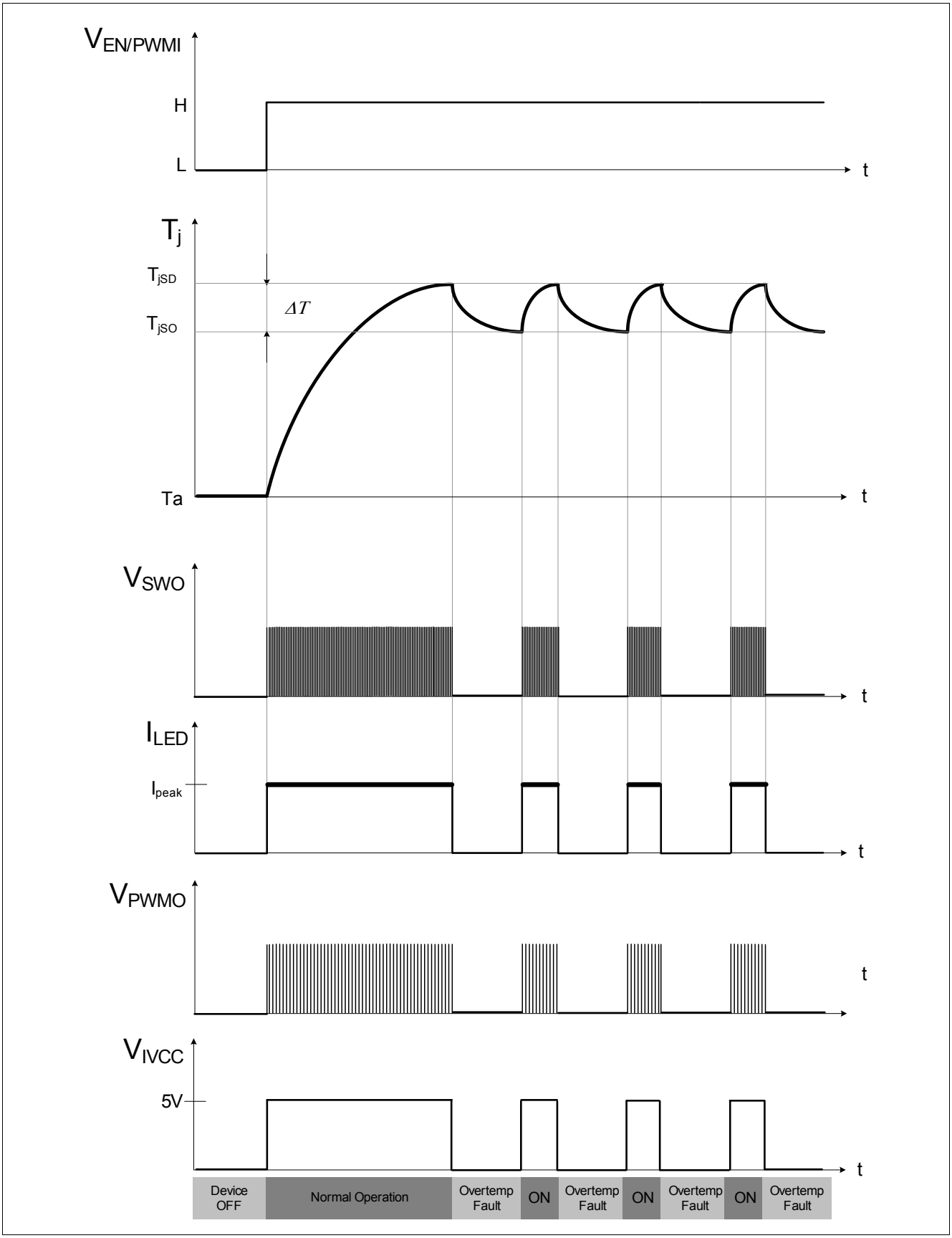


Figure 13 Device overtemperature protection behavior