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Email & Skype: info@chipsmall.com Web: www.chipsmall.com
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ILD2111

Digital DC/DC Buck Controller IC

Datasheet

Revision 1.0, 2015-04-08

Power Management & Multimarket

Digital DC/DC Controller with I-Set

Product highlights

- Assumes control of functionality where a microcontroller is required in conventional systems
- Device configurable by a comprehensive parameter set
- High efficiency over wide input and output ranges
- High accuracy of +/-5% over output current range and useful temperature

PG-DSO-8-58

Features

- Hysteretic current regulation
- Output current adjustable in up to 16 steps with a dynamic range of 1:4 between min. and max. configurable by an external resistor
- Flicker-free and phase-aligned PWM dimming based on input PWM signal
- Fully configurable internal and external smart overtemperature protection
- Open/short load protection
- Overpower protection

Applications

- LED drivers, e.g. 2-stage professional lighting systems
- Integrated electronic control gear for LED luminaires

Description

The ILD2111 is a high-performance microcontroller-based digital DC/DC buck LED controller, designed as a constant current source. The driving current is adjustable with a simple external resistor. Flicker-free dimming supported by means of phase-aligned PWM LED current. An ASSP digital microcontroller-based engine is highly configurable using a comprehensive parameter set to provide fine tuning of operation and protection features. High-precision hysteretic output current regulation is achieved thanks to the digital control loops.

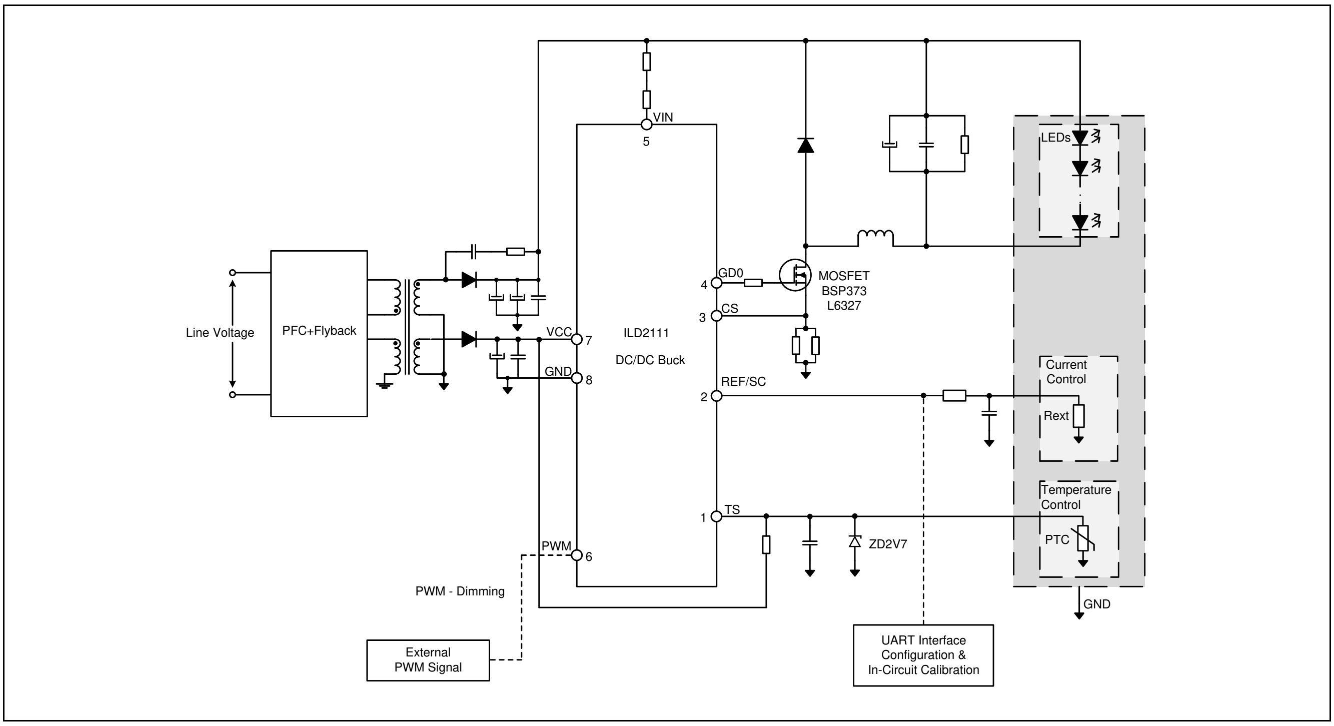

Figure 1. Typical Application

Product type	Package
ILD2111	PG-DSO-8-58

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1 Pin Configuration and Description

The pin configuration is shown in **Figure 2** and **Table 1-1**. The pin functions are described later.

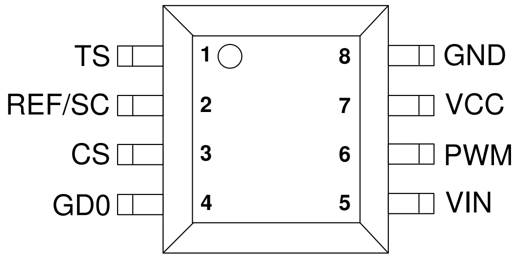


Figure 2. Pin Configuration

Table 1-1. Pin Definitions and Functions

Symbol	Pin	Type	Function
TS	1	I	**Temperature Sensor** The pin TS is used for external temperature measurement using PTC or an appropriate passive temperature sensor.
REF/SC	2	IO	**Reference/Serial Communication** The pin REF/SC is multiplexed. During startup it is used for reference current sensing by means of an external RC circuit. Afterwards, it serves as a UART serial communication interface.
CS	3	I	**Current Sense** Current measurement on an external shunt resistor.
GD0	4	O	**Gate Driver Output 0** Output for directly driving a power MOS.
VIN	5	I	**Voltage Input** Voltage input measurement. Requires an external series resistor for voltage sensing and current limitation.
PWM	6	I	**PWM Dimming Signal** Input for PWM-based dimming signal.
VCC	7	I	**Positive Voltage Supply** IC power supply.
GND	8	O	**Power and Signal Ground**

2 Block Diagram

The block diagram of ILD2111 is shown in **Figure 3**.

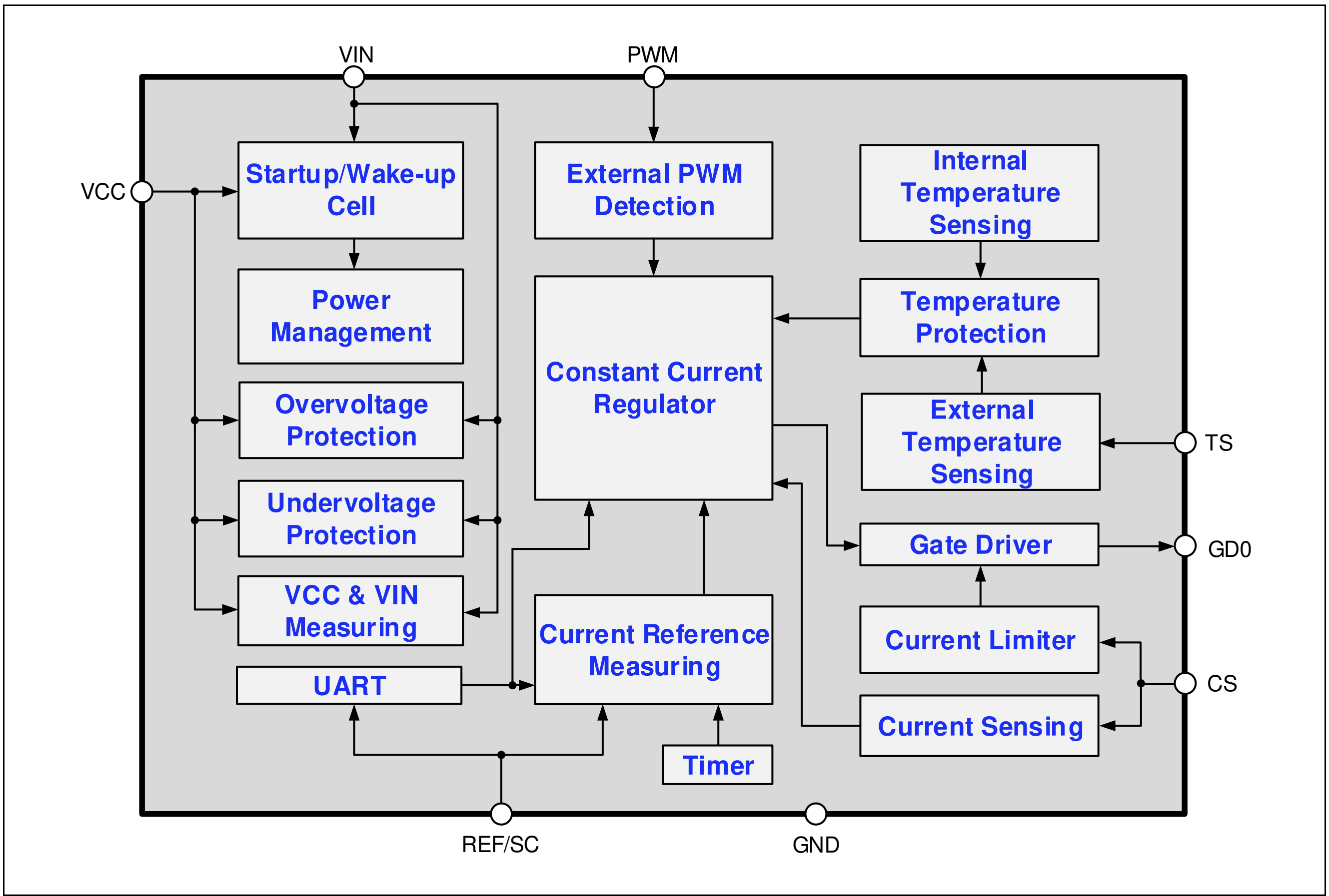


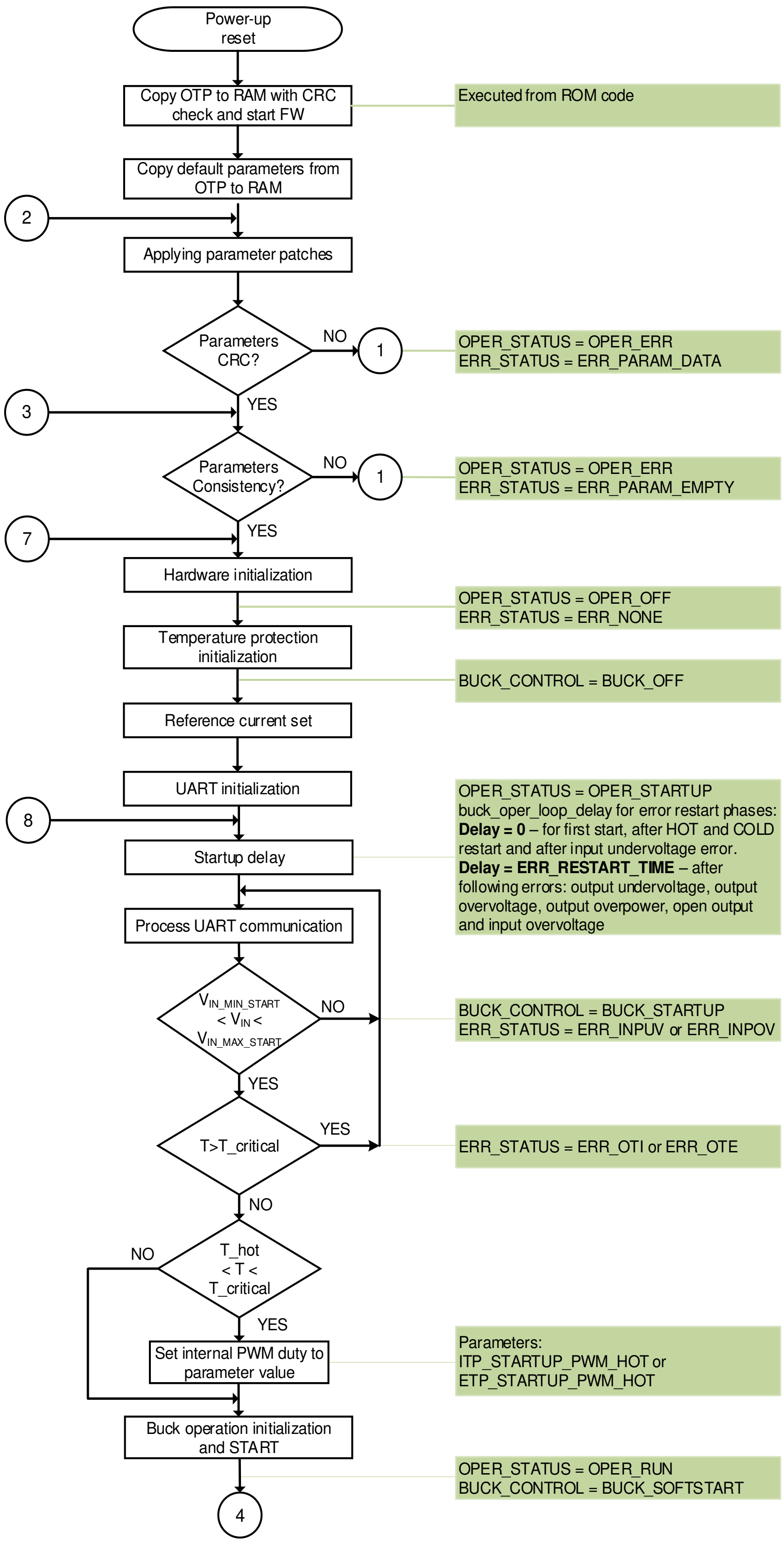
Figure 3. Block Diagram

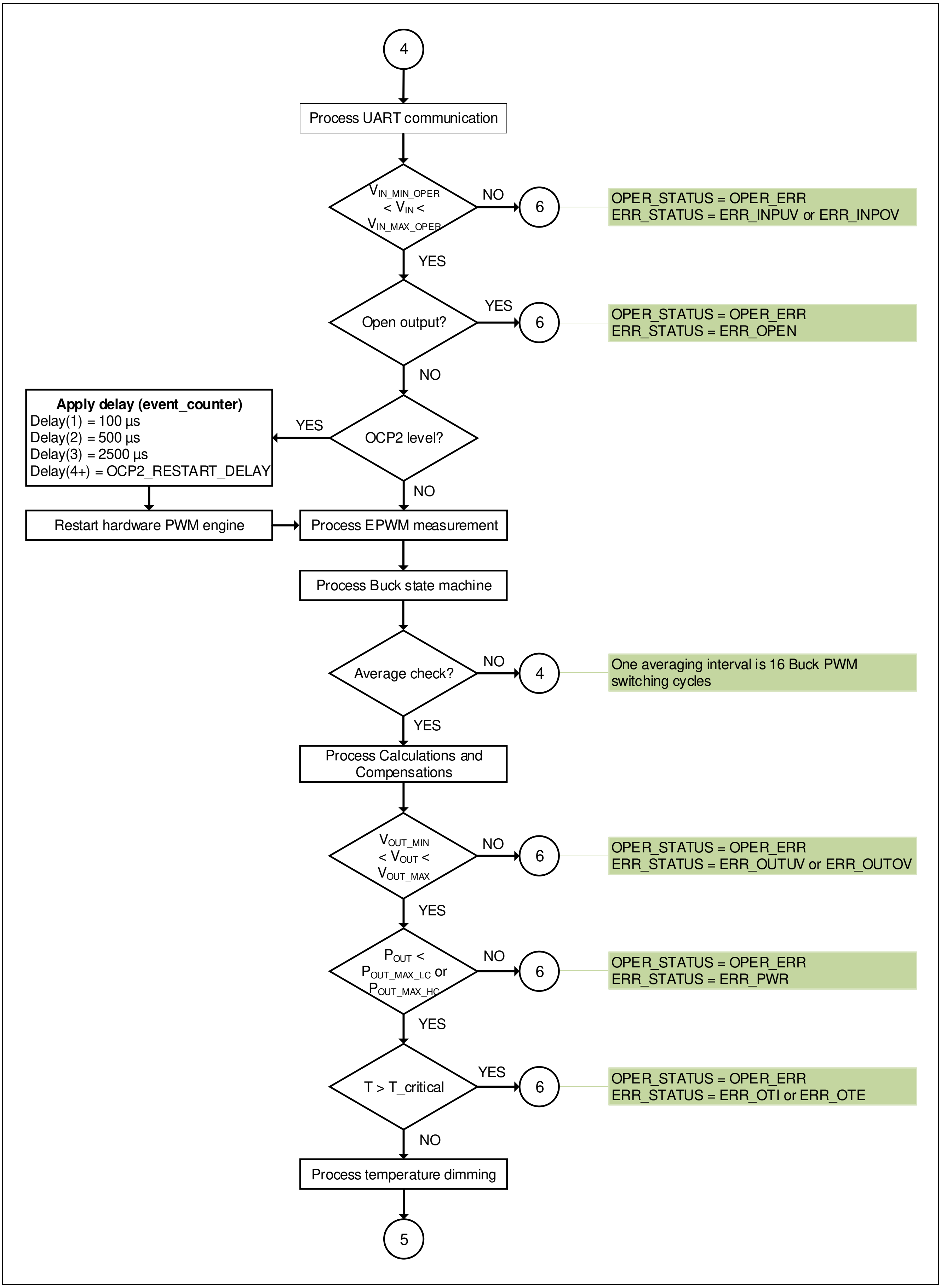
3 Functional Description

The functional description provides an overview of the integrated functions and features, and their relationship. The parameters and equations provided are based on typical values at T_A = 25°C. The corresponding minimum and maximum values are shown in Section **4**, Electrical Characteristics.

3.1 Introduction

The ILD2111 is a high-performance digital microcontroller-based DC/DC buck LED controller designed as a constant current source with hysteretic output current regulation. The controller typically uses a floating buck topology operating in a Continuous Conduction Mode (CCM). In order to reduce switching losses and increase efficiency, as well as to control the switching frequency over a wide variety of external component values, input voltage and load variations, a frequency ripple control is introduced. Both internal and external temperature measurements are implemented and accompanied with an intelligent temperature protection algorithm with two threshold values. The controller utilizes a variety of protection features, including overpower, open and short load conditions. The ILD2111 is a dimmable device controlled by an external PWM signal. The device can be parameterized by means of a single pin UART interface at the REF/SC pin (see Section **3.9**). A complete top-level device operation process, including protection and error handling, is shown in **Figure 4**. **Table 3-1** shows device operating statuses, buck statuses associated with the buck state machine, as well as error and associated error codes. The buck state machine diagram is shown in **Figure 5**.


Power-up reset
Copy OTP to RAM with CRC check and start FW
Executed from ROM code
Copy default parameters from OTP to RAM
2
Applying parameter patches
Parameters CRC?
NO
1
OPER_STATUS = OPER_ERR
ERR_STATUS = ERR_PARAM_DATA
YES
3
Parameters Consistency?
NO
1
OPER_STATUS = OPER_ERR
ERR_STATUS = ERR_PARAM_EMPTY
YES
7
Hardware initialization
OPER_STATUS = OPER_OFF
ERR_STATUS = ERR_NONE
Temperature protection initialization
BUCK_CONTROL = BUCK_OFF
Reference current set
UART initialization
8
Startup delay
OPER_STATUS = OPER_STARTUP
buck_oper_loop_delay for error restart phases:
Delay = 0 – for first start, after HOT and COLD restart and after input undervoltage error.
Delay = ERR_RESTART_TIME – after following errors: output undervoltage, output overvoltage, output overpower, open output and input overvoltage
Process UART communication
V_IN_MIN_START < V_IN < V_IN_MAX_START
NO
BUCK_CONTROL = BUCK_STARTUP
ERR_STATUS = ERR_INPUV or ERR_INPOV
YES
T>T_critical
YES
ERR_STATUS = ERR_OTI or ERR_OTE
NO
T_hot < T < T_critical
NO
YES
Set internal PWM duty to parameter value
Parameters:
ITP_STARTUP_PWM_HOT or
ETP_STARTUP_PWM_HOT
Buck operation initialization and START
OPER_STATUS = OPER_RUN
BUCK_CONTROL = BUCK_SOFTSTART
4


4
Process UART communication
V_IN_MIN_OPER < V_IN < V_IN_MAX_OPER
NO
6
OPER_STATUS = OPER_ERR
ERR_STATUS = ERR_INPUV or ERR_INPOV
YES
Open output?
YES
6
OPER_STATUS = OPER_ERR
ERR_STATUS = ERR_OPEN
NO
OCP2 level?
YES
Apply delay (event_counter)
Delay(1) = 100 µs
Delay(2) = 500 µs
Delay(3) = 2500 µs
Delay(4+) = OCP2_RESTART_DELAY
NO
Restart hardware PWM engine
Process EPWM measurement
Process Buck state machine
Average check?
NO
4
One averaging interval is 16 Buck PWM switching cycles
YES
Process Calculations and Compensations
V_OUT_MIN < V_OUT < V_OUT_MAX
NO
6
OPER_STATUS = OPER_ERR
ERR_STATUS = ERR_OUTUV or ERR_OUTOV
YES
P_OUT < P_OUT_MAX_LC or P_OUT_MAX_HC
NO
6
OPER_STATUS = OPER_ERR
ERR_STATUS = ERR_PWR
YES
T > T_critical
YES
6
OPER_STATUS = OPER_ERR
ERR_STATUS = ERR_OTI or ERR_OTE
NO
Process temperature dimming
5

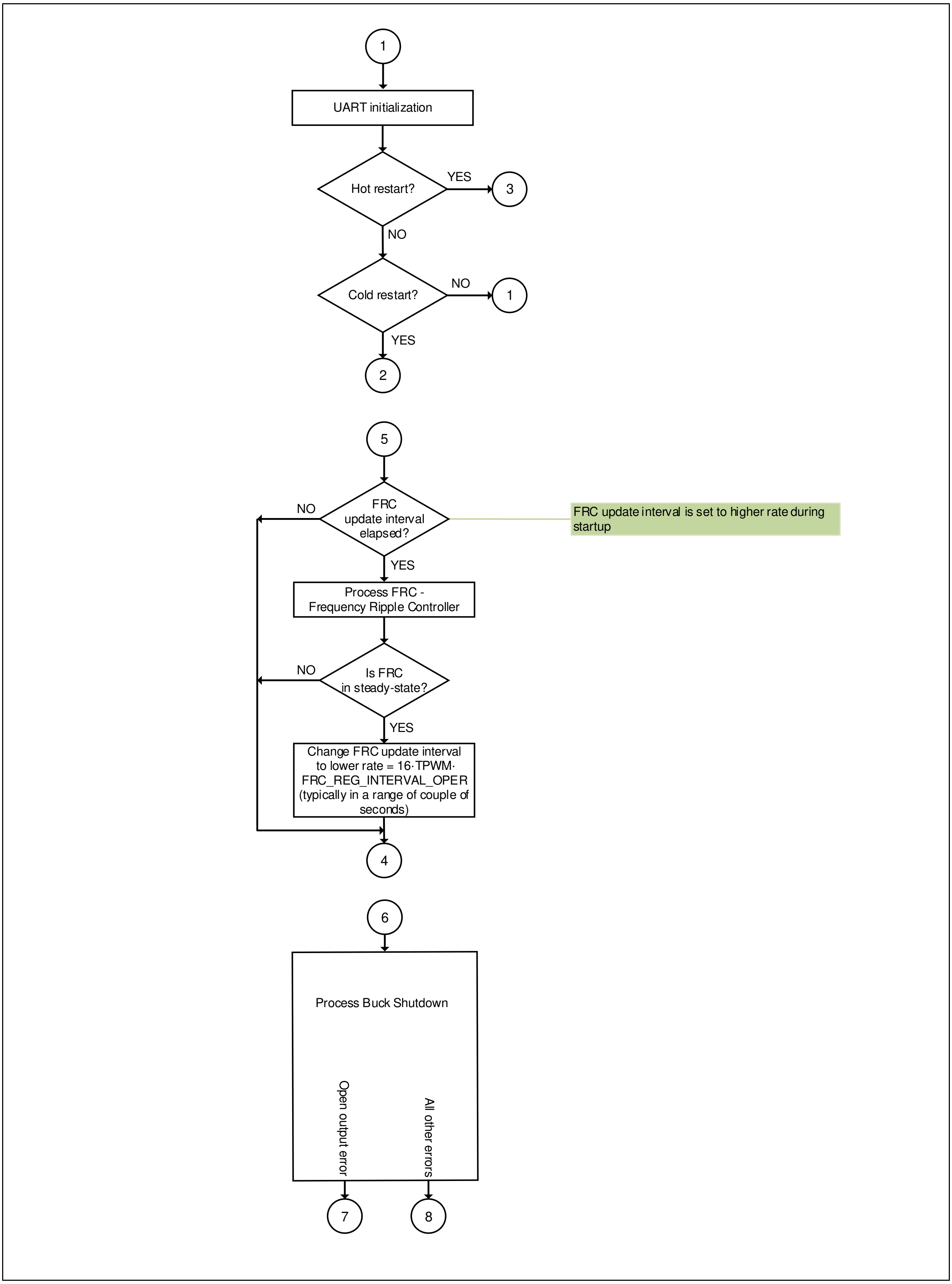


Figure 4. Device Operating Flowchart

Operating statuses are presented in **Table 3-1** below.

Table 3-1. Device Operating Statuses

Status		**Value**	**Description**
OPER_STATUS	OPER_OFF	0000_H	Off - initial buck state
	OPER_STARTUP	0001_H	Startup - Vin & temperature checking
	OPER_RUN	0002_H	Run
	OPER_ERR	0004_H	Stopped by error
	OPER_STOP	0008_H	Stopped by UART command
ERR_STATUS	ERR_NONE	0000_H	No errors
	ERR_INPUV	0001_H	Input undervoltage
	ERR_INPOV	0002_H	Input overvoltage
	ERR_OUTUV	0004_H	Output undervoltage
	ERR_OUTOV	0008_H	Output overvoltage
	ERR_PWR	0010_H	Output overpower
	ERR_OPEN	0020_H	Output open
	ERR_OCP	0040_H	OCP2 level detection
	ERR_OTI	0080_H	Overtemperature internal sensor
	ERR_OTE	0100_H	Overtemperature external sensor
	ERR_PARAM_EMPTY	0400_H	Default parameter block empty
	ERR_PARAM_DATA	0800_H	Default parameter block checksum error
ERR_MODE	ERR_MODE_LATCH		Error handling latch
	ERR_MODE_RESTART		Error handling auto restart
	ERR_MODE_OFF		Error handling is off
	ERR_MODE_NOP		Error handling does not affect auto restart counter
BUCK_STATUS [1)]	BUCK_OFF		Buck is off
	BUCK_STARTUP		Buck is in start-up phase (initialized, waiting for start-up condition, i.e. voltage and temperature)
	BUCK_SOFTSTART		Buck is in soft-start phase (implements increasing current slope until reaching reference current)
	BUCK_SHUTDOWN		Buck is in shutdown phase (implements current decreasing slope)
	BUCK_EXE_OFF		Buck is executing off, buck operation stopped
	BUCK_ERRC		Buck in error state (generate small error current)
	BUCK_ON [2)]		Buck is on (normal operation, default state of operation) During normal operation, in addition to the aforementioned operations, the following actions will be executed: − Open-output processing − Output current PWM dimming processing − V_{CC} / internal temperature measurement and processing − External temperature measurement and processing − OCP1 - peak current processing − OCP2 - peak current processing − EPWM measurement and processing − PI regulator processing − Input over- and undervoltage processing − Output over- and undervoltage processing − Output overpower processing

1) See buck state machine in **Figure 5**.

2) The number of averaged buck cycles for steady-state operation, where calculations and protections are handled, is defined by the constant Buck_steady_delay (see **Table 3-14**).

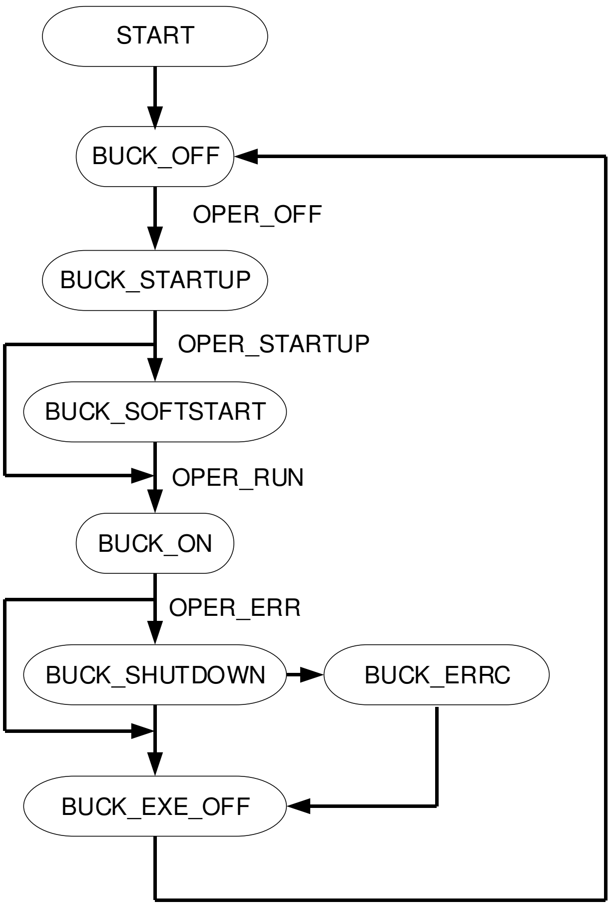


Figure 5. Buck State Machine

3.2 Main Supply (VCC)

The device is powered via the VCC pin. All device supply voltages are internally generated from the V_{CC} voltage.

3.3 Controller Features

Table 3-2 gives an overview of the controller features that are described in the referenced sections.

Table 3-2. Controller Features

Configurable Leading Edge Blanking (LEB) and Sample Time at Pin CS	Section 3.3.1
Configurable Gate Driver Output	Section 3.3.2
Reference Current Setup	Section 3.3.3
Output Current Control and Measuring	Section 3.3.4
Current Startup, Soft-Start and Shutdown Control	Section 3.3.5

3.3.1 Configurable Leading Edge Blanking (LEB) and Sampling Time at Pin CS

A configurable leading edge blanking time t_{CSLEB} is integrated into the current sensing path to provide more accurate output current sensing and regulation. Leading-edge spikes during the PowerMOS switch-on phase, as shown in **Figure 6**, can affect sampled output current values, resulting in imprecise current sensing. The LEB time is used to prevent false overcurrent detection, while the sample time defines the moment of the current sampling for A/D conversion. The time t_{CSLEB} and the sampling time are configured by the constants CS_blanking_time and CS_sample_time respectively (see **Table 3-19**) in order to provide output current sampling at the moment when no spikes are present.

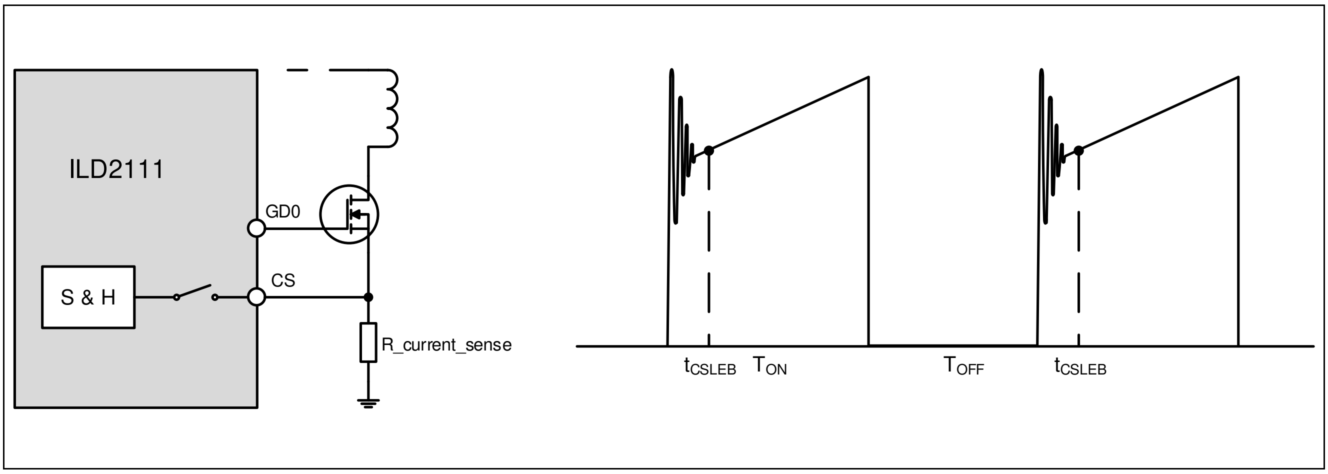


Figure 6. Configurable Leading Edge Blanking Time at Pin CS

3.3.2 Configurable Gate Driver Output

The gate driver output (GD0) can be configured with respect to the final voltage level and gate drive current, which influence the rising voltage slope for switching on the external PowerMOS (see **Figure 7**) and therefore a switch-on time. A compromise should and could be made between switching power losses and electromagnetic radiation by using these parameters (especially gate drive current values). The output gate voltage V_{GDH} and gate current I_{GD} can be programmed by the parameters, providing an adjustable PowerMOS turn-on time. The programmable output gate voltage range is from 4.5 V to 15 V (see **Table 3-8**). V_{GDH} cannot be higher than the power supply voltage V_{CC}, regardless of the programmed value. The programmable gate current range is from 30 mA to 118 mA (see **Table 3-8**). **Figure 7** shows the gate driver output voltage signal. Different rising slopes correspond to different gate driving currents. The slope is proportional to the current.

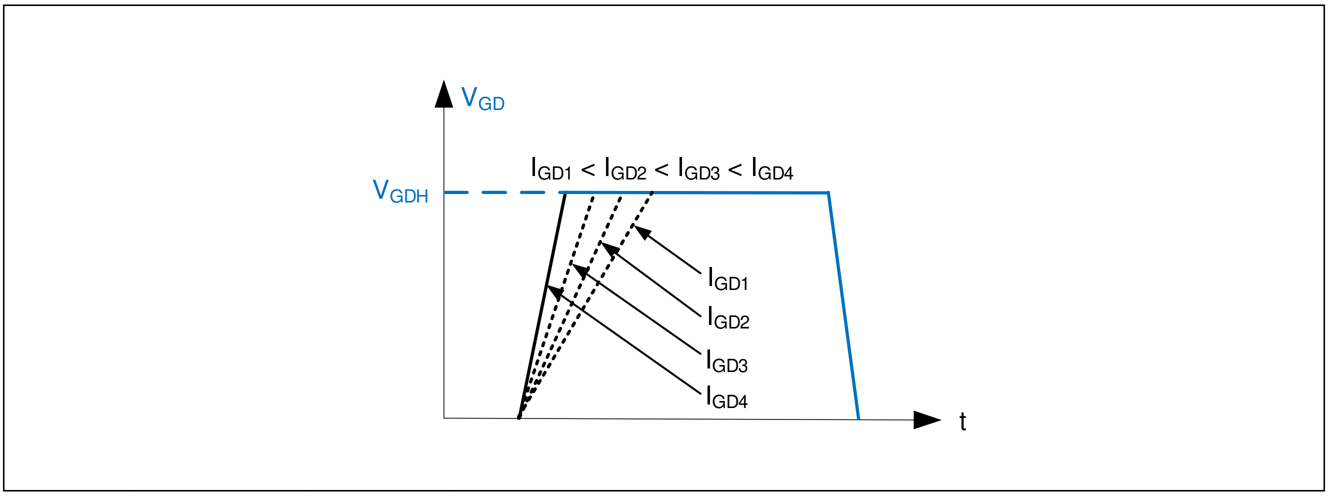


Figure 7. Configurable Gate Driver Output

3.3.3 Reference Current Setup

The reference current value is obtained by measurement using the value of the external resistor R_iset connected to the pin 'REF/SC' together with the reference capacitor C_ref via the discharge time of the capacitor (see **Figure 8** and **Figure 9**). Depending on the resistance of R_iset, the appropriate reference current, stored in a table of 16 currents (see **Table 3-12**), is used as a reference for the output current. The reference current setup procedure (I-set) will always be executed during the startup sequence or during Open output protection recovery – see Section **3.6.4**.

When the internal switch SW is turned on for a short period of time defined by the constant RC_cap_charge_time (see **Table 3-19**) while the digital output is high, the C_ref is fully charged to Vcref**,** where this voltage depends on the internal VDDP voltage and voltage divider R_ref_sc – R_iset. R_ref_sc is used for decoupling the reference current measurement circuitry and serial UART communication. Care must be taken that the ratio of R_iset to R_ref_sc is sufficient to have only a low impact on Vcref. Otherwise, it has to be included in the time thresholds calculation. When the switch is turned off, the C_ref discharges through the external resistor R_iset. The discharging time of the capacitor C_ref depends on the value of the external resistor. During the discharging interval, the pin voltage is measured by ADC while an internal timer measures the discharging time. When the capacitor voltage drops below the constant threshold level V_adc_th (constant V_ADC_th, see **Table 3-13**), the internal timer value is latched and used to determine the reference current from the predefined I-set table.

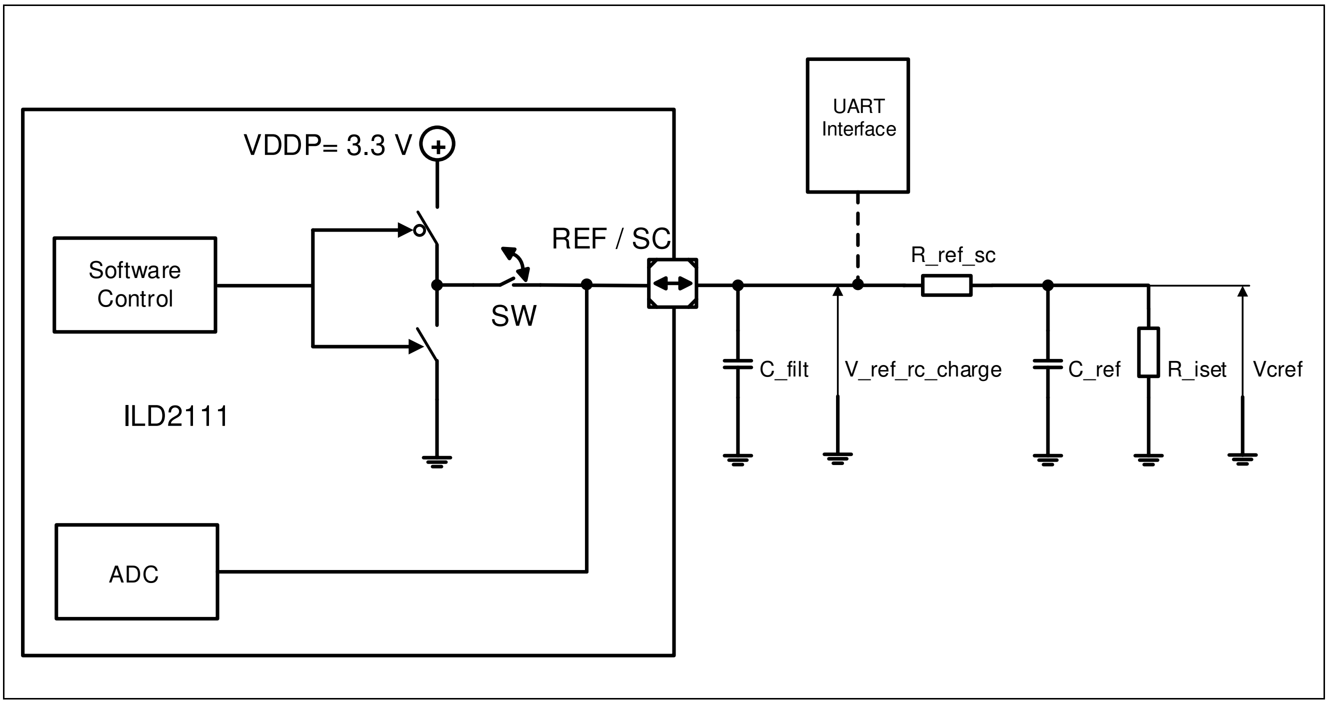


Figure 8. Charging and Discharging of the C_ref Capacitance Depending on the Switch State

C_filt is a ceramic capacitor used to filter noise, caused by the converter switching operation. Mainly it is used to suppress noise for ADC measurement as well as UART communication.

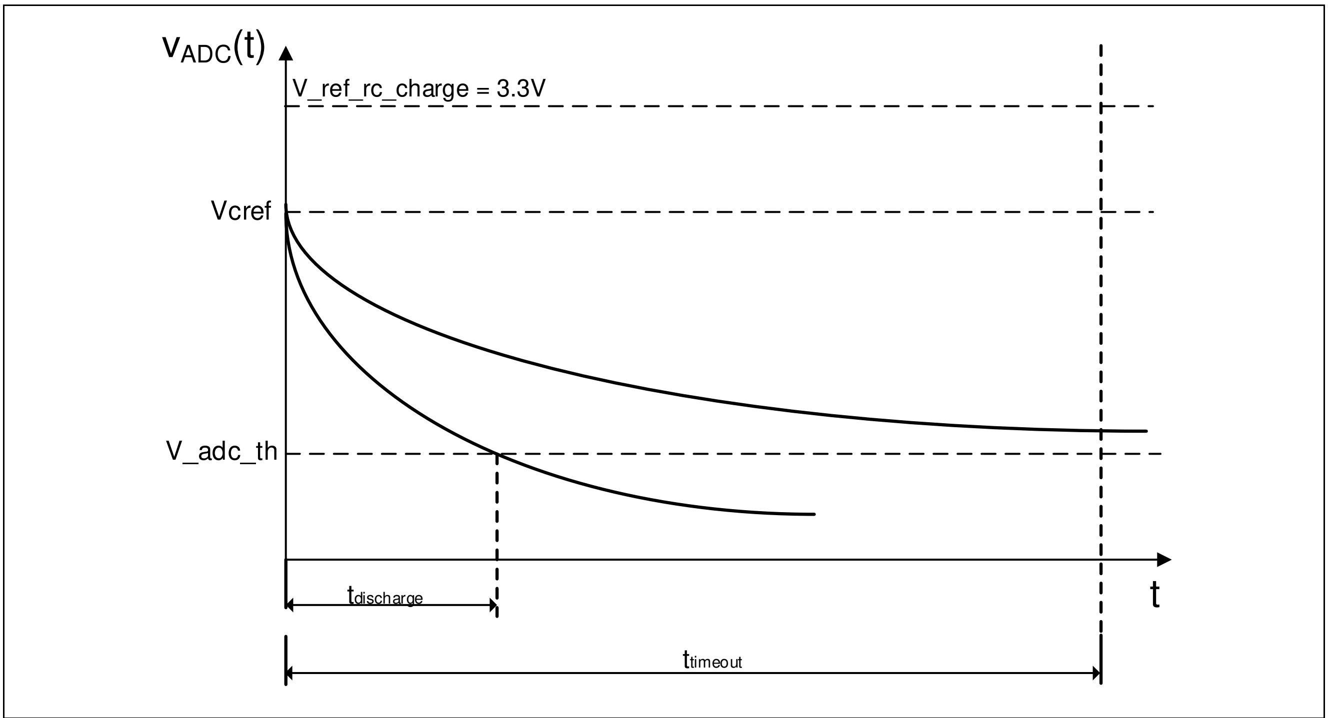


Figure 9. C_ref Discharging Interval Determined by the Reference Resistor Value

The charging voltage Vcref is calculated as:

$$Vcref = \frac{R\_iset}{R\_iset + R\_ref\_sc} \cdot V\_ref\_rc\_charge. \quad (1)$$

The equation for V_adc_th is:

$$V\_adc\_th = Vcref \cdot e^{-\frac{t_{discharge}}{R\_iset \cdot C\_ref}}. \quad (2)$$

Therefore:

$$t_{discharge} = R\_iset \cdot C\_ref \cdot ln \frac{Vcref}{V\_adc\_th}. \quad (3)$$

If a lower voltage threshold is not reached after the predefined time-out period $t_{timeout}$ (constant RC_measurement_timeout, see **Table 3-19**), the reference current determination process ends and the last value from the current table is taken as the reference (Ref_current_16, see **Table 3-12**). Component values and their tolerances must provide unique thresholds in order to be detected appropriately (see **Figure 10**).

More accurate equations will be obtained if typical component tolerance values are included.
The following are assumed:

- Maximum reference resistance: R_iset_max(n) = R_iset(n) + R_iset_tolerance[1]
- Minimum reference resistance: R_iset_min(n) = R_iset(n) - R_iset_tolerance
- Maximum reference capacitance: C_ref_max = C_ref + C_ref_tolerance[2]
- Minimum reference capacitance: C_ref_min = C_ref - C_ref_tolerance

[1] *The reference resistance R_ref_sc is used to decouple the UART interface and current set resistance R_iset due to multiplexed functionality of the REF/SC pin. In this case, the tolerance of the R_ref_sc resistance is not taken into account (its tolerance is ignored).*
[2] *Examples of C_ref_tolerance are the tolerance of the used capacitor as well as the cable capacitance that connects R_iset to the detection circuit.*

Therefore, minimum and maximum discharging times are given by:

$$T\_RC\_(n)\_min = R\_iset\_min(n) \cdot C\_ref\_min \cdot ln \frac{Vcref\_min(n)}{V\_adc\_th} \quad (4)$$

and

$$T\_RC\_(n)\_max = R\_iset\_max(n) \cdot C\_ref\_max \cdot ln \frac{Vcref\_max(n)}{V\_adc\_th}. \quad (5)$$

Where n is the ordinal number of the resistor, while Vcref_min and Vcref_max are the minimum and maximum voltage values of charged capacitance respectively:

$$Vcref\_min = \frac{R\_iset\_min}{R\_iset\_min + R\_ref\_sc} \cdot V\_ref\_rc\_charge \quad (6)$$

and

$$Vcref\_max = \frac{R\_iset\_max}{R\_iset\_max + R\_ref\_sc} \cdot V\_ref\_rc\_charge. \quad (7)$$

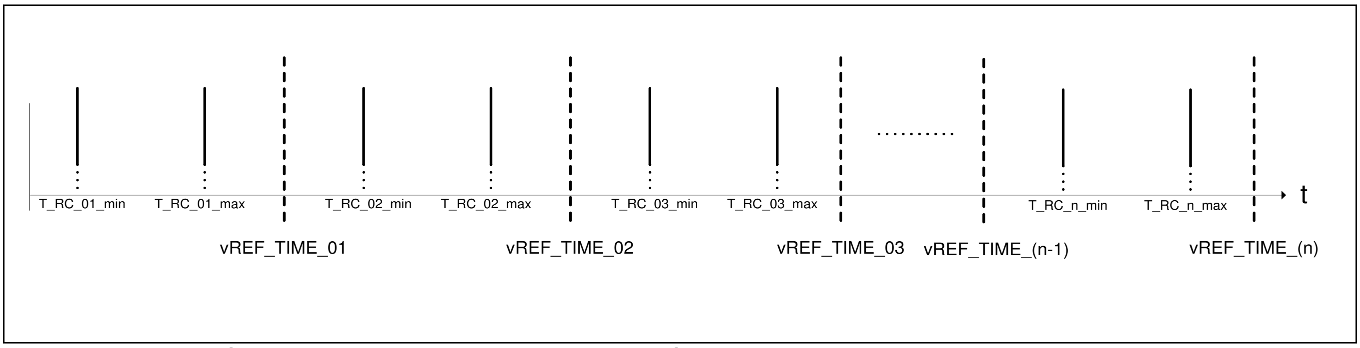


Figure 10. Time Constant vREF_TIME_n Threshold Calculations

As shown above, the discharging time threshold is obtained as follows:

$$vREF\_TIME\_n = T\_RC\_n\_max + \frac{T\_RC\_(n+1)\_min - T\_RC\_n\_max}{2}. \quad (8)$$

The last discharge time threshold is given by:

$$vREF\_TIME\_n = T\_RC\_n\_max + \frac{T\_RC\_n\_max - T\_RC\_n\_min}{2}. \quad (9)$$

The measured discharge time - $t_{discharge}$ is compared with the calculated thresholds, beginning with the smallest, and based on that, it will be determined which reference resistor is detected, hence reference output current. For example, if the measured discharge time is greater than vREF_TIME_01, vREF_TIME_02, vREF_TIME_03 and smaller than vREF_TIME_04, the 4th reference resistor and reference current from the list will be chosen (see **Table 3-3**).

The ratio between the maximum and minimum current has to be equal to or less than 4 (I_ref_max / I_ref_min ≤ 4) for best current accuracy. For example, if the minimum reference current is 250 mA, the maximum reference current from the range should not exceed 1000 mA.

The components (R_iset, C_ref) must be carefully selected to avoid overlapping time intervals, because in that case an appropriate threshold could not be calculated to provide unique detection. For example, if the resistance values are too close (including tolerances), discharge time intervals will overlap, and calculated thresholds will be set inside the overlapped area. Therefore it cannot be guaranteed that the same current will be selected across different IC production series and external component tolerances.
Reference current determination only takes place during the initial chip startup and after the load has been disconnected - open output is detected. During normal buck operation, the REF/SC pin can be used as a communication port.

Example
For typical applications, which cover – for example – the outputs ranging from 250 mA to 800 mA (in 50 mA steps), reference resistor values for the specific current values (assuming C_ref = 10 nF and threshold voltage value of V_adc_th = 0.6075 V) are given in **Table 3-3**. Resistors from the series E96 with a variation (tolerance) of 1% are used. The reference pin serial resistor is R_ref_sc = 3.3 kΩ. The recommended capacitor C_ref tolerance should be ≤ 5%[1]. The recommended C_ref capacitor type is a zero-drift CoG (NPO).

Table 3-3. Reference Resistor Values Example

Ordinal number	I_ref_n [mA]	R_iset_n [kΩ]	vREF_TIME_n [µs]
1	800	2.15	70
2	750	10.00	180
3	700	15.00	280
4	650	21.50	430
5	600	33.20	610
6	550	43.20	780
7	500	53.60	950
8	450	63.40	1110
9	400	71.50	1270
10	350	82.50	1430
11	300	90.90	1580
12	250	100.00	1860

Although, typically, the application uses less than 16 reference currents, all parameters (Ref_current_01- Ref_current_16, see **Table 3-12**) must be filled (arranged) in 4 groups, using copies with the same reference current. It is assumed that approximately the same currents have approximately the same parameters. Thereafter, all appropriate reference time thresholds (Reference_time_01 – Reference_time_16) will be automatically allocated to the groups (see **Table 3-19**). Each group consists of four consecutive currents and each group is associated with the unique set of FRC parameters. The currents from the same group will have the same minimum and maximum switching frequency limits and minimum and maximum current ripple limits as well (see **Table 3-20**).
One possible arrangement is given below in **Table 3-4**.

[1] *For different component tolerances, different discharge times will be obtained by equations. The resistor values in* ***Table 3-3*** *are given as examples. The number of different reference resistor values must match the number of different reference currents. For different applications (different output currents and output power), different values of the external resistors can be taken.*

Table 3-4. Reference Current Arrangement

Group number	Reference Currents
1.	800 mA, 750 mA, 700 mA
2.	650 mA, 600 mA, 550 mA
3.	500 mA, 450 mA, 400 mA
4.	350 mA, 300 mA, 250 mA

3.3.4 Output Current Control and Measuring

The output current is measured at the CS pin by means of an external shunt resistor. The controller, using floating buck topology, operates in a Continuous Conduction Mode (CCM) and is realized as a hysteretic current controller. The average output current is regulated using minimum and maximum currents (I_{MAX} and I_{MIN}, see **Figure 11**). Maximum and minimum current values are defined with respect to allowed output current ripple. The maximum current is set as a true analog comparator threshold value using an internal DAC. The minimum current value is regulated by the internal PI regulator controlling T_{OFF} time.

When the MOSFET is turned on, T_{ON} is approximately given as follows (all resistances and voltage drops of used components are neglected):

$$T_{ON} = (I_{MAX} - I_{MIN}) \cdot \frac{L_{EXT}}{V_{IN}-V_{OUT}} = I_{RIPPLE} \cdot \frac{L_{EXT}}{V_{IN}-V_{OUT}}. \quad (10)$$

When the MOSFET is turned off, T_{OFF} is approximately given as follows (all resistances and voltage drops of used components are neglected):

$$T_{OFF} = (I_{MAX} - I_{MIN}) \cdot \frac{L_{EXT}}{V_{OUT}} = I_{RIPPLE} \cdot \frac{L_{EXT}}{V_{OUT}}. \quad (11)$$

where V_{IN} and V_{OUT} are the input and output voltages respectively and L_{EXT} is the buck inductance.
Therefore, the switching frequency of the buck cycle can be rendered as:

$$f_{SW} = \frac{1}{T_{ON}+T_{OFF}} = \frac{1}{I_{RIPPLE} \cdot L_{EXT} \cdot (\frac{1}{V_{IN}-V_{OUT}} + \frac{1}{V_{OUT}})}. \quad (12)$$

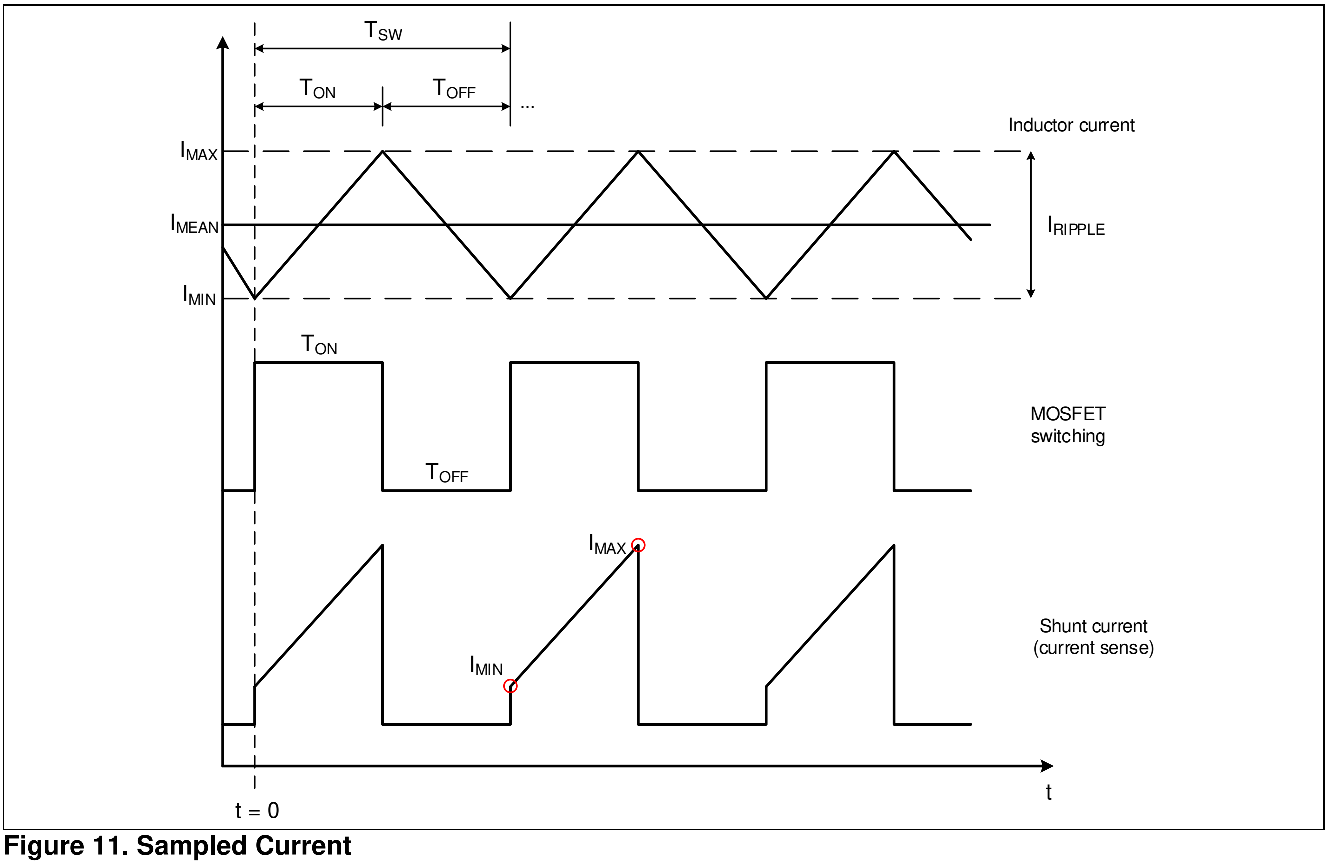


Figure 11. Sampled Current

When the current reaches its maximum value (I_{MAX}), the MOSFET is turned off for a duration of T_{OFF}, which is defined by the output of the PI regulator. After this interval elapses, the MOSFET is turned on again, the minimum current (I_{MIN}) is sampled and the mean current for the entire PWM interval is calculated as:

$$I_{MEAN} = \frac{I_{MAX}+I_{MIN}}{2}. \quad (13)$$

The minimum current samples are averaged and averaging happens every 16 switching cycles. This average value is then compared to a reference providing an error signal for the PI regulator, as shown in **Figure 12**. Based on that error, the PI regulator calculates the new T_{OFF} time resulting in output current regulation, hence closing the regulation loop.

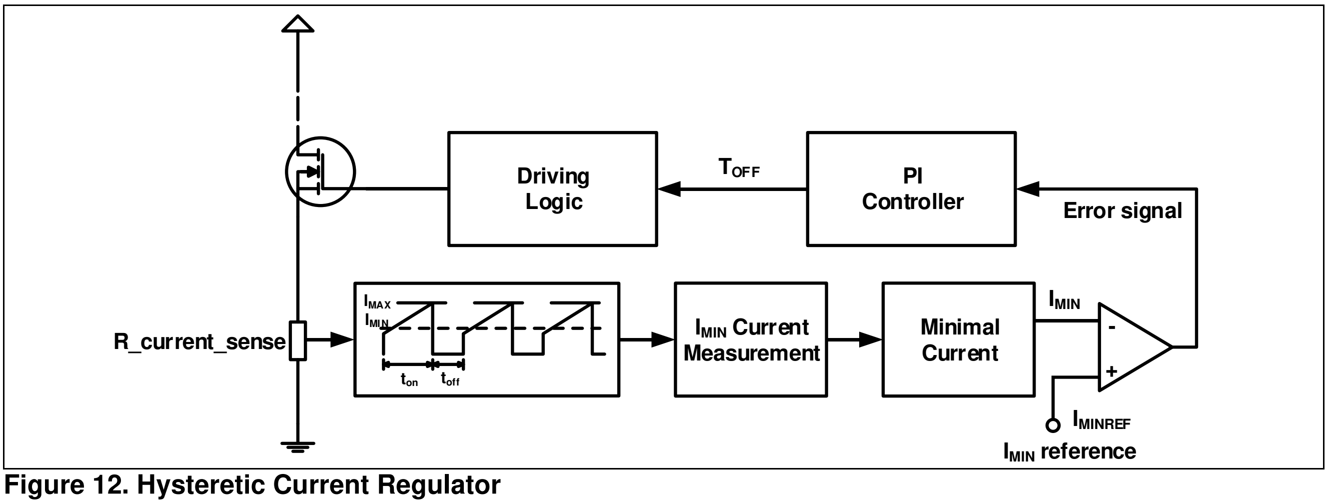


Figure 12. Hysteretic Current Regulator

PI regulator parameters can be adjusted for faster transient response (dynamic behavior) during startup and more stable output current during normal steady-state operation. These constants (PI_shift_softstart_lc, PI_gain_shift_softstart_hc, PI_gain_shift_lc and PI_gain_shift_hc, see **Table 3-17**) are divided into two groups depending on the current range (constant Ref_current_HCTH, see **Table 3-14**) and operating conditions (startup or normal). Constants for low currents (low range - LC) typically have larger values than high current parameter values (high range - HC) because, for lower currents, the error signal has to be multiplied by a larger number (Gain) to obtain appropriate behavior regarding response and stability of the output current.

3.3.5 Current Startup, Soft-Start and Shutdown Control

Current soft-start and shutdown control is implemented in order to keep the input voltage V_{IN} and supply voltage V_{CC}, which come from the primary stage (usually a flyback converter with a transformer auxiliary winding for VCC voltage), within the operating range and stable.

During the soft-start time, the output (mean) current increases slowly with programmable parameters. The startup current is defined by the constant Softstart_start_curr (see **Table 3-16**). Current and time steps are defined by the constant Softstart_curr_step (see **Table 3-16**) and parameter Softstart_time_step respectively (see **Table 3-11**, green line in **Figure 13**). The time step can be set as a number of system ticks (the default value is 100 µs). If any of the step (I_{CSUS} = Softstart_curr_step or t_{CSUS} = Softstart_time_step) values is zero, the buck converter will start with a 100% current, and without soft-start.

During soft shutdown time, the output current decreases slowly with programmable current and time steps (constant Softshutdown_curr_step - **Table 3-16** and parameter Softshutdown_time_step - **Table 3-11**, see red line in **Figure 13**). Hence, the input voltage V_{IN} and supply voltage V_{CC} remain in the operating range and the device will work correctly.
If the soft shutdown is not enough to provide an appropriate operating range (for V_{IN} and V_{CC}), some minimum current (ERROR CURRENT – I_{ERROR}) defined by the parameters Err_refcurrent_max and Err_refcurrent_min (see **Table 3-9** and **Figure 13**) will be generated for a defined time period (error time). When this time interval has elapsed (Error time timeout – constant Err_current_time, see **Table 3-14**), the output current is zero. If the current soft shutdown is not needed, it is necessary to set either the parameter to zero (I_{CSDS} = Softshutdown_curr_step or t_{CSDS} = Softshutdown_time_step).

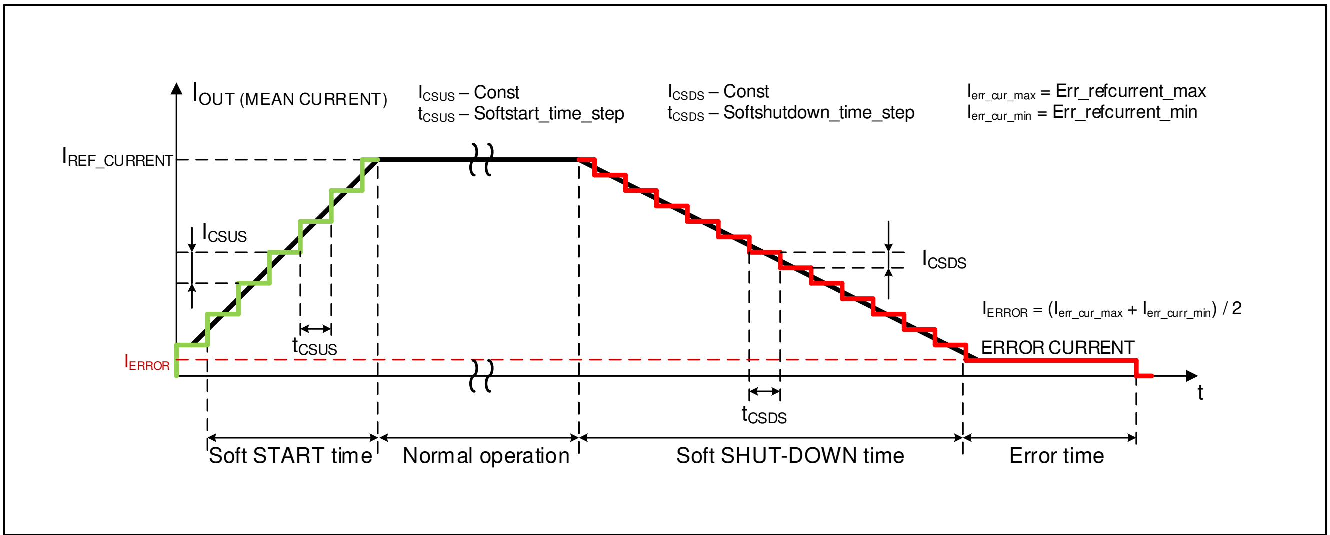


Figure 13. Soft-Start and Soft Shutdown Definitions

3.4 Current Ripple vs. Switching Frequency Control Scheme

The switching frequency and output current ripple must be handled in such a way as to ensure that the efficiency is as high as possible and that the ripple is in a proper range with sufficient margin to the specified maximum. Two options for implementing a suitable system are described below.

3.4.1 Fixed Current Ripple

For a fixed current ripple, it is necessary to choose an appropriate value for the current ripple (parameter Curr_ripple_perc, see **Table 3-12**) so the switching frequency does not exceed the maximum allowed frequency around the output voltage $V_{OUT} = V_{IN}/2$. The maximum switching frequency should not exceed 250 kHz. Examples for three different current values are shown in **Figure 14**.

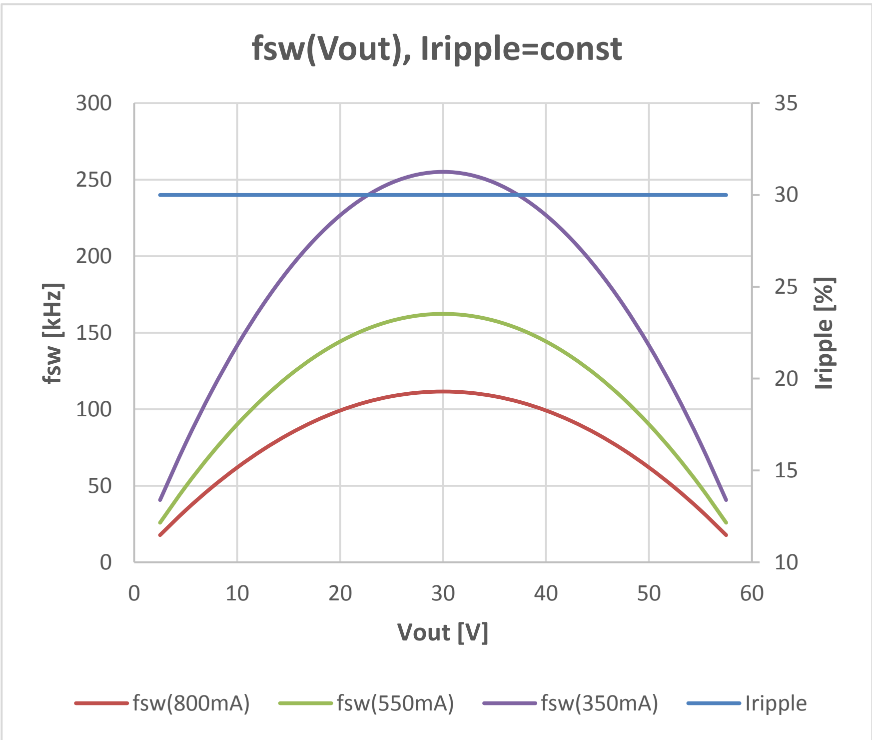


Figure 14. Switching Frequency vs. Output Voltage for Constant Output Current Ripple Iripple = 30%

3.4.2 Frequency and Ripple Control

The ILD2111 supports a powerful Frequency Ripple Controller (FRC) because the switching frequency of the Buck converter is not constant due to different loads (different number of LEDs leading to different output voltages). The main idea is to stabilize the operating point within configurable limits (operating area – green field, see **Figure 15**). During startup and normal operation, the frequency-ripple control update interval is defined by the constants FRC_reg_interval_start and FRC_reg_interval_oper (see **Table 3-20**). The number of FRC passes, before being considered steady, is defined by the constant FRC_pass_oper_th (see **Table 3-20**).

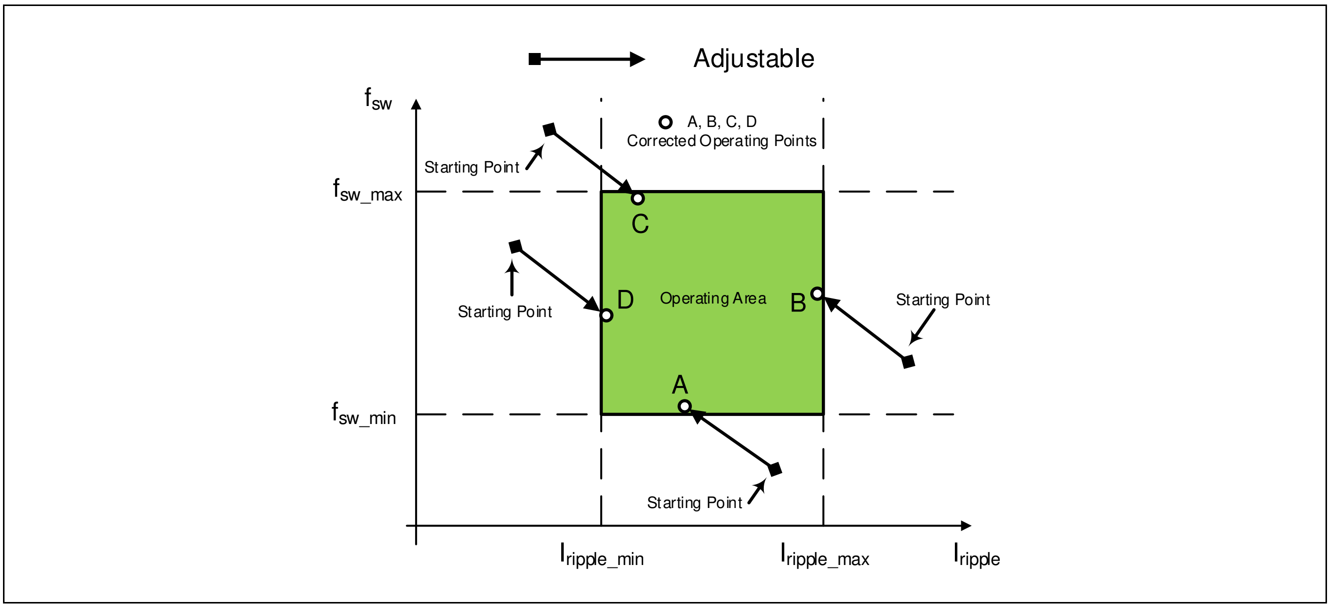


Figure 15. FRC Operating Area

All reference current values will be arranged in four groups (see **Table 3-12**) where currents from the same group have the same switching frequency and current ripple limits, as explained in Section **3.3.3**.

For each group, there are predefined (available) parameters and constants (see **Table 3-12** and **Table 3-20**):

1) Curr_ripple_perc – Initial (starting) current ripple (in percentage form).
2) Curr_ripple_min_(group) – Minimum allowed ripple value (minimum absolute output current ripple value, I_{ripple_min} in mA, not in percentage form).
3) Curr_ripple_max_(group) – Maximum allowed ripple value (maximum absolute output current ripple value, I_{ripple_max} in mA, not in percentage form).
4) FRC_freq_min_limit_(group) – Maximum allowed T_{PWM} (defining the minimum switching frequency allowed, f_{sw_min}).
5) FRC_freq_max_limit_(group) – Minimum allowed T_{PWM} (defining the maximum switching frequency allowed, f_{sw_max}).

An example is provided below for better understanding. The following parameters apply in this example for I_{OUT} = 350 mA:

1. I_{ripple_init} = 30% (or 105 mA) – Initial starting current ripple.
2. I_{ripple_min} = 25% (or 87.5 mA) – Minimum allowed current ripple.
3. I_{ripple_max} = 50% (or 175 mA) – Maximum allowed current ripple.
4. f_{sw_min} = 100 kHz (or $T_{PWM\_max} = 1/f_{sw\_min}$ = 10 µs) – Minimum allowed switching frequency.
5. f_{sw_max} = 150 kHz (or $T_{PWM\_min} = 1/f_{sw\_max}$ = 6.67 µs) – Maximum allowed switching frequency.

The Frequency Ripple Control algorithm works as following:

The system begins to operate with the defined ripple, which is given as a percentage of the average current (e.g. I_{ripple_init} = 30% I_{OUT}). This value is used to calculate the maximum (adding the half-ripple value to the reference current value) and minimum (subtracting the half-ripple value to the reference current value) hysteretic currents. There are several possible cases depending on the output voltage:

1) If the achieved operating frequency is within allowed borders (defined by f_{sw_min} and f_{sw_max}), and the starting value of the ripple is within allowed absolute ripple borders (defined by I_{ripple_min} and I_{ripple_max}), no correction will be performed (e.g. Vout = 10 V – orange curve, operating point B is in the operating area, B=B', see **Figure 16**).
2) If the achieved operating frequency is above the maximum allowed switching frequency f_{sw_max} (e.g. Vout = 15 V – grey curve, point C; Vout = 20 V – yellow curve, point D), the firmware will start to slowly increase the ripple in order to lower the operating frequency (the slope of this increasing ripple depends on the buck inductance L_{EXT}, see equation (12) on page **17**). It will continue increasing the ripple until the frequency falls below the high threshold f_{sw_max} (corrected points C' and D', see **Figure 16**).
3) If the achieved operating frequency is above the maximum allowed switching frequency f_{sw_max} (e.g. Vout = 25 V – dark blue curve, point E; Vout = 30 V – green curve, point F), the firmware will start to slowly increase the ripple in order to lower the operating frequency (the slope of this increasing ripple depends on the buck inductance L_{EXT}, see equation (12) on page **17**). It will continue increasing the ripple until it hits its maximum allowed value I_{ripple_max}. The switching frequency will be determined by I_{ripple_max} and could be outside the predefined borders (corrected points E' and F', see **Figure 17**).
4) If the achieved operating frequency is below the minimum allowed switching frequency f_{sw_min} (e.g. Vout = 5 V – blue curve, point A), the firmware will start to slowly decrease the ripple in order to raise the operating frequency (the slope of this decreasing ripple depends on the buck inductance L_{EXT}, see equation (12) on page **17**). It will continue decreasing the ripple until the frequency reaches the low threshold value defined by the parameter f_{sw_min}, or if the ripple hits the minimum allowed value defined by the parameter I_{ripple_min}. In this case, the switching frequency could be outside the predefined borders (corrected point A', see **Figure 17**).

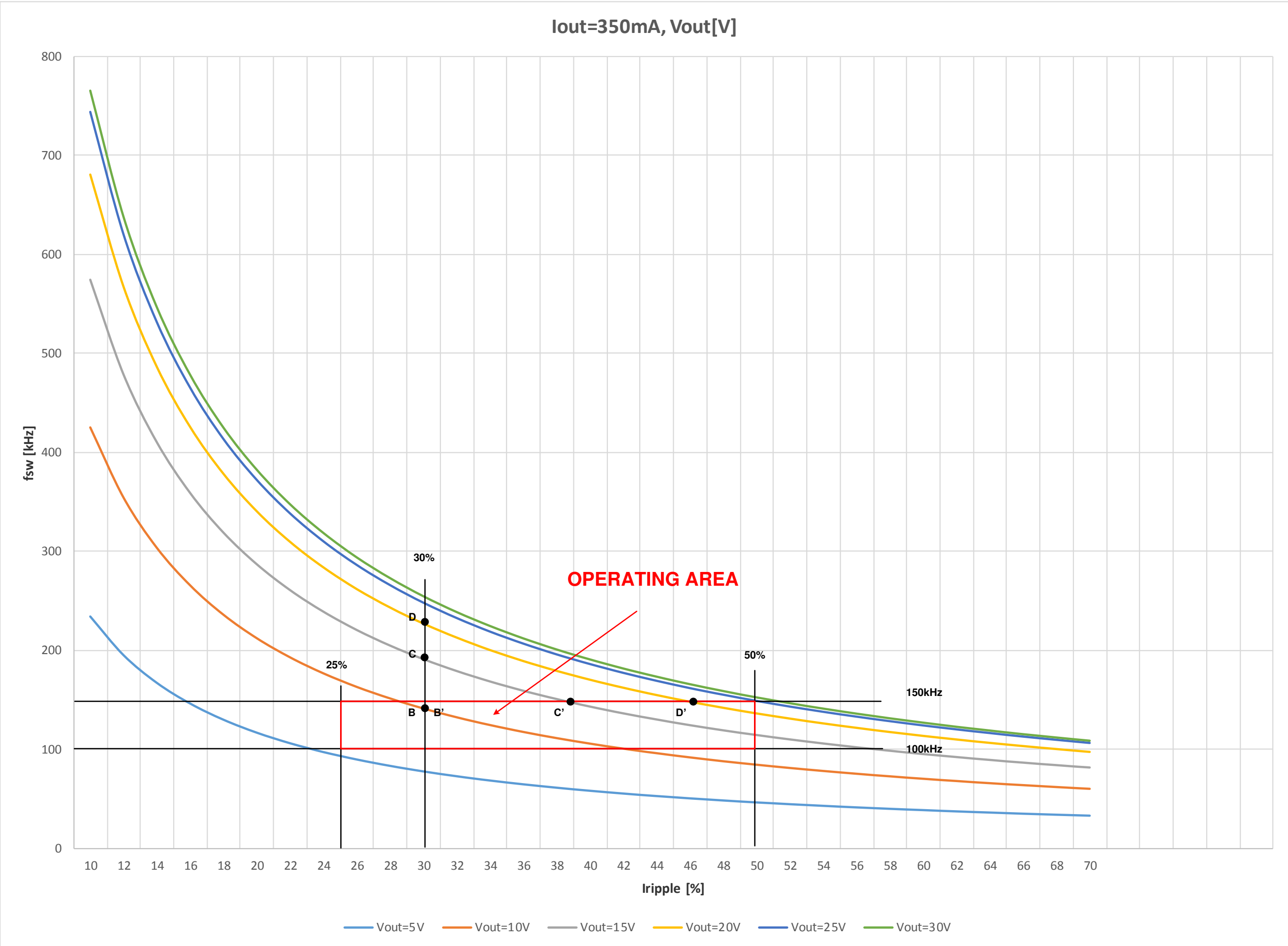


Figure 16. FRC Algorithm Example – Operating Point successfully put into Operating Area

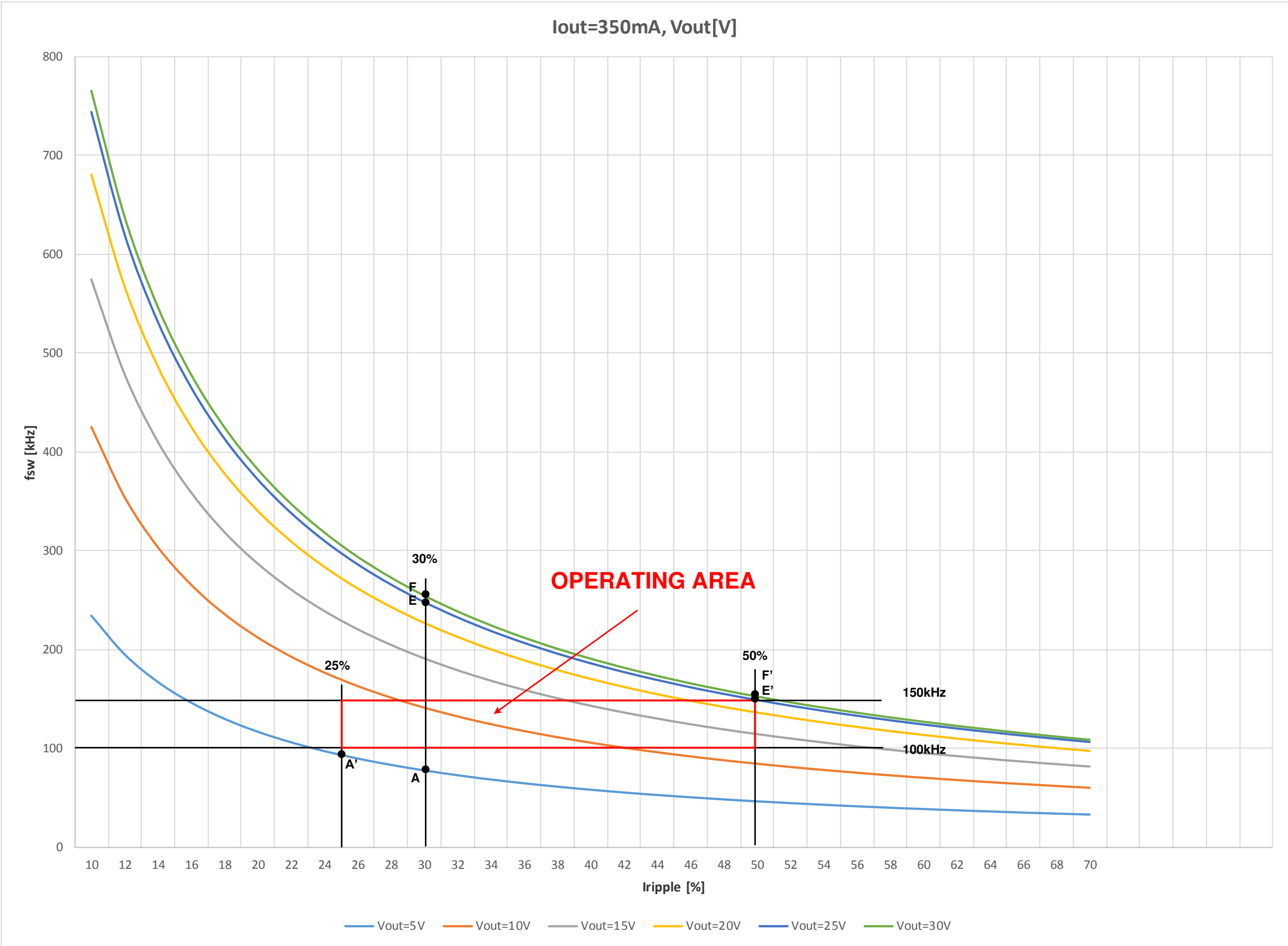


Figure 17. FRC Algorithm Example – Operating Point is outside the Predefined Borders

An example of a frequency ripple control scheme is shown below in Figure 18, Figure 19 and Figure 20. Resistances and voltage drops of used components (V_D – forward voltage of the freewheeling diode, R_L – inductor resistance, R_{ON} = R_{DS} – channel resistance when the MOSFET is ON, R_{CS} – shunt resistance connected to the CS pin, $V_{OUT} = N \cdot V_{LED} + N \cdot R_{LED} \cdot I_{OUT}$ – output voltage (LED lighting load), N – number of LEDs, V_{LED} – LED forward voltage, R_{LED} – LED forward resistance) are included in calculations.

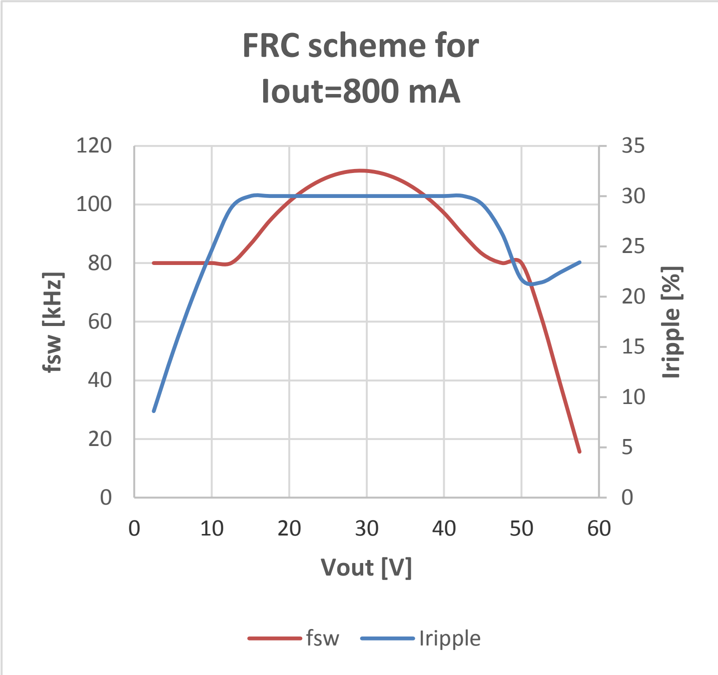


Figure 18. 800 mA FRC Scheme

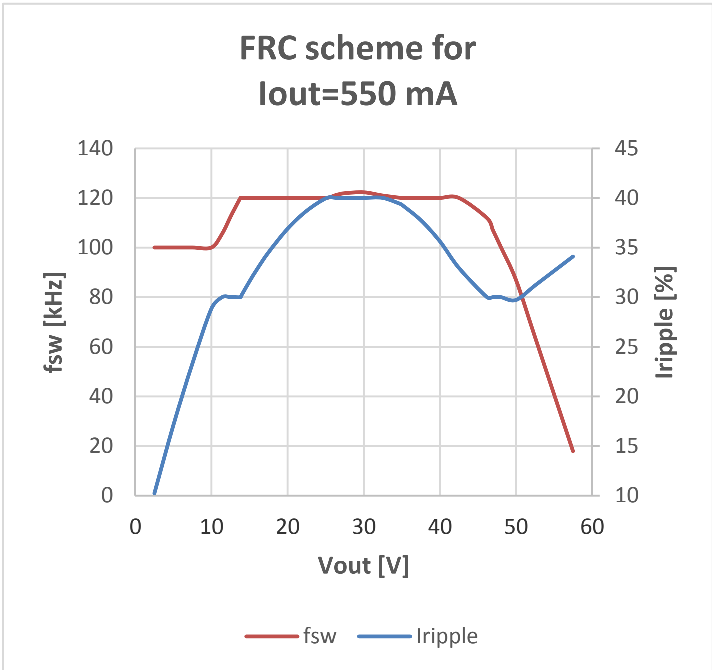


Figure 19. 550 mA FRC Scheme