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W7100A Datasheet

Version 1.2.3

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1 Overview

1.1 Introduction

iMCU W7100A is the one-chip solution which integrates an 8051 compatible microcontroller, 64KB SRAM and hardwired TCP/IP Core for high performance and easy development.

The TCP/IP core is a market-proven hardwired TCP/IP stack with an integrated Ethernet MAC & PHY. The Hardwired TCP/IP stack supports the TCP, UDP, IPv4, ICMP, ARP, IGMP and PPPoE which has been used in various applications for years.

1.2 W7100A Features

- Fully software compatible with industrial standard 8051
- Pipelined architecture which enables execution of instructions 4~5 times faster than a standard 8051
- 10BaseT/100BaseTX Ethernet PHY embedded
- Power down mode supported for saving power consumption
- Hardwired TCP/IP Protocols: TCP, UDP, ICMP, IPv4 ARP, IGMP, PPPoE, Ethernet
- Auto Negotiation (Full-duplex and half duplex), Auto MDI/MDIX
- ADSL connection with PPPoE Protocol with PAP/CHAP Authentication mode support
- 8 independent sockets which are running simultaneously
- 32Kbytes Data buffer for the Network
- Network status LED outputs (TX, RX, Full/Half duplex, Collision, Link, and Speed)
- Not supports IP fragmentation
- 2 Data Pointers (DPTRs) for fast memory blocks processing
  - Advanced INC & DEC modes
  - Auto-switch of current DPTR
- 64KBytes Data Memory (RAM)
- 255Bytes data FLASH, 64KBytes Code Memory, 2KBytes Boot Code Memory
- Up to 16M bytes of external (off-chip) data memory
- Interrupt controller
  - 2 priority levels
  - 4 external interrupt sources
  - 1 Watchdog interrupt
- Four 8-bit I/O Ports
- Three timers/counters
- Full-duplex UART
- Programmable Watchdog Timer
- DoCD™ compatible debugger
- High Product Endurance
  - Minimum 100,000 program/erase cycles
  - Minimum 10 years data retention

1.3 W7100A Block Diagram & Features

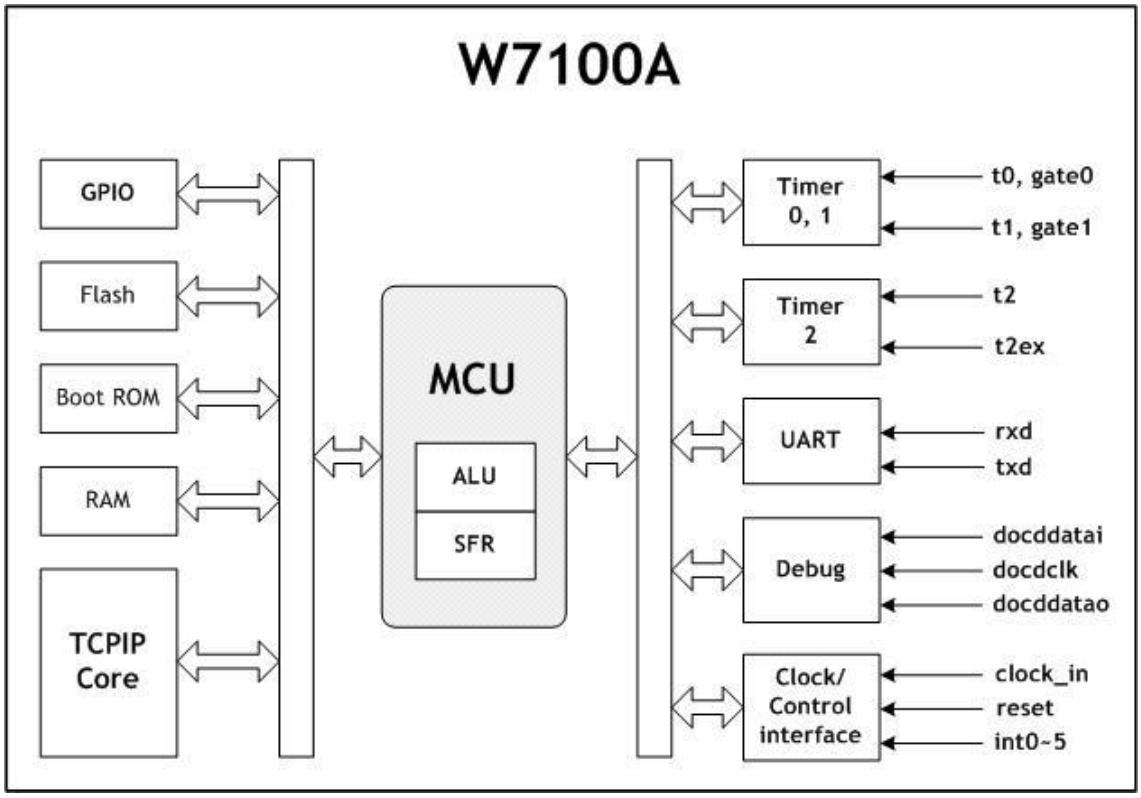

Figure 1.1 W7100A Block Diagram

The W7100A internal block diagram is shown in the Figure 1.1. Details of block functions are described as follows:

ALU – Performs arithmetic and logic operations during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), B registers, and related logics such as arithmetic unit, logic unit, multiplier, and divider.

SFR – Controls the access of special registers. It contains standard and user defined registers and related logic. User defined external devices can be quickly accessed (read, write, modified) using all direct addressing mode instructions.

1.3.1 ALU (Arithmetic Logic Unit)

W7100A is fully compatible with the standard 8051 microcontroller, and maintains all instruction mnemonics and binary compatibility. W7100A incorporates many great architectural enhancements which enable the W7100A MCU to execute instructions with high speed.

The ALU of W7100A MCU performs extensive data manipulation and is comprised of the 8-bit arithmetic logic unit (ALU), an ACC (0xE0) register, a B (0xF0) register and a PSW (0xD0) register

ACC (0xE0)

7	6	5	4	3	2	1	0	Reset
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	0x00

Figure 1.2 Accumulator A Register

The B register is used during multiplication and division operations. In other cases, this register is used as normal SFR.

B (0xF0)

7	6	5	4	3	2	1	0	Reset
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	0x00

Figure 1.3 B Register

The ALU performs arithmetic operations such as addition, subtraction, multiplication, and division, and other operations such as increment, decrement, BCD-decimal-add-adjust, and compare. Logic unit uses AND, OR, Exclusive OR, complement, and rotation to perform different operations. The Boolean processor performs bit operations such as set, clear, complement, jump-if-not-set, jump-if-set-and-clear, and move to/from carry.

PSW (0xD0)

7	6	5	4	3	2	1	0	Reset
CY	AC	F0	RS1	RS0	OV	F1	P	0x00

Figure 1.4 Program Status Word Register

CY	Carry flag	
AC	Auxiliary carry	
F0	General purpose flag 0	
RS[1:0]	Register bank select bits	
	RS[1:0]	Function Description
	00	-Bank 0, data address 0x00 - 0x07
	01	-Bank 1, data address 0x08 - 0x0F
	10	-Bank 2, data address 0x10 - 0x17
	11	-Bank 3, data address 0x18 - 0x1F
OV	Overflow flag	
F1	General purpose flag 1	
P	Parity flag	

Figure 1.5 PSW Register

The PSW register contains several bits that can reflect the current state of MCU.

1.3.2 TCPIPCore

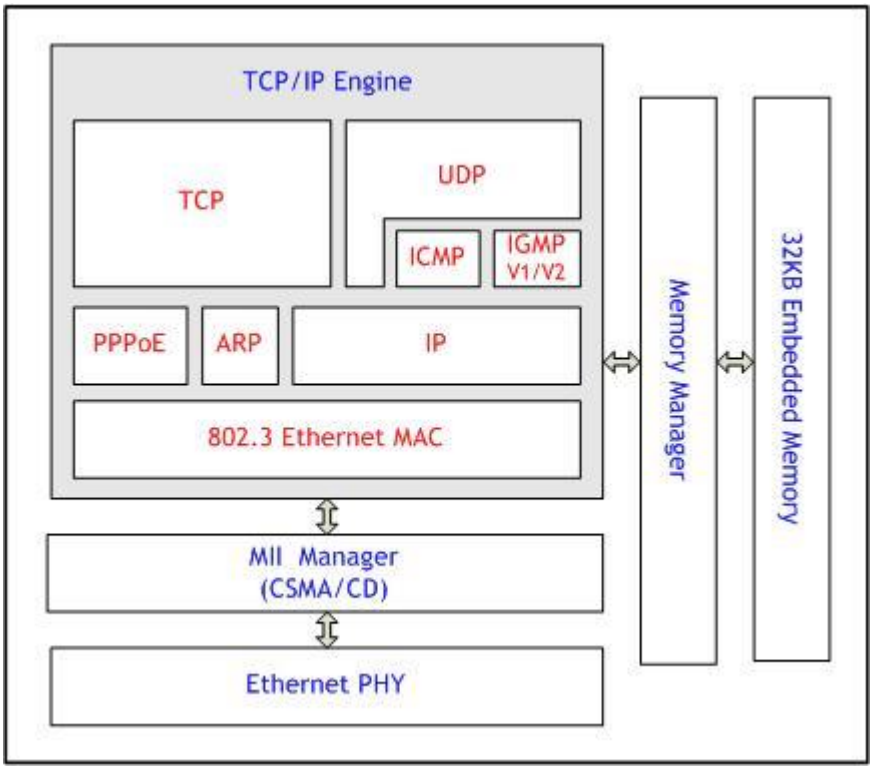

Figure 1.6 TCPIPCore Block Diagram

Ethernet PHY

The W7100A includes 10BaseT/100BaseTX Ethernet PHY. It supports half-duplex/full-duplex, auto-negotiation and auto-MDI/MDIX. It also supports 6 network indicator LED outputs such as Link, TX, RX status, Collision, speed and duplex.

TCPIP Engine

TCPIP Engine is a hardwired logic based network protocol which contains technology of WIZnet.

- **802.3 Ethernet MAC(Media Access Control)**

  This controls Ethernet access of CSMA/CD(Carrier Sense Multiple Access with Collision Detect). The protocol is based on a 48-bit source/destination MAC address.

- **PPPoE(Point-To-Point Protocol over Ethernet)**

  This protocol uses PPP service over Ethernet. The payload (PPP frame) is encapsulated inside an Ethernet frame during a transmission. When receiving, it de-capsulates the PPP frame. PPPoE supports PPP communication with PPPoE server and PAP/CHAP authentications.

- **ARP(Address Resolution Protocol)**

  ARP is the MAC address resolution protocol by using IP address. This protocol exchanges ARP-reply and ARP-request from peers to determine the MAC address of each other

- **IP (Internet Protocol)**

  This protocol operates in the IP layer and provides data communication. IP fragmentation is not supported. It is not possible to receive the fragmented packets. All protocol number is supported except for TCP or UDP. In case of TCP or UDP, use the hardwired embedded TCPIP stack.

- **ICMP(Internet Control Message Protocol)**

  ICMP is a protocol which provides information, unreachable destination. When a Ping-request ICMP packet is received, a Ping-reply ICMP packet is sent.

- **IGMPv1/v2(Internet Group Management Protocol version 1/2)**

  This protocol processes IGMP messages such as the IGMP Join/Leave. The IGMP is only enabled in UDP multicast mode. Only version 1 and 2 of IGMP logic is supported. When using a newer version of IGMP, IGMP should be manually implemented in the IP layer.

- **UDP(User Datagram Protocol)**

  It is a protocol which supports data communication at the UDP layer. User datagram such as unicast, multicast, and broadcast are supported

- **TCP(Transmission Control Protocol)**

  This protocol operates in the TCP layer and provides data communication. Both TCP server and client modes are supported.

1.4 Pin Description

1.4.1 Pin Layout

Package type: LQFP 100

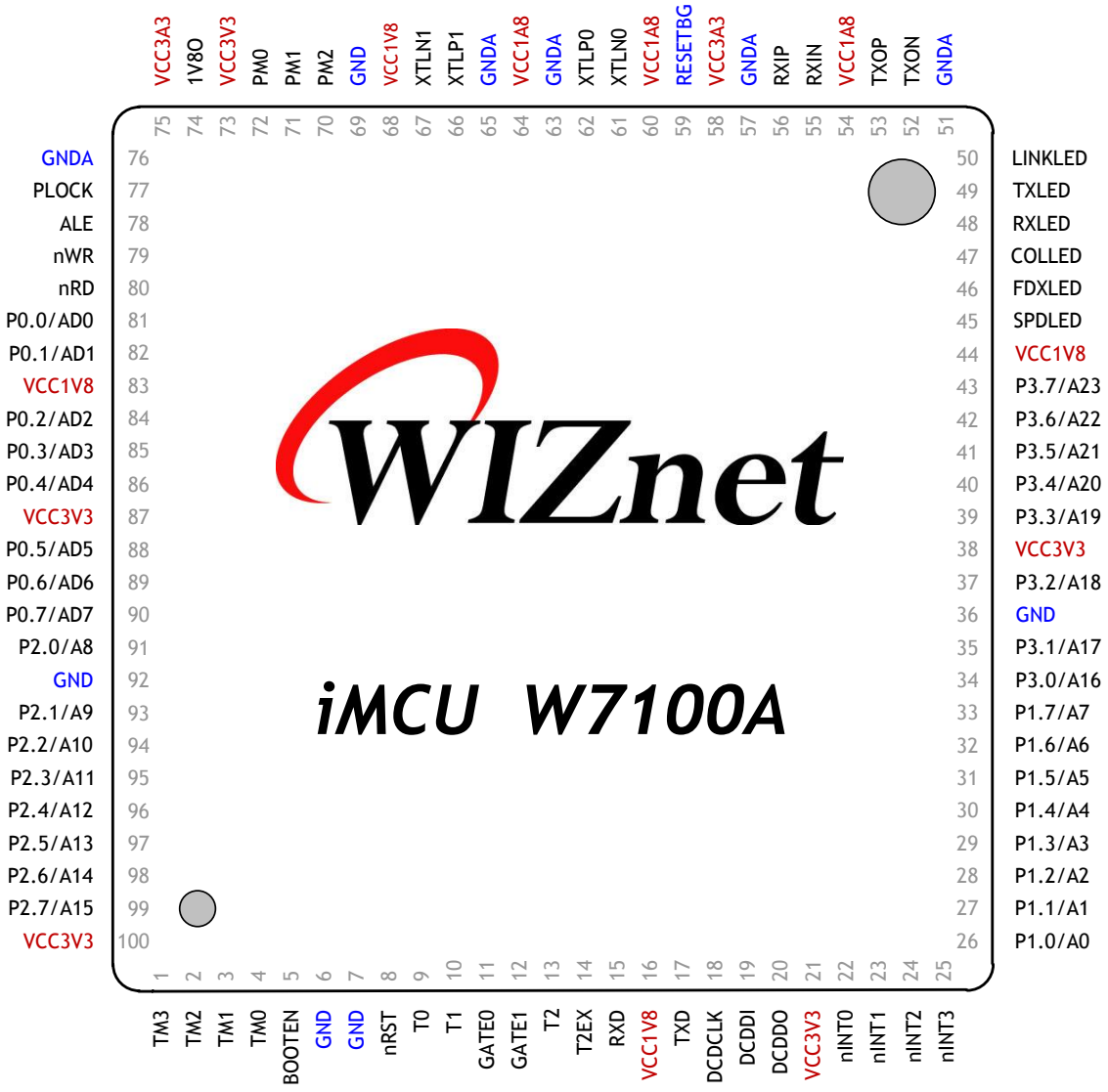

Figure 1.7 W7100A Pin Layout

Package type: QFN 64

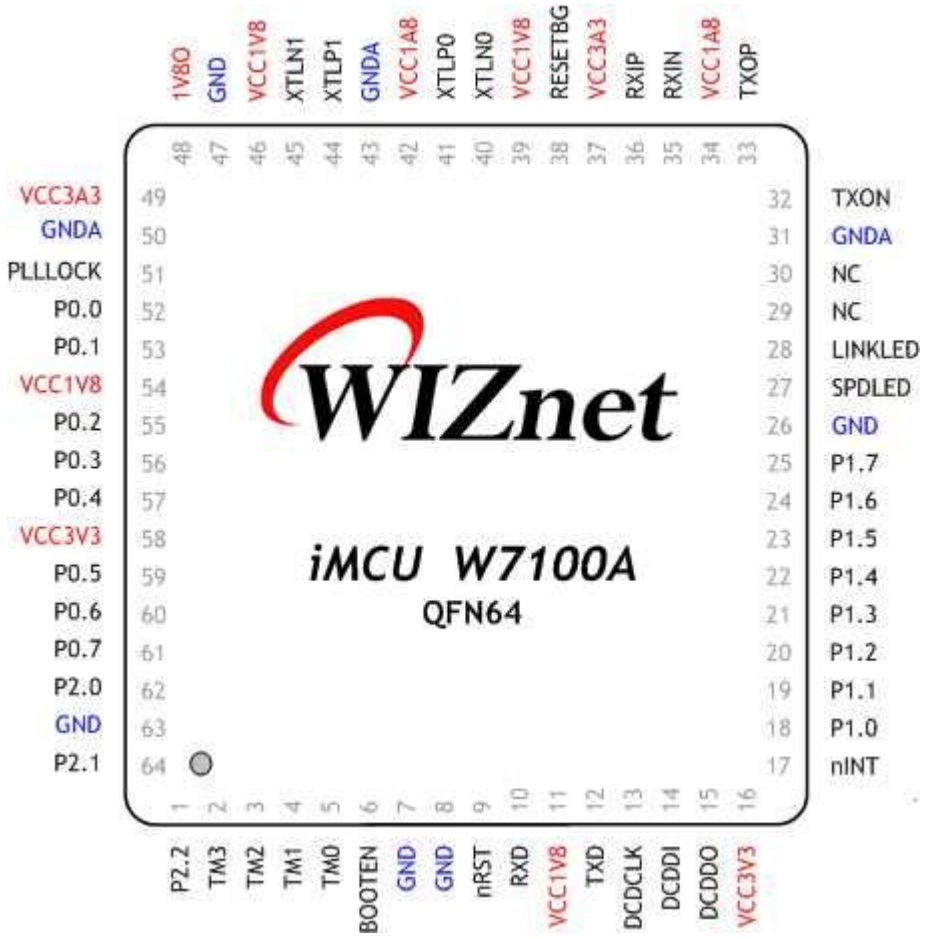

Figure 1.8 W7100A QFN 64 Pin Layout

1.4.2 Pin Description

The pin functionalities are described in the following table. There are no tri-state output pins and internal signals.

Type	Description
I	Input
O	Output with 8mA driving current
IO	Input/Output (Bidirectional)
Pu	Internal pulled-up with 4.7KΩ resistor
Pd	Internal pulled-down with 85KΩ resistor

1.4.2.1 Configuration

<table>
<tr><th rowspan="2">Pin name</th><th colspan="2">Pin number</th><th rowspan="2">I/O</th><th rowspan="2">Pu/Pd</th><th rowspan="2">Description</th></tr>
<tr><th>100pin</th><th>64pin</th></tr>
<tr><td>nRST</td><td>8</td><td>9</td><td>I</td><td>Pu</td><td>Global asynchronous reset, Active low</td></tr>
<tr><td>TM3-0</td><td>1,2,
3,4</td><td>2,3,
4,5</td><td>I</td><td>Pd</td><td>Must be connected to GND; value ‘0000’</td></tr>
<tr><td>PM2 - 0</td><td>70,
71,
72</td><td>-</td><td>I</td><td>Pd</td><td>PHY Mode
<table>
<tr><th colspan="3">PM</th><th rowspan="2">Description</th></tr>
<tr><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Normal Operation Mode
Auto-negotiation enabled with all functionalities</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Auto-negotiation with 100 BASE-TX FDX/HDX ability</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Auto-negotiation with 10 BASE-T FDX/HDX ability</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Manual selection of 100 BASE-TX FDX</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Manual selection of 100 BASE-TX HDX</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Manual selection of 10 BASE-T FDX</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Manual selection of 10 BASE-T HDX</td></tr>
</table>
FDX : Full-Duplex, HDX : Half-Duplex</td></tr>
<tr><td>BOOTEN</td><td>5</td><td>6</td><td>I</td><td>Pd</td><td>Boot Enable/Disable
0 – Enable User Application mode
Jump to 0x0000, the start address of user Code FLASH.
1- Enable Boot mode
Run boot code in Boot ROM</td></tr>
<tr><td>PLOCK</td><td>77</td><td>51</td><td>O</td><td>-</td><td>PLL Lock line, It notifies when internal PLL is locked</td></tr>
</table>

1.4.2.2 Timer

Pin name	Pin number		I/O	Pu/Pd	Description
	100pin	64pin			
Timer0, 1 Interface					
T0	9	-	I	Pu	Timer0 external clock input
T1	10	-	I	Pu	Timer1 external clock input
GATE0	11	-	I	Pd	Timer0 gate control
GATE1	12	-	I	Pd	Timer1 gate control
Timer2 Interface					
T2	13	-	I	Pu	Timer2 external clock input
T2EX	14	-	I	Pu	Timer2 Capture/Reload trigger

1.4.2.3 UART

Pin name	Pin number		I/O	Pu/Pd	Description
	100pin	64pin			
RXD	15	10	I	-	Serial receiver
TXD	17	12	O	-	Serial transmitter

1.4.2.4 DoCD™ Compatible Debugger

Pin name	Pin number		I/O	Pu/Pd	Description
	100pin	64pin			
DCDCLK	18	13	O	-	DoCD clock
DCDDI	19	14	I	Pu	DoCD data input
DCDDO	20	15	O		DoCD data output

1.4.2.5 Interrupt / Clock

Pin name	Pin number		I/O	Pu/Pd	Description
	100pin	64pin			
nINT0	22	17	I	-	External interrupt0
nINT1	23	-	I	Pu	External interrupt1
nINT2	24	-	I	Pu	External interrupt2
nINT3	25	-	I	Pu	External interrupt3
XTLN0	61	40	O	-	Crystal output for WIZnet Core, A parallel-resonant 25MHz crystal or ceramic is connected. If use oscillator, this pin can be floated.
XTLP0	62	41	I	-	Crystal input for WIZnet Core, A parallel-

					resonant 25MHz crystal or ceramic is connected. If use oscillator, this pin connected with 1.8V output of OSC.
XTLN1	67	45	O	-	Crystal output for MCU core, A parallel-resonant 11.0592MHz crystal or ceramic is connected. If oscillator is uesd, this pin can be floated.
XTLP1	66	44	I	-	Crystal input for MCU core, A parallel-resonant 11.0592MHz crystal or ceramic is connected. If oscillator is used, this pin is connected with 1.8V output of OSC.

1.4.2.6 GPIO

Pin name	Pin number		I/O	Pu/Pd	Description
	100pin	64pin			
P0.0	81	52	IO	-	Port0 input/output, Ext Memory Data0, Addr0
P0.1	82	53	IO	-	Port0 input/output, Ext Memory Data1, Addr1
P0.2	84	55	IO	-	Port0 input/output, Ext Memory Data2, Addr2
P0.3	85	56	IO	-	Port0 input/output, Ext Memory Data3, Addr3
P0.4	86	57	IO	-	Port0 input/output, Ext Memory Data4, Addr4
P0.5	87	59	IO	-	Port0 input/output, Ext Memory Data5, Addr5
P0.6	89	60	IO	-	Port0 input/output, Ext Memory Data6, Addr6
P0.7	90	61	IO	-	Port0 input/output, Ext Memory Data7, Addr7
P1.0	26	18	IO	-	Port1 input/output, Ext Memory Addr0
P1.1	27	19	IO	-	Port1 input/output, Ext Memory Addr1
P1.2	28	20	IO	-	Port1 input/output, Ext Memory Addr2
P1.3	29	21	IO	-	Port1 input/output, Ext Memory Addr3
P1.4	30	22	IO	-	Port1 input/output, Ext Memory Addr4
P1.5	31	23	IO	-	Port1 input/output, Ext Memory Addr5
P1.6	32	24	IO	-	Port1 input/output, Ext Memory Addr6
P1.7	33	25	IO	-	Port1 input/output, Ext Memory Addr7
P2.0	91	62	IO	-	Port2 input/output, Ext Memory Addr8
P2.1	93	64	IO	-	Port2 input/output, Ext Memory Addr9
P2.2	94	1	IO	-	Port2 input/output, Ext Memory Addr10
P2.3	95	-	IO	-	Port2 input/output, Ext Memory Addr11
P2.4	96	-	IO	-	Port2 input/output, Ext Memory Addr12
P2.5	97	-	IO	-	Port2 input/output, Ext Memory Addr13
P2.6	98	-	IO	-	Port2 input/output, Ext Memory Addr14

P2.7	99	-	IO	-	Port2 input/output, Ext Memory Addr15
P3.0	34	-	IO	-	Port3 input/output, Ext Memory Addr16
P3.1	35	-	IO	-	Port3 input/output, Ext Memory Addr17
P3.2	37	-	IO	-	Port3 input/output, Ext Memory Addr18
P3.3	39	-	IO	-	Port3 input/output, Ext Memory Addr19
P3.4	40	-	IO	-	Port3 input/output, Ext Memory Addr20
P3.5	41	-	IO	-	Port3 input/output, Ext Memory Addr21
P3.6	42	-	IO	-	Port3 input/output, Ext Memory Addr22
P3.7	43	-	IO	-	Port3 input/output, Ext Memory Addr23

Note: User can control the GPIO I/O driving voltage using PxPU/PxPD SFR.

Note: In that case, GPIO0~3 is used to transfer External memory address and data. Please refer to the '2.3 External Data Memory Access'

1.4.2.7 External Memory Interface

Pin name	Num	I/O Type	Description
ALE	78	O	Data memory address bus [7:0] latch enable
nWR	79	OL	External data memory write
nRD	80	OL	External data memory read

Note: When user using External memory by standard 8051 interface, P0[7:0] can transfer Data[7:0] or Address[7:0] by ALE pin control.

1.4.2.8 Media Interface

Pin name	Pin number		I/O	Pu/Pd	Description
	100pin	64pin			
TXON	52	32	O	-	TXON/TXOP Signal Pair, The differential data is transmitted to the media on the TXON/TXOP signal pair
TXOP	53	33	O	-	
RXIN	55	35	I	-	RXIN/RXIP Signal Pair, The differential data from the media is received on the RXIN/RXIP Signal pair
RXIP	56	36	I	-	
RESETBG	59	38	I	-	PHY Off-chip resistor, Connect a resistor of 12.3 kΩ±1% to the ground. Refer to the "Reference schematic"

For the best performance,

1. Make the length of RXIP / RXIN signal pair (RX) same if possible.
2. Make the length of TXOP / TXON signal pair (TX) same if possible.
3. Locate the RXIP and RXIN signal as near as possible.

4. Locate the TXOP and TXON signal as near as possible.
5. Locate the RX and TX signal pairs far from noisy signals such as bias resistor or crystal.
6. Keep regular between TX/RX signal pair.

For more details, refer to “W5100 Layout Guide.pdf.”

1.4.2.9 Network Indicator LED

Pin name	Pin number		I/O	Pu/Pd	Description
	100pin	64pin			
SPDLED	45	27	O	-	Link speed LED Low: 100Mbps High: 10Mbps
FDXLED	46	-	O	-	Full duplex LED Low: Full-duplex High: Half-duplex
COLLED	47	-	O	-	Collision LED Low: Collision detected (only half-duplex)
RXLED	48	-	O	-	Receive activity LED Low: Receive signal detected on RXIP/RXIN
TXLED	49	-	O	-	Transmit activity LED Low: Transmit signal detected on TXOP/TXON
LINKLED	50	28	O	-	Link LED Low: Link (10/100M) is detected

1.4.2.10 Power Supply Signal

Pin name	Pin number		I/O	Pu/Pd	Description
	100pin	64pin			
VCC3A3	58, 75	37, 49	Power	-	Analog 3.3V power supply Be sure to connect a 10uF tantalum capacitor between VCC3A3 and GNDA in order to prevent power compensation
VCC3V3	21, 38, 73, 87, 100	16, 58	Power	-	Digital 3.3V power supply A 0.1uF decoupling capacitor should be connected between each pair of VCC and GND. A 1uH ferrite bead should be used to separate the VCC3V3 and VCC3A3
VCC1A8	54,	34, 42	Power	-	Analog 1.8V power supply

	60, 64				A 10uF tantalum capacitor and a 0.1uF capacitor should be connected between VCC1A8 and GNDA to filter out core power noise
VCC1V8	16, 44, 68, 83	39, 46, 54, 11	Power	-	Digital 1.8V power supply Between each pair of VCC and GND, a 0.1uF decoupling capacitor should be connected
GNDA	51, 57, 63, 65, 76	31, 43, 50	Power	-	Analog ground Design the analog ground plane as wide as possible during PCB layout
GND	6, 7, 36, 69, 92	7, 8, 26, 47, 63	Power	-	Digital ground Design the digital ground plane as wide as possible during PCB layout
1V8O	74	48	Power	-	1.8V regulated output voltage 1.8V/150mA power generated by internal power regulator which is used for core operation power (VCC1A8, VCC1V8). Between the 1V8O and GND, Be sure to connect a 3.3uF tantalum capacitor for output frequency compensation and a 0.1uF capacitor for high frequency noise decoupling. 1V8O is connected to VCC1V8, separated to 1uH inductor and connected to VCC1A8. <Notice> 1V8O is the power supply for W7100A use only. This supply should not be connected with any other devices.

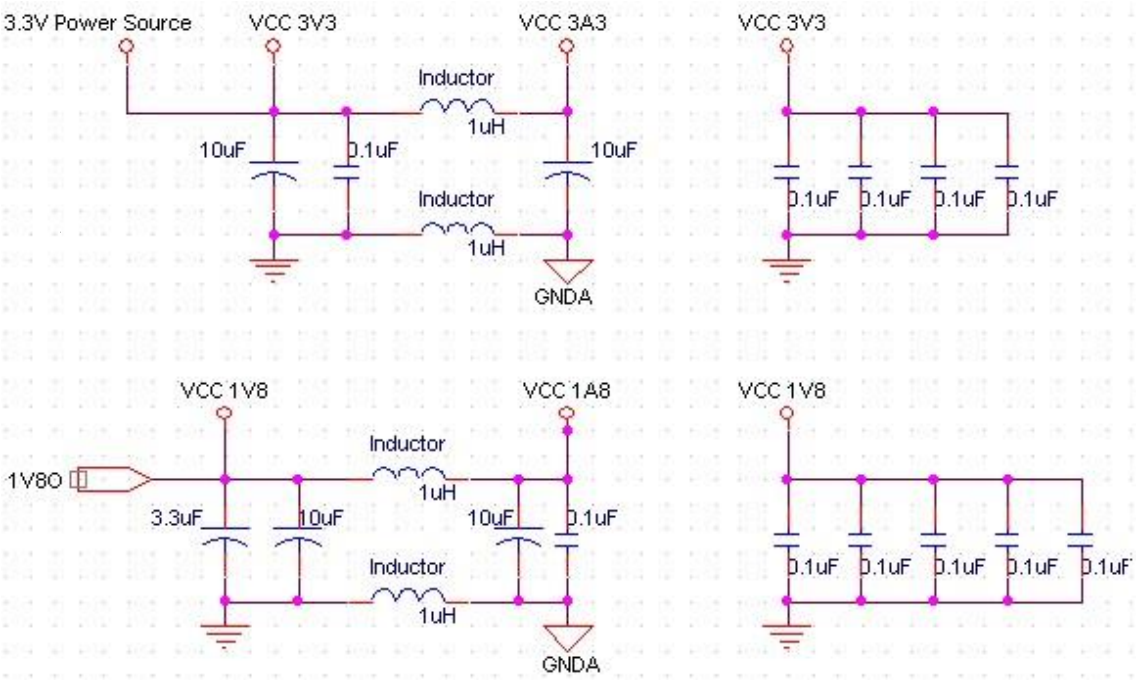

Figure 1.9 Power Design

1.5 64pin package description

1.5.1 Difference between 100 and 64pin package

Difference	64 pin	100 pin
Deleted pin	T0, T1, GATE0, GATE1, T2, T2EX, nINT1, nINT2, nINT3, FDXLED, COLLED, RXLED, TXLED, PM2, PM1, PM0, EXTALE, EXTDATAWR, EXTDATARD, GPIO3[0:7], GPIO2[3:7]	-
External memory	X	O
PHY mode setting	only use SFR	use SFR or PM pins
GPIO	max 19pin	max 32pin

*Note: In case of 64pin package, the PHY mode is must be set by PHYCONF SFR. So, user must set the MODE_EN bit to enable the MODE2 ~ 0 bit configuration. Then set the MODE2 ~ 0 value and reset the PHY controlling the PHY_RSTn bit. After the reset the 64pin package chip will be successfully initialized and operate properly. **When the user uses the 64pin package chip, the code below must be executed in chip initialize routine.**

For more detailed information about the PHYCONF SFR, please refer to the section 2.5.10 'New & Extended SFR'.

```
PHYCONF |= 0x08;    // MODE_EN bit enable
PHYCONF &= 0xF8;    // MODE2 ~ 0 value is 0 (normal mode); Auto configuration mode
PHYCONF |= 0x20;    // Set the PHY_RSTn bit (reset bit)
Delay();                  // Delay for reset timing (refer to the section 10 'Reset Timing')
PHYCONF &= ~(0x20); // Clear the PHY_RSTn bit
```