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InnoSwitch3-Pro Family

Digitally Controllable Off-Line CV/CC QR Flyback Switcher IC
with Integrated High-Voltage MOSFET, Synchronous Rectification
and FluxLink Feedback

Product Highlights

Digitally Controlled via I²C Interface

- Dynamic adjustment of power supply voltage and current
- Telemetry for power supply status and fault monitoring
- Comprehensive set of configurable protection features

Highly Integrated, Compact Footprint

- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, 650 V or 725 V MOSFET, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Instantaneous transient response
- Drives low-cost N-channel MOSFET series load switch
- Integrated 3.6 V supply for external MCU

EcoSmart™ – Energy Efficient

- Less than 30 mW no-load including line sense and MCU
- Enables power supply designs that easily comply with all global energy efficiency regulations
- Low heat dissipation

Advanced Protection / Safety Features

- Input voltage monitoring with accurate brown-in/brown-out and overvoltage protection
- Output OV/UV fault detection with independently configured responses
- Secondary FET / diode short protection
- Open SR FET gate detection
- Hysteretic thermal shutdown
- Programmable watchdog timer for system faults

Full Safety and Regulatory Compliance

- Reinforced insulation
- Isolation voltage >4000 VAC
- 100% production HIPOT compliance testing
- UL1577 and TUV (EN60950) safety approved

Green Package

- Halogen free and RoHS compliant

Applications

- High efficiency USB PD 3.0 + PPS/QC adapters
- Multiprotocol adapters including QuickCharge, AFC, FCP, SCP
- Direct-charge mobile device chargers
- Multi-chemistry tool and general purpose battery chargers
- Adjustable CV and CC LED ballast

Description

The InnoSwitch™3-Pro series family of ICs dramatically simplifies the development and manufacturing of fully programmable, highly efficient power supplies, particularly those in compact enclosures. The universal I²C interface enables dynamic control of output voltage and current along with many configurable features. Telemetry provides reporting of programmed features and fault modes.

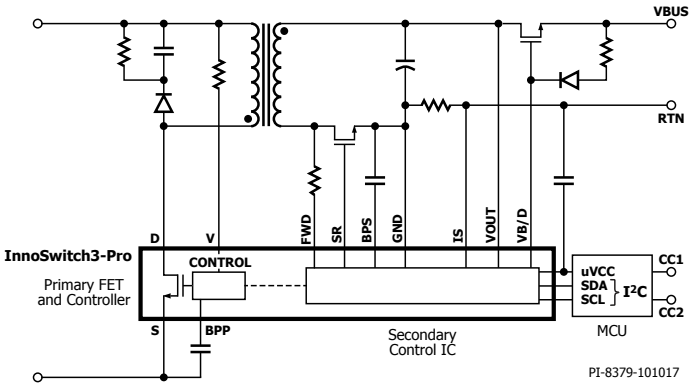

Figure 1. Typical Application.

Figure 2. High Creepage, Safety-Compliant InSOP-24D Package.

Output Power Table[1]

Product[4,5]	230 VAC ± 15%		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
INN3365C/3375C	25 W	30 W	22 W	25 W
INN3366C/3376C	35 W	40 W	27 W	36 W
INN3377C	40 W	45 W	36 W	40 W
INN3367C	45 W	50 W	40 W	45 W
INN3368C	55 W	65 W	50 W	55 W

Table 1. Output Power Table.

Notes:
1. Maximum output power is dependent on the design, with maximum IC package temperature kept <125 °C.
2. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient.
3. Minimum peak power capability.
4. C Package: InSOP-24D.
5. INNxx6xC – 650 V MOSFET, INNxx7xC – 725 V MOSFET.

InnoSwitch3-Pro devices are ideal for AC/DC power supply applications where fine (10 mV, 50 mA) output voltage and current adjustment are necessary. Typical implementations comprise a system microprocessor or dedicated microcontroller with an I²C port that is used to configure, control and supervise operation of the power sub-system. The uVCC pin provides a bias supply for the microprocessor in stand-alone implementations such as USB PD adapters and chargers.

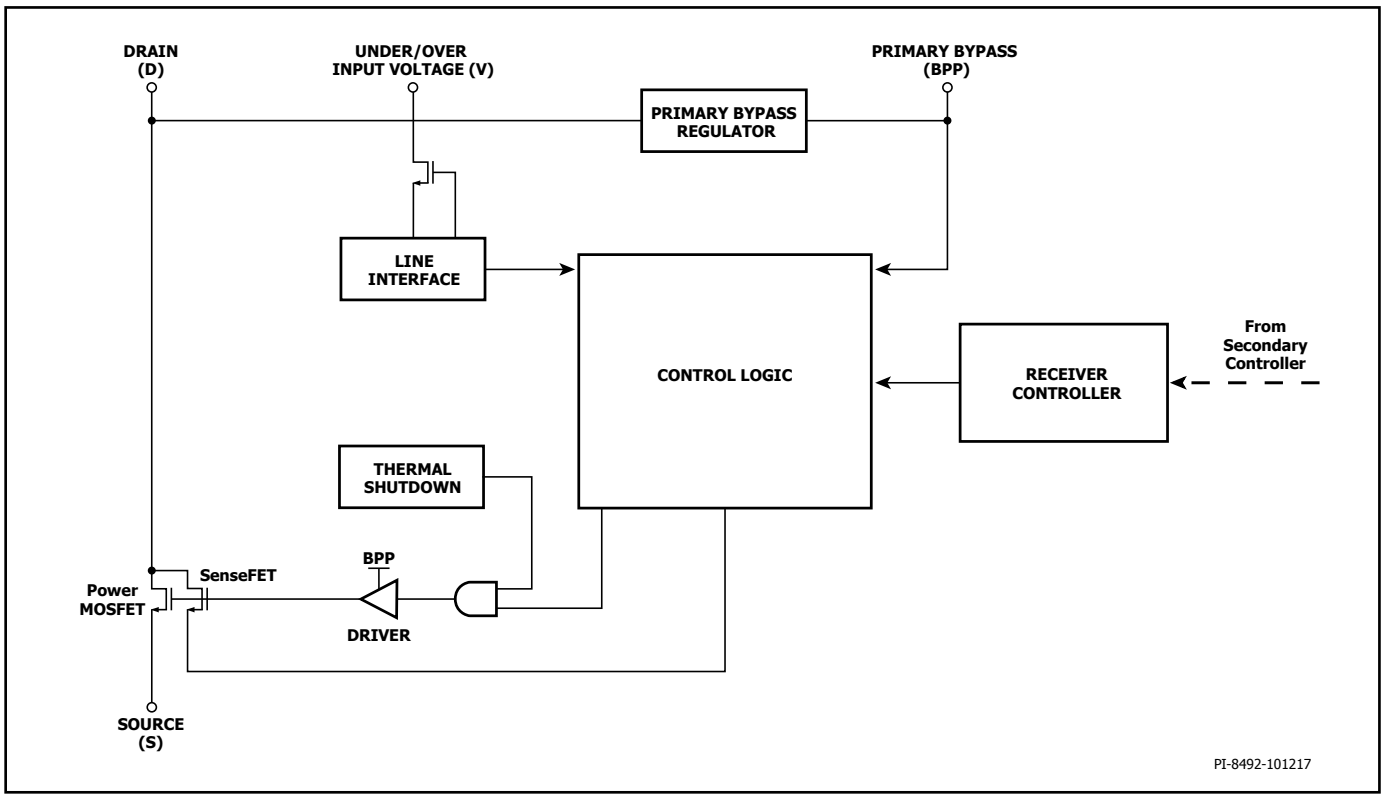

Figure 3. Primary Controller Block Diagram.

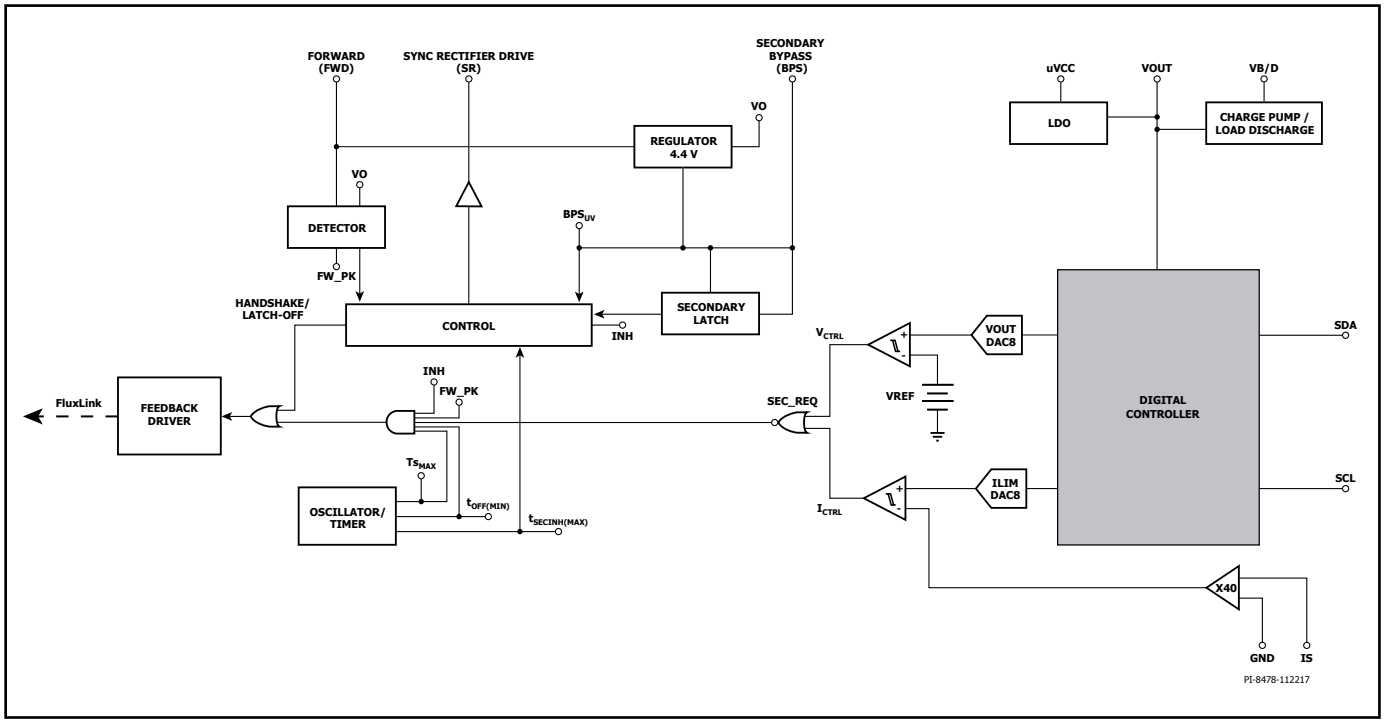

Figure 4. Secondary Controller Block Diagram.

Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply return output terminals. An external current sense resistor should be connected between this and the SECONDARY GROUND pin.

SECONDARY GROUND (GND) (Pin 2)
GND for the secondary IC. Note this is not the power supply output GND due to the presence of the sense resistor between this and the ISENSE pin.

NC Pin (Pin 3)
Leave open. Should not be connected to any other pins.

SECONDARY BYPASS (BPS) Pin (Pin 4)
It is the connection point for an external bypass capacitor for the secondary IC supply.

I²C Clock (SCL) Pin (Pin 5)
I²C serial communication protocol clock line sourced by the Bus master (max 700 kHz).

I²C Serial Data (SDA) Pin (Pin 6)
I²C serial communication protocol data line sourced by the Bus master (max 700 kHz).

External VCC Supply (uVCC) Pin (Pin 7)
This is a 3.6 V supply for an external controller.

VBUS Series Switch Drive and Load Discharge (VB/D) Pin (Pin 8)
VBUS enable and driver for NMOS gate for VOUT to VBUS pass MOSFETs. This pin can also be used to discharge output load voltage.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 9)
Gate driver output and connection to external SR FET gate terminal.

OUTPUT VOLTAGE (VOUT) Pin (Pin 10)
Connected directly to the output voltage providing current for the secondary IC and sense for output voltage regulation. Also active pull-down current source for minimum load.

FORWARD (FWD) Pin (Pin 11)
The connection point to the switching node of the transformer output winding providing information on the primary switch timing plus providing power for the secondary IC when V_{OUT} is below a threshold value.

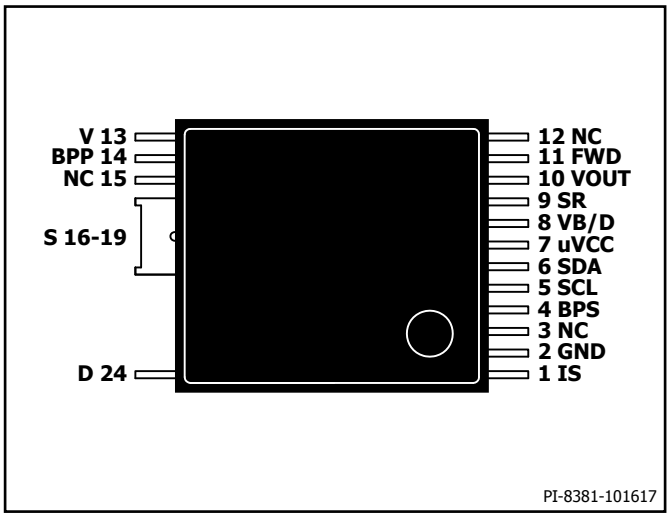

Figure 5. Pin Configuration.

NC Pin (Pin 12)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting under and overvoltage conditions at the power supply input. When connected to the AC side of the bridge, a high-voltage switch is opened when not sensing to reduce power consumption. This pin should be tied to GND to disable UV/OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
It is the connection point for an external bypass capacitor for the primary IC supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1.

NC Pin (Pin 15)
Leave open. Should not be connected to any other pins.

SOURCE (S) Pin (Pin 16-19)
These pins are the power MOSFET source connection. It is also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
This pin is the power MOSFET drain connection.

InnoSwitch3-Pro Functional Description

The InnoSwitch3-Pro combines a high-voltage power MOSFET switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme using the package lead frame and bond wires to provide a safe, reliable, and low-cost means to communicate accurate direct sensing of the output voltage and output current on the secondary IC to the primary IC.

The primary controller on InnoSwitch3-Pro is a Quasi-Resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection, leading edge blanking, secondary output diode/SR FET short protection circuit and a 650 V / 725 V power MOSFET.

The InnoSwitch3-Pro secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, an I^2C interface to control power supply parameters and telemetry functions, a 4.4 V regulator on the SECONDARY BYPASS pin, synchronous rectifier MOSFET driver, QR mode circuit, oscillator and timing functions, and a host of integrated protection features.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller with the most important features.

Primary Controller

InnoSwitch3-Pro has variable frequency QR controller plus CCM/CrM/DCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power MOSFET is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power MOSFET is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch3-Pro to be powered externally through a bias winding, decreasing the no-load consumption to less than 30 mW in a 5 V output design.

Primary Bypass ILIM Programming

InnoSwitch3-Pro ICs allows the user to adjust current limit (ILIM) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used.

There are 2 selectable capacitor sizes - 0.47 μF and 4.7 μF for setting standard and increased ILIM settings respectively.

Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power MOSFET when the PRIMARY BYPASS pin voltage drops below ~4.5 V (V_{BPP} - $V_{BP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to V_{BP} to re-enable turn-on of the power MOSFET.

Primary Bypass Output Overvoltage Function

The PRIMARY BYPASS pin has a latching OV protection feature. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds ISD, the device will latch-off or disable the power MOSFET switching for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation.

VOUT OV protection is also included as an integrated feature on the secondary controller.

Over-Temperature Protection

The thermal shutdown circuitry senses the primary MOSFET die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response.

Hysteretic response: If the die temperature rises above the threshold, the power MOSFET is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power MOSFET is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

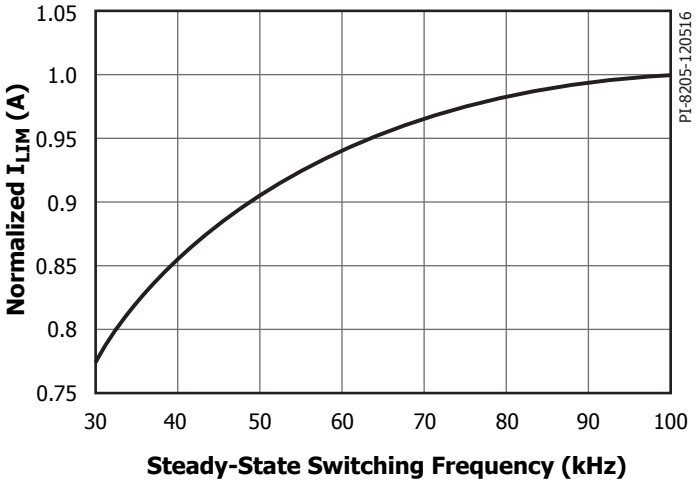

Figure 6. Normalized Primary Current vs. Frequency.

Current Limit Operation
The primary-side controller has a current limit threshold ramp that is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary MOSFET turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current approaching 100% I_{LIM}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

Jitter
The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart
In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch3-Pro enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below ~ 3 V or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

In auto-restart, switching of the power MOSFET is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency (~110 kHz) for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for > $t_{AR(SK)}$.

The second is included to ensure that if communication is lost, the primary tries to restart. Although this should never be the case in normal operation, it can be useful when system ESD events (for example) causes a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

The first auto-restart off-time is short ($t_{AR(OFF)SH}$). This short auto-restart time is to provide quick recovery under fast reset conditions. The short auto-restart off-time allows the controller to quickly check to determine whether the auto-restart condition is maintained beyond $t_{AR(OFF)SH}$.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection
In the event that there are two consecutive cycles where the I_{LIM} is reached within ~500 ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or ~25 µs (based on full frequency of 100 kHz). This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring
The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A 4 MΩ resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to primary GND.

At power-up, after the primary bypass capacitor is charged and the ILIM state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-in for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of a internal high-voltage (V_V) MOSFET on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. The controller samples the input line at light load conditions when the time between switching cycles is 50 µsec or more. At >50 µsec between switching cycles, the high-voltage MOSFET will remain on making sensing continuous.

Primary-Secondary Handshake
At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from the OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

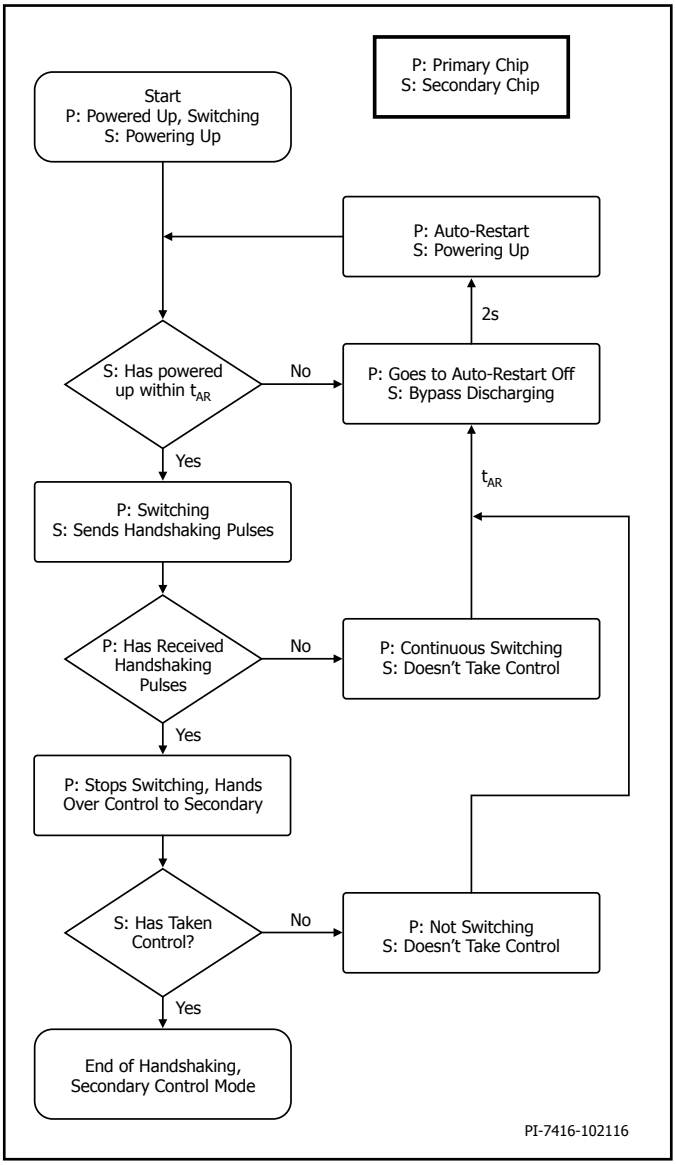

Figure 7. Primary-Secondary Handshake Flow Chart.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If secondary does not detect that the primary responds to switching requests for 6 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 6 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross-conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen

When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 ms, the primary will infer secondary control and begin switching in slave mode. If no pulses occur during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine

The InnoSwitch3-Pro features an active audible noise reduction mode whereby the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 7 kHz and 12 kHz - 142 μs and 83 μs. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power MOSFET is inhibited.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered through regulator 4.4 V block by either VOUT or FW connections to the SECONDARY BYPASS pin. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin is used to sense when to turn off the SR FET in discontinuous mode operation when the voltage across the FET on resistance drops below the $V_{SR(TH)}$ threshold.

In continuous conduction mode (CCM) operation of the SR FET is turned off when the feedback pulse is sent to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off while operating in continuous mode.

The output voltage is regulated on the VOUT pin and defaults to 5 V at start-up.

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins regulates the output current in constant current regulator mode.

Programmable Voltage and Current
The operating voltage and current set points are set fully programmable through I²C interface. The output voltage is fully user programmable with a range from 3 V to 24 V. The fast response feedback loop of the IC features 10 mV (ΔV_{OUT}) voltage change resolution. The programmable current set point features 20% to 100% operating range, with a programming step size of 0.8% of full scale current. Below 5 V and for load current less than 50 mA, voltage command step size of 10 mV may result in non-montonicity since operating frequency is very low.

Internal uVCC Generation, Bus Switch Driver and Discharge
The internal LDO generates 3.6 V uVCC for MCU which simplifies the system design. InnoSwitch3-Pro also has an internal driver that guarantees turn-on of an n-channel MOSFET series bus switch with source voltage as high as 24 V. The VB/D pin which enables the bus switch is also configurable as the discharge path for the load.

Programmable Protections
User programmable protection features include output undervoltage (UV) and overvoltage (OV) protection and over-temperature protection. The UV/OV thresholds are dynamically programmable. Users can program three responses to these protections, including auto-restart, latch-off and no-response. An auto-restart (AR) or latch-off (LO) response does not inherently open the series bus switch. The I²C master must send a command to open it if this is the desired behavior.

The secondary controller also features generation of an interrupt signal if one or more of the faults is detected. The SCL pin is pulled down for ~55 µs to generate an interrupt for MCU.

In the case when the MCU loses communication with the secondary controller, a watchdog timer triggers a reset to reassert a safe 5 V condition and opens the series bus switch.

Telemetry Feature
The controller communicates to the MCU to report back the status of the power supply. Output voltage and current is measured by internal ADC and available to MCU through I²C. The telemetry features also covers CV, CC and constant power set points, OV/UV thresholds, all protection settings, interrupt status, and complete fault status.

Minimum Off-Time
The secondary controller initiates a cycle request using the inductive-connection to the primary. The maximum frequency of secondary-cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency
The maximum switch-request frequency of the secondary controller is f_{SREQ}.

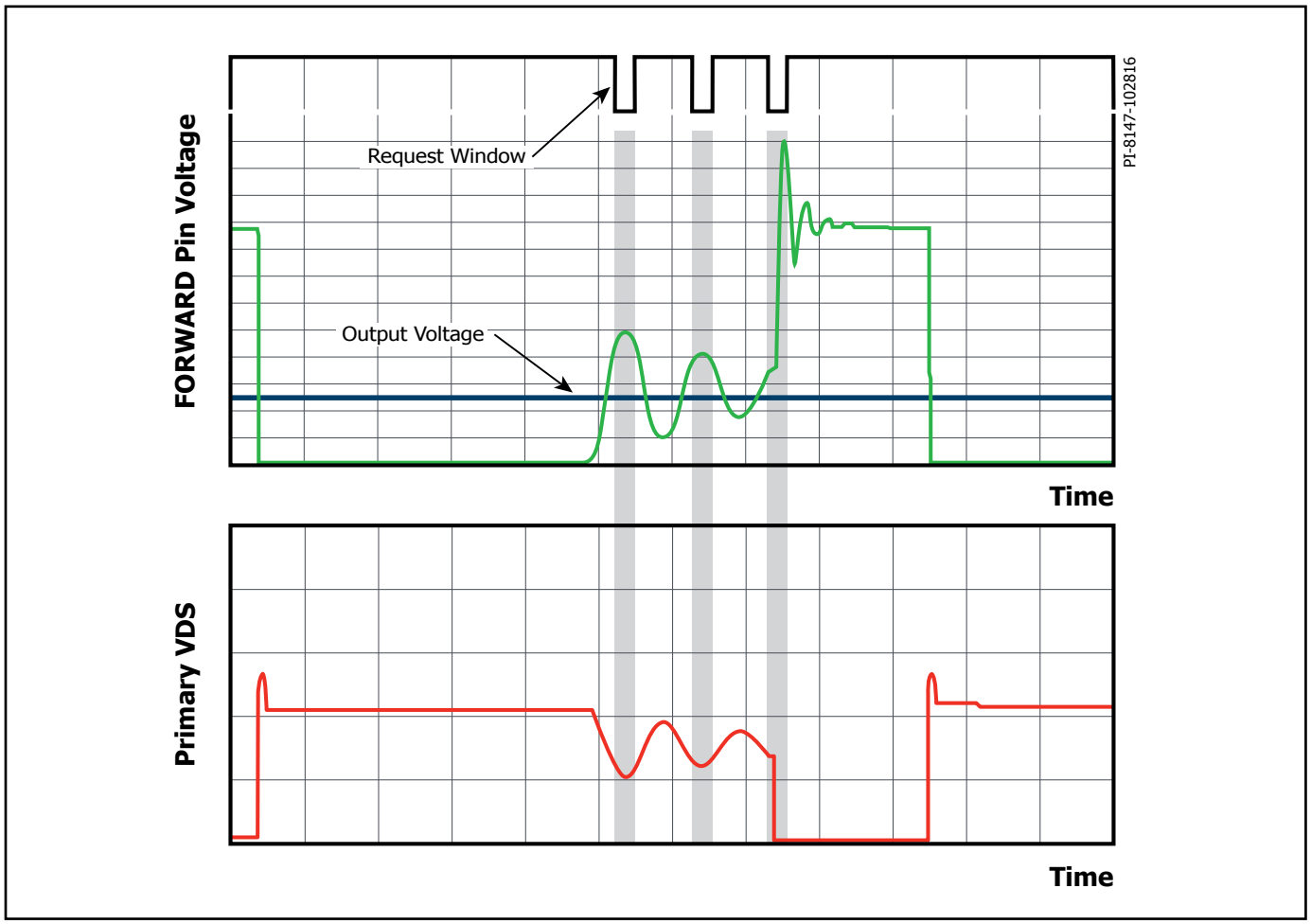

Figure 8. Intelligent Quasi-Resonant Mode Switching.

Frequency Soft-Start
At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 70% of the maximum programmed current limit (at f_{SREQ} operation).

After hand-shake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the $t_{SS(RAMP)}$ time period.

In the event of a short-circuit or overload at start-up, the device will move directly into CC (constant-current) mode. The device will go into auto-restart (AR), if the output voltage does not rise above the 3.6 V before the expiration of the soft start timer ($t_{SS(RAMP)}$) after handshake has occurred.

If the output voltage reaches regulation within the $t_{SS(RAMP)}$ time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant-detection programming has already occurred.

Maximum Secondary Inhibit Period
Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30 µs.

Output Voltage Weak Bleeder
In the event that the sensed voltage on the OUTPUT VOLTAGE pin is 2% higher than the regulation threshold, a bleed current of ~2.5 mA (3 mA max) is applied on the OUTPUT VOLTAGE pin (weak bleed). The current sink on the OUTPUT VOLTAGE pin is intended to discharge the output voltage after momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

SECONDARY BYPASS Pin Overvoltage Protection
The InnoSwitch3-Pro secondary controller features a SECONDARY BYPASS pin OV feature similar to PRIMARY BYPASS pin OV feature. When the secondary is in control, in the event that the SECONDARY BYPASS pin current exceeds $I_{BPS(SD)}$ the secondary will send a command to the primary to initiate an auto-restart off-time ($t_{AR(OFF)}$) or latch-off.

SR Disable Protection
In each cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event that the voltage on the ISENSE pin exceeds approximately 3 times the CC threshold, the SR FET drive is disabled until the surge current has diminished to nominal levels.

SR Static Pull-Down
To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has a nominally "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection
In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. At start-up the controller will apply a current to the SYNCHRONOUS RECTIFIER DRIVE pin; an internal threshold will correlate to a capacitance of 100 pF. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 100 pF the resulting voltage is above the reference voltage, and the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above 100 pF (the resulting voltage is below the reference voltage), the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.

Intelligent Quasi-Resonant Mode Switching
In order to improve conversion efficiency and reduce switching losses, the InnoSwitch3-Pro features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation is automatically engaged in DCM and disabled once the converter moves to continuous-conduction mode (CCM). See Figure 8.

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power MOSFET.

Quasi-Resonant (QR) mode is enabled for 20 µsec after DCM is detected. QR switching is disabled after 20 µsec, at which point switching may occur at any time a secondary request is initiated.

The secondary controller includes blanking of ~1 µs to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground.

Register Definition

I²C Slave Address

The InnoSwitch3-Pro 7-bit slave address is 0x18 (7'b001 1000).

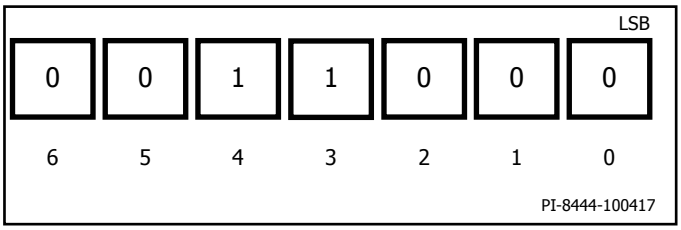

Figure 9. PI Slave Address.

I²C Protocol Format is 3-Byte Write Command

Write commands:
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][Byte][A] or
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][Low Byte][A][High Byte][A]

Write and Read Command I²C Protocol

[A] denotes a Slave Acknowledgement
[a] denotes a Master Acknowledgement
[na] denotes a Master nack
[W] denotes Write (1'b0)
[r] denotes Read (1'b1)
[PI_SLAVE_ADDRESS] = 0x18 (7'b001 1000)
[PI_COMMAND] (see PI COMMAND Register Address Assignments, Description and Control Range Section)
[TELEMETRY_REGISTER_ADDRESS] (see Telemetry (Read-Back) Registers Address Assignment and Description Section)

Every I²C transaction should have at least a 150 µsec delay between commands. If this delay is not provided commands may be ignored. The InnoSwitch3-Pro does not support clock stretching.

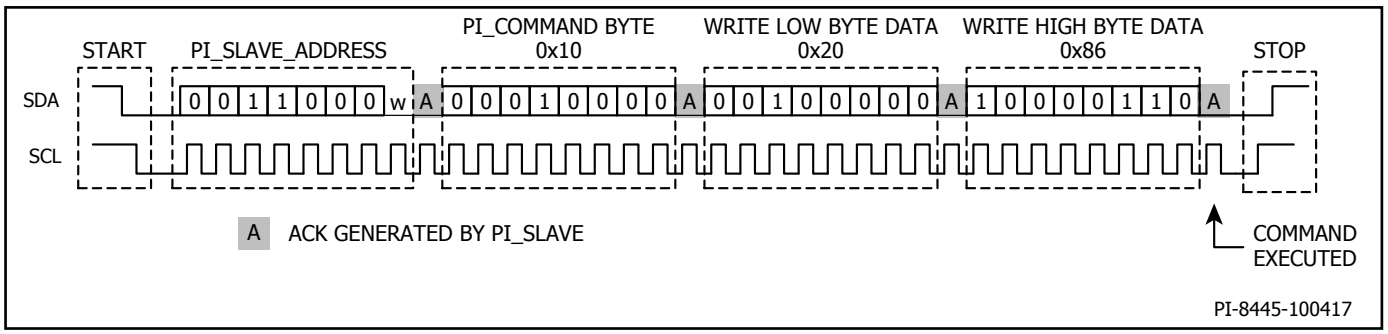

Figure 10. Example Register Write Command Sequence (CV set to 8 V).

I²C Protocol Format is 2-Byte Read Command

Word Read transaction:
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][START_TELEMETRY_REGISTER_ADDRESS]
[A][END_TELEMETRY_REGISTER_ADDRESS [A]
[PI_SLAVE_ADDRESS] [r][A]{PI Slave responds Low Byte}[a]{PI Slave responds High Byte}[na]

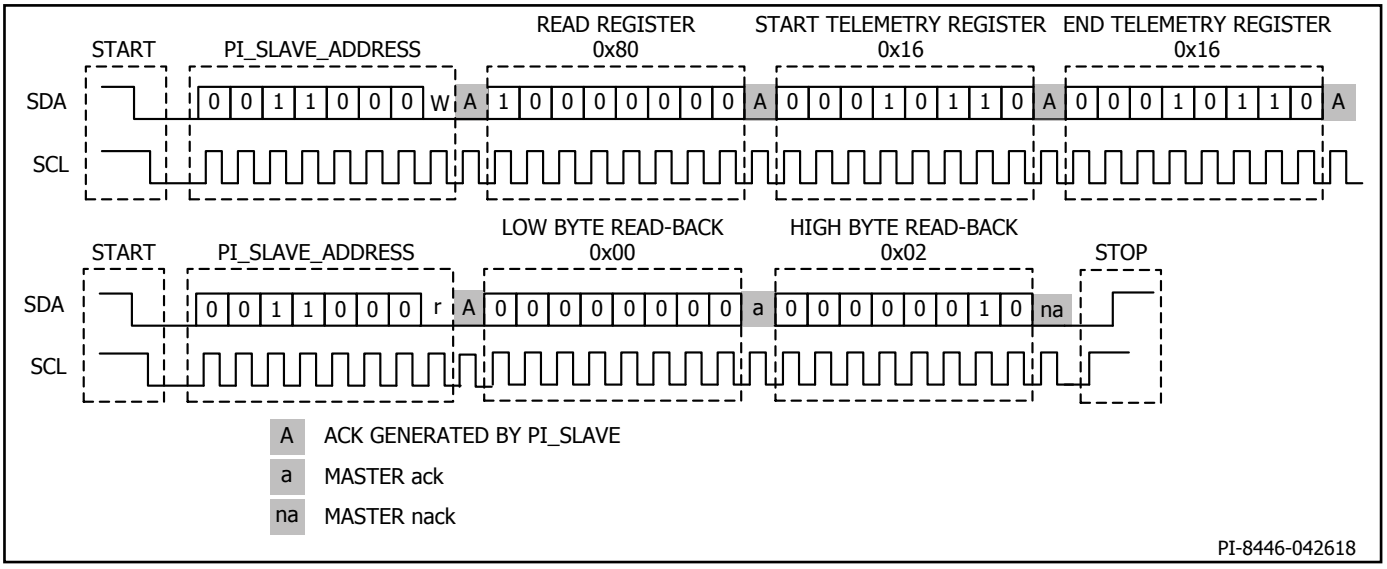

Figure 11. Example Read Register Sequence (Read Fault Register READ11). Note: START and END TELEMETRY Register Addresses Does Not Have to Point to Same Register to Read multiple Registers in Single Command.

PI COMMAND Register Address Assignments, Description and Control Range

All command register addresses in InnoSwitch3-Pro are odd-parity addressing. Some select registers (some highlighted below) also employ odd parity error bit to the high and low bytes of data.

Name	Function	Adjustment Range	Register Address		Type	Default	Description		
			Address	Address with Odd Parity					
VBEN	Series Bus Switch Control	Enable or Disabled?	0x04		WR_Byte	0x0	bit[7]	Parity	
							bit[1:0]	{11} Enable VBEN/Disable VDIS {00} Disable VBEN	
BLEEDER	Activate Bleeder (V_{OUT}) Function	Enable or Disabled?	0x06	0x86	WR_Byte	0x0	bit[0]	{0}: Disabled {1}: Enabled OTP clears this register	
VDIS	Load (VBUS) Discharge	Enable or Disabled?	0x08		W/R_Byte	0x0	bit[7]	Parity	
							bit[1:0]	{11} Enable Discharge/Disable VBEN	
							bit[3:2]	{11} Disable Discharge	
Turn-Off PSU	Latch-off Device	Enable or Disabled?	0x0A	0x8A	W/R_Byte	0x0	bit[0]	{0}: Disabled {1}: Enabled	
Fast VI Command	Speed of CV/CC Update	10 ms Update Limit or No Speed Limit?	0x0C	0x8C	W/R_Byte	0x0	bit[0]	{1}: Disable 10 msec update limit	
CVO	Constant-Voltage Only	Only CV Mode	0x0E		W/R_Byte	0x0	bit[0]	{1}: CV Only Mode/No CC Regulation	
CV	Output Voltage	3 V to 24 V (10 mV/step)	0x10		W/R_Word	500 (5 V)	bit[15]	High Byte Parity	Range {300 to 2400} 10 mV/LSB
							bit[12:8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
OVA	Overvoltage Threshold	6.2 V to 25 V (100 mV/step)	0x12	0x92	W/R_Word	62 (6.2 V)	bit[15]	High Byte Parity	Range {62 to 250} 100 mV/LSB
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
UVA	Undervoltage Threshold	3 V to 24 V (100 mV/step)	0x14	0x94	W/R_Word	36 (3.6 V)	bit[15]	High Byte Parity	Range {30 to 240} 100 mV/LSB
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
CDC	Cable Drop Compensation	0 mV to 600 mV (50 mV/step)	0x16		W/R_Word	0 (0 V)	bit[3:0]	Range {0 to 12} 50 mV/LSB	
CC	Constant Current Regulation	20% to 100% of CC, (0.25 mV/step/Rs)	0x18	0x98	W/R_Word	128 (100%)	bit[15]	High Byte Parity	Range {25 (20%) to 128 (100%)}
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		

Table 2. Command Register Assignments.

Name	Function	Adjustment Range	Register Address		Type	Default	Description	
			Address	Address with Odd Parity				
V_{KP}	Constant Output Power Knee Voltage	5.3 V to 24 V (100 mV/step)	0x1A		W/R_Word	240 (24V)	bit[15]	High Byte Parity
							bit[8]	Range {53 to 240} 100 mV/LSB
							bit[7]	Low Byte Parity
							bit[6:0]	
OVL	Overvoltage Fault Response	Latch-off or AR or No Response?	0x1C		W/R_Byte	0x02	bit[1:0]	{00}: No Response {01}: Latch-off {10}: Auto-Restart
UVL	Undervoltage Fault Response	Latch-off or AR or No Response?	0x1E	0x9E	W/R_Byte	0x0	bit[1:0]	{00}: Auto-Restart {01}: Latch-off {10}: No Response
ISSC	IS-pin Short Fault Response and Detection Frequency	Latch-off or AR or No Response?	0x22	0xA2	W/R_Byte	0x00	bit[1:0]	{00}: No Response {01}: Latch-off {10}: Auto-Restart
		Frequency? (30kHz/40kHz/ 50kHz/60kHz)					bit[3:2]	Frequency Detection Threshold {00}: 50kHz {01}: 30kHz {10}: 40kHz {11}: 60kHz
UVL Timer	UVL Fault Timer	8/16/32/64 msec	0x24	0xA4	W/R_Byte	0x03 (64 msec)	bit[1:0]	{00}: 8 msec {01}: 16 msec {10}: 32 msec {11}: 64 msec
Watchdog Timer	Communication Rate Monitor	Disable/0.5 s/1 s/2 s	0x26		W/R_Byte	0x01 (0.5 sec)	bit[1:0]	{00}: No Watch-Dog {01}: 0.5 sec {10}: 1 sec {11}: 2 sec
CVOL	Constant Voltage Mode Fault Response	Latch-off or AR or No Response?	0x28	0xA8	W/R_Byte	0x00	bit[1:0]	{00}: No Response {01}: Auto-Restart {10}: Latch-off
CVOL Timer	Constant Voltage Fault Timer	8/16/32/64 msec	0x2A		W/R_Byte	0x00 (8 msec)	bit[1:0]	{00}: 8 msec {01}: 16 msec {10}: 32 msec {11}: 64 msec
Interrupt	Interrupt Mask	Writing a non-zero value enables interrupt Interrupt is automatically disabled after one interrupt pulse sent out	0x2C		W/R_Byte	0x00	bit[6]	Control Secondary
							bit[5]	BPS Current Latch-off
							bit[4]	CVO Mode Peak load timer
							bit[3]	IS-pin Short
							bit[2]	
							bit[1]	Vout(UV)
							bit[0]	Vout(OV)
OTP	Secondary Over-Temperature Fault Hysteresis	40°C/60°C	0x2E	0xAE	W/R_Byte	0x00	bit[0]	{0}: 40°C {1}: 60°C

Table 2. Command Register Assignments (cont).

Telemetry (Read-Back) Registers Address Assignment and Description

	Name	Register Name	Register Address		Type	Register Bit Assignments		
			Address	Address with Odd Parity				
	READ0	Rev ID	0x00	0x80	R_Word	bit[15:0]	[Rev ID]	
Command Register Read-Back	READ1	Output Voltage Set-Point	0x02		R_Word	bit[15]	High Byte Parity	{Reg_CV}
						bit[12:8]		
						bit[7]	Low Byte Parity	
						bit[6:0]		
	READ2	Undervoltage Threshold	0x04		R_Word	bit[15]	High Byte Parity	{Reg_UVA}
						bit[8]		
						bit[7]	Low Byte Parity	
						bit[6:0]		
	READ3	Overvoltage Threshold	0x06		R_Word	bit[15]	High Byte Parity	{Reg_OVA}
						bit[8]		
						bit[7]	Low Byte Parity	
						bit[6:0]		
	READ4	VBUS Switch Enable	0x08		R_Word	bit[14]	{Reg_VBEN}	
		Minimum Load				bit[13]	{Reg_BLEEDER}	
		Turn PSU Off				bit[12]	{Reg_PSUOFF}	
		Fast VI Commands				bit[11]	{Reg_FSTVIC}	
		Constant-Voltage Mode Only				bit[10]	{Reg_CVO}	
		Over-Temperature Fault Hysteresis				bit[9]	{Reg_OTP_HYS}	
		Cable Drop Compensation				bit[3:0]	{Reg_CDC}	
	READ5	Constant Current Set-Point	0x0A		R_Word	bit[15:8]	{Reg_CC}	
		Constant Power Threshold				bit[7:0]	{Reg_VKP}	
Programmed Fault Respose	READ6	Overvoltage Fault	0x0C		R_Word	bit[15:14]	{Reg_OVL}	
		Undervoltage Fault				bit[13:12]	{Reg_UVL}	
		IS-pin Short				bit[9:8]	{Reg_ISSC}	
		Undervoltage Time Out				bit[7:6]	{Reg_UVLTIMER}	
		Watchdog Time Out				bit[5:4]	{Reg_WD_TIMER}	
		CV Mode				bit[3:2]	{Reg_CVMODE}	
		CV Mode Timer				bit[1:0]	{Reg_CVTIMER}	
Measurement	READ7	Measured Output Current	0x0E		R_Word	bit[15]	High Byte Parity	{Reg_MEASURED_I}
						bit[8]		
						bit[7]	Low Byte Parity	
						bit[6:0]		
	READ9	Measured Output Voltage	0x12		R_Word	bit[15:12]	4'b0	
						bit[11:0]	{Reg_MEASURED_V}	
							Vout Range	Report-back resolution
							3 - 7.2 V	20 mV
							7.2 - 10 V	50 mV
							10 - 20 V	100 mV

Table 3. Telemetry (Read-Back) Register Assignments.

Name	Description	Register Address		Type	Register Name	
		Address	Address with Odd Parity			
READ10 (Instantaneous)	Interrupt Enable	0x14		R_Word	bit[15]	{Reg_INTERRUPT_EN}
	System Ready Signal				bit[14]	{Reg_CONTROL_S}
	Output Discharge				bit[13]	{Reg_VDIS}
	Switching Frequency High?				bit[12]	{Reg_HIGH_FSW}
	Over-Temperature Protection Fault?				bit[9]	{Reg_OTP}
	2% Bleeder Enabled				bit[5]	{Reg_VOUT2PCT}
	VOUTADC > 1.1*Vout				bit[4]	{Reg_VOUT10PCT}
	IS-pin Short Circuit Detected				bit[3]	{Reg_ISSC}
	Output Voltage UV Fault Comparator				bit[1]	{Reg_VOUT_UV}
	Output Voltage OV Fault Comparator				bit[0]	{Reg_VOUT_OV}
READ11 (Latched)	CVO Mode AR	0x16		R_Word	bit[15]	{Reg_ar _CV}
	IS-pin Short-Circuit AR				bit[12]	{Reg_ar_ISSC}
	Output Voltage OV AR				bit[10]	{Reg_ar_VOUT_OV}
	Output Voltage UV AR				bit[9]	{Reg_ar_VOUT_UV}
	Latch-Off (LO) Occurred				bit[7]	{Reg_LO}
	CVO Mode LO				bit[6]	{Reg_Lo_CVO}
	PSU Turn-Off CMD Received				bit[5]	{Reg_PSUOFF}
	IS-pin Short-Circuit LO				bit[4]	{Reg_Lo_ISSC}
	Output Voltage OV LO				bit[2]	{Reg_Lo_VOUT_OV}
	Output Voltage UV LO				bit[1]	{Reg_Lo_VOUT_UV}
	BPS-pin LO				bit[0]	{Reg_BPS_OV}
READ12	Interrupts	0x18		R_Word	Mask	Status
					bit[14]	bit[6]	{Reg_CONTROL_S}
					bit[13]	bit[5]	{Reg_LO_Fault}
					bit[12]	bit[4]	{Reg_CCAR}
					bit[11]	bit[3]	{Reg_ISSC}
					bit[10]	bit[2]	
					bit[9]	bit[1]	{Reg_VOUT_UV}
					bit[8]	bit[0]	{Reg_VOUT_OV}
READ13	Average Output Current	0x1A		R_Word	bit[15:12]	4b'0
					bit[11:0]	16 sample average of READ 9
READ14	Average Output Voltage	0x1C		R_Word	bit[15:8]	8b'0
					bit[7:0]	16 sample average of READ 7
READ15	Voltage DAC	0x5C		R_Word	bit[15:8]	DAC_100mV
					bit[7:0]	DAC_10mV

Table 3. Telemetry (Read-Back) Register Assignments (cont.)

Command Registers

System Ready Status Register

The system ready bit {Reg_control_s} must be read prior to the start of any I²C transactions and after the InnoSwitch3-Pro has entered into a reset state resulting from auto-restart (AR), latch-off (LO) or initial power-up.

When the {Reg_control_s} bit is set to "1", it means InnoSwitch3-Pro is ready to receive I²C commands.

To read the {Reg_control_s} bit, write the READ10 sub address 0x14 into the 0x80 address. Then read High Byte data back from address 0x80. The bit 14 is {Reg_control_s}.

Constant current regulation is based on the average current measurement register (READ13).

For a 5 A CC threshold, the current sense resistor is 6.4 mΩ.
The current limit step size for this example is 39.1 mA/step.

Example: For a power supply with maximum CC of 5 A (Rs = 6.4mΩ), the following demonstrates changing the CC set point from 5 A to 2.5 A. This corresponds to change in CC from 100% (0x80) to 50% (0x40) – with odd parity this becomes 0x8040:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CC Register (0x98)
Low Byte:	0x40 (8'b0100 0000)
High Byte:	0x80 (8'b1000 0000)

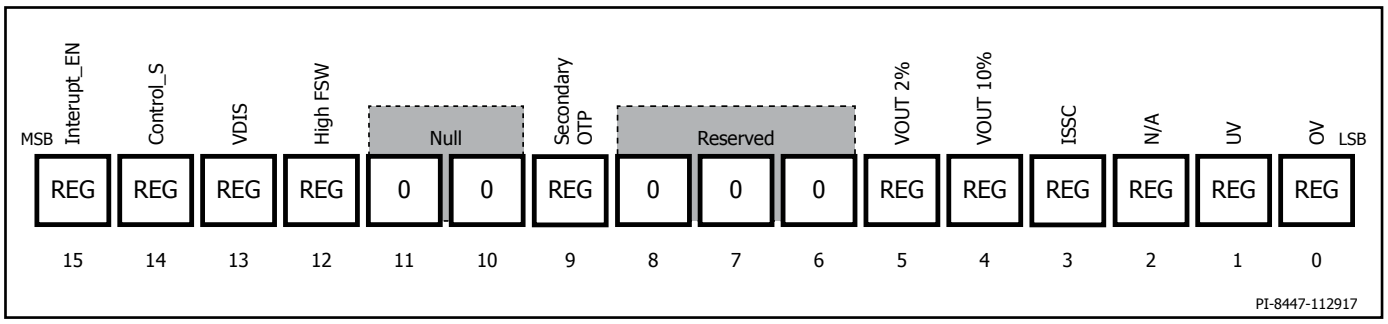

Figure 12. {Reg_Control_s} Telemetry Register.

Example: Reading the {Reg_control_s} bit:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
Read Register:	0x80
PI_Command:	READ10 (0x14), READ10 (0x14)
PI_SLAVE_ADDRESS [r]:	0x31 (8'b0011 0001)

Programming Output Voltage (CV), Output Constant Current (CC), Constant Power Mode (CP), Cable Drop Compensation (CDC) and Constant Voltage Only Mode (CVO)

CV Register (0x10)
The output voltage of the power supply is regulated on the Vout-pin. The valid programming range is from 3 V to 24 V with 10 mV / lsb. The default CV register value is 5 V. Below 5 V and at light load below 50 mA, output monotonicity may not be visible with 10 mV / steps.

Example: to change CV from 5 V to 8 V
Convert 8 V to lsb representation: 8/(10mV/lsb) = 800
Convert to hex format (800 = 0x0320)
With odd parity bits added the hex data is 0x8620)
The bit I²C command for this is shown below:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CV Register (0x10)
Low Byte:	0x20 (8'b0010 0000)
High Byte:	0x86 (8'b1000 0110)

This sequence of commands is shown in Figure 10 and Figure 23.

CC Register (0x98)
The constant current regulation register address is 0x18 and with odd parity it is 0x98. The constant current regulation threshold is adjustable from 20% (d'25) CC up to 100% (d'128) of the full scale. The full-scale constant-current threshold is set with the sense resistor between the IS and GND pins. The typical value for the full-scale current voltage drop is 32 mV ($I_{SV(TH)}$). The resolution step size is (0.78%/step):

32 mV/128 = 0.25 mV/step/Rs

Constant Output Power Voltage Threshold V_{KP} (0x1A)
A constant output power characteristic is programmed via the "knee power voltage" in conjunction with the 100% constant current regulation threshold (full-scale current setting). If the full-scale CC is 2.5 A and the knee power voltage is set to 8 V, the constant power is 20 W. If the V_{KP} register were set to 12 V, the resultant constant power characteristic above the V_{KP} threshold would be 30 W.

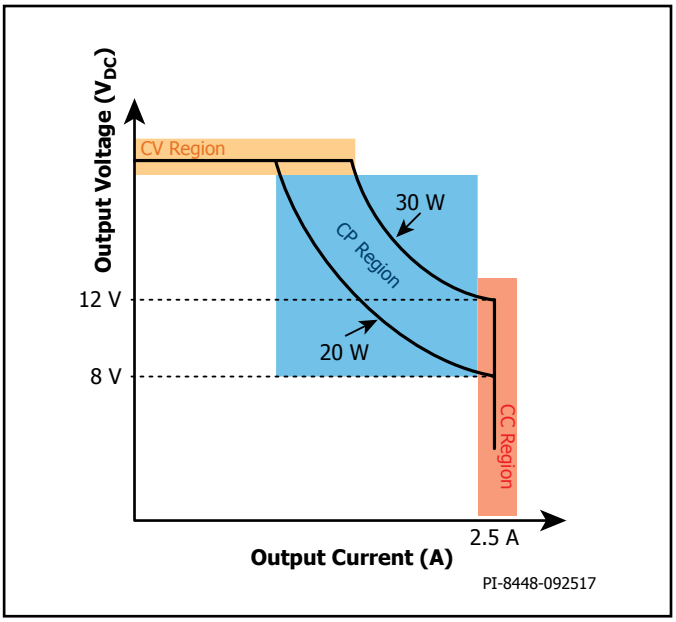

Figure 13. Constant Output Power Profile.

From no-load to heavy loading conditions, InnoSwitch3-Pro will operate in CV then transition into CP then into CC region below the V_{KP} threshold. Setting V_{KP} to maximum value (24 V) results in no Constant Output Power regulation region.

Example: To change V_{KP} from 24 V (d'240) (0xF0 = 0x0170 with odd parity) to 8 V (0x50 = 0x80D0):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VKP Register (0x1A)
Low Byte:	0xD0 (8'b1101 0000)
High Byte:	0x80 (8'b1000 0000)

Reducing the constant current regulation threshold does not modify the maximum programmed output power with a given V_{KP} setting. From the example shown above, setting CC regulation to 2 A (full-scale CC is still 2.5 A), with V_{KP} = 8 V, would result in output profile shown below with CP characteristic intercept of 10 V for the same 20 W constant power characteristic.

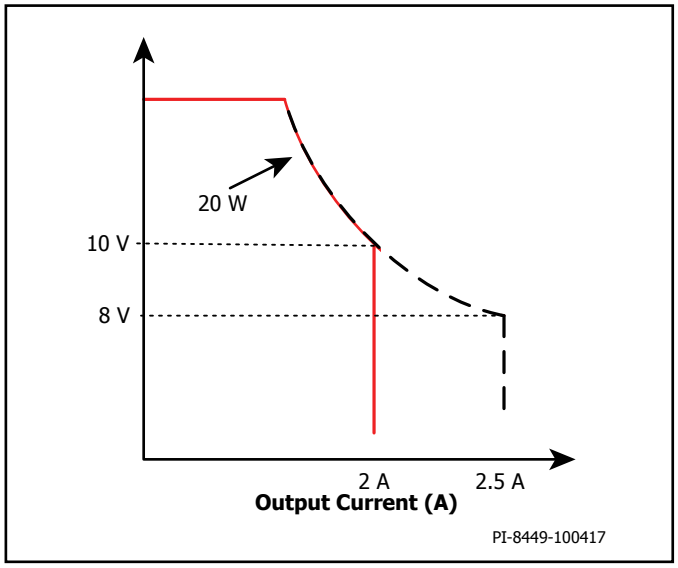

Figure 14. Constant Output Power Profile with Reduced CC Regulation Threshold.

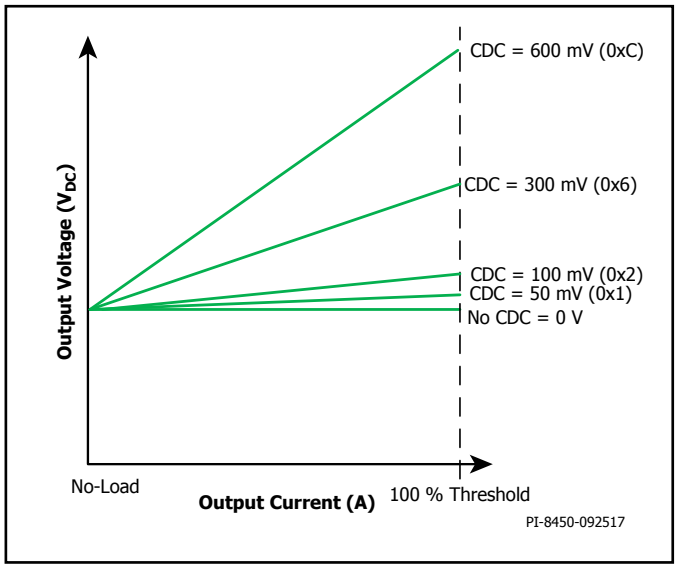

Figure 15. CDC as Function of Load Current.

Cable Drop Compensation (CDC) (0x16)

The amount of cable drop compensation has a controllable range of 0 V to 600 mV in 50 mV/steps. CDC is applied as a function of the current through the sense resistor (resistor between IS and GND pins) used to program the constant current regulation threshold. At no-load there is no CDC and the compensation is increased linearly as load increases and reaches the maximum programmed value at the onset of the 100% constant-current regulation threshold (full-scale voltage across the current sense resistor).

The table below shows the register values to program the desired CDC:

CDC (mV)	Hex Value	Binary
0	0x00	4'b0000
100	0x02	4'b0010
150	0x03	4'b0011
200	0x04	4'b0100
250	0x05	4'b0101
300	0x06	4'b0110
350	0x07	4'b0111
400	0x08	4'b1000
450	0x09	4'b1001
500	0x0A	4'b1010
550	0x0B	4'b1011
600	0x0C	4'b1100

Table 4. Cable Drop Compensation.

If the current sense resistor between IS pin to GND pin is shorted, there will be neither any cable drop compensation nor any constant current regulation.

Example: To change CDC from 0 V to 300 mV (0x06):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b1011 0000)
PI_Command:	CDC Register (0x16)
Byte:	0x06 (4'b0110)

Constant Voltage Only Mode (0x0E)

The InnoSwitch3-Pro can be programmed to operate with constant-voltage only and have no constant current regulation mode. The set output current register (0x98) sets the over-load threshold instead of regulating the constant current when the CVO mode is enabled. Once the load current exceeds the programmed current a peak load timer (t_{PLT}) is started. The options for the peak load timer (CVOL Timer Register 0x2A) are 8/16/32 and 64 ms. If the peak load exceeds the programmable timer, the InnoSwitch3-Pro can be programmed to respond to this fault as auto-restart, latch-off or no-response through the CVOL Register 0xA8. The default response for CVOL (CVO response) is no-response with 8 ms timer.

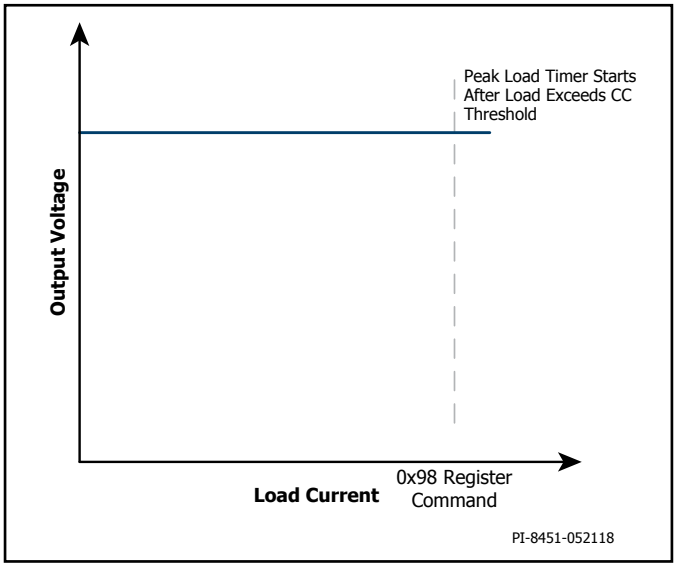

Figure 16. Constant Voltage Only (CVO) Mode.

Example: Enable CVO Mode, set t_{PLT} to 16 msec and fault response to latch-off (LO):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CVO Register (0x0E)
Byte:	0x01 (1'b1)
PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CVOL Timer Register (0x2A)
Byte:	0x01 (2'b01)
PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CVOL Register (0xA8)
Byte:	0x02 (2'b10)

The output undervoltage protection mode discussed in Output Overvoltage and Undervoltage Protection Thresholds/Fault Behavior section is still active in the CVO mode of operation even if the individual UV fault response is set to 'No response'. The following control flow-chart shows the expected behavior of the device under the different potential programming scenarios.

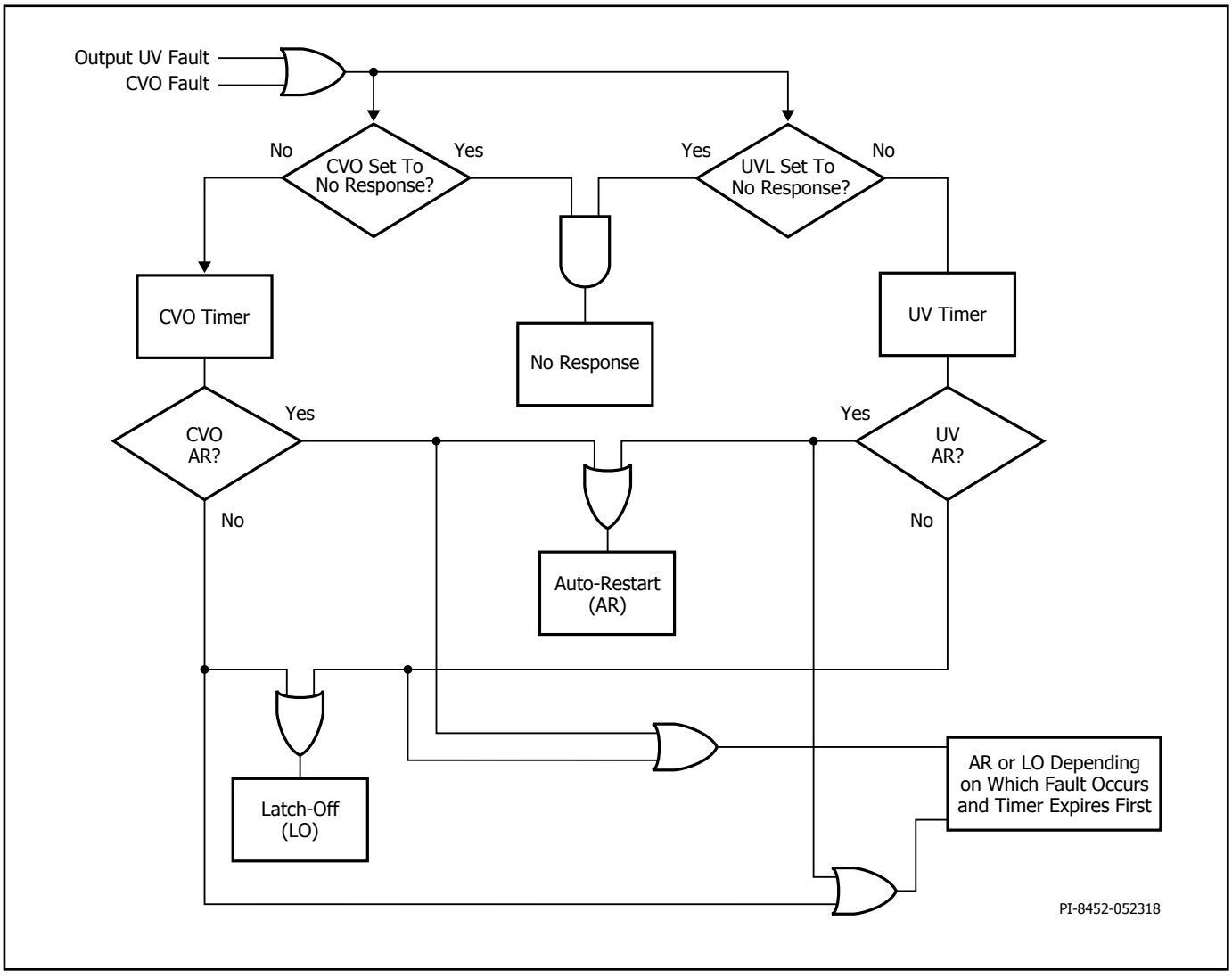

Figure 17. CVO and Output UV Control.

Programmable Protection Mechanisms

Output Overvoltage and Undervoltage Protection Thresholds/Fault Behavior

Besides the ability of programing the OV/UV thresholds on the fly as a function of the set CV, the behavior of the power supply once a fault occurs (a. No-Fault which just sets the fault register, b. Auto-restart (AR) or c. Latch-off (LO) the power supply) and timing for the UV fault detection (8 to 64 msec) is programmable as well. The output overvoltage delay is fixed at ~80 µs. All faults that are programmed to have no-fault respose will be logged into the telemetry read-back fault register. Since the minimum UV setting is 3 V, the response should be set to no-response for 3 V operation.

OVA(0x92) : write to this address to specify the overvoltage threshold
UVA(0x94) : write to this address to specify the undervoltage threshold
OVL(0x1C) : write to this address to specify the behavior to OV fault
UVL(0x9E) : write to this address to specify the behavior to UV fault
UVL Timer(0xA4) : write to this register specify the UV timer

Example: To change the absolute output undervoltage threshold 3 V (d'30) (0x809E with odd parity) fault response to latch-off (LO) (0x01) and configure fault timer to 64 msec (0x03):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	UVA Register (0x94)
Low Byte:	0x9E (8'b1001 1110)
High Byte:	0x80 (8'b1000 0000)

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	UVL Register (0x9E)
Byte:	0x01 (2'b01)

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	UVL Timer Register (0xA4)
Byte:	0x03 (2'b11)

IS Pin Short-Circuit Fault Protection

The InnoSwitch3-Pro can be configured to monitor whether a short-circuit fault occurs across the output current sense resistor or a short-circuit fault across the IS to GND pins.

A fault is annunciated in the event the IS pin voltage does not exceed approximately 50% of the full constant-current threshold ($IS_{V(TH)}$) with a switching frequency exceeding a programmed threshold. The switching frequency can be selected in a range from 30 to 60 kHz. This must be carefully selected to suit the expected operating conditions of the design.

An IS pin short (ISSC) can be programmed to have a response to be a. No-fault, b. Auto-restart (AR) or c. Latch-off (LO). In the event the behavior is a No-fault, the Telemetry Read-Back Fault Register is logged.

ISSC(0xA2) : write to this address to specify the behavior for an IS-GND short.

Example: To set the behavior of an IS pin short to AR for switching frequency exceeding 40 kHz. (4'b10 10 = 0x10):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	ISSC register (0xA2)
Byte:	0x10 (4'b1010)

Watchdog Timer (0x26)

The Watchdog timer supervises the communication on the I²C command lines and has an adjustable time-out. InnoSwitch3-Pro will go into a reset state if I²C commands are not received within the programmable time interval. The watchdog timer does not engage until the master issues the first I²C command (Read or Write). In the reset state the following occurs:

1. VBUS Switch is Disabled (Series switch is open).
2. VOUT pin voltage regulates at the default 5 V threshold.
3. All command Registers are cleared.

By writing 0x00 into register 0x26, the Watchdog timer is disabled. Disabling this feature can be useful in initial software debugging or checking functionality of the device on the bench.

Example: To disable the Watchdog timer:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Watchdog Timer Register (0x26)
Byte:	0x00 (2'b00)

Opening and Closing the Series VBUS Switch (0x04)

Enabling VBEN (closing the VBUS Series Switch) speeds up the ADC sampling frequency in order to achieve high control accuracy. Write commands cannot be accepted faster than 80 msec when the VBEN is disabled (Series VBUS Switch open).

Write 0x03 (with odd parity this becomes 0x8083) into the VBEN register (0x04) to close the series VBUS Switch and write 0x00 to this register to open the switch. When the VBUS switch is open (VBEN disabled), the system is reset to the default output voltage set point of 5 V. Disabling the series VBUS switch also resets all the programmable command registers to their default values. The InnoSwitch3-Pro controller is in a state of reset when VBEN is disabled or the VDIS register is enabled. For both these commands, since the controller is in reset, an ACK or Nack at the end of the command should not be expected.

Enabling the VBEN register automatically disables the VDIS register (0x08) described in Active VOUT Pin Bleeder and Output Load Discharge Functions section.

Example: Enabling (Closing) the Series VBUS Switch (0x8083):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VBEN Register (0x04)
Byte:	0x83 (8'b1000 0011)

Prior to sending command to open the series bus switch, a command to set the output voltage (CV registor 0x10) to 5 V is recommended. In the event of an auto-restart or latch-off, the bus switch is not disabled.

Turn-Off the Power Supply (0x8A)

The I²C master has the ability to turn-off the power supply (through an I²C command), which will require AC power cycling to restart the power supply.

Example: Turn-off the power supply:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Turn-Off PSU Register (0x8A)
Byte:	0x01 (1'b1)

Fast VI Command

By default, the maximum speed in which CV (0x10) and CC (0x98) commands can be sent to program output voltage/current respectively is 10 msec. However, the speed limit can be removed by setting 0x1 to the Fast VI Command Register (0x8C).

Example: To disable speed limit for V/I commands:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Fast VI Speed Register (0x8C)
Byte:	0x01 (1'b1)

Active VOUT Pin Bleeder and Output Load Discharge Functions

There may be circumstances where the VOUT pin strong bleeder function must be activated to discharge the output voltage from a high to low regulation set point.

The VOUT bleeder can be activated by writing 0x01 into BLEEDER Register (0x86).

The BLEEDER register must not be enabled for extended period of time to prevent excessive power dissipation in the controller. When the BLEEDER function is being used to bleed the output voltage from high to low set point, the status of the V_{OUT}10PCT register (bit 4 in the READ10 0x14 read register) should be used to disable the function. The VOUT10PCT register is set once the output voltage is above 10% of the target regulation voltage. The 2% Bleeder Enabled Register, READ10 (0X14) bit 5 can be used instead of the VOUT10PCT to determine when the BLEEDER register should be disabled for no-load transients from high to low output voltage transitions.

The InnoSwitch3-Pro automatically activates a weak current bleeder (>5mA) on the VOUT pin until the output voltage settles to less than 2% of the set regulation threshold.

The InnoSwitch3-Pro can also discharge the VBUS output voltage by bringing the VB/D pin to ground. The discharge circuit is a series diode + resistor tied from the VBUS output to the VB/D pin shown in the typical application schematic. Load discharge function can be activated by writing 0x03 (0x8083 with odd parity) into VDIS register (0x08).

Enabling the VDIS register will automatically disable the VBEN register (0x04) and reset the device to the default state.

The I²C master can use telemetry to monitor the VOUT pin voltage or a fixed timer to help determine when to disable both these functions.

Example: Activate the Vout Bleeder:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: BLEEDER Register (0x86)
Byte: 0x01 (1'b1)

Example: Discharge the VBUS Output:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: VDIS Register (0x08)
Byte: 0x83 (8'b1000 0011)

Secondary Over-Temperature Protection (0xAE)

As the secondary controller die temperature increases beyond ~125 °C, the active VOUT pin bleeder function described above will be turned off. The bleeder will not be permitted to be re-enabled until the controller temperature falls below the programmable hysteresis value.

Example: Set Secondary OTP Hysteresis to 60 °C:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: OTP Register (0xAE)
Byte: 0x01 (1'b1)

Transient Response

If faster transient response is required in the application the InnoSwitch3-Pro includes command registers to reduce the time for low to high output voltage transitions. The command register addresses and recommended settings are shown in the table below:

Command Register Address	Default		Recommended for Speed Up	
	MSB	LSB	MSB	LSB
0x32	0x28	0x1E	0x14	0x0A
0x34	0x08	0xC8	0x0F	0x84

Using values other than the default or recommended settings about could lead to oscillatory behavior.

Constant Voltage Load

The constant current regulation mode in the InnoSwitch3-Pro can be optimized for constant voltage (CV) type load if this is required by the end application. Enabling this command register reduces the output current ripple for CV load only. The command register and setting below should only be used if CV load must be supported.

Command Register Address	Default		Recommended for CV Load	
	MSB	LSB	MSB	LSB
0x30		0x20		0x80

Telemetry (Read-back) Registers

Telemetry read registers (READ1 to READ6) show the content of all the command registers in Table 2.

Fault Registers

All the command registers including set voltage, set current, constant-power knee voltage, control (Series VBUS Switch, VOUT pin Bleeder, Load discharge etc.) and all fault status can be read-back using the Telemetry functionality of the InnoSwitch3-Pro through I²C.

The READ10 telemetry registers are instantaneous and are cleared whenever the condition is no longer valid.

The READ11 (0x16) Register contains fault register data for auto-restart and latch-off. This register is only cleared when the BPS pin falls below its undervoltage threshold or the series VBUS switch is opened.

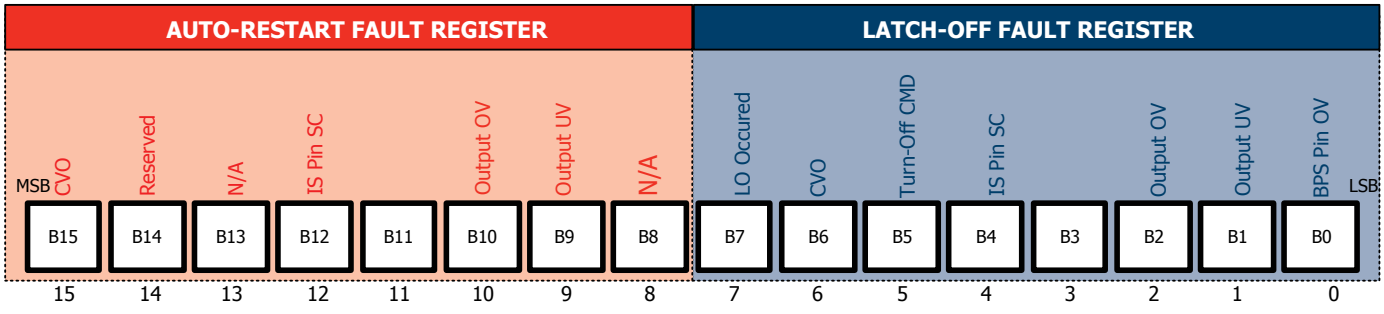

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Figure 18. READ11 Fault Telemetry Register Assignments.

Example: Read the Fault Telemetry Register to determine an auto-restart occurred due to an output undervoltage (UV) Fault:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
Read Register: 0x80
Telemetry Register: 0x16, 0x16

PI_SLAVE_ADDRESS [r]: 0x31 (8'b0011 0001)

PI_Slave Response: Low Byte 8'b0000 0000 (0x00)
High Byte 8'b0000 0010 (0x02)

Refer to Figure 11 and Figure 24 that illustrates this read sequence.

Type of Fault	High-Byte	Low-Byte
Auto-Restart: CVO Mode	0x80	0x00
Auto-Restart: IS pin Short-Circuit	0x10	0x00
Auto-Restart: Output Voltage OV	0x04	0x00
Auto-Restart: Output Voltage UV	0x02	0x00

Table 5. Summary of Telemetry Fault Codes.

Main Regulation DAC Input

The READ15 telemetry register is the input into the main regulation loop that controls constant voltage, constant current and constant output power regulation. If this register is the same as the Set CV Register (0x10) the converter is operating in constant-voltage mode. If the READ15 is less than the Set CV Register (0x10) the converter is operating in constant-current (CC) or constant-power (CP) mode depending on the value of the Constant Power Knee Voltage Register (0x1A).

The output voltage from the READ15 register is computed as V_{OUT} = 5 V + (MSB × 100 mV) – (LSB x 10 mV).

Example: READ15 (0x5C): MSB = 0x00, LSB = 0x0E
LSB is d'14 so the computed V_{OUT} = 5 – (14 × 10 mV) = 4.86 V

Fault Signaling Interrupt Through SCL Pin

In order to improve the fault reporting, an active interrupt reporting scheme is featured on the SCL pin during I²C idle state (when both SDA and SCL pins are pulled high).

When a fault occurs, the SCL pin will behave in one of the following two conditions:

1. When the SCL pin is in idle mode (see Figure 19), the fault interrupt will happen as soon as the fault is detected. The interrupt pulls down the SCL pin for 50 µsec then releases it back to HI State.

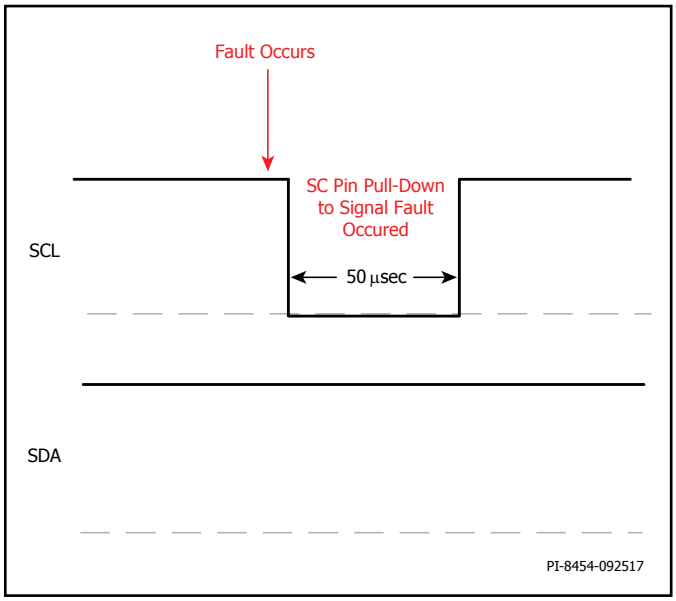

Figure 19. Interrupt Mask During Idle I²C.

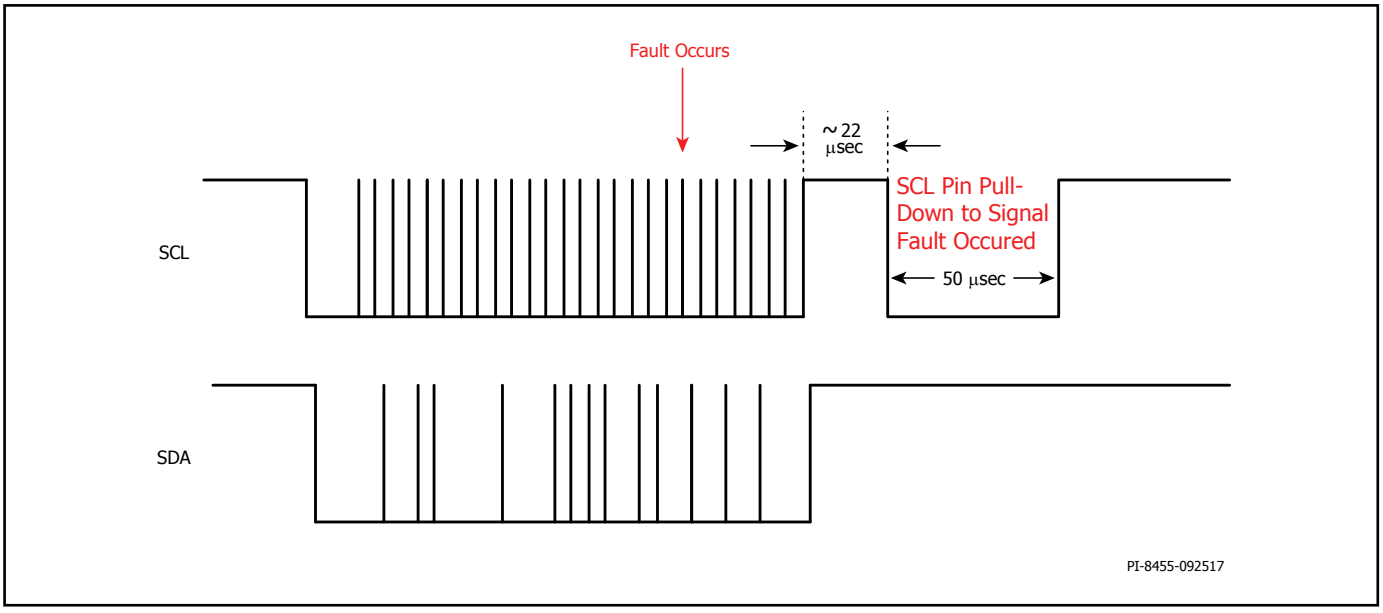

Figure 20. Interrupt Mask During Active I²C Transaction.

2. When the SCL pin is busy (active I²C transaction) (see Figure 20), the fault interrupt will wait for the I²C transaction to be completed, wait ~22 µsec and then pull down the SCL line for 50 µsec (minimum) then releases it back to HI State.

The Interrupt Mask Write Register (0x2C) must be enabled for each of the individual fault conditions shown below in order to activate this feature. Once a fault occurs, the Interrupt Mask is reset and the particular faults of interest must be re-enabled to activate the SCL reporting scheme. The Control Secondary Interrupt (Bit 6) is an indication that the secondary controller is waiting to handshake with primary. Several system faults could trigger this event such as primary-side thermal shutdown or an input line under or overvoltage condition.

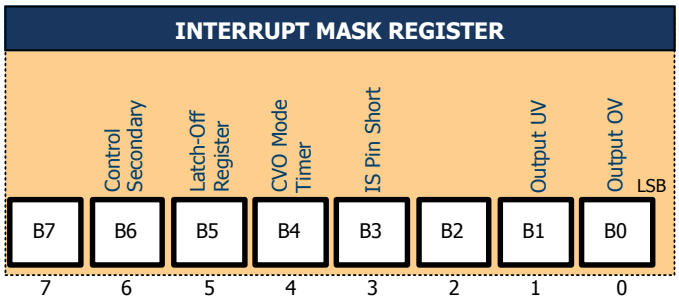

Figure 21. Interrupt Mask Register.

Example: Set the Interrupt Write Register to flag SCL pin fault for output OV, UV or short-circuit only:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: INTM Register (0x2C)
Byte: 0x07 (8'b0000 0111)

Output Voltage Measurement

The voltage on the VOUT pin is available on the Telemetry Register READ 9 (0x12). The tolerance of this telemetry register is ±5% over the entire regulation range of 3 to 24 V.

When the output voltage is below 5 V at loads below ~50 mA, the read back voltage may fluctuate due to very low switching frequency of the converter. This is normal and expected behavior.

The output voltage report back is in 12-bit format but the resolution depends on the output voltage range as shown in Table 6. This telemetry register is for indication only, in steady-state operation the VOUT pin is very tightly regulated per the CV Write Register (0x10) discussed in CV Register (0x10) section.

The report back resolution step size depending on output voltage is tabulated below:

Output Voltage Range (V)		Resolution Step Size
3	7.2	20 mV
7.2	10	50 mV
10	24	100 mV

Table 6. Output Voltage Report Back Resolution.

If the actual output voltage is 5.11 V (CV Write Register 0x10 set to 0x837F.)

The READ9 register will be at 5.10 V or 5.12 V since the resolution step size is 20 mV in this range

Example: If the READ 9 read-back register value is 0xA801 recalling that low byte precedes the high byte, the proper hex to decimal conversion would be from 0x01A8 = 424 in decimal.

The full output voltage range the report back should be divided by 10 mV to convert into actual output voltage, which in this example results in an output voltage of 4.24 V.

Read-back of the output voltage set-point READ1 (0x02) as with all the read registers is formatted with low-byte preceding the high-byte.

Output Current Measurement

The load output current is also available on the Telemetry Register.

Telemetry Register READ7 (0x0E) contains the measured relative output load current data. The load current is available on a relative basis with respect to the full-scale constant current regulation threshold programmed by the sense resistor tied between the IS and GND pin of the InnoSwitch3-Pro.

The ADC full range is 128, which denotes 100% threshold across the current sense resistor.

The accuracy of the output current read-back is tightest at full scale and decreases as the voltage threshold across the current sense resistor decreases as shown in Figure 22.

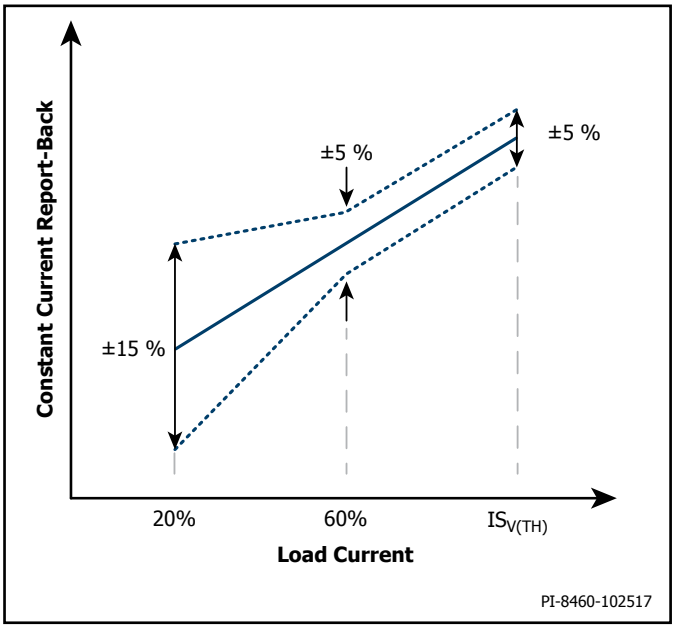

Figure 22. Constant-Current Report Back Tolerance.

Example: If a 16 mΩ sense resistor is used and the read-back register is 0x8040.

Removing the odd parity bit from high byte results in 0x40 = 64 in decimal.

Sensed current value = N (decimal) x $0.25/R_{SENSE}$.
64 x 0.25/16 = 1A. This is the measured output current value:

(0.25 mV = 32 mV/128, where 32 mV ($I_{SV(TH)}$) is the full range R_{SENSE} voltage, 128 is the ADC full range).

The READ13 and READ14 are 16 sample rolling averages of the measured output current and output voltage respectively. The value of these average registers is more stable than the instantaneous registers (READ7 and READ9) but take slightly longer to stabilize. When the series BUS switch is opened these registers are cleared and values are reset to zero until the measurement start to accumulate. The resolution of READ 13 and READ 14 is the same as the READ7 and READ 9 respectively.

The output voltage and current measurement registers are updated every 100 μs.

I²C Connection

uVCC External Power Supply

The uVCC pin provides an accurately regulated 3.6 V supply to an external controller. The maximum load current capability of this supply is 50 mA (I_{uVCC})for 0.5 seconds when the VOUT pin is greater than or equal to 5 V. For steady-state operation, it is expected the current drawn from uVCC is less than 10 mA. The uVCC pin should be decoupled to the GND pin with at least a 2.2 μF ceramic capacitor. When the VOUT pin voltage is less than 3.9 V, the internal LDO will droop and follow VOUT pin voltage. Under these conditions, the uVCC pin voltage is dependent on load current and internal series impedance. At VOUT pin = 3 V and 6 mA load current on uVCC, the expected output on uVCC will be ~2.85 V (3 V – 24 Ω x 6 mA).

If the VOUT pin voltage falls sufficiently to cause the uVCC pin to go below the $uVCC_{RST}$ threshold, communication through I²C is no longer available.

SCL/SDA Pull-up Requirements

The SCL and SDA-pins should be pulled-up to the uVCC pin with a resistor. The maximum pull-up resistance is dependent on the capacitance of the SCL/SDA pins and I²C Master. The resultant voltage fall-time to the V_{IL} threshold assuming a total capacitance of 20 pF is tabulated as function of SCL clock frequency in the table below.

Max Frequency (kHz)	Max Pull-Up Resistance (kΩ)	t_F (ns)
400	13	300
500	10	240
600	8	200
700	7	178

Table 7. I²C Pull-Up Resistor Values.

I²C Example Waveforms

Setting The Output Voltage To 8 V

Same as Example shown in Figure 10.

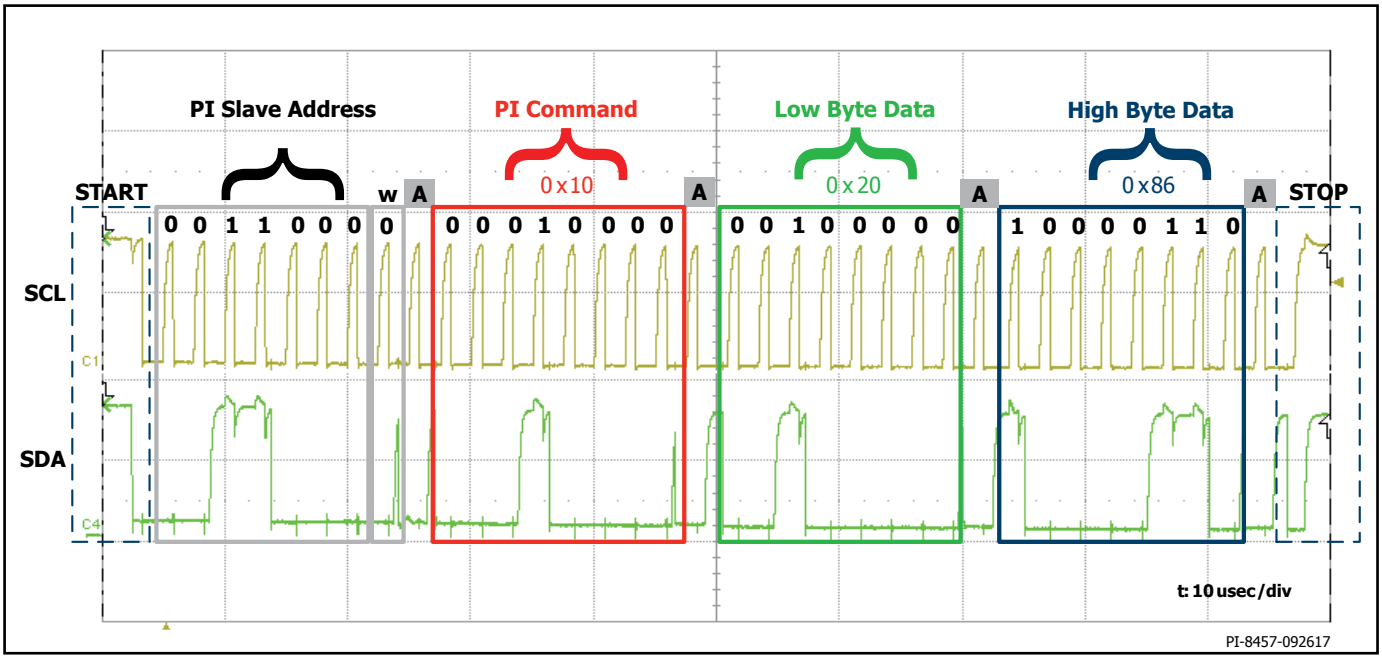

Figure 23. I²C Waveforms for Setting Output Voltage to 8 V.

Reading Telemetry Fault Register After AR Event Caused by Undervoltage

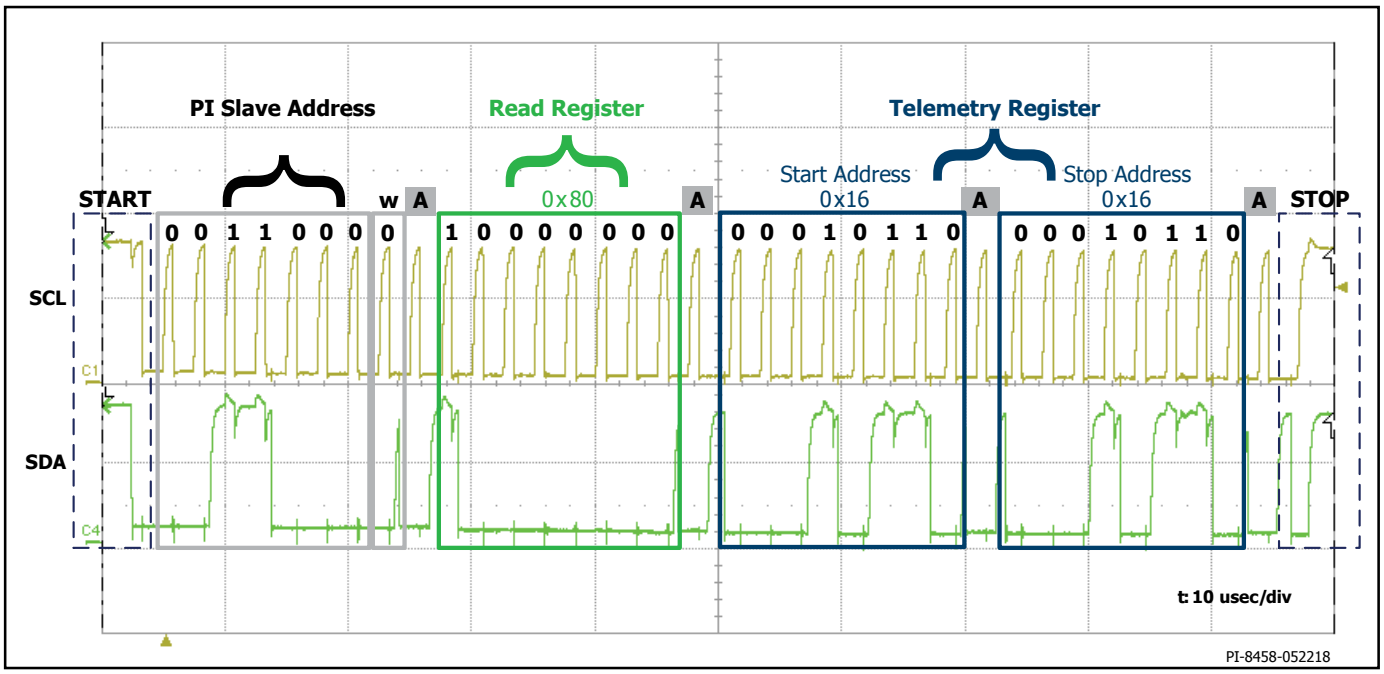

Figure 24. I²C Waveforms for Writing Address of Fault Register READ11 in Read Register (READ0) in Order to Read Back READ11.

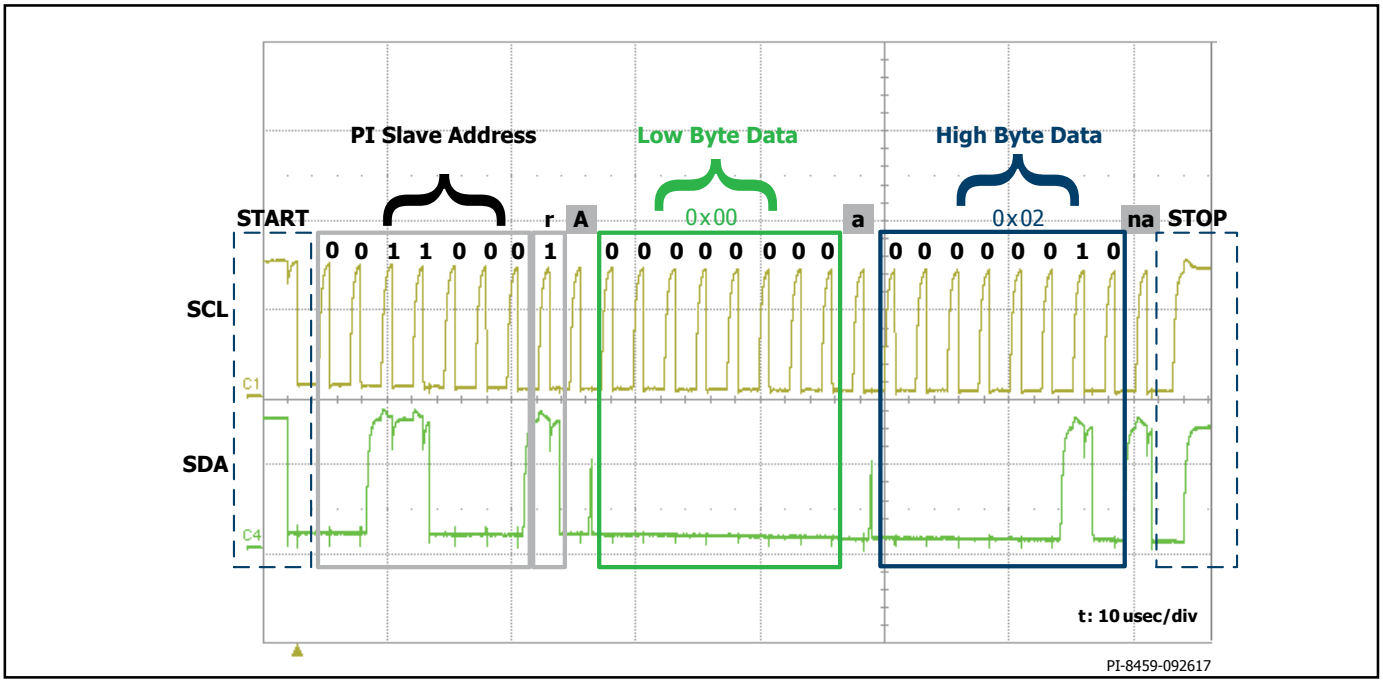

Figure 25. I²C Waveforms for Read Value From READ11 Register.

Applications Example

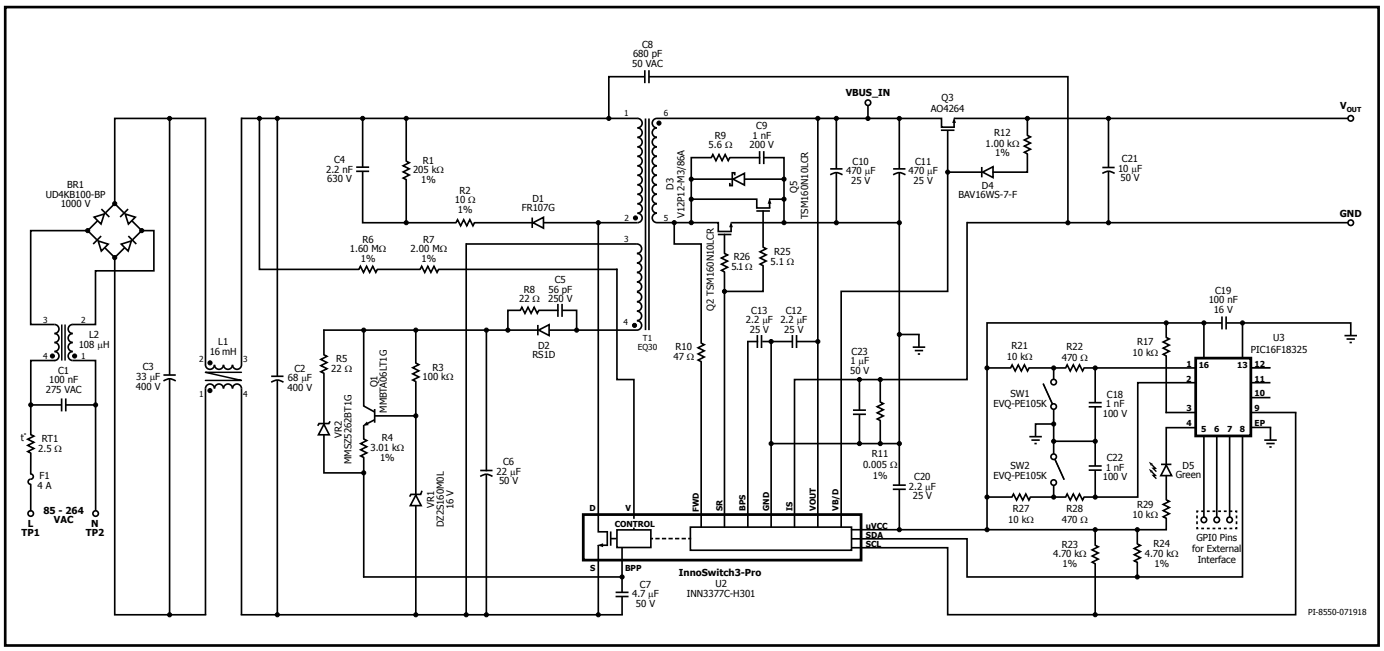

Figure 26. 3 V – 8 V, 5 A; 8 V – 20 V Constant Power 40 W Programmable Power Supply.

The circuit shown in Figure 26 is a 3 V – 8 V, 5 A; 8 V – 20 V constant power 40 W programmable power supply using the INN3377C IC. The power stage is controlled by a general purpose PIC16F18325 microcontroller. This design features DOE Level 6 and EC CoC 5 compliance.

Common mode choke L1 and L2 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Fuse F1 isolates the circuit and provides protection from component failure.

One end of the transformer primary is connected to the rectified DC bus; the other end is connected to the drain terminal of the integrated MOSFET in the InnoSwitch3-Pro IC (U1).

A low-cost RCD clamp formed by diode D1, resistors R1, R2 and capacitor C4 limits the peak Drain voltage of U1 at the instant of turn-off of the MOSFET inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The InnoSwitch3-Pro IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C7) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6. Resistors R3 and R4 along with Q1 and VR1 form a linear regulator circuit to limit the current being supplied to the PRIMARY BYPASS pin of the InnoSwitch3-Pro IC (U1) irrespective of the output voltage. The Zener diode VR2 along with resistor R5 provides latching OVP in the event of an output overvoltage condition.

In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In the event of an overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2. This causes a current to flow into the PRIMARY BYPASS pin of InnoSwitch3-Pro IC (U1). If the current flowing into the PRIMARY BYPASS pin increases above the I_{SD} threshold, the InnoSwitch3-Pro IC controller will latch-off and prevent any further increase in output voltage.

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and output current sensing along with drive to a MOSFET providing synchronous rectification. The secondary output of the transformer is rectified by MOSFETs Q2, Q5 and filtered by capacitors C10 and C11. High frequency ringing during switching transients that would otherwise create radiated EMI, is reduced via a RC snubber, R9 and C9. Current sharing of the two FETs Q2 and Q5 are obtained by adding the resistors R25 and R26 in series with the gates of the respective FETs.

The gate of Q2 and Q5 are turned on by secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R10 and fed into the FORWARD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary-side requesting the start of a new switching cycle from the primary. In discontinuous or continuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of $V_{SR(TH)}$. Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C13, connected to SECONDARY BYPASS pin of InnoSwitch3-Pro IC (U1) provides decoupling for the internal circuitry. Capacitor C12 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C13 via resistor R10 and an internal

regulator. This allows output current regulation to be maintained down to the minimum auto-restart threshold set by the I²C interface. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed by monitoring the voltage drop across resistor R11 between the IS and SECONDARY GROUND pins. A threshold of approximately 32 mV reduces losses. A decoupling capacitor C23 is needed between the IS and SECONDARY GROUND pin to improve CC accuracy. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current.

When the output current is below the CC threshold, the device operates in constant voltage mode. The output voltage is set by the I²C interface.

The PIC microcontroller gets its supply through the µVCC pin of InnoSwitch3-Pro. Switch1 (SW1) increments output voltage while Switch2 (SW2) decrements output voltage. Such a design is used in a system where output voltage is required to be controlled through an external interface.

The PIC microcontroller communicates over its I²C lines to the SDA and SCL pins (which are both 3.3 V and 5 V compatible) of the InnoSwitch3-Pro IC. The SDA and SCL lines need pull-up resistors R24 and R23 respectively to the µVCC pin. The µVCC pin needs a decoupling capacitor C20.

N-MOSFET Q3 forms the bus switch and is controlled by the VB/D pin on the InnoSwitch3-Pro IC. Resistor R12 and diode D4 are needed from the Source of the MOSFET to its gate for providing a voltage discharge path when the bus switch is opened. Capacitor C21 is needed at the output for ESD protection.

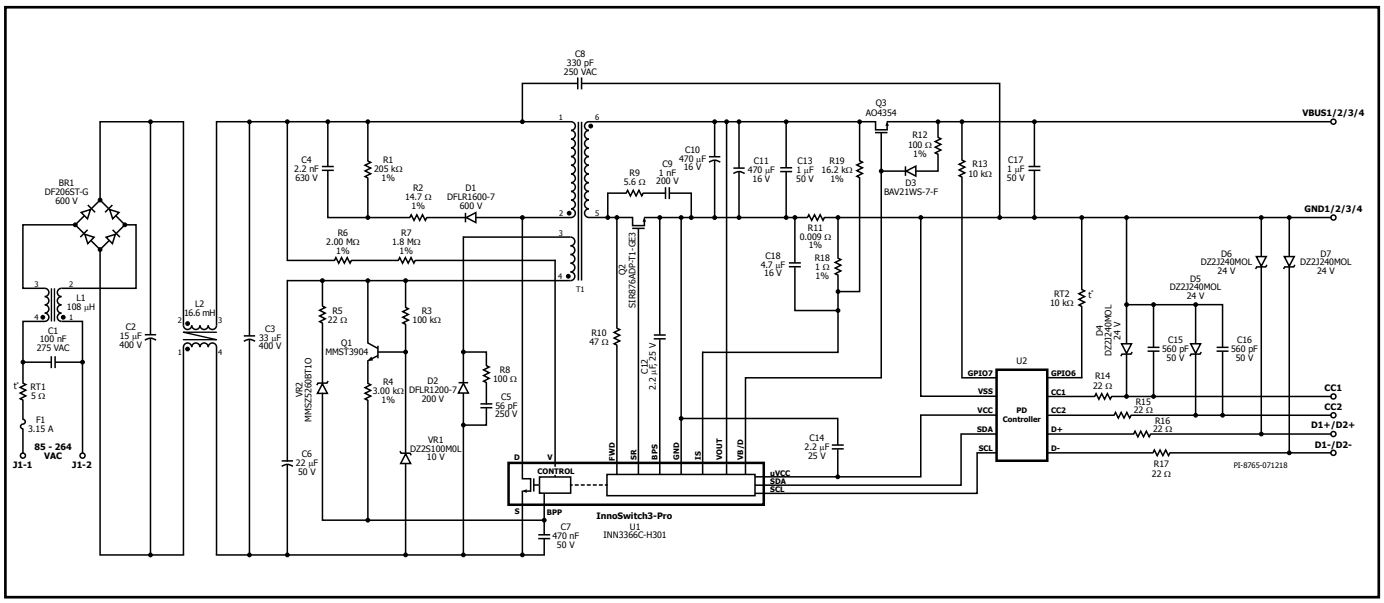

Figure 27. 5 V / 3 A; 9 V / 3 A; 3 V – 11 V PPS USB PD 3.0 Compliant Adapter.

The circuit shown in Figure 27 is a 5 V / 3 A; 9 V / 3 A; 3 V – 11 V PPS USB PD 3.0 compliant adapter using INN3366C IC. The power stage is controlled by a USB PD controller. This design features DOE Level 6 and EC CoC 5 compliance.

Common mode choke L1 and L2 provides attenuation for EMI. Bridge rectifier BR1 and BR2 rectify the AC line voltage and provides a full wave rectified DC. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Fuse F1 isolates the circuit and provides protection from component failure. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply.

One end of the transformer primary is connected to the rectified DC bus; the other end is connected to the drain terminal of the integrated MOSFET in the InnoSwitch3-Pro IC (U1).

A low-cost RCD clamp formed by diode D1, resistors R1 and R2 and capacitor C4 limits the peak Drain voltage of U1 at the instant of turn-off of the MOSFET inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The InnoSwitch3-Pro IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS BPP pin capacitor (C7) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6. Resistor R3 and R4 along with Q1 and VR1 form a linear regulator circuit to limit the current being supplied to the PRIMARY BYPASS pin of the InnoSwitch3-Pro IC (U1) irrespective of the output voltage. The Zener VR2 along with resistor R5 provides latching OVP in the event of an output overvoltage condition.

In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In the event of an overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2. This causes a current to flow into the PRIMARY BYPASS pin of InnoSwitch3-Pro IC (U1). If the current flowing into the PRIMARY BYPASS pin increases above the I_{SD} threshold, the InnoSwitch3-Pro IC controller will latch-off and prevent any further increase in output voltage.

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and output current sensing along with drive to a MOSFET providing synchronous rectification. The secondary output of the transformer is rectified by MOSFET Q2 and filtered by capacitors C10 and C11. High frequency ringing during switching transients that would otherwise create radiated EMI, is reduced via a RC snubber, R9 and C9.

The gate of Q2 is turned on by secondary-side controller inside U1, based on the winding voltage sensed via resistor R10 and fed into the FORWARD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary-side requesting the start of a new switching cycle from the primary. In discontinuous or continuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of $V_{SR(TH)}$. Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C12, connected to the SECONDARY BYPASS BPS pin of InnoSwitch3-Pro IC U1 provides decoupling for the internal circuitry. Capacitor C13 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS decoupling capacitor C12 via resistor R10 and an internal