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SSD1963

Advance Information

1215KB Embedded Display SRAM
LCD Display Controller

Appendix: IC Revision history of SSD1963 Specification

Version	Change Items	Effective Date
0.10 21-Nov-08	1st Release	24-Nov-08
0.10 08-Dec-08	1. Changed the set_pll_mnk to set_pll_mn in section 7.2 2. Change register name in section 8 3. Removed ABC 4. Revised description for REG 0x00, 0x01, 0x0C, 0x0D, 0x0E, 0x10, 0x11, 0x21, 0x26, 0x28, 0x2A, 0x2B, 0x2C, 0x2E, 0x33, 0x34, 0x35, 0x36, 0x37, 0x3A, 0x3C, 0x3E, 0x44, 0x45, 0xA1, 0xB0, 0xB1, 0xB4, 0xB5, 0xB6, 0xB7, 0xB8, 0xB9, 0xBE, 0xBF, 0xD0, 0xD1, 0xD4, 0xE5. 5. Added max VIH in Table 12-1 6. Added Table 9-1 7. Added Table 11-1 8. Revised Figure 9-19 9. Revised Figure 14-2 10. Revised Figure 13-5 11. Corrected typo for Table 7-2 12. Revised test condition for 12 and 13	10-Dec-08
1.0 07-May-09	1. Changed status to Advance Information 2. Update min/max rating of VDDD and VDDPLL in Table 11-1 3. Added tape and reel drawing of 128-pin LQFP package in Section 15.3 4. Revised Section 13.2 5. 5. Added 12 bits for Table 7-1 6. Removed TTL interface 7. Revised section 7.1.5 8. Change the title of section 7.2 9. Revised command description in section 8 10. Removed the command 0x0C and 0x3A 11. Added figures in section 13.4 12. Revised figures in section 13.3 13. Revise Table 6-1	18-May-09
1.1 23-Dec-09	1. Update Table 7-1 2. Revised section 9.72	18-Jan-10
1.2 31-May-10	1. Add Table 13-7	15-Jul-10
1.3 11-Nov-10	1. Update Section 7.2 reset timing 2. Correct Section 13.4 the serial RGB timing Correct Table 6.1-6.5 Pin Mapping -> Pin description	07-Dec-10

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1963 is a display controller of 1215K byte frame buffer to support up to 864 x 480 x 24bit graphics content. It also equips parallel MCU interfaces in different bus width to receive graphics data and command from MCU. Its display interface supports common RAM-less LCD driver of color depth up to 24 bit-per-pixel.

2 FEATURES

- Display feature
  - Built-in 1215K bytes frame buffer. Support up to 864 x 480 at 24bpp display
  - Support TFT 18/24-bit generic RGB interface panel
  - Support 8-bit serial RGB interface
  - Hardware rotation of 0, 90, 180, 270 degree
  - Hardware display mirroring
  - Hardware windowing
  - Programmable brightness, contrast and saturation control
  - Dynamic Backlight Control (DBC) via PWM signal
- MCU connectivity
  - 8/9/16/18/24-bit MCU interface
  - Tearing effect signal
- I/O Connectivity
  - 4 GPIO pins
- Built-in clock generator
- Deep sleep mode for power saving
- Core supply power (V_{DDPLL} and V_{DDD}): 1.2V±0.1V
- I/O supply power(V_{DDIO}): 1.65V to 3.6V
- LCD interface supply power (V_{DDLCD}): 1.65V to 3.6V

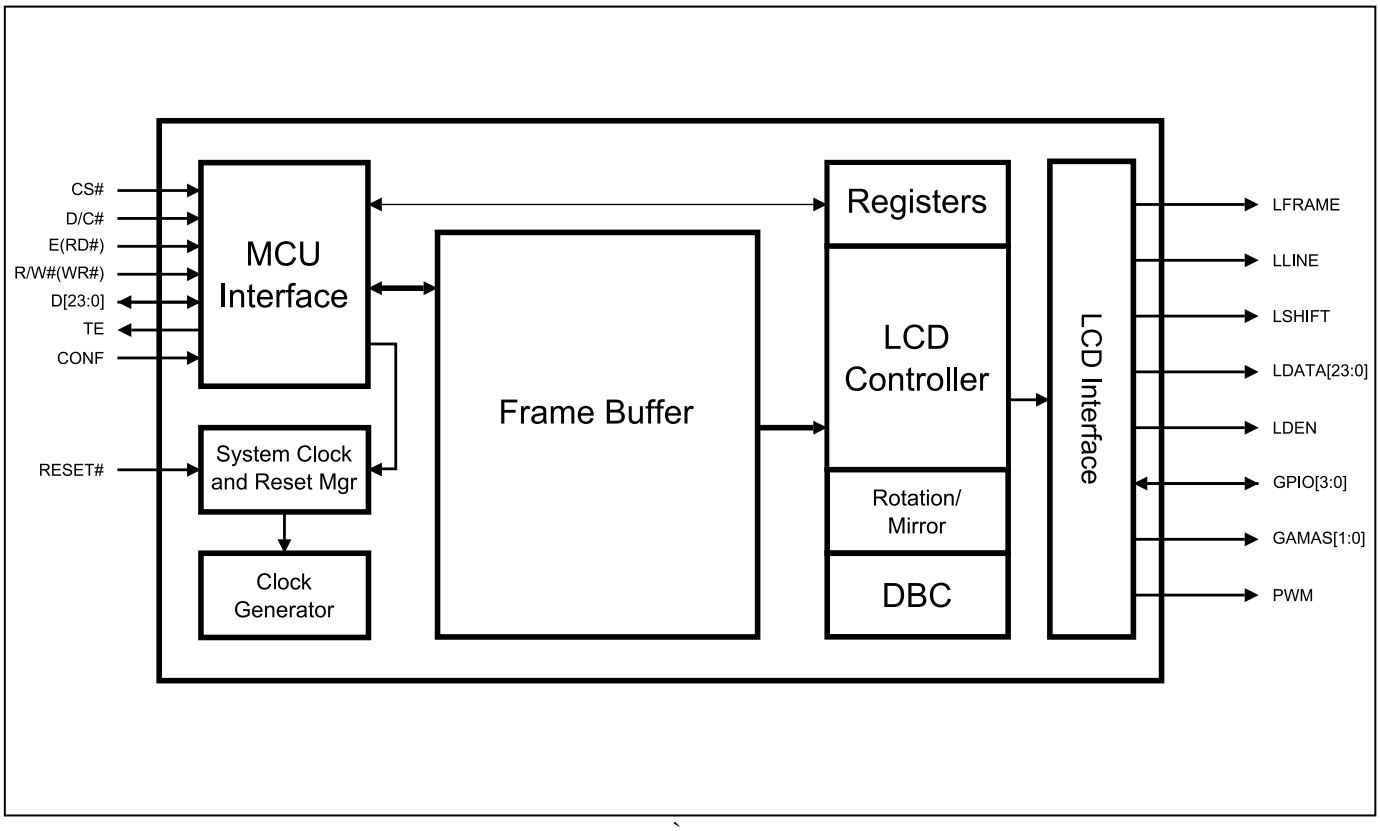
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form
SSD1963G41	TFBGA-80 (Tray)
SSD1963QL9	LQFP-128 (Tray)
SSD1963QL9R	LQFP-128 (Tape & Reel)

4 BLOCK DIAGRAM

Figure 4-1: SSD1963 Block Diagram



5 PIN ARRANGEMENT

5.1 80 balls TFBGA

Figure 5-1: Pinout Diagram –TFBGA (Topview)

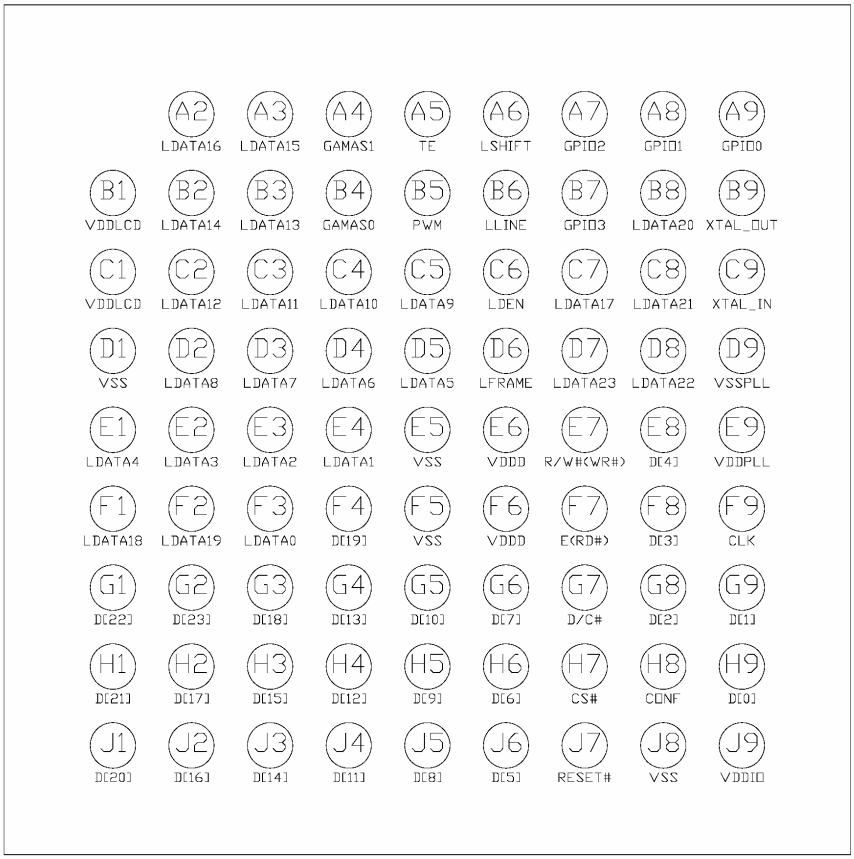


Table 5-1: TFBGA Pin Assignment Table

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
A1	-	C1	VDDLCD	E1	LDATA4	G1	D[22]	J1	D[20]
A2	LDATA16	C2	LDATA12	E2	LDATA3	G2	D[23]	J2	D[16]
A3	LDATA15	C3	LDATA11	E3	LDATA2	G3	D[18]	J3	D[14]
A4	GAMAS1	C4	LDATA10	E4	LDATA1	G4	D[13]	J4	D[11]
A5	TE	C5	LDATA9	E5	VSS	G5	D[10]	J5	D[8]
A6	LSHIFT	C6	LDEN	E6	VDDD	G6	D[7]	J6	D[5]
A7	GPIO2	C7	LDATA17	E7	R/W# (WR#)	G7	D/C#	J7	RESET#
A8	GPIO1	C8	LDATA21	E8	D[4]	G8	D[2]	J8	VSS
A9	GPIO0	C9	XTAL_IN	E9	VDDPLL	G9	D[1]	J9	VDDIO
B1	VDDLCD	D1	VSS	F1	LDATA18	H1	D[21]		
B2	LDATA14	D2	LDATA8	F2	LDATA19	H2	D[17]		
B3	LDATA13	D3	LDATA7	F3	LDATA0	H3	D[15]		
B4	GAMAS0	D4	LDATA6	F4	D[19]	H4	D[12]		
B5	PWM	D5	LDATA5	F5	VSS	H5	D[9]		
B6	LLINE	D6	LFRAME	F6	VDDD	H6	D[6]		
B7	GPIO3	D7	LDATA23	F7	E(RD#)	H7	CS#		
B8	LDATA20	D8	LDATA22	F8	D[3]	H8	CONF		
B9	XTAL_OUT	D9	VSSPLL	F9	CLK	H9	D[0]		

5.2 128 pins LQFP

Figure 5-2 : Pinout Diagram – LQFP (Topview)

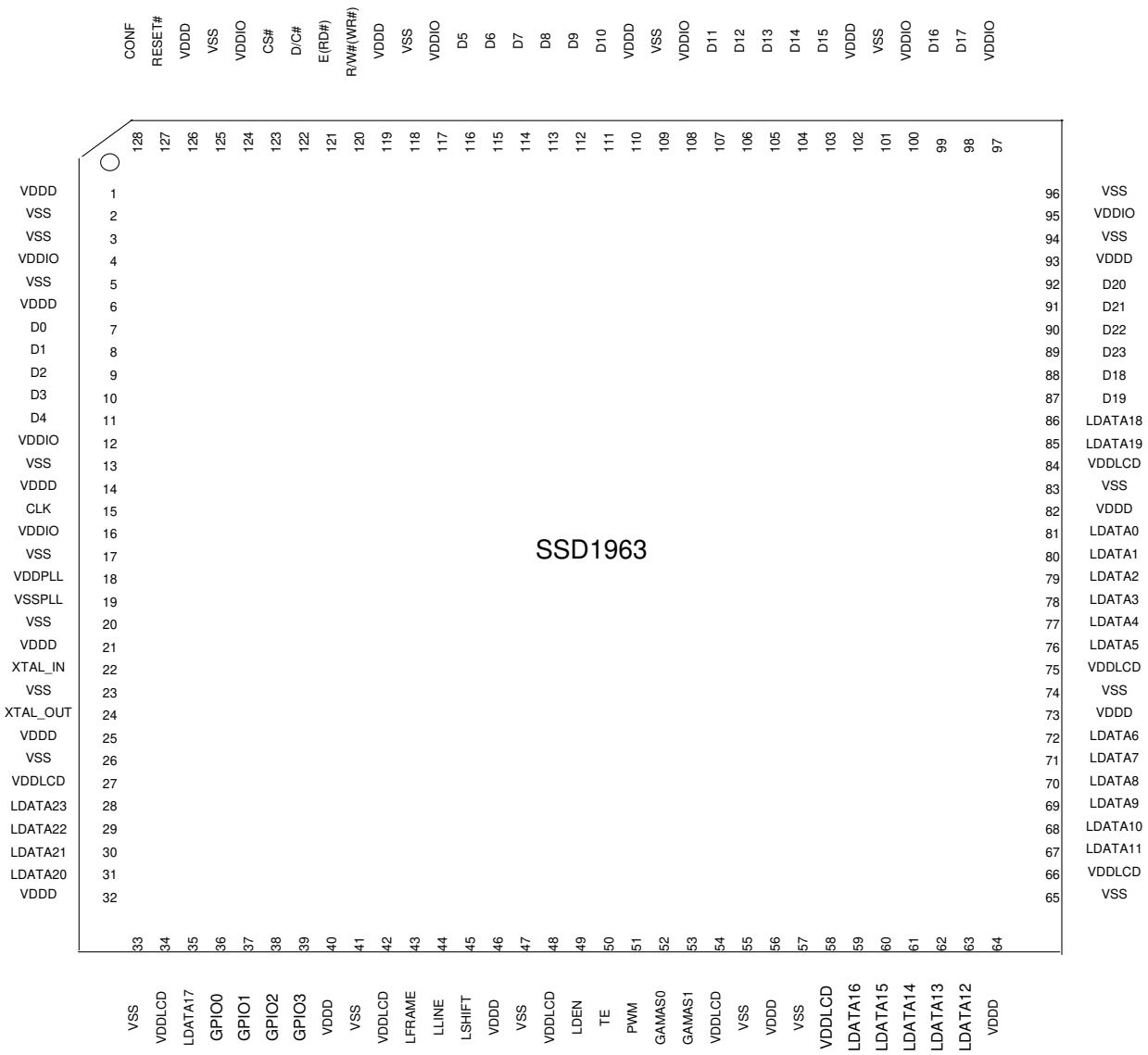


Table 5-2 : LQFP Pin Assignment Table

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	VDDD	33	VSS	65	VSS	97	VDDIO
2	VSS	34	VDDLCD	66	VDDLCD	98	D17
3	VSS	35	LDATA17	67	LDATA11	99	D16
4	VDDIO	36	GPIO0	68	LDATA10	100	VDDIO
5	VSS	37	GPIO1	69	LDATA9	101	VSS
6	VDDD	38	GPIO2	70	LDATA8	102	VDDD
7	D0	39	GPIO3	71	LDATA7	103	D15
8	D1	40	VDDD	72	LDATA6	104	D14
9	D2	41	VSS	73	VDDD	105	D13
10	D3	42	VDDLCD	74	VSS	106	D12
11	D4	43	LFRAME	75	VDDLCD	107	D11
12	VDDIO	44	LLINE	76	LDATA5	108	VDDIO
13	VSS	45	LSHIFT	77	LDATA4	109	VSS
14	VDDD	46	VDDD	78	LDATA3	110	VDDD
15	CLK	47	VSS	79	LDATA2	111	D10
16	VDDIO	48	VDDLCD	80	LDATA1	112	D9
17	VSS	49	LDEN	81	LDATA0	113	D8
18	VDDPLL	50	TE	82	VDDD	114	D7
19	VSSPLL	51	PWM	83	VSS	115	D6
20	VSS	52	GAMAS0	84	VDDLCD	116	D5
21	VDDD	53	GAMAS1	85	LDATA19	117	VDDIO
22	XTAL_IN	54	VDDLCD	86	LDATA18	118	VSS
23	VSS	55	VSS	87	D19	119	VDDD
24	XTAL_OUT	56	VDDD	88	D18	120	R/W#(WR#)
25	VDDD	57	VSS	89	D23	121	E(RD#)
26	VSS	58	VDDLCD	90	D22	122	D/C#
27	VDDLCD	59	LDATA16	91	D21	123	CS#
28	LDATA23	60	LDATA15	92	D20	124	VDDIO
29	LDATA22	61	LDATA14	93	VDDD	125	VSS
30	LDATA21	62	LDATA13	94	VSS	126	VDDD
31	LDATA20	63	LDATA12	95	VDDIO	127	RESET#
32	VDDD	64	VDDD	96	VSS	128	CONF

6 PIN DESCRIPTIONS

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin
Hi-Z = High impedance

Table 6-1: MCU Interface Pin Description

Pin Name	Type	Reference Voltage Level	TFBGA Pin #	LQFP Pin #	Description
CLK	I	VDDIO	F9	15	TTL clock input. This pin should be tied to VSS if TTL clock input is not used
XTAL_IN	I	-	C9	22	Crystal oscillator input. This pin should be tied to VSS if not used
XTAL_OUT	O	-	B9	24	Crystal oscillator output. This pin should be floating if not used
CS#	I	VDDIO	H7	123	Chip select
D/C#	I	VDDIO	G7	122	Data/Command select
E(RD#)	I	VDDIO	F7	121	6800 mode: E (enable signal) 8080 mode: RD# (read strobe signal)
R/W#(WR#)	I	VDDIO	E7	120	6800 mode: R/W# 0: Write cycle 1: Read cycle 8080 mode: WR# (write strobe signal)
D[23:0]	IO	VDDIO	E8, F4, F8, G1, G2, G3, G4, G5, G6, G8, G9, H1, H2, H3, H4, H5, H6, H9, J1, J2,J3, J4, J5, J6	7, 8, 9, 10, 11, 87, 88, 89, 90, 91, 92, 98, 99, 103, 104, 105, 106, 107, 111, 112, 113, 114, 115, 116	Data bus. Pins not used should be floating
TE	O	VDDLCD	A5	50	Tearing effect

Table 6-2: LCD Interface Pin Description

Pin Name	Type	Reference Voltage Level	TFBGA Pin #	LQFP Pin #	Description
LFRAME	O	VDDLCD	D6	43	Vertical sync (Frame pulse)
LLINE	O	VDDLCD	B6	44	Horizontal sync (Line pulse)
LSHIFT	O	VDDLCD	A6	45	Pixel clock (Pixel shift signal)
LDEN	O	VDDLCD	C6	49	Data valid
LDATA[23:0]	O	VDDLCD	A2, A3, B2, B3, B8, C2, C3, C4, C5, C7, C8, D2, D3, D4, D5, D7, D8, E1, E2, E3, E4, F1, F2, F3	28, 29, 30, 31, 35, 59, 60, 61, 62, 63, 67, 68, 69, 70, 71, 72, 76, 77, 78, 79, 80, 81, 85, 86	RGB data
GPIO[3:0]	IO	VDDLCD	A7, A8, A9, B7	36, 37, 38, 39	These pins can be configured for display miscellaneous signals or as general purpose I/O. Default as input
GAMAS [1:0]	O	VDDLCD	A4, B4	52, 53	Gamma selection for panel
PWM	O	VDDLCD	B5	51	PWM output for backlight driver

Table 6-3: Control Signal Pin Description

Pin Name	Type	Reference Voltage Level	TFBGA Pin #	LQFP Pin #	Description
RESET#	I	VDDIO	J7	127	Master synchronize reset
CONF	I	VDDIO	H8	128	MCU interface configuration 0: 6800 Interface 1: 8080 Interface

Table 6-4: Power Pin Description

Pin Name	Type	TFBGA Pin #	LQFP Pin #	Description
VDDD	P	E6, F6	1, 6, 14, 21, 25, 32, 40, 46, 56, 64, 73, 82, 93, 102, 110, 119, 126	Power supply for internal digital circuit
VDDLCD	P	B1, C1	27, 34, 42, 48, 54, 58, 66, 75, 84	Power supply for LCD interface related pads
VDDPLL	P	E9	18	Power supply for internal analog circuit and analog I/O pads
VDDIO	P	J9	4, 12, 16, 95, 97, 100, 108, 117, 124	Power supply for digital I/O pads
VSS	P	D1, E5, F5, J8	2, 3, 5, 13, 17, 20, 23, 26, 33, 41, 47, 55, 57, 65, 74, 83, 94, 96, 101, 109, 118, 125	Ground for internal digital circuit
VSSPLL	P	D9	19	Ground for internal analog circuit and analog I/O pads

Table 6-5 : LCD Interface Pin Mapping

Pin Names	24-bit	18-bit	8-bit serial
LFRAME	FRAME		
LLINE	LINE		
LSHIFT	SHIFT		
LDEN	DEN		
LDATA23	R7	Drive 0	Drive 0
LDATA22	R6	Drive 0	Drive 0
LDATA21	R5	Drive 0	Drive 0
LDATA20	R4	Drive 0	Drive 0
LDATA19	R3	Drive 0	Drive 0
LDATA18	R2	Drive 0	Drive 0
LDATA17	R1	R5	Drive 0
LDATA16	R0	R4	Drive 0
LDATA15	G7	R3	Drive 0
LDATA14	G6	R2	Drive 0
LDATA13	G5	R1	Drive 0
LDATA12	G4	R0	Drive 0
LDATA11	G3	G5	Drive 0
LDATA10	G2	G4	Drive 0
LDATA9	G1	G3	Drive 0
LDATA8	G0	G2	Drive 0
LDATA7	B7	G1	D7
LDATA6	B6	G0	D6
LDATA5	B5	B5	D5
LDATA4	B4	B4	D4
LDATA3	B3	B3	D3
LDATA2	B2	B2	D2
LDATA1	B1	B1	D1
LDATA0	B0	B0	D0

Note

(1) These pin mappings use signal names commonly used for each panel type, however signal names may differ between panel manufacturers.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 MCU Interface

The MCU interface connects the MCU and SSD1963 graphics controller. The MCU interface can be configured as 6800 mode and 8080 mode by the CONF pin. By pulling the CONF pin to VSSIO, the MCU interface will be configured as 6800 mode interface. If the CONF pin is connected to VDDIO, the MCU interface will be configure in 8080 mode.

7.1.1 6800 Mode

The 6800 mode MCU interface consist of CS#, D/C#, E, R/W#, D[23:0], and TE signals (Please refer to Table 6-1 for pin multiplexed with 8080 mode). This interface supports both fixed E and clock E scheme to define a read/write cycle. If the E signal is kept high and used as enable signal, the CS# signal acts as a bus clock, the data or command will be latched into the system at the rising edge of CS#. If the user wants to use the E pin as the clock pin, the CS# pin then need to be fixed to logic 0 to select the chip. Then the falling edge of the E signal will latch the data or command. For details, please refer to the timing diagram in chapter 13.2.1.

7.1.2 8080 Mode

The 8080 mode MCU interface consist of CS#, D/C#, RD#, WR#, D[23:0] and TE signals (Please refer to Table 6-1 for pin multiplexed with 6800 mode). This interface use WR# to define a write cycle and RD# for read cycle. If the WR# goes low when the CS# signal is low, the data or command will be latched into the system at the rising edge of WR#. Similarly, the read cycle will start when RD# goes low and end at the rising edge of RD#. The detailed timing will show in the chapter 13.2.2.

7.1.3 Register Pin Mapping

When user access the registers via the parallel MCU interface, only D[7:0] will be used regardless the width of the pixel data is. Therefore, D[23:8] will only be used to address the display data only. This provided the possibility that the pixel data format as shown in Table 7-1 can be configured by command 0xF0.

7.1.4 Pixel Data Format

Both 6800 and 8080 support 8-bit, 9-bit, 16-bit, 18-bit and 24-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Table 7-1: Pixel Data Format

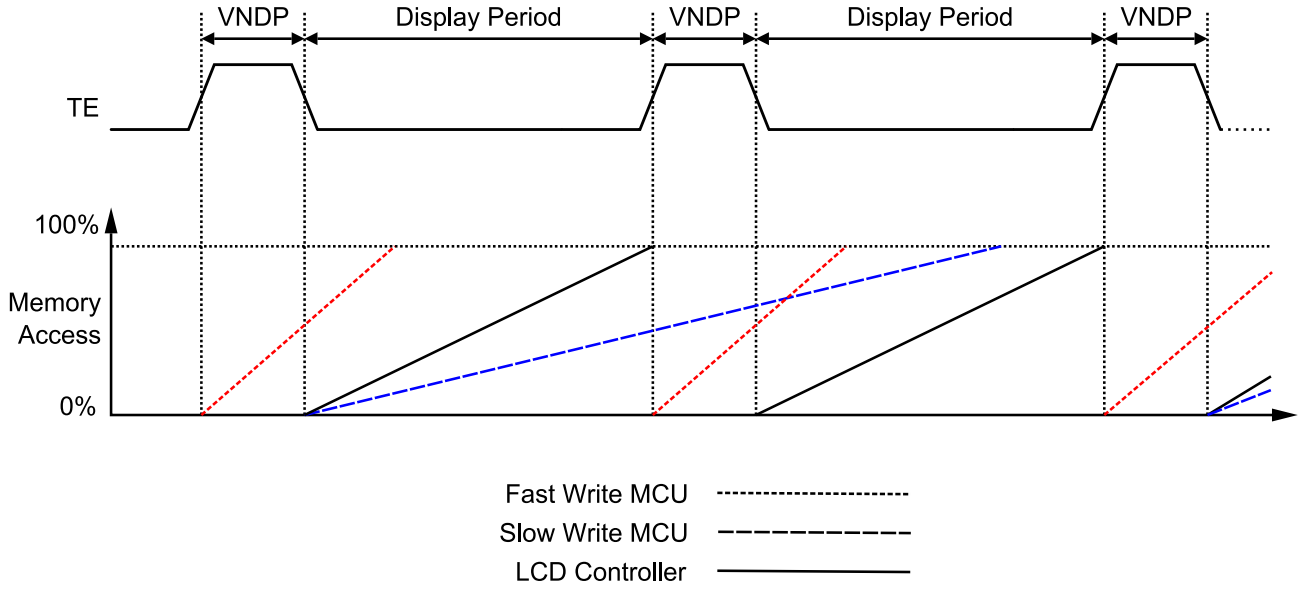
Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24 bits	1st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18 bits	1st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
16 bits	1st									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
	2nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
	3rd									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
12 bits	1st													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
	2nd													G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
9 bits	1st																R5	R4	R3	R2	R1	R0	G5	G4	G3
	2nd																G2	G1	G0	B5	B4	B3	B2	B1	B0
8 bits	1st																	R7	R6	R5	R4	R3	R2	R1	R0
	2nd																	G7	G6	G5	G4	G3	G2	G1	G0
	3rd																	B7	B6	B5	B4	B3	B2	B1	B0

7.1.5 Tearing Effect Signal (TE)

The Tearing Effect Signal (TE) is a feedback signal from the LCD Controller to MCU. This signal reveals the display status of LCD controller. In the non-display period, the TE signal will go high. Therefore, this signal enables the MCU to send data by observing the non-display period to avoid tearing.

Figure 7-1 shows how the TE signal helps to avoid tearing. If the MCU writing speed is slower than the display speed, the display data should be updated after the LCD controller start to scan the frame buffer. Then the LCD controller will always display the old memory content until the next frame. However, if the MCU is faster than the LCD controller, it should start updating the display content in the vertical non-display period (VNDP) to enable the LCD controller will always get the newly updated data.

Figure 7-1: Relationship between Tearing Effect Signal and MCU Memory Writing



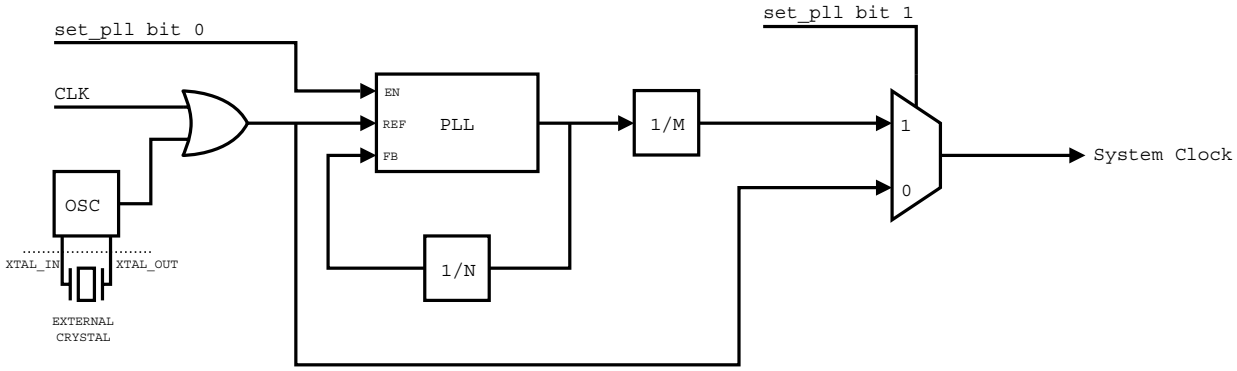
In SSD1963, users can configure the TE signal to reflect the vertical non-display period only or reflect both vertical and horizontal non-display period. With the additional horizontal non-display period information, the MCU can control the refresh action in more accurately by counting the horizontal line scanned by the LCD controller. Usually, a fast MCU will not need horizontal non-display period. But a slow MCU will need it to ensure the frame buffer update process always lags behind the LCD controller.

7.2 System Clock Generation

The system clock of SSD1963 is generated by the built-in PLL. The reference clock of the PLL can come from either the CLK pin or the external crystal oscillator. Since the CLK pin and the output of the oscillator was connected to PLL with an "OR" gate, the unused clock must be tied to VSS.

Before the PLL output is configured as the system clock by the bit 1 of "set_pll" command 0xE0, the system will be clocked by the reference clock. This enables the user to send the "set_pll_mn" command 0xE2 to the PLL for frequency configuration. When the PLL frequency is configured and the PLL was enabled with the bit 0 of "set_pll" command 0xE0, the user should still wait for 100us for the PLL to lock. Then the PLL is ready and can be configured as system clock with the bit 1 of "set_pll" command 0xE0.

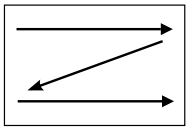
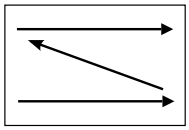
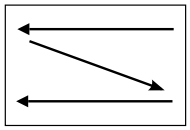
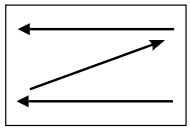
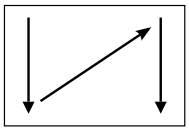
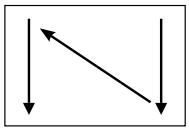
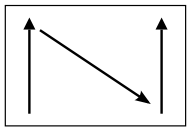
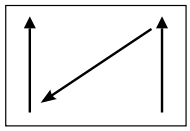
Figure 7-2: Clock Control Diagram



7.3 Frame Buffer

There are 1215K bytes built-in SRAM inside SSD1963 to use as frame buffer. When the frame buffer is written or read, the "address counter" will automatically increase by one or decrease by one depends on the frame buffer settings.

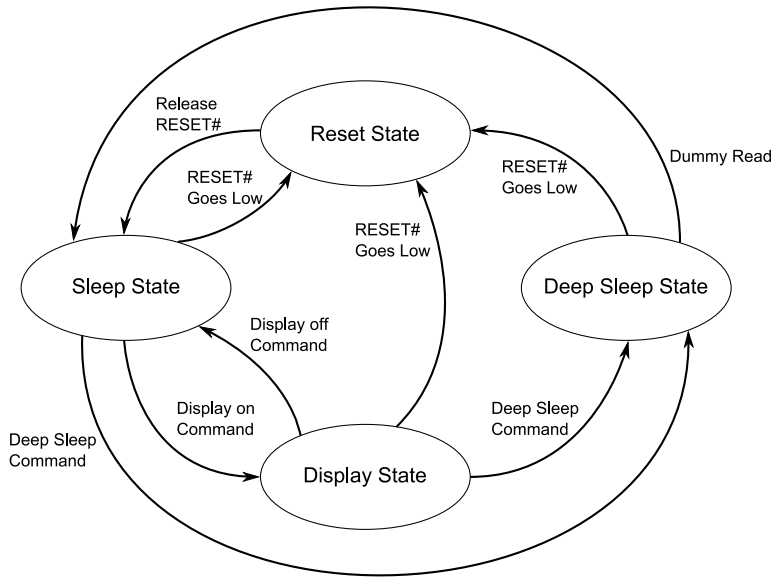
Table 7-2: Frame Buffer Settings regarding to set_address_mode command 0x36

	Option 1 Horizontal: Increment Vertical: Increment B6 = 0; B7 = 0	Option 2 Horizontal: Increment Vertical: Decrement B6 = 0; B7 = 1	Option 3 Horizontal: Decrement Vertical: Increment B6 = 1; B7 = 0	Option 4 Horizontal: Decrement Vertical: Decrement B6 = 1; B7 = 1
Horizontal Frame Buffer Mode B5 = 0	00000h  5DC00h	00000h  5DC00h	00000h  5DC00h	00000h  5DC00h
Vertical Frame Buffer Mode B5 = 1	00000h  5DC00h	00000h  5DC00h	00000h  5DC00h	00000h  5DC00h

7.4 System Clock and Reset Manager

The "System Clock and Reset Manager" distributes the reset signal and clock signal to the entire system. It controls the Clock Generator and contains clock gating circuitry to turn on and off the clock of each functional module. Also, it divides the root clock from Clock Generator to operation clocks for different module. The System Clock and Reset Manager also manage the reset signals to ensure all the module are reset to appropriate status when the system are in reset state, deep sleep state, sleep state and display state. Figure 7-3 shows a state diagram of four operation states of SSD1963.

Figure 7-3: State Diagram of SSD1963



Reset State:	Deep Sleep State:	Sleep State:	Display State:
Clock Generator Stop	Clock Generator Stop	Clock Generator On	Clock Generator On
Unable to Receive Command	Unable to Receive Command	Able to Receive Command	Able to Receive Command
Unable to Update Frame Buffer	Unable to Update Frame Buffer	Able to Update Frame Buffer	Able to Update Frame Buffer
Display Off	Display Off	Display Off	Display On
All Settings Reset	All Settings Retain	All Settings Retain	All Settings Retain

7.5 LCD Controller

7.5.1 Display Format

The LCD controller reads the frame buffer and generates display signals according to the selected display panel format. SSD1963 supports common RAM-less TFT driver using generic RGB data format.

7.5.2 General Purpose Input/Output (GPIO)

The GPIO pins can operate in 2 modes, GPIO mode and miscellaneous display signal mode. When the pins are configured as GPIOs, these pins can be controlled directly by MCU. Therefore, user can use these pins to emulate other interface such as SPI or I2C. If these pins are configured as display signals, they will toggle with display periodically according to the signal settings. They can be set to toggle once a frame, once a line or in arbitrary period. Therefore they can be configured as some common signal needed for different panels such as STH or LP.

8 COMMAND TABLE

Hex Code	Command	Description
0x00	nop	No operation
0x01	soft_reset	Software Reset
0x0A	get_power_mode	Get the current power mode
0x0B	get_address_mode	Get the frame buffer to the display panel read order
0x0C	Reserved	Reserved
0x0D	get_display_mode	The SSD1963 returns the Display Image Mode.
0x0E	get_tear_effect_status	Get the Tear Effect status
0x0F	Reserved	Reserved
0x10	enter_sleep_mode	Turn off the panel. This command will pull low the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x11	exit_sleep_mode	Turn on the panel. This command will pull high the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x12	enter_partial_mode	Part of the display area is used for image display.
0x13	enter_normal_mode	The whole display area is used for image display.
0x20	exit_invert_mode	Displayed image colors are not inverted.
0x21	enter_invert_mode	Displayed image colors are inverted.
0x26	set_gamma_curve	Selects the gamma curve used by the display panel.
0x28	set_display_off	Blanks the display panel
0x29	set_display_on	Show the image on the display panel
0x2A	set_column_address	Set the column address
0x2B	set_page_address	Set the page address
0x2C	write_memory_start	Transfer image information from the host processor interface to the SSD1963 starting at the location provided by set_column_address and set_page_address
0x2E	read_memory_start	Transfer image data from the SSD1963 to the host processor interface starting at the location provided by set_column_address and set_page_address
0x30	set_partial_area	Defines the partial display area on the display panel
0x33	set_scroll_area	Defines the vertical scrolling and fixed area on display area
0x34	set_tear_off	Synchronization information is not sent from the SSD1963 to the host processor
0x35	set_tear_on	Synchronization information is sent from the SSD1963 to the host processor at the start of VFP
0x36	set_address_mode	Set the read order from frame buffer to the display panel
0x37	set_scroll_start	Defines the vertical scrolling starting point
0x38	exit_idle_mode	Full color depth is used for the display panel
0x39	enter_idle_mode	Reduce color depth is used on the display panel.
0x3A	Reserved	Reserved
0x3C	write_memory_continue	Transfer image information from the host processor interface to the SSD1963 from the last written location
0x3E	read_memory_continue	Read image data from the SSD1963 continuing after the last read_memory_continue or read_memory_start

Hex Code	Command	Description
0x44	set_tear_scanline	Synchronization information is sent from the SSD1963 to the host processor when the display panel refresh reaches the provided scanline
0x45	get_scanline	Get the current scan line
0xA1	read_ddb	Read the DDB from the provided location
0xA8	Reserved	Reserved
0xB0	set_lcd_mode_	Set the LCD panel mode and resolution
0xB1	get_lcd_mode	Get the current LCD panel mode, pad strength and resolution
0xB4	set_hori_period	Set front porch
0xB5	get_hori_period	Get current front porch settings
0xB6	set_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0xB7	get_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0xB8	set_gpio_conf	Set the GPIO configuration. If the GPIO is not used for LCD, set the direction. Otherwise, they are toggled with LCD signals.
0xB9	get_gpio_conf	Get the current GPIO configuration
0xBA	set_gpio_value	Set GPIO value for GPIO configured as output
0xBB	get_gpio_status	Read current GPIO status. If the individual GPIO was configured as input, the value is the status of the corresponding pin. Otherwise, it is the programmed value.
0xBC	set_post_proc	Set the image post processor
0xBD	get_post_proc	Set the image post processor
0xBE	set_pwm_conf	Set the image post processor
0xBF	get_pwm_conf	Set the image post processor
0xC0	set_lcd_gen0	Set the rise, fall, period and toggling properties of LCD signal generator 0
0xC1	get_lcd_gen0	Get the current settings of LCD signal generator 0
0xC2	set_lcd_gen1	Set the rise, fall, period and toggling properties of LCD signal generator 1
0xC3	get_lcd_gen1	Get the current settings of LCD signal generator 1
0xC4	set_lcd_gen2	Set the rise, fall, period and toggling properties of LCD signal generator 2
0xC5	get_lcd_gen2	Get the current settings of LCD signal generator 2
0xC6	set_lcd_gen3	Set the rise, fall, period and toggling properties of LCD signal generator 3
0xC7	get_lcd_gen3	Get the current settings of LCD signal generator 3
0xC8	set_gpio0_rop	Set the GPIO0 with respect to the LCD signal generators using ROP operation. No effect if the GPIO0 is configured as general GPIO.
0xC9	get_gpio0_rop	Get the GPIO0 properties with respect to the LCD signal generators.
0xCA	set_gpio1_rop	Set the GPIO1 with respect to the LCD signal generators using ROP operation. No effect if the GPIO1 is configured as general GPIO.
0xCB	get_gpio1_rop	Get the GPIO1 properties with respect to the LCD signal generators.
0xCC	set_gpio2_rop	Set the GPIO2 with respect to the LCD signal generators using ROP operation. No effect if the GPIO2 is configured as general GPIO.

Hex Code	Command	Description
0xCD	get_gpio2_rop	Get the GPIO2 properties with respect to the LCD signal generators.
0xCE	set_gpio3_rop	Set the GPIO3 with respect to the LCD signal generators using ROP operation. No effect if the GPIO3 is configured as general GPIO.
0xCF	get_gpio3_rop	Get the GPIO3 properties with respect to the LCD signal generators.
0xD0	set_dbc_conf	Set the dynamic back light configuration
0xD1	get_dbc_conf	Get the current dynamic back light configuration
0xD4	set_dbc_th	Set the threshold for each level of power saving
0xD5	get_dbc_th	Get the threshold for each level of power saving
0xE0	set_pll	Start the PLL. Before the start, the system was operated with the crystal oscillator or clock input
0xE2	set_pll_mn	Set the PLL
0xE3	get_pll_mn	Get the PLL settings
0xE4	get_pll_status	Get the current PLL status
0xE5	set_deep_sleep	Set deep sleep mode
0xE6	set_lshift_freq	Set the LSHIFT (pixel clock) frequency
0xE7	get_lshift_freq	Get current LSHIFT (pixel clock) frequency setting
0xE8	Reserved	Reserved
0xE9	Reserved	Reserved
0xF0	set_pixel_data_interface	Set the pixel data format of the parallel host processor interface
0xF1	get_pixel_data_interface	Get the current pixel data format settings
0xFF	Reserved	Reserved

9 COMMAND DESCRIPTIONS

9.1 nop

Command 0x00
Parameters None

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	0	0	0	0	0	00

Description
No operation.

9.2 soft_reset

Command 0x01
Parameters None

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	0	0	0	0	1	01

Description
The SSD1963 performs a software reset. All the configuration register will be reset except command 0xE0 to 0xE5.

Note :

The host processor must wait 5ms before sending any new commands to a SSD1963 following this command.

9.3 get_power_mode

Command 0x0A
Parameters 1

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	0	1	0	1	0	0A
Parameter 1	1	0	A_6	A_5	A_4	A_3	A_2	0	0	xx

Description
Get the current power mode

A[6] : Idle mode on/off (POR = 0)
0 Idle mode off
1 Idle mode on

A[5] : Partial mode on/off (POR = 0)
0 Partial mode off
1 Partial mode on

A[4] : Sleep mode on/off (POR = 0)
0 Sleep mode on
1 Sleep mode off

A[3] : Display normal mode on/off (POR = 1)
0 Display normal mode off

1 Display normal mode on (partial mode and vertical scroll off)

A[2] : Display on/off (POR = 0)
0 Display is off
1 Display is on

9.4 get_address_mode

Command 0x0B
Parameters 1

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	0	1	0	1	1	0B
Parameter 1	1	A_7	A_6	A_5	A_4	A_3	A_2	0	0	xx

Description
Get the frame buffer to the display panel read order

A[7] : Page address order (POR = 0)
0 Top to bottom
1 Bottom to top

A[6] : Column address order (POR = 0)
0 Left to right
1 Right to left

A[5] : Page / Column order (POR = 0)
0 Normal mode
1 Reverse mode

A[4] : Line address order (POR = 0)
0 LCD refresh top to bottom
1 LCD refresh bottom to top

A[3] : RGB / BGR order (POR = 0)
0 RGB
1 BGR

A[2] : Display data latch data (POR = 0)
0 LCD refresh left to right
1 LCD refresh right to left

9.5 get_display_mode

Command 0x0D
Parameters 1

	D/C	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	0	0	0	0	0	1	1	0	1	0D
Parameter 1	1	A_7	0	A_5	0	0	A_2	A_1	A_0	xx

Description
Get the Display Image Mode status.

A[7] : Vertical scrolling on/off (POR = 0)
0 Vertical scrolling is off