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W5500 Datasheet

Version 1.0.7

http://www.wiznet.co.kr

W5500

The W5500 chip is a Hardwired TCP/IP embedded Ethernet controller that provides easier Internet connection to embedded systems. W5500 enables users to have the Internet connectivity in their applications just by using the single chip in which TCP/IP stack, 10/100 Ethernet MAC and PHY embedded.

WIZnet's Hardwired TCP/IP is the market-proven technology that supports TCP, UDP, IPv4, ICMP, ARP, IGMP, and PPPoE protocols. W5500 embeds the 32Kbyte internal memory buffer for the Ethernet packet processing. If you use W5500, you can implement the Ethernet application just by adding the simple socket program. It's faster and easier way rather than using any other Embedded Ethernet solution. Users can use 8 independent hardware sockets simultaneously.

SPI (Serial Peripheral Interface) is provided for easy integration with the external MCU. The W5500's SPI supports 80 MHz speed and new efficient SPI protocol for the high speed network communication. In order to reduce power consumption of the system, W5500 provides WOL (Wake on LAN) and power down mode.

Features

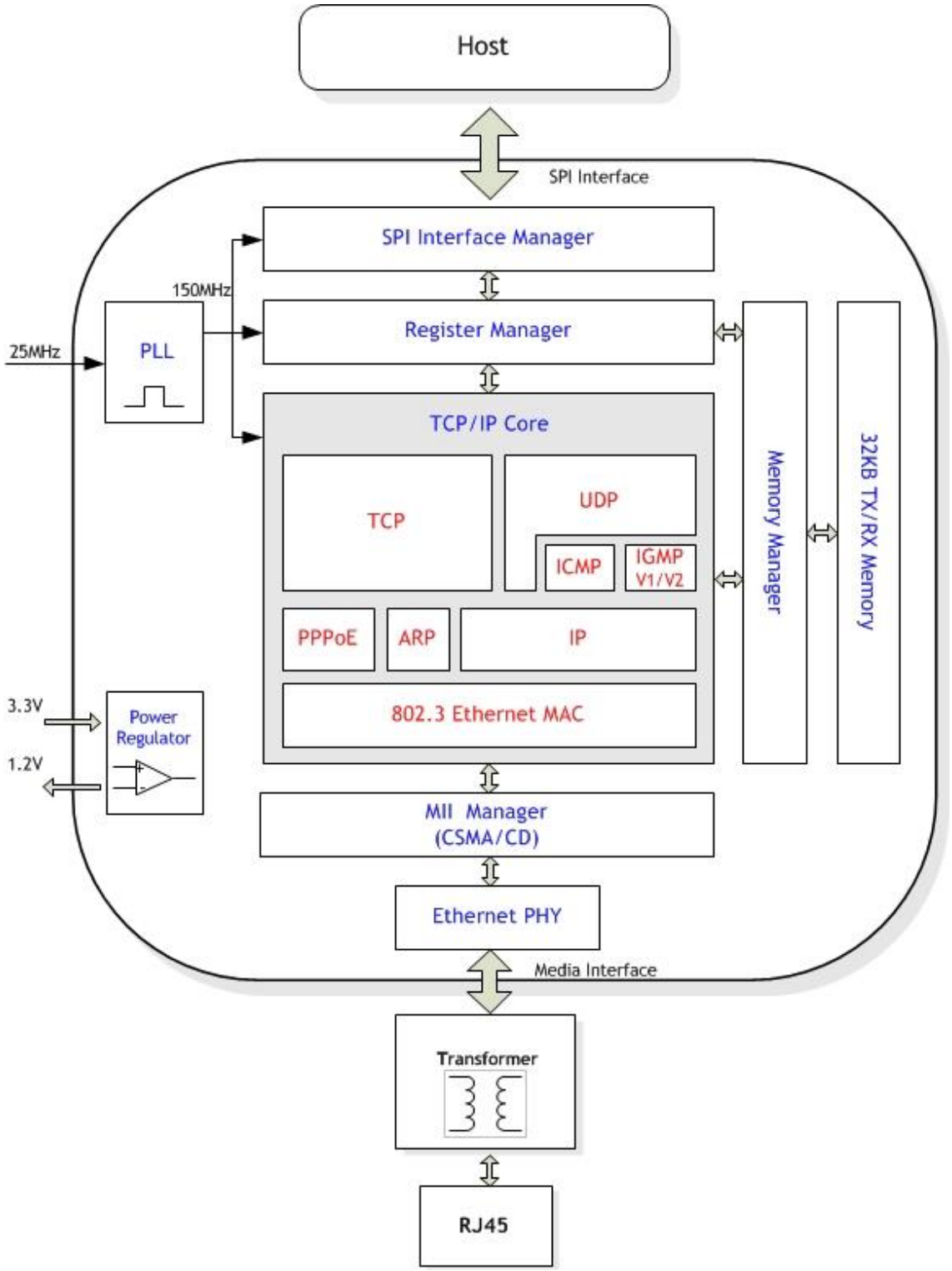
- Supports Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
- Supports 8 independent sockets simultaneously
- Supports Power down mode
- Supports Wake on LAN over UDP
- Supports High Speed Serial Peripheral Interface(SPI MODE 0, 3)
- Internal 32Kbytes Memory for TX/RX Buffers
- 10BaseT/100BaseTX Ethernet PHY embedded
- Supports Auto Negotiation (Full and half duplex, 10 and 100-based)
- Not supports IP Fragmentation
- 3.3V operation with 5V I/O signal tolerance
- LED outputs (Full/Half duplex, Link, Speed, Active)
- 48 Pin LQFP Lead-Free Package (7x7mm, 0.5mm pitch)

Target Applications

W5500 is suitable for the following embedded applications:

- Home Network Devices: Set-Top Boxes, PVRs, Digital Media Adapters
- Serial-to-Ethernet: Access Controls, LED displays, Wireless AP relays, etc.
- Parallel-to-Ethernet: POS / Mini Printers, Copiers
- USB-to-Ethernet: Storage Devices, Network Printers
- GPIO-to-Ethernet: Home Network Sensors
- Security Systems: DVRs, Network Cameras, Kiosks
- Factory and Building Automations
- Medical Monitoring Equipment
- Embedded Servers

Block Diagram



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1 Pin Assignment

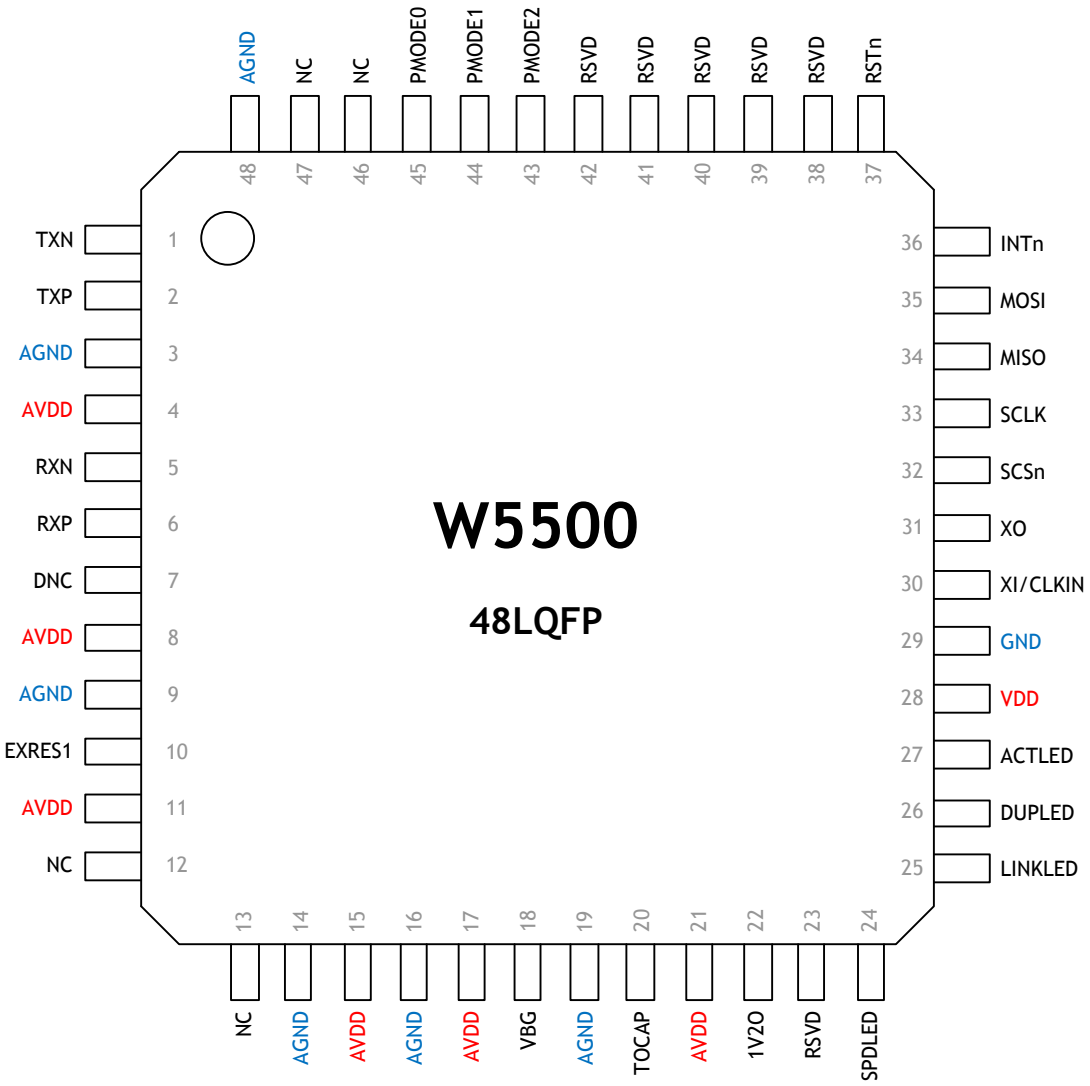


Figure 1. W5500 Pin Layout

1.1 Pin Descriptions

Table 1. Pin Type Notation

Type	Description
I	Input
O	Output
I/O	Input / Output
A	Analog
PWR	3.3V power
GND	Ground

Table 2. W5500 Pin Description

Pin No	Symbol	Internal Bias[1]	Type	Description
1	TXN	-	AO	**TXP/TXN Signal Pair** The differential data is transmitted to the media on the TXP/TXN signal pair.
2	TXP	-	AO	
3	AGND	-	GND	**Analog ground**
4	AVDD	-	PWR	**Analog 3.3V power**
5	RXN	-	AI	**RXP/RXN Signal Pair** The differential data from the media is received on the RXP/RXN signal pair.
6	RXP	-	AI	
7	DNC	-	AI/O	**Do Not Connect Pin**
8	AVDD	-	PWR	**Analog 3.3V power**
9	AGND	-	GND	**Analog ground**
10	EXRES1	-	AI/O	**External Reference Resistor** It should be connected to an external resistor (12.4KΩ, 1%) needed for biasing of internal analog circuits. Refer to the 'External reference resistor' (Figure.2) for details.
11	AVDD	-	PWR	**Analog 3.3V power**
12	-		-	**NC**
13	-		-	**NC**
14	AGND	-	GND	**Analog ground**
15	AVDD	-	PWR	**Analog 3.3V power**
16	AGND	-	GND	**Analog ground**
17	AVDD	-	PWR	**Analog 3.3V power**
18	VBG	-	AO	**Band Gap Output Voltage** This pin will be measured as 1.2V at 25℃. It must be left floating.
19	AGND	-	GND	**Analog ground**
20	TOCAP	-	AO	**External Reference Capacitor** This pin must be connected to a 4.7uF capacitor. The trace length to capacitor should be short to stabilize the internal signals.
21	AVDD	-	PWR	**Analog 3.3V power**
22	1V2O	-	AO	**1.2V Regulator output voltage**

[1] Internal Bias after hardware reset

				This pin must be connected to a 10nF capacitor. This is the output voltage of the internal regulator.
23	RSVD	Pull-down	I	It must be tied to GND.
24	SPDLED	-	O	**Speed LED** This shows the Speed status of the connected link. Low: 100Mbps High: 10Mbps
25	LINKLED	-	O	**Link LED** This shows the Link status. Low: Link is established High: Link is not established
26	DUPLED	-	O	**Duplex LED** This shows the Duplex status for the connected link. Low: Full-duplex mode High: Half-duplex mode
27	ACTLED	-	O	**Active LED** This shows that there is Carrier sense (CRS) from the active Physical Medium Sub-layer (PMD) during TX or RX activity. Low: Carrier sense from the active PMD High: No carrier sense
28	VDD	-	PWR	**Digital 3.3V Power**
29	GND	-	GND	**Digital Ground**
30	XI/CLKIN	-	AI	**Crystal input / External Clock input** External 25MHz Crystal Input. This pin can also be connected to single-ended TTL oscillator (CLKIN). 3.3V clock should be applied for the External Clock input. If this method is implemented, XO should be left unconnected. Refer to the 'Crystal reference schematic' (Figure.3) for details.
31	XO	-	AO	**Crystal output** External 25MHz Crystal Output Note: Float this pin if using an external clock being driven through XI/CLKIN
32	SCSn	Pull-up	I	**Chip Select for SPI bus** This pin can be asserted low to select W5500 in SPI interface. Low: selected

<table>
<tr><td></td><td></td><td></td><td></td><td>High: deselected</td></tr>
<tr><td>33</td><td>SCLK</td><td>-</td><td>I</td><td>SPI clock input
This pin is used to receive SPI Clock from SPI master.</td></tr>
<tr><td>34</td><td>MISO</td><td>-</td><td>O</td><td>SPI master input slave(W5500) output
When SCSn is Low, this pin outputs SPI data.
When SCSn is High, this pin becomes High Impedance (logically disconnected).</td></tr>
<tr><td>35</td><td>MOSI</td><td>-</td><td>I</td><td>SPI master output slave(W5500) input</td></tr>
<tr><td>36</td><td>INTn</td><td>-</td><td>O</td><td>Interrupt output
(Active low)
Low: Interrupt asserted from W5500
High: No interrupt</td></tr>
<tr><td>37</td><td>RSTn</td><td>Pull-up</td><td>I</td><td>Reset
(Active low)
RESET should be held low at least 500 us for W5500 reset.</td></tr>
<tr><td>38</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>39</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>40</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>41</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>42</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>43</td><td>PMODE2</td><td>Pull-up</td><td>I</td><td rowspan="3">PHY Operation mode select pins
These pins determine the network mode. Refer to the below table for details.
<table>
<tr><th colspan="3">PMODE [2:0]</th><th rowspan="2">Description</th></tr>
<tr><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>10BT Half-duplex, Auto-negotiation disabled</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>10BT Full-duplex, Auto-negotiation disabled</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>100BT Half-duplex, Auto-negotiation disabled</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>100BT Full-duplex, Auto-negotiation disabled</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>100BT Half-duplex, Auto-negotiation enabled</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Not used</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Not used</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>All capable, Auto-negotiation enabled</td></tr>
</table></td></tr>
<tr><td>44</td><td>PMODE1</td><td>Pull-up</td><td>I</td></tr>
<tr><td>45</td><td>PMODE0</td><td>Pull-up</td><td>I</td></tr>
<tr><td>46</td><td>-</td><td>-</td><td>-</td><td>NC</td></tr>
<tr><td>47</td><td>-</td><td>-</td><td>-</td><td>NC</td></tr>
<tr><td>48</td><td>AGND</td><td>-</td><td>GND</td><td>Analog ground</td></tr>
</table>

The 12.4KΩ(1%) Resistor should be connected between EXRES1 pin and analog ground (AGND) as below.

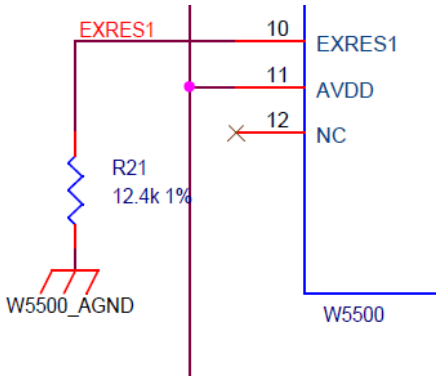


Figure 2. External reference resistor

The crystal reference schematic is shown as below.

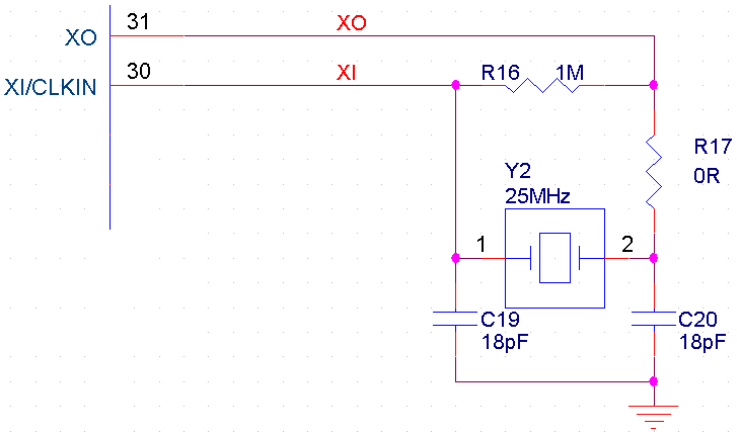


Figure 3. Crystal reference schematic

2 HOST Interface

W5500 provides SPI (Serial Peripheral Interface) Bus Interface with 4 signals (SCSn, SCLK, MOSI, MISO) for external HOST interface, and operates as a SPI Slave.

The W5500 SPI can be connected to MCU as shown in Figure 4 and Figure 5 according to its operation mode (Variable Length Data / Fixed Length Data Mode) which will be explained in Chapter 2.3 and Chapter 2.4.

In Figure 4, SPI Bus can be shared with other SPI Devices. Since the SPI Bus is dedicated to W5500, SPI Bus cannot be shared with other SPI Devices. It is shown in Figure 5.

At the Variable Length Data mode (as shown in Figure 4), it is possible to share the SPI Bus with other SPI devices. However, at the Fixed Length Data mode (as shown in Figure 5), the SPI Bus is dedicated to W5500 and can't be shared with other devices.

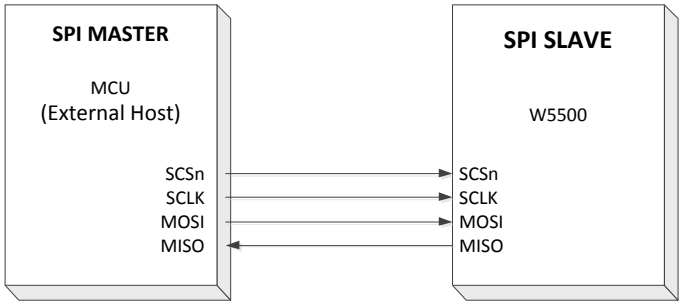


Figure 4. Variable Length Data Mode (SCSn controlled by the host)

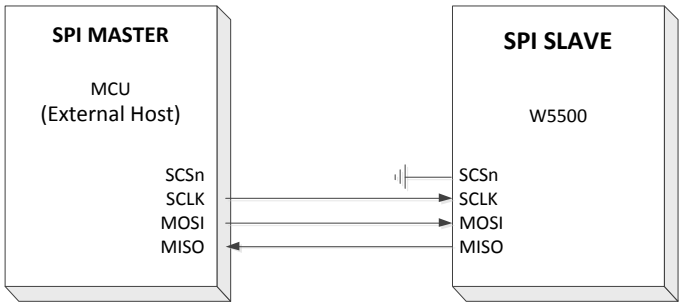


Figure 5. Fixed Length Data Mode (SCSn is always connected by Ground)

The SPI protocol defines four modes for its operation (Mode 0, 1, 2, 3).Each mode differs according to the SCLK polarity and phase. The only difference between SPI Mode 0 and SPI Mode 3 is the polarity of the SCLK signal at the inactive state.

With SPI Mode 0 and 3, data is always latched in on the rising edge of SCLK and always output on the falling edge of SCLK.

The W5500 supports SPI Mode 0 and Mode 3. Both MOSI and MISO signals use transfer sequence from Most Significant Bit (MSB) to Least Significant Bit (LSB) when MOSI signal transmits and MISO signal receives. MOSI & MISO signals always transmit or receive in sequence from the Most Significant Bit (MSB) to Least Significant Bit (LSB).

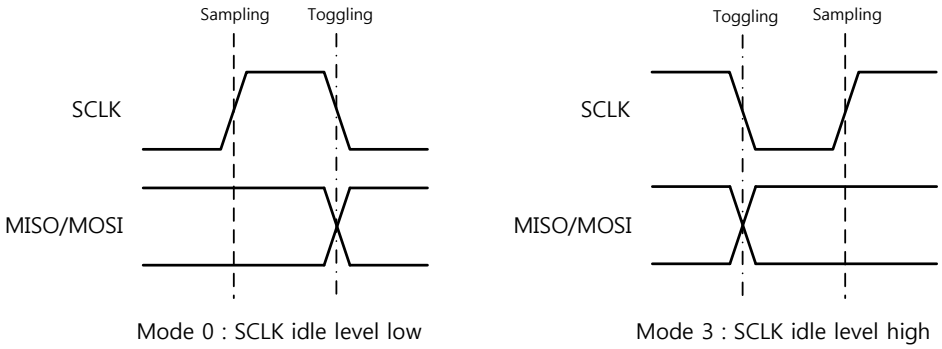


Figure 6. SPI Mode 0 & 3

2.1 SPI Operation Mode

W5500 is controlled by SPI Frame (Refer to the Chapter 2.2 SPI Frame) which communicates with the External Host. W5500 SPI Frame consists 3 phases, Address Phase, Control Phase and Data Phase.

Address Phase specifies 16 bits Offset Address for W5500 Register or TX/RX Memory. Control Phase specifies the block to which Offset (set by Address Phase) belongs, and specifies Read/Write Access Mode and SPI Operation Mode (Variable Length Data / Fixed Length Data Mode).
And Data Phase specifies random length (N-bytes, 1 ≤ N) Data or 1 byte, 2 bytes and 4 bytes Data.

If SPI Operation Mode is set as Variable Length Data Mode (VDM), SPI Bus Signal SCSn must be controlled by the External Host with SPI Frame step.
At the Variable Length Data Mode, SCSn Control Start (Assert (High-to-Low)) informs W5500 of SPI Frame Start (Address Phase), and SCSn Control End (De-assert (Low-to-High) informs W5500 of SPI Frame End (Data Phase End of random N byte).

2.2 SPI Frame

W5500 SPI Frame consists of 16bits Offset Address in Address Phase, 8bits Control Phase and N bytes Data Phase as shown in Figure 7.

The 8bits Control Phase is reconfigured with Block Select bits (BSB[4:0]), Read/Write Access Mode bit (RWB) and SPI Operation Mode (OM[1:0]).

Block Select bits select the block to which the Offset Address belongs.

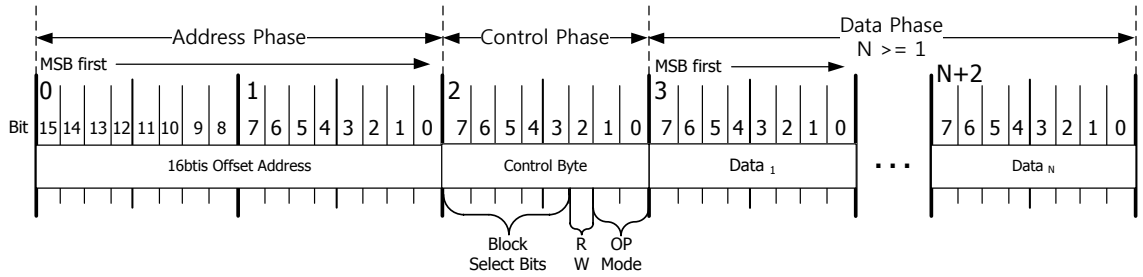


Figure 7. SPI Frame Format

W5500 supports Sequential Data Read/Write. It processes the data from the base (the Offset Address which is set for 2/4/N byte Sequential data processing) and the next data by increasing the Offset Address (auto increment addressing) by 1.

2.2.1 Address Phase

This Address Phase specifies the 16 bits Offset Address for the W5500 Registers and TX/RX Buffer Blocks.

The 16-bit Offset Address value is transferred from MSB to LSB sequentially.

The SPI frame with 2/4/N byte data phase supports the Sequential Data Read/Write in which Offset address automatically increases by 1 every 1 byte data.

2.2.2 Control Phase

The Control Phase specifies the Block to which the Offset Address (set by Address Phase) belongs, the Read/Write Access Mode and the SPI Operation Mode.

7	6	5	4	3	2	1	0
BSB4	BSB3	BSB2	BSB1	BSB0	RWB	OM1	OM0

Bit	Symbol	Description
7~3	BSB [4:0]	**Block Select Bits** W5500 has Common Register, 8 Socket Register, TX/RX Buffer Block for each Socket. The next table shows the Block selected by BSB[4:0].

BSB [4:0]	Meaning
00000	Selects Common Register.
00001	Selects Socket 0 Register
00010	Selects Socket 0 TX Buffer
00011	Selects Socket 0 RX Buffer
00100	Reserved
00101	Selects Socket 1 Register
00110	Selects Socket 1 TX Buffer
00111	Selects Socket 1 RX Buffer
01000	Reserved
01001	Selects Socket 2 Register
01010	Selects Socket 2 TX Buffer
01011	Selects Socket 2 RX Buffer
01100	Reserved
01101	Selects Socket 3 Register
01110	Selects Socket 3 TX Buffer
01111	Selects Socket 3 RX Buffer
10000	Reserved
10001	Selects Socket 4 Register
10010	Selects Socket 4 TX Buffer
10011	Selects Socket 4 RX Buffer
10100	Reserved
10101	Selects Socket 5 Register
10110	Selects Socket 5 TX Buffer
10111	Selects Socket 5 RX Buffer

		11000 Reserved 11001 Selects Socket 6 Register 11010 Selects Socket 6 TX Buffer 11011 Selects Socket 6 RX Buffer 11100 Reserved 11101 Selects Socket 7 Register 11110 Selects Socket 7 TX Buffer 11111 Selects Socket 7 RX Buffer If the Reserved Bits are selected, it can cause the mal-function of the W5500.
2	RWB	**Read/Write Access Mode Bit** This sets Read/Write Access Mode. '0' : Read '1' : Write
1~0	OM [1:0]	**SPI Operation Mode Bits** This sets the SPI Operation Mode. SPI Operation Mode supports two modes, the Variable Length Data Mode and the Fixed Length Data Mode. **- Variable Length Data Mode (VDM)** : Data Length is controlled by SCSn. External Host makes SCSn Signal Assert (High-to-Low) and informs the start of the SPI Frame Address Phase to W5500. Then the external host transfers the Control Phase with OM[1:0]='00'. After N-Bytes Data Phase transfers, SCSn Signal is De-asserted (Low-to-High) and informs the end of the SPI Frame Data Phase to W5500. In VDM Mode, the SCSn must be controlled with SPI Frame unit by the External Host. (Refer to the Figure 4) **- Fixed Length Data Mode (FDM)** : In FDM, the Data Length is set by OM[1:0], these are not '00' value. So, the SCSn signal should be Low state, and has one Length type (among 1 Bytes, 2 Bytes, 4 Bytes) according to the OM[1:0] value. (Refer to the Figure 5.) The next table shows the SPI Operation Mode according to the OM[1:0].

		OM[1:0]	Meaning
		00	Variable Data Length Mode, N-Bytes Data Phase (1 ≤ N)
		01	Fixed Data Length Mode , 1 Byte Data Length (N = 1)
		10	Fixed Data Length Mode , 2 Byte Data Length (N = 2)
		11	Fixed Data Length Mode , 4 Byte Data Length (N = 4)

2.2.3 Data Phase

With the Control Phase set by the SPI Operation Mode Bits OM[1:0], the Data Phase is set by two types of length, one type is the N-Bytes length (VDM mode) and the other type is 1/2/4 Bytes (FDM mode).

At this time, 1 byte data is transferred through MOSI or MISO signal from MSB to LSB sequentially.

2.3 Variable Length Data Mode (VDM)

In VDM mode, the SPI Frame Data Phase Length is determined by SCSn Control of the External Host. That means that the Data Phase Length can have random value (Any length from 1 Byte to N Bytes) according to the SCSn Control.

The OM[1:0] of the Control Phase should be '00' value in VDM mode.

2.3.1 Write Access in VDM

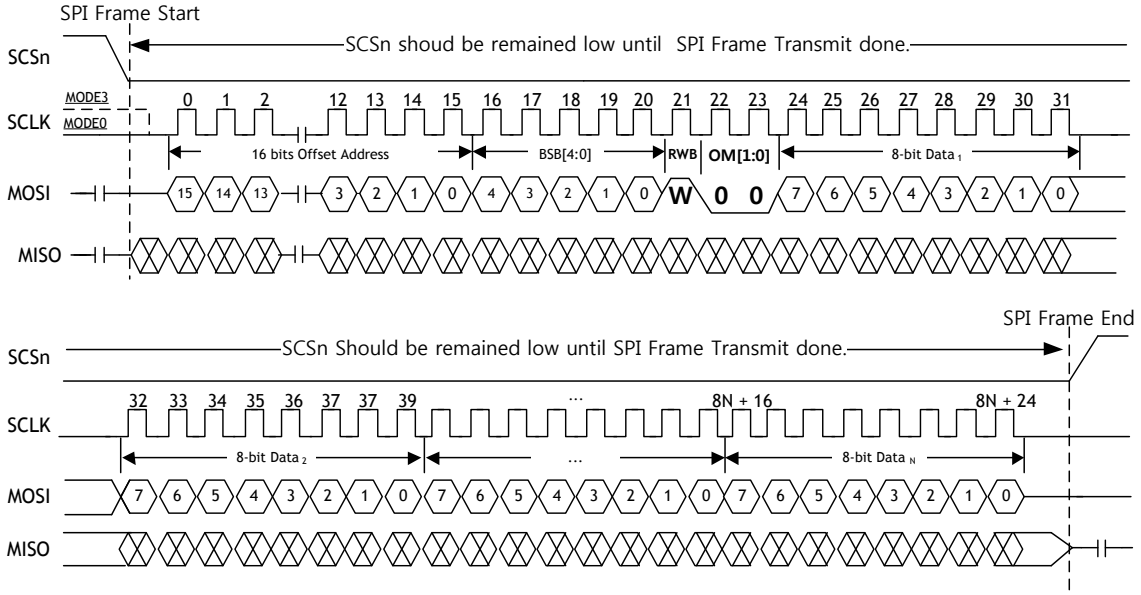


Figure 8. Write SPI Frame in VDM mode

Figure 8 shows the SPI Frame when the external host accesses W5500 for writing.

In VDM mode, the RWB signal is '1' (Write), OM[1:0] is '00' in SPI Frame Control Phase. At this time the External Host assert (High-to-Low) SCSn signal before transmitting SPI Frame. Then the Host transmits SPI Frame's all bits to W5500 through MOSI signal. All bits are synchronized with the falling edge of the SCLK. After finishing the SPI Frame transmit, the Host deasserts SCSn signal (Low-to-High).

When SCSn is Low and the Data Phase continues, the Sequential Data Write can be supported.

1 Byte WRITE Access Example

When the Host writes Data 0xAA to 'Socket Interrupt Mask Register (SIMR) of Common Register Block by using VDM mode, the data is written with the SPI Frame below.

```
Offset Address = 0x0018
BSB[4:0]       = '00000'
RWB            = '1'
OM[1:0]        = '00'
1st Data       = 0xAA
```

The External Host asserts (High-to-Low) SCSn before transmitting SPI Frame, then the Host transmits 1 bit with synchronizing the Toggle SCLK. The External Host de-asserts (Low-to-High) the SCSn at the end of SPI Frame transmit. (Refer to the Figure 9)

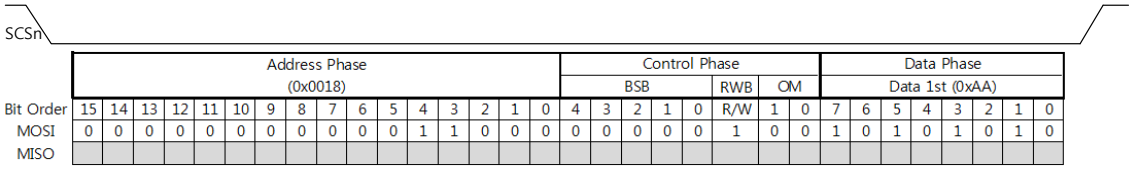


Figure 9. SIMR Register Write in VDM Mode

N-Bytes WRITE Access Example

When the Host writes 5 Bytes Data (0x11, 0x22, 0x33, 0x44, 0x55) to Socket 1's TX Buffer Block 0x0040 Address by using VDM mode, 5 bytes data are written with the SPI Frame below.

```
Offset Address = 0x0040
BSB[4:0]       = '00110'
RWB            =  '1'
OM[1:0]        = '00'
1st Data       = 0x11
2nd Data       = 0x22
3rd Data       = 0x33
4th Data       = 0x44
5th Data       = 0x55
```

The N-Bytes Write Access is shown in Figure 10.

The 5 bytes of Data (0x11, 0x22, 0x33, 0x44, 0x55) are written sequentially to Socket 1's Tx Buffer Block Address 0x0040 ~ 0x0044.

The External Host asserts (High-to-Low) SCSn before transmitting SPI Frame.

The External Host de-asserts (Low-to-High) the SCSn at the end of SPI Frame transmit.

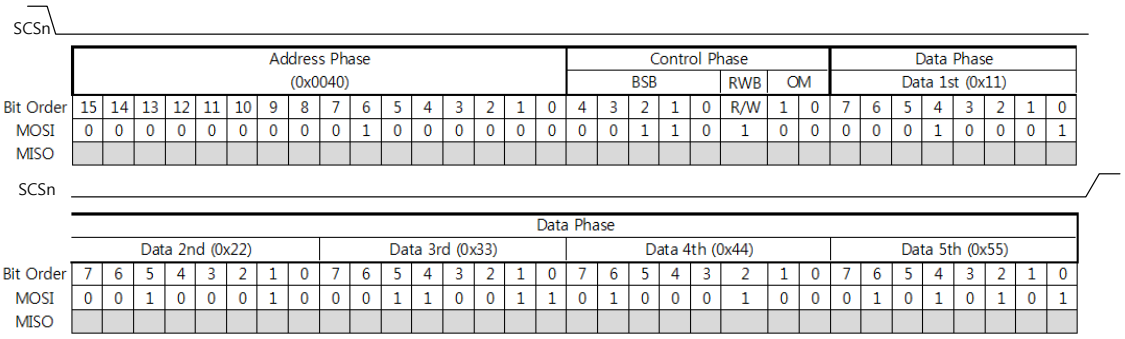


Figure 10. 5 Byte Data Write at 1th Socket's TX Buffer Block 0x0040 in VDM mode

2.3.2 Read Access in VDM

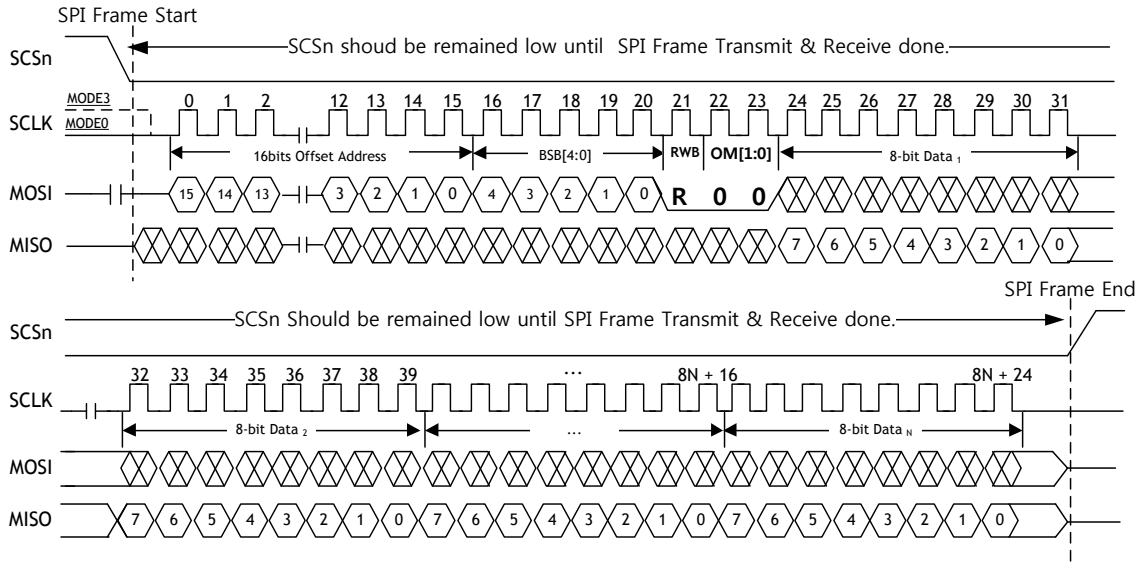


Figure 11. Read SPI Frame in VDM mode

Figure 11 shows the SPI Frame when external host accesses W5500 for reading In VDM mode, the RWB signal is '0' (Write), OM[1:0] is '00' in SPI Frame Control Phase. At this time the External Host assert (High-to-Low) SCSn signal before transmitting SPI Frame.

Then the Host transmits Address and Control Phase all bits to W5500 through MOSI signal. All bits are synchronized with the falling edge of the SCLK.

Then the Host receives all bits of Data Phase with synchronizing the rising edge of Sampling SCLK through MISO signal.

After finishing the Data Phase receive, the Host de-asserts SCSn signal (Low-to-High).

When SCSn is Low and the Data Phase continues to receive, the Sequential Data Read can be supported.

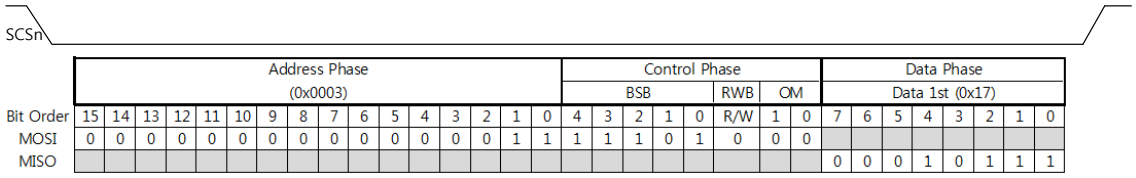
1 Byte READ Access Example

When the Host reads the 'Socket Status Register(S7_SR) of the Socket 7's Register Block by using VDM mode, the data is read with the SPI Frame below. Let's S7_SR to 'SOCK_ESTABLISHED (0x17)'.

```
Offset Address = 0x0003
BSB[4:0]       = '11101'
RWB            = '0'
OM[1:0]        = '00'
1st Data       = 0x17
```

The External Host asserts (High-to-Low) SCSn signal before transmitting SPI Frame, then the Host transmits Address and Control Phase to W5500 through the MOSI signal. Then the Host receives Data Phase from the MISO signal.

After finishing the Data Phase receives, the Host de-asserts SCSn signal (Low-to-High). (Refer to the Figure 12)



	Address Phase (0x0003)																Control Phase								Data Phase							
																	BSB					RWB	OM		Data 1st (0x17)							
Bit Order	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4	3	2	1	0	R/W	1	0	7	6	5	4	3	2	1	0
MOSI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0								
MISO																									0	0	0	1	0	1	1	1

Figure 12. S7_SR Read in VDM Mode

N-Bytes Read Access Example

When the Host reads 5 Bytes Data (0xAA, 0xBB, 0xCC, 0xDD, 0xEE) from the Socket 3's RX Buffer Block 0x0100 Address by using VDM mode, 5 bytes data are read with the SPI Frame as below.

```
Offset Address = 0x0100
BSB[4:0]       = '01111'
RWB            = '0'
OM[1:0]        = '00'
1st Data       = 0xAA
2nd Data       = 0xBB
3rd Data       = 0xCC
4th Data       = 0xDD
5th Data       = 0xEE
```

The N-Bytes Read Access is shown in Figure 13.

The 5 bytes of Data (0xAA, 0xBB, 0xCC, 0xDD, 0xEE) are read sequentially from the Socket 3's Rx Buffer Block Address 0x0100 ~ 0x0104.

The External Host asserts (High-to-Low) SCSn before transmitting SPI Frame.

The External Host de-asserts (Low-to-High) the SCSn at the end of the SPI Frame Data Phase.

SCSn

	Address Phase (0x0100)																Control Phase								Data Phase							
																	BSB					RWB	OM		Data 1st (0xAA)							
Bit Order	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4	3	2	1	0	R/W	1	0	7	6	5	4	3	2	1	0
MOSI	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0								
MISO																									1	0	1	0	1	0	1	0

SCSn

	Data Phase																															
	Data 2nd (0xBB)								Data 3rd (0xCC)								Data 4th (0xDD)								Data 5th (0xEE)							
Bit Order	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI																																
MISO	1	0	1	1	1	0	1	1	1	1	0	0	1	1	0	0	1	1	0	1	1	1	0	1	1	1	1	0	1	1	1	0

Figure 13. 5 Byte Data Read at Socket 3 RX Buffer Block 0x0100 in VDM mode

2.4 Fixed Length Data Mode (FDM)

The FDM mode can be used when the External Host cannot control SCSn signal. The SCSn signal should be tied to Low (Always connected to GND) and it is not possible to share the SPI Bus with other SPI Devices. (Refer to the Figure 5)

In VDM mode, Data Phase length is controlled by SCSn control. But in FDM mode, Data Phase length is controlled by OM[1:0] value ('01' / '10' / '11') which is the SPI Operation Mode Bits of the Control Phase.

As the SPI Frame of FDM mode is the same as SPI Frame of VDM mode (1Byte, 2 Bytes, 4 Bytes SPI Frame) except for the SCSn signal control and OM[1:0] setting, the detail about FDM mode is not described in this section.

It is not recommended to use the FDM mode unless you are in inevitable status. In addition, we use only 1/2/4 Bytes SPI Frame, as described in 'Chapter 2.4.1' & 'Chapter 2.4.2'. Using SPI Frame with other length of Data will cause malfunction of W5500.

2.4.1 Write Access in FDM

1 Bytes WRITE Access

	Address Phase (Any)																Control Phase								Data Phase							
																	BSB (Any)					RWB	OM		Data 1st (any)							
Bit Order	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4	3	2	1	0	R/W	1	0	7	6	5	4	3	2	1	0
MOSI	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	**0**	**1**	*	*	*	*	*	*	*	*
MISO																																

Figure 14. 1 Byte Data Write SPI Frame in FDM mode

2 Bytes WRITE Access

	Address Phase (Any)																Control Phase								Data Phase							
																	BSB					RWB	OM		Data 1st (any)							
Bit Order	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4	3	2	1	0	R/W	1	0	7	6	5	4	3	2	1	0
MOSI	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	**1**	**0**	*	*	*	*	*	*	*	*
MISO																																

	Data Phase							
	Data 2nd (any)							
Bit Order	7	6	5	4	3	2	1	0
MOSI	*	*	*	*	*	*	*	*
MISO								

Figure 15. 2 Bytes Data Write SPI Frame in FDM mode

4 Bytes WRITE Access

	Address Phase (Any)																Control Phase								Data Phase							
																	BSB					RWB	OM		Data 1st (any)							
Bit Order	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4	3	2	1	0	R/W	1	0	7	6	5	4	3	2	1	0
MOSI	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	**1**	**1**	*	*	*	*	*	*	*	*
MISO																																

	Data Phase								Data Phase								Data Phase							
	Data 2nd (any)								Data 3rd (any)								Data 4th (any)							
Bit Order	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
MISO																								

Figure 16. 4 Bytes Data Write SPI Frame in FDM mode