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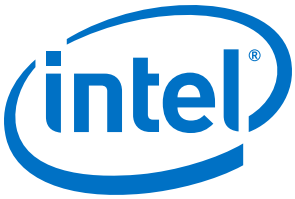

Low Latency Ethernet 10G MAC Intel® FPGA IP User Guide

Updated for Intel® Quartus® Prime Design Suite: **18.1**

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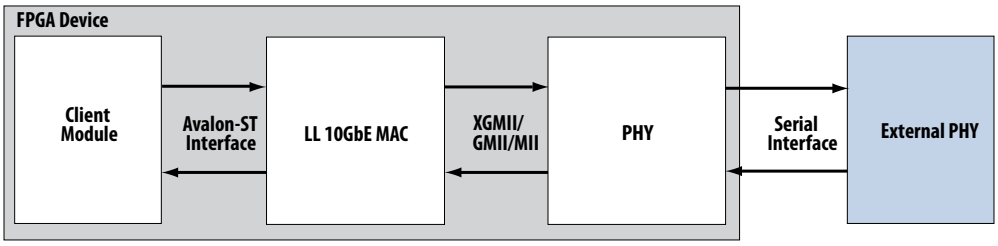
Contents

1. About LL Ethernet 10G MAC

The Low Latency (LL) Ethernet 10G (10GbE) Media Access Controller (MAC) Intel® FPGA IP core is a configurable component that implements the IEEE 802.3-2008 specification. To build a complete Ethernet subsystem in an Intel FPGA device and connect it to an external device, you can use the LL 10GbE Intel FPGA IP core with an Intel FPGA PHY IP core or any of the supported PHYs.

The following figure shows a system with the LL 10GbE MAC Intel FPGA IP core.

Figure 1. Typical Application of LL 10GbE MAC



Note: Intel FPGAs implement and support the LL 10GbE Media Access Control (MAC) and Multi-Rate Ethernet PHY (PCS + PMA) IP to interface in a chip-to-chip or chip-to-module channel with external MGBASE-T and NBASE-T (1G/2.5G/5G/10Gb Ethernet) PHY standard devices. However, Intel FPGAs do not comply with or support these interface specifications to directly interface with the required twisted-pair copper cables such as CAT-5/6/7.

Related Information

- Low Latency Ethernet 10G MAC Intel FPGA IP User Guide Archives on page 119
  Provides a list of user guides for previous versions of the Low Latency Ethernet 10G MAC Intel FPGA IP core.
- Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide
- Low Latency Ethernet 10G MAC Intel Arria 10 FPGA IP Design Example User Guide
- Low Latency Ethernet 10G MAC Intel Cyclone 10 GX FPGA IP Design Example User Guide
- 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel Stratix 10 FPGA IP User Guide

1.1. Features

This Intel FPGA IP core is designed to the *IEEE 802.3–2008 Ethernet Standard* available on the IEEE website (www.ieee.org). All LL 10GbE Intel FPGA IP core variations include MAC only and are in full-duplex mode. These Intel FPGA IP core variations offer the following features:

- MAC features:
  - Full-duplex MAC in eight operating modes: 10G, 1G/10G, 1G/2.5G, 1G/2.5G/10G, 10M/100M/1G/2.5G/5G/10G (USXGMII), 10M/100M/1G/10G, 10M/100M/1G/2.5G, and 10M/100M/1G/2.5G/10G.
  - Three variations for selected operating modes: MAC TX only block, MAC RX only block, and both MAC TX and MAC RX block.
  - 10GBASE-R register mode on the TX and RX datapaths, which enables lower latency.
  - Programmable promiscuous (transparent) mode.
  - Unidirectional feature as specified by IEEE 802.3 (Clause 66).
  - Priority-based flow control (PFC) with programmable pause quanta. PFC supports 2 to 8 priority queues.
- Interfaces:
  - Client-side—32-bit Avalon®-ST interface.
  - Management—32-bit Avalon-MM interface.
  - PHY-side—32-bit XGMII for 10GbE, 16-bit GMII for 2.5GbE, 8-bit GMII for 1GbE, or 4-bit MII for 10M/100M.
- Frame structure control features:
  - Virtual local area network (VLAN) and stacked VLAN tagged frames decoding (type 'h8100).
  - Cyclic redundancy code (CRC)-32 computation and insertion on the TX datapath. Optional CRC checking and forwarding on the RX datapath.
  - Deficit idle counter (DIC) for optimized performance with average inter-packet gap (IPG) for LAN applications.
  - Supports programmable IPG.
  - Ethernet flow control using pause frames.
  - Programmable maximum length of TX and RX data frames up to 64 Kbytes (KB).
  - Preamble passthrough mode on TX and RX datapaths, which allows user defined preamble in the client frame.
  - Optional padding insertion on the TX datapath and termination on the RX datapath.
- Frame monitoring and statistics:
  - Optional CRC checking and forwarding on the RX datapath.
  - Optional statistics collection on TX and RX datapaths.

- Optional timestamping as specified by the IEEE 1588v2 standard for the following configurations:
  - 10GbE MAC with 10GBASE-R PHY IP core
  - 1G/10GbE MAC with 1G/10GbE PHY IP core
  - 1G/2.5GbE MAC with 1G/2.5G Multi-rate Ethernet PHY IP core
  - 1G/2.5G/10GbE MAC with 1G/2.5G/10G (MGBASE-T) Multi-rate Ethernet PHY IP core
  - 10M/100M/1G/10GbE MAC with 10M-10GbE PHY IP core
  - 10M/100M/1G/2.5G/5G/10G (USXGMII) MAC with 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP core

1.1.1. LL Ethernet 10G MAC and Legacy 10-Gbps Ethernet MAC

Current users of the legacy 10-Gbps Ethernet MAC IP core can use the following table to consider migrating to the LL Ethernet 10G MAC Intel FPGA IP core.

Table 1. Features Comparison

Feature	LL 10GbE MAC	Legacy 10GbE MAC
Operating mode	• 10G • 1G/10G • 1G/2.5G • 1G/2.5G/10G • 10M/100M/1G/10G • 10M/100M/1G/2.5G/5G/10G (USXGMII) • 10M/100M/1G/2.5G • 10M/100M/1G/2.5G/10G	• 10G • 1G/10G, 10M/100M/1G/10G
Device support (1)	• Intel Arria® 10 • Intel Cyclone® 10 GX • Intel Stratix® 10 • Stratix V	• Arria V • Arria II • Cyclone V • Cyclone IV • Stratix V • Stratix IV
Operating frequency	• 312.5 MHz • 322.265625 MHz (10GBASE-R register mode enabled)	• 156.25MHz
Latency (TX + RX)	For Intel Arria 10 and Intel Cyclone 10 GX devices: • 60.8 ns (10G MAC) • 307 ns (1G MAC) For Intel Stratix 10 devices: • 70.4 ns (10G MAC) • 319.9 ns (1G MAC)	• 140.8 ns (10G MAC) • 422.4 ns (1G MAC)
Resource utilization	For Intel Arria 10 and Intel Cyclone 10 GX devices:	2,300 ALMs, 3,100 ALUTs, 4,400 Registers, 2 M20Ks (10G with all options disabled)

continued...

(1) Device support depends on the operating mode. Refer to the individual user guides for further details.

Feature	LL 10GbE MAC	Legacy 10GbE MAC
	• 1,600 ALMs • 2,400 ALUTs • 2,800 Registers (10G with all options disabled) For Intel Stratix 10 devices: • 2,000 ALMs • 2,700 ALUTs • 2,900 Registers (10G with all options disabled)	
Avalon-ST interface data width	• 32 bits • 64 bits, when the backward compatibility to the legacy MAC is enabled.	• 64 bits
XGMII data width	• 32 bits • Supports backward compatibility with the legacy MAC	• 64 bits
Configuration registers	• 10-bit address bus • Supports backward compatibility with the legacy MAC	• 13-bit address bus
Error detection and correction (ECC)	Supported	Not supported
10GBASE-R register mode	Supported	Not supported
96-bit and 64-bit ToD clock formats	Supported	Not supported
Programmable IPG	Supported	Not supported

Related Information

Altera Low Latency Ethernet 10G MAC IP Core Migration Guidelines

Provides more information on migrating from the legacy 10G Ethernet MAC IP core to the Low Latency Ethernet 10G MAC Intel FPGA core.

1.2. Release Information

Table 2. Release Information of the LL Ethernet 10G MAC Intel FPGA IP Core

Item	Description
Version	18.1
Release Date	September 2018
Ordering Code (without the IEEE 1588v2 feature)	IP-10GEUMAC
Ordering Code (with the IEEE 1588v2 feature)	IP-10GEUMACF
Vendor ID	6AF7

Intel verifies that the current version of the Intel Quartus® Prime software compiles the previous version of each Intel FPGA IP core function, if this Intel FPGA IP core function was included in the previous release. Any exceptions to this verification are reported in the *Intel FPGA IP Release Notes*. Intel does not verify compilation with Intel FPGA IP core function versions older than the previous release.

Related Information

- Intel FPGA IP Release Notes
- Errata for Low Latency Ethernet 10G MAC Intel FPGA IP Core in the Knowledge Base

1.3. LL Ethernet 10G MAC Operating Modes

Table 3. Speed Mode Comparison of the LL Ethernet 10G MAC Intel FPGA IP Core

Speed Mode	Default Speed	MAC Interface	Intel PHY Compliance
10G	10G	• 32-bit XGMII • 64-bit XGMII (Use legacy Ethernet 10G MAC XGMII interface enabled)	• 10GBASE-R PHY • 10GBASE-KR PHY • Intel Arria 10/Intel Cyclone 10 GX Transceiver Native PHY with presets: — 10GBASE-R — 10GBASE-R Low Latency — 10GBASE-R register mode — 10GBASE-R with KR-FEC • Intel Stratix 10 Transceiver Native PHY with presets: — 10GBASE-R — 10GBASE-R Low Latency — 10GBASE-R 1588 — 10GBASE-R with KR-FEC
1G/10G	10G	• 8-bit GMII • 32-bit XGMII • 64-bit XGMII (Use legacy Ethernet 10G MAC XGMII interface enabled)	1G/10GbE Ethernet PHY IP

continued...

Speed Mode	Default Speed	MAC Interface	Intel PHY Compliance
10M/100M/1G/10G	10G	• 4-bit MII • 8-bit GMII • 32-bit XGMII • 64-bit XGMII (Use legacy Ethernet 10G MAC XGMII interface enabled)	1G/10GbE Ethernet PHY IP
1G/2.5G	2.5G	16-bit GMII	1G/2.5G/5G/10G Multi-rate Ethernet PHY
1G/2.5G/10G	10G	• 16-bit GMII • 32-bit XGMII • 64-bit XGMII (Use legacy Ethernet 10G MAC XGMII interface enabled)	1G/2.5G/5G/10G Multi-rate Ethernet PHY (MGBASE-T)
10M/100M/1G/ 2.5G/5G/10G	10G	32-bit USXGMII	1G/2.5G/5G/10G Multi-rate Ethernet PHY (NBASE-T)
10M/100M/1G/2.5G	2.5G	16-bit GMII	1G/2.5G/5G/10G Multi-rate Ethernet PHY
10M/100M/1G/ 2.5G/10G	10G	• 16-bit GMII • 32-bit XGMII • 64-bit XGMII (Use legacy Ethernet 10G MAC XGMII interface enabled)	1G/2.5G/5G/10G Multi-rate Ethernet PHY (MGBASE-T)

1.4. Device Family Support

Table 4. Intel FPGA IP Core Device Support Levels

Device Support Level	Definition
Preliminary	Intel verifies the IP core with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. This IP core can be used in production designs with caution.
Final	Intel verifies the IP core with final timing models for this device family. The IP core meets all functional and timing requirements for the device family. This IP core is ready to be used in production designs.

The IP core provides the following support for Intel FPGA device families.

Table 5. Device Family Support for LL 10GbE MAC

Device Family	Support	Minimum Speed Grade	
		With 1588 Feature	Without 1588 Feature
Intel Stratix 10	Preliminary	-I2, -E2	-I3, -C3
Intel Arria 10	Final	-I2, -E2	-I3, -E3
Intel Cyclone 10 GX	Final	-I5, -E5	-I6, -E6
Stratix V	Final	-I3, -C3	-I4, -C4
Arria V	Final	-I3, -C3	-I4, -C4

The following table lists possible LL 10GbE MAC and PHY configurations and the devices each configuration supports:

Table 6. Device Family Support for LL 10GbE MAC and PHY Configurations

LL 10GbE MAC Mode	PHY	Arria V	Intel Arria 10	Intel Cyclone 10 GX	Stratix V	Intel Stratix 10
10G	10GBASE-R	Arria V GZ	—	—	Yes	—
	10GBASE-R with IEEE 1588v2 feature	Arria V GZ	—	—	Yes	—
	• 10GBASE-R • 10GBASE-R Low Latency • 10GBASE-R Register Mode • 10GBASE-R with KR-FEC	—	Yes	Yes	—	
	• 10GBASE-R • 10GBASE-R Low Latency • 10GBASE-R with IEEE 1588v2 feature • 10GBASE-R with KR-FEC	—	—	—	—	Yes

continued...

LL 10GbE MAC Mode	PHY	Arria V	Intel Arria 10	Intel Cyclone 10 GX	Stratix V	Intel Stratix 10
1G/2.5G/10G	1G/2.5G/10G (MGBASE-T) Multi-rate (2)	—	Yes	Yes	—	Yes
	1G/2.5G/10G (MGBASE-T) Multi-rate with IEEE 1588v2 feature	—	—	—	—	Yes
10M/100M/1G/2.5G/5G/10G (USXGMII)	10M/100M/1G/2.5G/5G/10G (USXGMII) Multi-rate (3)	—	Yes	Yes	—	Yes
	10M/100M/1G/2.5G/5G/10G (USXGMII) Multi-rate with IEEE 1588v2 feature	—	—	—	—	Yes
1G/2.5G	1G/2.5G Multi-rate	Arria V GX/GT/SX/ST	Yes	Yes	—	Yes
	1G/2.5G Multi-rate with IEEE 1588v2 feature	Arria V GX/GT/SX/ST	Yes	Yes	—	Yes
	2.5G Multi-rate	Arria V GX/GT/SX/ST	Yes	—	—	Yes
1G/2.5G with IEEE 1588v2 feature	2.5G Multi-rate with IEEE 1588v2 feature	Arria V GX/GT/SX/ST	Yes	—	—	Yes
10M/100M/1G/10G	—	Arria V GZ	Yes	Yes	Yes	Yes
10M/100M/1G/10G MAC with IEEE 1588v2 feature	—	Arria V GZ	Yes	Yes	Yes	Yes
10M/100M/1G/10G	1G/10GbE	Arria V GZ	Yes	Yes	Yes	—
10G	Backplane Ethernet 10GBASE-KR	—	—	—	—	Yes
1G/10G	1G/10GbE	Yes	Yes	Yes	Yes	—
1G/10G with IEEE 1588v2 feature	1G/10GbE with IEEE 1588v2 feature	Yes	Yes	Yes	Yes	—
10M/100M/1G/10G MAC with IEEE 1588v2 feature	1G/10GbE	Arria V GZ	Yes	Yes	Yes	—
10M/100M/1G/2.5G	1G/2.5G Multi-rate with SGMII bridge enabled	—	—	—	—	Yes
10M/100M/1G/2.5G/10G	1G/2.5G/10G (MGBASE-T) Multi-rate with SGMII bridge enabled	—	—	—	—	Yes

(2) Connected to an external MGBASE-T PHY.

(3) Connected to an external NBASE-T PHY.

Related Information

- Intel Stratix 10 10GBASE-KR PHY IP Core User Guide
- 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel Stratix 10 FPGA IP User Guide

1.5. Performance and Resource Utilization

1.5.1. Resource Utilization

The estimated resource utilization for all operating modes are obtained by compiling the LL Ethernet 10G MAC Intel FPGA IP core with the Intel Quartus Prime software targeting on Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices. These estimates are generated by the fitter, excluding the virtual I/Os.

Table 7. Resource Utilization for LL Ethernet 10G MAC for Intel Stratix 10 Devices

MAC Settings			ALMs	ALUTs	Logic Registers	Memory Block (M20K)
Operating Mode	Enabled Options					
10G	None.		2,000	2,700	2,900	0
10G	Memory-based statistics counters.		2,700	3,600	4,300	4
1G/2.5G	Supplementary addresses. Memory-based statistics counters.		3,500	4,300	5,900	4
1G/2.5G	Supplementary addresses. Memory-based statistics counters. Timestamping. Time of day: 96b and 64b.		7,000	8,100	13,100	19
1G/2.5G/10G	Supplementary addresses. Memory-based statistics counters.		3,600	4,500	6,200	4
10M/100M/1G/2.5G/5G/10G (USXGMII)	Supplementary addresses. Memory-based statistics counters.		3,000	4,200	5,100	4
10M/100M/1G/2.5G/5G/10G (USXGMII)	Supplementary addresses. Memory-based statistics counters. Timestamping.	Time of day: 96b and 64b.	5,800	7,800	10,700	21
		Time of day: 96b	5,400	7,100	9,800	20
		Time of day format: 64b	4,800	6,300	8,900	17
10M/100M/1G/10G	Memory-based statistics counters.		3,400	4,400	5,500	4
10M/100M/1G/10G	Memory-based statistics counters. Timestamping.	Time of day: 96b and 64b.	6,800	8,300	12,100	17
		Time of day: 96b	6,300	7,700	11,000	17
		Time of day format: 64b	5,600	6,700	10,000	13
10M/100M/1G/10G	All options enabled except the options to maintain compatibility with the legacy Ethernet 10G MAC.		7,200	8,600	12,400	27
10M/100M/1G/2.5G	Supplementary addresses. Memory-based statistics counters.		3,500	4,600	6,100	4
10M/100M/1G/2.5G/10G	Supplementary addresses. Memory-based statistics counters.		3,600	4,800	6,800	4

Table 8. Resource Utilization for LL Ethernet 10G MAC for Intel Arria 10 and Intel Cyclone 10 GX Devices

MAC Settings			ALMs	ALUTs	Logic Registers	Memory Block (M20K)
Operating Mode	Enabled Options					
10G	None.		1,600	2,400	2,800	0
10G	Memory-based statistics counters.		2,400	3,300	4,000	4
1G/2.5G	Supplementary addresses. Memory-based statistics counters.		2,700	4,100	5,400	5
1G/2.5G	Supplementary addresses. Memory-based statistics counters. Timestamping. Time of day: 96b and 64b.		5,500	8,100	13,300	22
1G/2.5G/10G	Supplementary addresses. Memory-based statistics counters.		2,900	4,200	5,800	4
10M/100M/1G/2.5G/5G/10G (USXGMII)	Supplementary addresses. Memory-based statistics counters.		2,400	3,900	4,700	4
10M/100M/1G/10G	Memory-based statistics counters.		2,600	4,000	5,200	4
10M/100M/1G/10G	Timestamping. Memory-based statistics counters.	Time of day: 96b and 64b.	5,000	7,600	13,000	21
		Time of day: 96b	4,700	7,000	11,800	20
		Time of day format: 64b	4,200	6,300	10,700	17
10M/100M/1G/10G	All options enabled except the options to maintain compatibility with the legacy Ethernet 10G MAC.		5,400	7,900	13,300	27
10M/100M/1G/2.5G	Supplementary addresses. Memory-based statistics counters.		2,900	4,300	5,700	5
10M/100M/1G/2.5G/10G	Supplementary addresses. Memory-based statistics counters.		3,000	4,400	6,000	4

1.5.2. TX and RX Latency

The TX and RX latency values are based on the following definitions and assumptions:

- TX latency is the time taken for the data frame to move from the Avalon-ST interface to the PHY-side interface.
- RX latency is the time taken for the data frame to move from the PHY-side interface to the Avalon-ST interface.
- No backpressure on the Avalon-ST TX and RX interfaces.
- All options under **Legacy Ethernet 10G MAC interfaces**, that allow compatibility with the legacy MAC are disabled.

Table 9. TX and RX Latency Values for Intel Stratix 10 Devices

These latency values are MAC-only latencies and do not include the PHY latencies.

MAC Operating Mode	Speed	Latency (ns)		
		TX	RX	Total
10G	10 Gbps	28.8	41.6	70.4
1G/10G	1 Gbps	156	163.9	319.9
1G/2.5G/10G	1 Gbps	182.7	199.1	381.8
1G/2.5G/10G	2.5 Gbps	106	92.8	198.8
1G/2.5G/10G	10 Gbps	35.2	35.2	70.4
1G/2.5G	1 Gbps	235.2	222.4	457.6
1G/2.5G	2.5 Gbps	140.8	121.7	262.5
10M/100M/1G/10G	10 Mbps	1484.9	20827.7	22312.6
10M/100M/1G/10G	100 Mbps	245.3	2106.1	2351.4
10M/100M/1G/2.5G/5G/10G (USXGMII)	10 Gbps	28.8	41.6	70.4
10M/100M/1G/2.5G/5G/10G (USXGMII)	5 Gbps	41.6	67.2	108.8
10M/100M/1G/2.5G/5G/10G (USXGMII)	2.5 Gbps	57.6	118.4	176
10M/100M/1G/2.5G/5G/10G (USXGMII)	1 Gbps	137.6	272.0	409.6
10M/100M/1G/2.5G/5G/10G (USXGMII)	100 Mbps	1162	2576.8	3738.8
10M/100M/1G/2.5G/5G/10G (USXGMII)	10 Mbps	12365.5	25624.0	37989.5
10M/100M/1G/2.5G	100 M	1360	1664	3024
10M/100M/1G/2.5G	10 M	12561	17662	30223
10M/100M/1G/2.5G/10G	100 M	1289	1640	2929
10M/100M/1G/2.5G/10G	10 M	14230	17641	31871

Table 10. TX and RX Latency Values for Intel Arria 10 and Intel Cyclone 10 GX Devices

These latency values are MAC-only latencies and do not include the PHY latencies.

MAC Operating Mode	Speed	Latency (ns)		
		TX	RX	Total
10G	10 Gbps	22.4	38.4	60.8
1G/10G	1 Gbps	148	159	307
1G/2.5G/10G	1 Gbps	182.7	195.9	378.6
1G/2.5G/10G	2.5 Gbps	93.2	89.7	182.9
1G/2.5G/10G	10 Gbps	28.8	32	60.8
1G/2.5G	1 Gbps	238.4	219.2	457.6
1G/2.5G	2.5 Gbps	137.1	112.5	249.6

continued...

MAC Operating Mode	Speed	Latency (ns)		
		TX	RX	Total
10M/100M/1G/10G	10 Mbps	1492.9	20822.9	22315.8
10M/100M/1G/10G	100 Mbps	253.3	2104.5	2357.8
10M/100M/1G/2.5G/5G/10G (USXGMII)	10 Gbps	22.4	38.4	60.8
10M/100M/1G/2.5G/5G/10G (USXGMII)	5 Gbps	35.2	64	99.2
10M/100M/1G/2.5G/5G/10G (USXGMII)	2.5 Gbps	60.8	115.2	176.0
10M/100M/1G/2.5G/5G/10G (USXGMII)	1 Gbps	137.6	268.9	406.5
10M/100M/1G/2.5G/5G/10G (USXGMII)	100 Mbps	1162.0	2573.6	3735.6
10M/100M/1G/2.5G/5G/10G (USXGMII)	10 Mbps	12362.3	25620.8	37983.1
10M/100M/1G/2.5G	100 M	1360	1657.6	3017.6
10M/100M/1G/2.5G	10 M	12561	17656	30217
10M/100M/1G/2.5G/10G	100 M	1289	1637	2926
10M/100M/1G/2.5G/10G	10 M	14227	17638	31865

2. Getting Started

This chapter provides a general overview of the Intel FPGA IP core design flow to help you quickly get started with LL Ethernet 10G MAC.

2.1. Introduction to Intel FPGA IP Cores

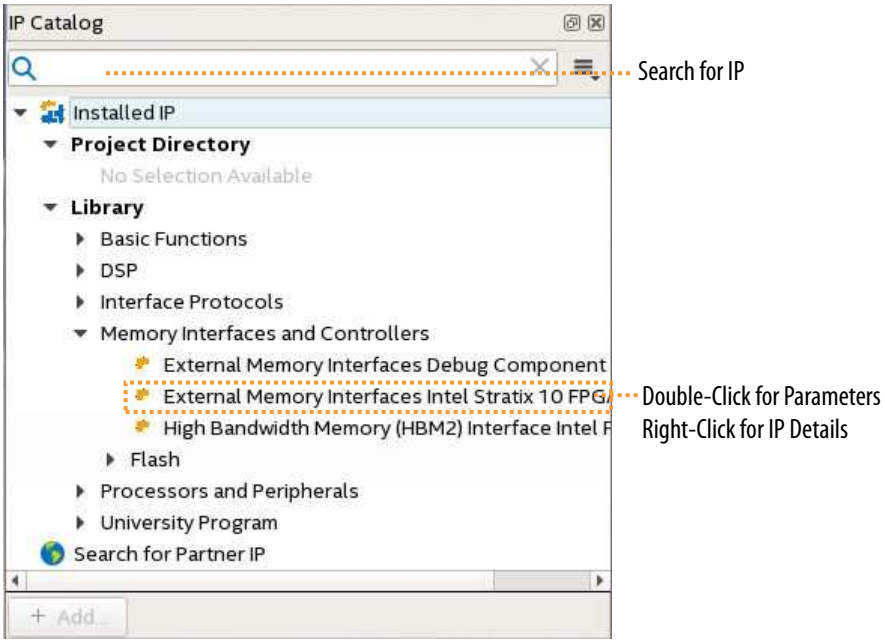
Intel and strategic IP partners offer a broad portfolio of configurable IP cores optimized for Intel FPGA devices.

The Intel Quartus Prime software installation includes the Intel FPGA IP library. Integrate optimized and verified Intel FPGA IP cores into your design to shorten design cycles and maximize performance. The Intel Quartus Prime software also supports integration of IP cores from other sources. Use the IP Catalog (**Tools ➤ IP Catalog**) to efficiently parameterize and generate synthesis and simulation files for your custom IP variation. The Intel FPGA IP library includes the following types of IP cores:

- Basic functions
- DSP functions
- Interface protocols
- Low power functions
- Memory interfaces and controllers
- Processors and peripherals

This document provides basic information about parameterizing, generating, upgrading, and simulating stand-alone IP cores in the Intel Quartus Prime software.

Figure 2. IP Catalog



2.2. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 3. IP Core Installation Path

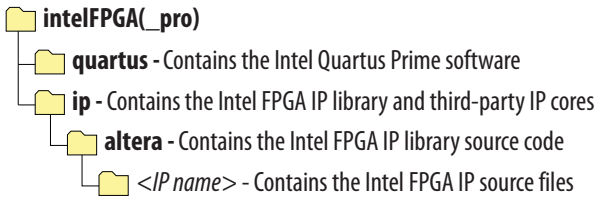


Table 11. IP Core Installation Locations

Location	Software	Platform
<*drive*>:\intelFPGA_pro\quartus\ip\altera	Intel Quartus Prime Pro Edition	Windows*
<*drive*>:\intelFPGA\quartus\ip\altera	Intel Quartus Prime Standard Edition	Windows
<*home directory*>:/intelFPGA_pro/quartus/ip/altera	Intel Quartus Prime Pro Edition	Linux*
<*home directory*>:/intelFPGA/quartus/ip/altera	Intel Quartus Prime Standard Edition	Linux

Note: The Intel Quartus Prime software does not support spaces in the installation path.

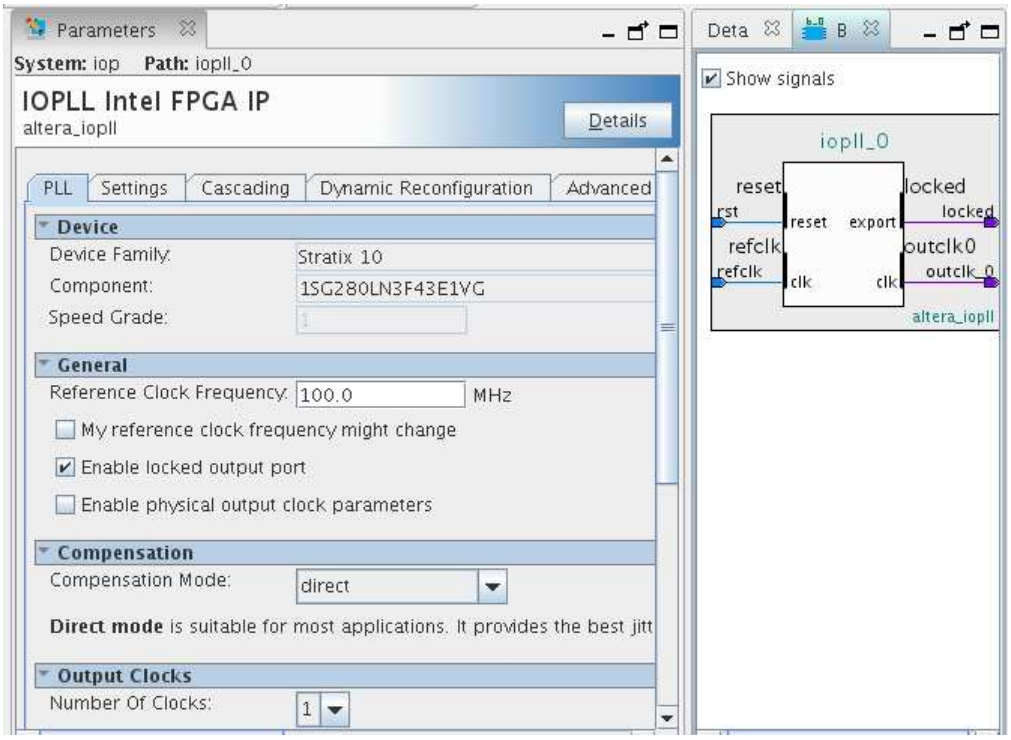
2.3. Generating IP Cores (Intel Quartus Prime Pro Edition)

Quickly configure Intel FPGA IP cores in the Intel Quartus Prime parameter editor. Double-click any component in the IP Catalog to launch the parameter editor. The parameter editor allows you to define a custom variation of the IP core. The parameter editor generates the IP variation synthesis and optional simulation files, and adds the `.ip` file representing the variation to your project automatically.

Follow these steps to locate, instantiate, and customize an IP core in the parameter editor:

1. Create or open an Intel Quartus Prime project (`.qpf`) to contain the instantiated IP variation.
2. In the IP Catalog (**Tools ➤ IP Catalog**), locate and double-click the name of the IP core to customize. To locate a specific component, type some or all of the component's name in the IP Catalog search box. The New IP Variation window appears.
3. Specify a top-level name for your custom IP variation. Do not include spaces in IP variation names or paths. The parameter editor saves the IP variation settings in a file named <*your_ip*>.ip. Click **OK**. The parameter editor appears.

Figure 4. IP Parameter Editor (Intel Quartus Prime Pro Edition)



4. Set the parameter values in the parameter editor and view the block diagram for the component. The **Parameterization Messages** tab at the bottom displays any errors in IP parameters:
   - Optionally, select preset parameter values if provided for your IP core. Presets specify initial parameter values for specific applications.
   - Specify parameters defining the IP core functionality, port configurations, and device-specific features.
   - Specify options for processing the IP core files in other EDA tools.

   Note: Refer to your IP core user guide for information about specific IP core parameters.
5. Click **Generate HDL**. The **Generation** dialog box appears.
6. Specify output file generation options, and then click **Generate**. The synthesis and simulation files generate according to your specifications.
7. To generate a simulation testbench, click **Generate ➤ Generate Testbench System**. Specify testbench generation options, and then click **Generate**.
8. To generate an HDL instantiation template that you can copy and paste into your text editor, click **Generate ➤ Show Instantiation Template**.
9. Click **Finish**. Click **Yes** if prompted to add files representing the IP variation to your project.
10. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

Note: Some IP cores generate different HDL implementations according to the IP core parameters. The underlying RTL of these IP cores contains a unique hash code that prevents module name collisions between different variations of the IP core. This unique code remains consistent, given the same IP settings and software version during IP generation. This unique code can change if you edit the IP core's parameters or upgrade the IP core version. To avoid dependency on these unique codes in your simulation environment, refer to *Generating a Combined Simulator Setup Script*.

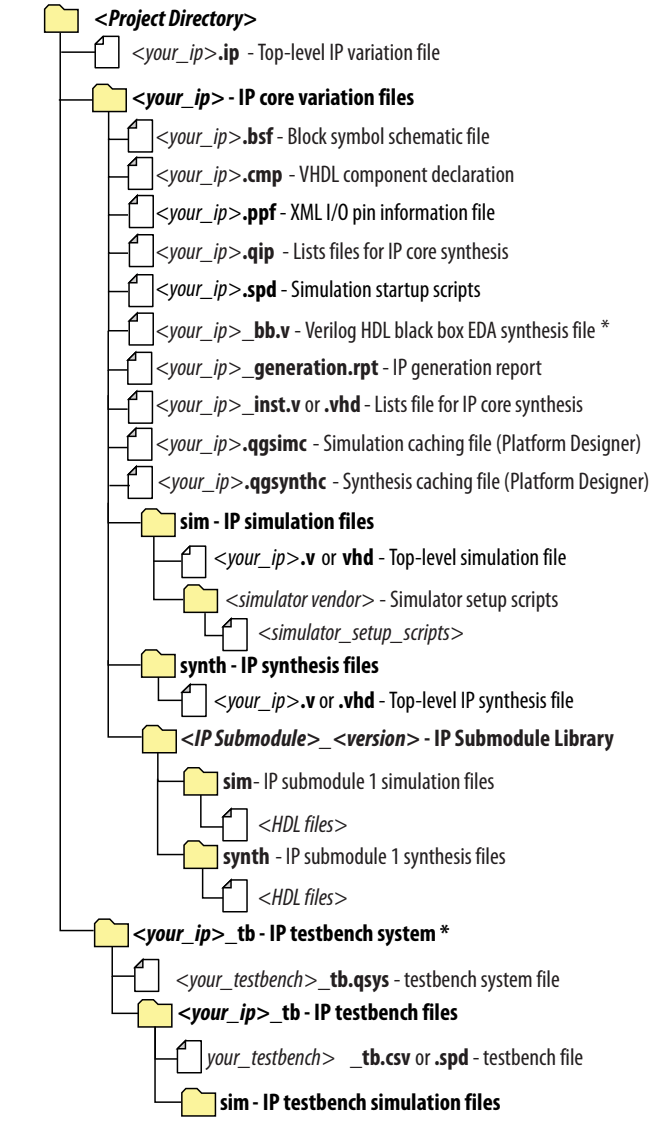
Related Information

- Low Latency Ethernet 10G MAC Intel Stratix 10 FPGA IP Design Example User Guide
- Low Latency Ethernet 10G MAC Intel Arria 10 FPGA IP Design Example User Guide
- Low Latency Ethernet 10G MAC Intel Cyclone 10 GX FPGA IP Design Example User Guide
- Intel FPGA IP Release Notes
- IP User Guide Documentation

2.4. IP Core Generation Output (Intel Quartus Prime Pro Edition)

The Intel Quartus Prime software generates the following output file structure for individual IP cores that are not part of a Platform Designer system.

Figure 5. Individual IP Core Generation Output (Intel Quartus Prime Pro Edition)



* If supported and enabled for your IP core variation.

Table 12. Output Files of Intel FPGA IP Generation

File Name	Description
<your_ip>.ip	Top-level IP variation file that contains the parameterization of an IP core in your project. If the IP variation is part of a Platform Designer system, the parameter editor also generates a .qsys file.
<your_ip>.cmp	The VHDL Component Declaration (.cmp) file is a text file that contains local generic and port definitions that you use in VHDL design files.
<your_ip>_generation.rpt	IP or Platform Designer generation log file. Displays a summary of the messages during IP generation.

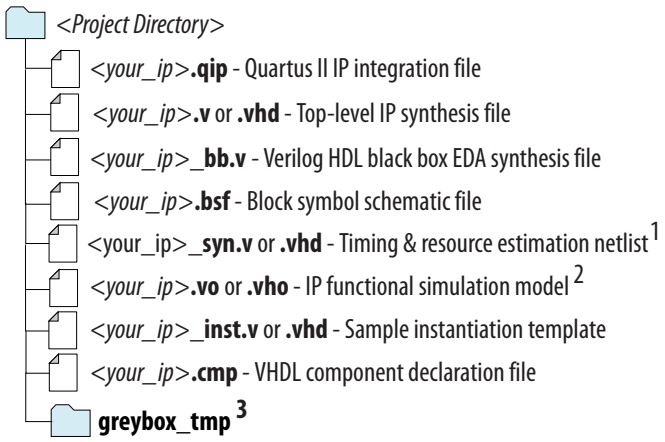
continued...

File Name	Description
<*your_ip*>.qgsimc (Platform Designer systems only)	Simulation caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.
<*your_ip*>.qgsynth (Platform Designer systems only)	Synthesis caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.
<*your_ip*>.qip	Contains all information to integrate and compile the IP component.
<*your_ip*>.csv	Contains information about the upgrade status of the IP component.
<*your_ip*>.bsf	A symbol representation of the IP variation for use in Block Diagram Files (.bdf).
<*your_ip*>.spd	Input file that ip-make-simscript requires to generate simulation scripts. The .spd file contains a list of files you generate for simulation, along with information about memories that you initialize.
<*your_ip*>.ppf	The Pin Planner File (.ppf) stores the port and node assignments for IP components you create for use with the Pin Planner.
<*your_ip*>_bb.v	Use the Verilog blackbox (_bb.v) file as an empty module declaration for use as a blackbox.
<*your_ip*>_inst.v or _inst.vhd	HDL example instantiation template. Copy and paste the contents of this file into your HDL file to instantiate the IP variation.
<*your_ip*>.regmap	If the IP contains register information, the Intel Quartus Prime software generates the .regmap file. The .regmap file describes the register map information of master and slave interfaces. This file complements the .sopcinfo file by providing more detailed register information about the system. This file enables register display views and user customizable statistics in System Console.
<*your_ip*>.svd	Allows HPS System Debug tools to view the register maps of peripherals that connect to HPS within a Platform Designer system. During synthesis, the Intel Quartus Prime software stores the .svd files for slave interface visible to the System Console masters in the .sof file in the debug session. System Console reads this section, which Platform Designer queries for register map information. For system slaves, Platform Designer accesses the registers by name.
<*your_ip*>.v <*your_ip*>.vhd	HDL files that instantiate each submodule or child IP core for synthesis or simulation.
mentor/	Contains a msim_setup.tcl script to set up and run a simulation.
aldec/	Contains a script riviera pro_setup.tcl to setup and run a simulation.
/synopsys/vcs /synopsys/vcsmx	Contains a shell script vcs_setup.sh to set up and run a simulation. Contains a shell script vcsmx_setup.sh and synopsys_sim.setup file to set up and run a simulation.
/cadence	Contains a shell script ncsim_setup.sh and other setup files to set up and run an simulation.
/xcelium	Contains an Parallel simulator shell script xcelium_setup.sh and other setup files to set up and run a simulation.
/submodules	Contains HDL files for the IP core submodule.
<*IP submodule*>/	Platform Designer generates /synth and /sim sub-directories for each IP submodule directory that Platform Designer generates.

2.5. Files Generated for Intel IP Cores (Legacy Parameter Editor)

The Intel Quartus Prime generates the following output for IP cores that use the legacy MegaWizard parameter editor.

Figure 6. IP Core Generated Files



Notes:
1. If supported and enabled for your IP variation
2. If functional simulation models are generated
3. Ignore this directory

2.6. Simulating Intel FPGA IP Cores

The Intel Quartus Prime software supports IP core RTL simulation in specific EDA simulators. IP generation creates simulation files, including the functional simulation model, any testbench (or example design), and vendor-specific simulator setup scripts for each IP core. Use the functional simulation model and any testbench or example design for simulation. IP generation output may also include scripts to compile and run any testbench. The scripts list all models or libraries you require to simulate your IP core.

The Intel Quartus Prime software provides integration with many simulators and supports multiple simulation flows, including your own scripted and custom simulation flows. Whichever flow you choose, IP core simulation involves the following steps:

1. Generate simulation model, testbench (or example design), and simulator setup script files.
2. Set up your simulator environment and any simulation scripts.
3. Compile simulation model libraries.
4. Run your simulator.