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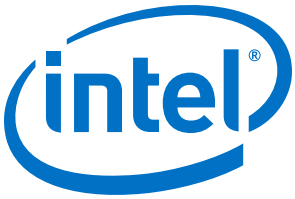

HDMI Intel® FPGA IP User Guide

Updated for Intel® Quartus® Prime Design Suite: **18.0**

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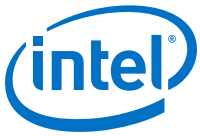


1. HDMI Intel® FPGA Quick Reference

The Intel® FPGA High-Definition Multimedia Interface (HDMI) IP core provides support for next-generation video display interface technology. The HDMI Intel FPGA IP core is part of the Intel FPGA IP Library, which is distributed with the Intel Quartus® Prime software and downloadable from www.altera.com.

Information		Description
Release Information	Version	18.0
	Release	May 2018
	Ordering Code	IP-HDMI
IP Core Information	Core Features	• Conforms to the *High-Definition Multimedia Interface (HDMI) Specification versions 1.4 and 2.0b* • Supports transmitter and receiver on a single device transceiver quad • Supports pixel frequency up to 600 MHz • Supports RGB and YCbCr 444, 422, and 420 color modes • Accepts standard H-SYNC, V-SYNC, data enable, RGB video format, and YCbCr video format • Supports up to 32 audio channels in 2-channel and 8-channel layouts. • Supports 1, 2, or 4 symbols per clock • Supports 8, 10, 12, or 16 bits per component (bpc) • Supports single link Digital Visual Interface (DVI) • Supports High Dynamic Range (HDR) InfoFrame insertion and filter through the provided design examples • Supports up to 1,536 kHz audio sample frequency
	Typical Application	• Interfaces within a PC and monitor • External display connections, including interfaces between a PC and monitor or projector, between a PC and TV, or between a device such as a DVD player and TV display
	Device Family	Supports Intel Stratix® 10 (H-Tile), Intel Arria® 10, Intel Cyclone® 10 GX, Arria V, and Stratix V FPGA devices
	Design Tools	• Intel Quartus Prime software for IP design instantiation and compilation • Timing Analyzer in the Intel Quartus Prime software for timing analysis • ModelSim* - Intel FPGA Edition or ModelSim - Intel FPGA Starter Edition, NCSim, Riviera-PRO*, VCS*, VCS MX, and Xcelium* Parallel software for design simulation

Related Information

- HDMI Intel Arria 10 FPGA IP Design Example User Guide
  For more information about the Intel Arria 10 design examples.
- HDMI Intel Cyclone 10 GX FPGA IP Design Example User Guide
  For more information about the Intel Cyclone 10 GX design examples.

- HDMI Intel Stratix 10 FPGA IP Design Example User Guide
  For more information about the Intel Stratix 10 design examples.
- HDMI Intel FPGA IP Core User Guide Archives on page 81
  Provides a list of user guides for previous versions of the HDMI Intel FPGA IP.

2. HDMI Overview

The HDMI Intel FPGA IP core provides support for next generation video display interface technology.

The HDMI standard specifies a digital communications interface for use in both internal and external connections:

- Internal connections—interface within a PC and monitor
- External display connections—interface between a PC and monitor or projector, between a PC and TV, or between a device such a DVD player and TV display.

The HDMI system architecture consists of sinks and sources. A device may have one or more HDMI inputs and outputs.

The HDMI cable and connectors carry four differential pairs that make up the Transition Minimized Differential Signaling (TMDS) data and clock channels. You can use these channels to carry video, audio, and auxiliary data.

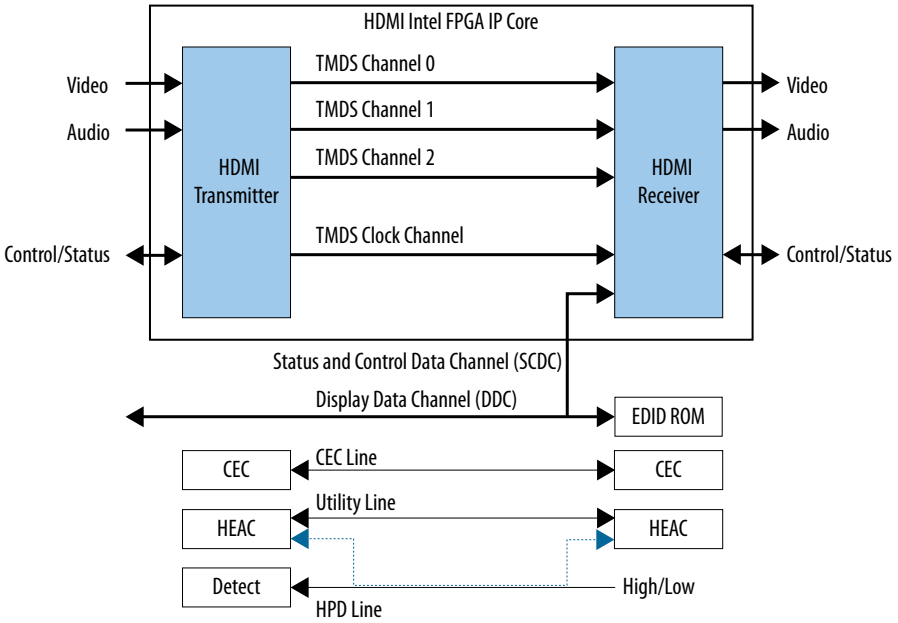
The HDMI also carries a Video Electronics Standards Association (VESA) Display Data Channel (DDC) and Status and Control Data Channel (SCDC). The DDC configures and exchanges status between a single source and a single sink. The source uses the DDC to read the sink's Enhanced Extended Display Identification Data (E-EDID) to discover the sink's configuration and capabilities.

The optional Consumer Electronics Control (CEC) protocol provides high-level control functions between various audio visual products in your environment.

The optional HDMI Ethernet and Audio Return Channel (HEAC) provides Ethernet compatible data networking between connected devices and an audio return channel in the opposite direction of TMDS. The HEAC also uses Hot-Plug Detect (HPD) line for signal transmission.

Figure 1. HDMI Intel FPGA Core Block Diagram

The figure below illustrates the blocks in the HDMI Intel FPGA IP core.



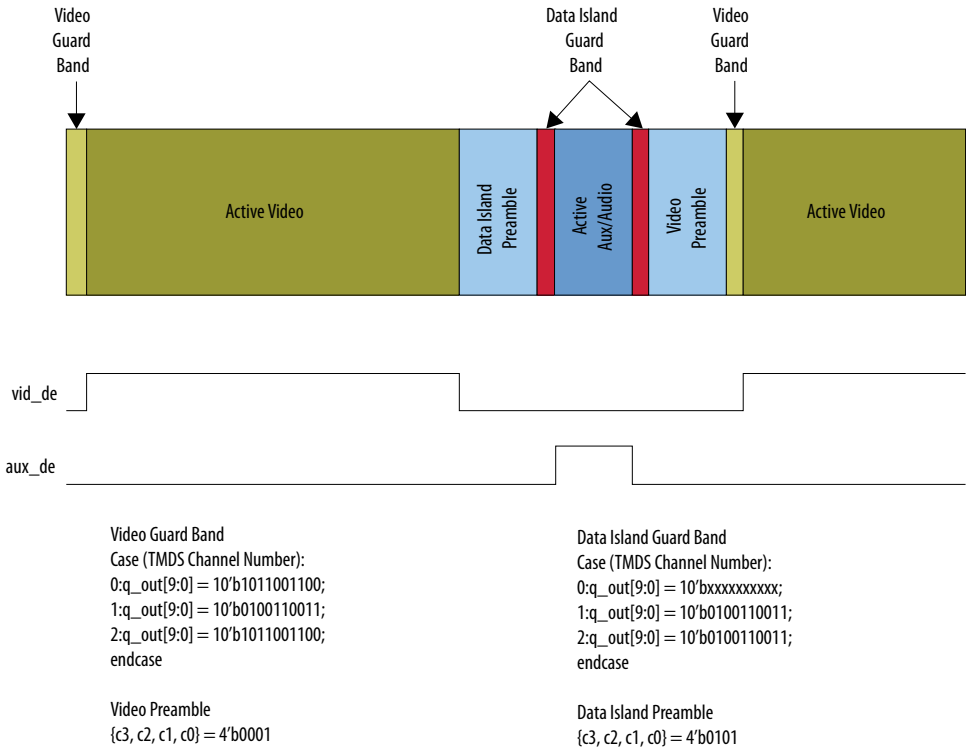
Based on TMDS encoding, the HDMI protocol allows the transmission of both audio and video data between source and sink devices.

An HDMI interface consists of three color channels accompanied by a single clock channel. You can use each color line to transfer both individual RGB colors and auxiliary data.

The receiver uses the TMDS clock as a frequency reference for data recovery on the three TMDS data channels. This clock typically runs at the video pixel rate.

TMDS encoding is based on an 8-bit to 10-bit algorithm. This protocol attempts to minimize data channel transition, and yet maintain sufficient transition so that a sink device can lock reliably to the data stream.

Figure 2. HDMI Intel FPGA Video Stream Data



The figure above illustrates two data streams:

- Data stream in green—transports color data
- Data stream in dark blue—transports auxiliary data

Table 1. Video Data and Auxiliary Data

The table below describes the function of the video data and auxiliary data.

Data	Description
Video data	• Packed representation of the video pixels clocked at the source pixel clock. • Encoded using the TMDS 8-bit to 10-bit algorithm.
Auxiliary data	• Transfers audio data together with a range of auxiliary data packets. • Sink devices use auxiliary data packets to correctly reconstruct video and audio data. • Encoded using the TMDS Error Reduction Coding–4 bits (TERC4) encoding algorithm.

Each data stream section is preceded with guard bands and pre-ambles. The guard bands and pre-ambles allow for accurate synchronization with received data streams.

The following figures show the arrangement of the video data, video data enable, video H-SYNC, and video V-SYNC in 1, 2, and 4 symbols per clock.

Figure 3. Video Data, Video Data Valid, H-SYNC, and V-SYNC—1 Symbol per Clock

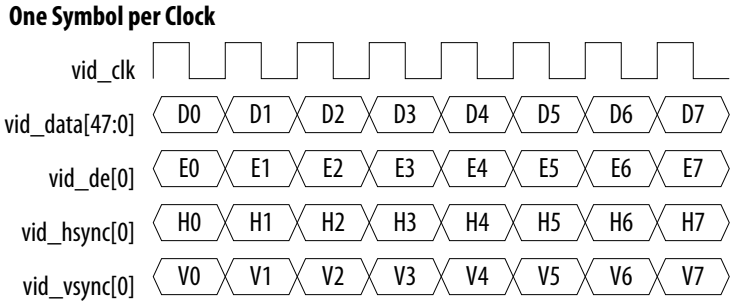


Figure 4. Video Data, Video Data Valid, H-SYNC, and V-SYNC—2 Symbols per Clock

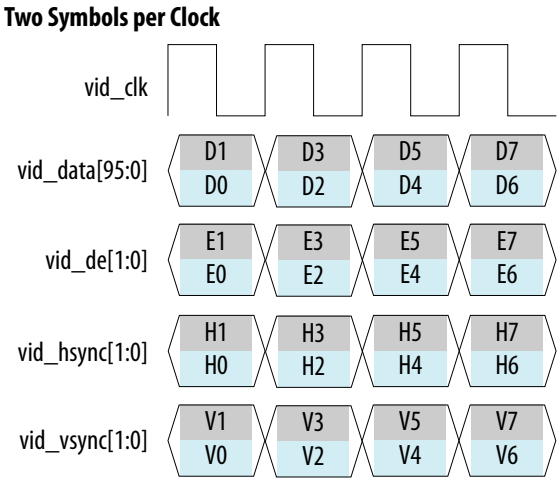
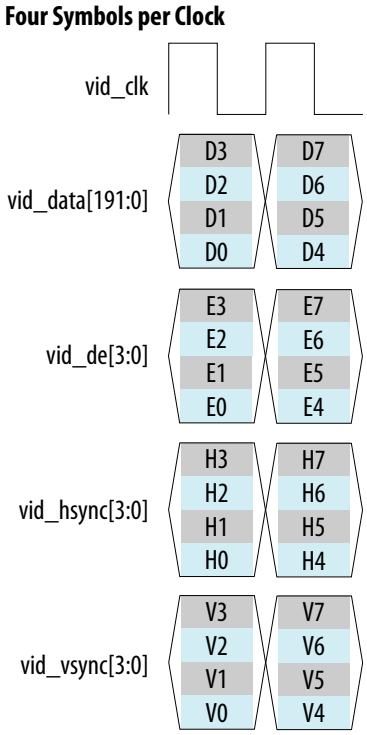


Figure 5. Video Data, Video Data Valid, H-SYNC, and V-SYNC—4 Symbols per Clock



2.1. Device Family Support

Table 2. Intel Device Family Support

Device Family	Support Level
Intel Stratix 10 (H-Tile)	Preliminary
Intel Arria 10	Final
Intel Cyclone 10 GX	Final
Arria V	Final
Stratix V	Final

The following terms define device support levels for Intel FPGA IP cores:

- Advance support—the IP core is available for simulation and compilation for this device family. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
- Preliminary support—the IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.
- Final support—the IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

2.2. Resource Utilization

The resource utilization data indicates typical expected performance for the HDMI Intel FPGA IP core.

Table 3. HDMI Data Rate

The table lists the maximum data rates for HDMI Intel FPGA IP core configurations of 1, 2, and 4 symbols per clock.

Devices	Maximum Data Rate (Mbps)		
	1 Symbol per Clock	2 Symbols per Clock	4 Symbols per Clock
Intel Stratix 10	Not Supported	5,940 (Example: 4Kp60 8 bpc)	Not Supported
Intel Arria 10	Not Supported	5,940 (Example: 4Kp60 8 bpc)	Not Supported
Intel Cyclone 10 GX	Not Supported	5,940 (Example: 4Kp60 8 bpc)	Not Supported
Arria V GX	1,875 (Example: 1080p60 10 bpc)	3,276.8 (Example: 4Kp30 8 bpc)	5,940 (Example: 4Kp60 8 bpc)
Stratix V	2,970 (Example: 4Kp30 8 bpc)	5,940 (Example: 4Kp60 8 bpc)	Not Supported

Table 4. Color Depth Supported for Each Pixel Encoding

Pixel Encoding	Color Depth			
	8	10	12	16
RGB	Yes	Yes	Yes	Yes
YCbCr 4:4:4	Yes	Yes	Yes	Yes
YCbCr 4:2:2(1)	Not applicable	Not applicable	Yes	Not applicable
YCbCr 4:2:0	Yes	Yes	Yes	Yes

Table 5. HDMI Intel FPGA Resource Utilization

The table lists the performance data for the different Intel FPGA devices.

Device	Symbols per Clock	Direction	ALMs	Logic Registers		Memory	
				Primary	Secondary	Bits	M10K or M20K
Intel Stratix 10	2	RX	4,083	5,663	984	38,400	14
	2	TX	4,677	7,497	1,704	37,568	13
Intel Arria 10	2	RX	3,359	4,276	795	38,400	14
	2	TX	3,374	5,014	1,543	12,680	13
Intel Cyclone 10 GX	2	RX	2,933	4,595	779	38,400	14
	2	TX	2,901	5,220	1,429	20,776	13
Arria V GX	1	RX	2,630	4,039	402	35,712	13
	1	TX	2,700	4,462	417	11,108	11
	2	RX	3,446	4,656	531	38,400	14
	2	TX	3,759	6,091	450	12,680	13
	4	RX	4,895	5,937	614	43,776	20
	4	TX	6,135	9,156	445	15,824	18
Stratix V	1	RX	2,592	3,946	398	35,712	13
	1	TX	2,634	4,415	461	11,108	11
	2	RX	3,337	4,619	440	38,400	14
	2	TX	3,644	5,919	680	12,680	13

Table 6. Recommended Speed Grades for Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX Devices

Device	Lane Rate (Mbps)	Interface Width (bits)	Speed Grades
Intel Stratix 10	6,000	20	-1, -2
Intel Arria 10	6,000	20	-1, -2
Intel Cyclone 10 GX	6,000	20	-5

(1) According to *HDMI 1.4b Specification Section 6.5.1*, 8 and 10 bpc use the same pixel encoding as 12 bpc, but the valid bits are left-justified with zeros padding the bits below the least significant bit.

3. HDMI Intel FPGA Getting Started

This chapter provides a general overview of the Intel IP core design flow to help you quickly get started with the HDMI Intel FPGA IP core. The Intel FPGA IP Library is installed as part of the Intel Quartus Prime installation process. You can select and parameterize any Intel FPGA IP core from the library. Intel provides an integrated parameter editor that allows you to customize the HDMI Intel FPGA IP core to support a wide variety of applications. The parameter editor guides you through the setting of parameter values and selection of optional ports.

Related Information

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Platform Designer Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

3.1. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 6. IP Core Installation Path

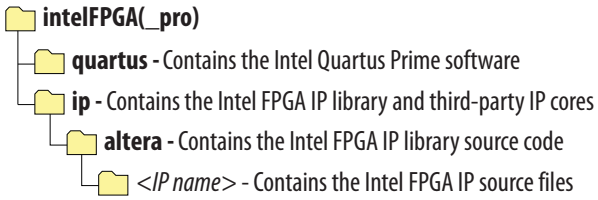


Table 7. IP Core Installation Locations

Location	Software	Platform
<*drive*>:\intelFPGA_pro\quartus\ip\altera	Intel Quartus Prime Pro Edition	Windows*
<*drive*>:\intelFPGA\quartus\ip\altera	Intel Quartus Prime Standard Edition	Windows
<*home directory*>:/intelFPGA_pro/quartus/ip/altera	Intel Quartus Prime Pro Edition	Linux*
<*home directory*>:/intelFPGA/quartus/ip/altera	Intel Quartus Prime Standard Edition	Linux

3.1.1. Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

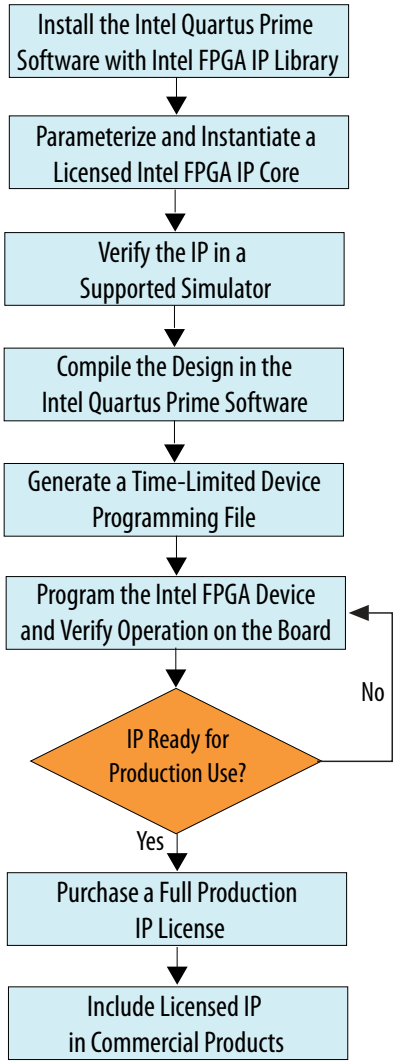
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (<*project name*>_time_limited.sof) that expires at the time limit.

Figure 7. Intel FPGA IP Evaluation Mode Flow



Note: Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the Self-Service Licensing Center or contact your local Intel FPGA representative.

The Intel FPGA Software License Agreements govern the installation and use of licensed IP cores, the Intel Quartus Prime design software, and all unlicensed IP cores.

Related Information

- Intel Quartus Prime Licensing Site
- Intel FPGA Software Installation and Licensing

3.2. Specifying IP Core Parameters and Options

Follow these steps to specify the HDMI Intel FPGA IP core parameters and options.

1. Create a Intel Quartus Prime project using the **New Project Wizard** available from the File menu.
2. On the **Tools** menu, click **IP Catalog**.
3. Under **Installed IP**, double-click **Library ➤ Interface ➤ Protocols ➤ Audio&Video ➤ HDMI Intel FPGA**.
   The parameter editor appears.
4. Specify a top-level name for your custom IP variation. This name identifies the IP core variation files in your project. If prompted, also specify the targeted FPGA device family and output file HDL preference. Click **OK**.
5. Specify parameters and options in the HDMI parameter editor:
   - Optionally select preset parameter values. Presets specify all initial parameter values for specific applications (where provided).
   - Specify parameters defining the IP core functionality, port configurations, and device-specific features.
   - Specify options for generation of a timing netlist, simulation model, testbench, or example design (where applicable).
   - Specify options for processing the IP core files in other EDA tools.
6. Click **Generate** to generate the IP core and supporting files, including simulation models.
7. Click **Close** when file generation completes.
8. Click **Finish**.
9. If you generate the HDMI Intel FPGA IP core instance in a Intel Quartus Prime project, you are prompted to add `Intel Quartus Prime IP File (.qip)` and `Intel Quartus Prime Simulation IP File (.sip)` to the current Intel Quartus Prime project.

4. HDMI Hardware Design Examples

Intel offers design examples that you can simulate, compile, and test in hardware.

The implementation of the HDMI Intel FPGA IP on hardware requires additional components specific to the targeted device.

4.1. HDMI Hardware Design Examples for Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 Devices

The HDMI Intel FPGA IP core offers design examples that you can generate through the IP catalog in the Intel Quartus Prime Pro Edition software.

Related Information

- HDMI Intel Arria 10 FPGA IP Design Example User Guide
  For more information about the Intel Arria 10 design examples.
- HDMI Intel Cyclone 10 GX FPGA IP Design Example User Guide
  For more information about the Intel Cyclone 10 GX design examples.
- HDMI Intel Stratix 10 FPGA IP Design Example User Guide
  For more information about the Intel Stratix 10 design examples.

4.2. HDMI Hardware Design Examples for Arria V and Stratix V Devices

The HDMI hardware design example helps you evaluate the functionality of the HDMI Intel FPGA IP core and provides a starting point for you to create your own design for Arria V and Stratix V devices.

The design example runs on the following device kits:

- Arria V GX starter kit
- Stratix V GX development kit
- Bitec HDMI HSMC 2.0 Daughter Card Revision 8

Related Information

AN 837: Design Guidelines for Intel FPGA HDMI

4.2.1. HDMI Hardware Design Components

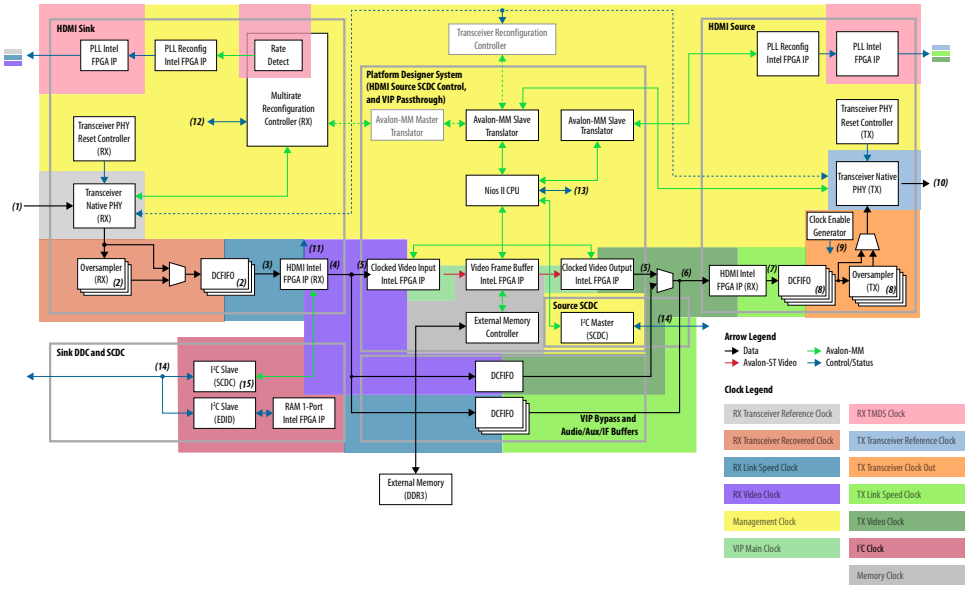
The demonstration designs instantiate the Video and Image Processing (VIP) Suite IP cores or FIFO buffers to perform a direct HDMI video stream passthrough between the HDMI sink and source.

The hardware demonstration design comprises the following components:

- HDMI sink
  - Transceiver Native PHY (RX)
  - Transceiver PHY Reset Controller (RX)
  - PLL
  - PLL Reconfiguration
  - Multirate Reconfiguration Controller (RX)
  - Oversampler (RX)
  - DCFIFO
- Sink Display Data Channel (DDC) and Status and Control Data Channel (SCDC)
- Transceiver Reconfiguration Controller
- VIP bypass and Audio, Auxiliary and InfoFrame buffers
- Platform Designer system
  - VIP passthrough for HDMI video stream
  - Source SCDC controller
  - HDMI source reconfiguration controller
- HDMI source
  - Transceiver Native PHY (TX)
  - Transceiver fPLL
  - Transceiver PHY Reset Controller (TX)
  - PLL
  - PLL Reconfiguration
  - Oversampler (TX)
  - DCFIFO
  - Clock Enable Generator

Figure 8. HDMI Hardware Design Example Block Diagram

The figure below shows a high level architecture of the design.



The following details of the design example architecture correspond to the numbers in the block diagram.

1. The sink TMDS data has three channels: data channel 0 (blue), data channel 1 (green), and data channel 2 (red).
2. The Oversampler (RX) and dual-clock FIFO (DCFIFO) instances are duplicated for each TMDS data channel (0,1,2).
3. The video data input width for each color channel of the HDMI RX core is equivalent to RX transceiver PCS-PLD parallel data width per channel.
4. Each color channel is fixed at 16 bpc. The video data output width of the HDMI RX core is equivalent to the value of symbols per clock*16*3.
5. The video data input width of the Clocked Video Input (CVI) and Clocked Video Output (CVO) IP cores are equivalent to the value of NUMBER_OF_PIXELS_IN_PARALLEL * BITS_PER_PIXEL_PER_COLOR_PLANE * NUMBER_OF_COLOR_PLANES. To interface with the HDMI core, the values of NUMBER_OF_PIXELS_IN_PARALLEL, BITS_PER_PIXEL_PER_COLOR_PLANE, and NUMBER_OF_COLOR_PLANES must match the symbols per clock, 16 and 3 respectively.
6. The video data input width of the HDMI TX core is equivalent to the value of symbols per clock*16*3. You can use the user switch to select the video data from the CVO IP core (VIP passthrough) or DCFIFO (VIP bypass).
7. The video data output width for each color channel of the HDMI TX core is equivalent to TX transceiver PCS-PLD parallel data width per channel.
8. The DCFIFO and the Oversampler (TX) instances are duplicated for each TMDS data channel (0,1,2) and clock channel.
9. The Oversampler (TX) uses the clock enable signal to read data from the DCFIFO.
10. The source TMDS data has four channels: data channel 0 (blue), data channel 1 (green), data channel 2 (red), and clock channel.

11. The RX Multirate Reconfiguration Controller requires the status of `TMDS_Bit_clock_Ratio` port to perform appropriate RX reconfiguration between the TMDS character rates below 340 Mcsc (HDMI 1.4b) and above 340 Mcsc (HDMI 2.0b). The status of the port is also required by the Nios II processor and the HDMI TX core to perform appropriate TX reconfiguration and scrambling.
12. The reset control and lock status signals from HDMI PLL, RX Transceiver Reset Controller and HDMI RX core.
13. The reset and oversampling control signals for HDMI PLL, TX Transceiver Reset Controller, and HDMI TX core. The lock status and rate detection measure valid signals from the HDMI sink initiate the TX reconfiguration process.
14. The I^2C SCL and SDA lines with tristate buffer for bidirectional configuration. Use the ALTIOBUF IP core for Arria V and Stratix V devices.
15. The SCDC is mainly designed for the source to update the `TMDS_Bit_Clock_Ratio` and `Scrambler_Enable` bits of the sink TMDS Configuration register. .

4.2.1.1. Transceiver Native PHY (RX)

- Transceiver Native PHY in Arria V devices
  - To operate the TMDS bit rate up to 3,400 Mbps, configure the Transceiver Native PHY at 20 bits at PCS – PLD interface with the HDMI RX core at 2 symbols per clock. When the PCS – PLD interface width is 20 bits, the minimum link rate is 611 Mbps.
  - To operate the TMDS bit rate up to 6,000 Mbps, configure the Transceiver Native PHY at 40 bits with the HDMI RX core at 4 symbols per clock. When the PCS – PLD interface width is 40 bits, the minimum link rate is 1,000 Mbps.
  - Oversampling is required for TMDS bit rate which is below the minimum link rate.
- Transceiver Native PHY in Stratix V devices
  - To operate the TMDS bit rate up to 6,000 Mbps, configure the Transceiver Native PHY at 20 bits at PCS – PLD interface with the HDMI RX core at 2 symbols per clock. When the PCS – PLD interface width is 20 bits, the minimum link rate is 611 Mbps.

Table 8. Arria V and Stratix V Transceiver Native PHY (RX) Configuration Settings (6,000 Mbps)

This table shows an example of Arria V and Stratix V Transceiver Native PHY (RX) configuration settings for TMDS bit rate of 6,000 Mbps.

Parameters	Settings
Datapath Options	
Enable TX datapath	Off
Enable RX datapath	On
Enable Standard PCS	On
Initial PCS datapath selection	Standard
Number of data channels	3
Enable simplified data interface	On

RX PMA	
Data rate	6,000 Mbps
Enable CDR dynamic reconfiguration	On
Number of CDR reference clocks	2 (2)
Selected CDR reference clock	0 (2)
Selected CDR reference clock frequency	600 MHz
PPM detector threshold	1,000 PPM
Enable rx_pma_clkout port	On
Enable rx_is_lockedtodata port	On
Enable rx_is_lockedtoref port	On
Enable rx_set_locktodata and rx_set_locktoref ports	On

Standard PCS	
Standard PCS protocol	Basic
Standard PCS/PMA interface width	• 10 (for 1 symbol per clock) • 20 (for 2 and 4 symbols per clock)
Enable RX byte deserializer	• Off (for 1 and 2 symbols per clock) • On (for 4 symbols per clock)

(2) The Bitec HDMI HSMC 2.0 daughter card routes the TMDS clock pin to the transceiver serial data pin. To use the TMDS clock to drive the HDMI PLL, the TMDS clock must also drive the transceiver dedicated reference clock pin. The number of CDR reference clocks is 2 with reference clock 1 (unused) driven by the TMDS clock and reference clock 0 driven by the HDMI PLL output clock. The selected CDR reference clock will be fixed at 0.

Table 9. Arria V and Stratix V Transceiver Native PHY (RX) Common Interface Ports

This table describes the Arria V and Stratix V Transceiver Native PHY (RX) common interface ports.

Signals	Direction	Description
Clocks		
rx_cdr_refclk[1:0]	Input	Input reference clock for the RX CDR circuitry. • To support arbitrary wide data rate range from 250 Mbps to 6,000 Mbps, you need a generic core PLL to obtain a higher clock frequency from the TMDS clock. You need a higher clock frequency to create oversampled stream for data rates below the minimum transceiver data rate—for example, 611 Mbps or 1,000 Mbps). • If the TMDS clock pin is routed to the transceiver dedicated reference clock pin, you only need to create one transceiver reference clock input. You can use the TMDS clock as reference clock for a generic core PLL to drive the transceiver. • If you use Bitec HDMI HSMC 2.0 daughter card, the TMDS clock pin is routed to the transceiver serial data pin. In this case, to use the TMDS clock as a reference clock for a generic core PLL, the clock must also drive the transceiver dedicated reference clock. Connect bit 0 to the generic core PLL output and bit 1 to the TMDS clock and set the selected CDR reference clock at 0.
rx_std_clkout[2:0]	Output	RX parallel clock output. • The CDR circuitry recovers the RX parallel clock from the RX data stream when the CDR is configured at lock-to-data mode. • The RX parallel clock is a mirror of the CDR reference clock when the CDR is configured at lock-to-reference mode.
rx_std_coreclkin[2:0]	Input	RX parallel clock that drives the read side of the RX phase compensation FIFO. Connect to rx_std_clkout ports.
rx_pma_clkout[2:0]	Output	RX parallel clock (recovered clock) output from PMA. Leave unconnected.
Resets		
rx_analogreset[2:0]	Input	Active-high, edge-sensitive, asynchronous reset signal. When asserted, resets the RX CDR circuit, deserializer. Connect to Transceiver PHY Reset Controller IP core.
rx_digitalreset[2:0]	Input	Active-high, edge-sensitive, asynchronous reset signal. When asserted, resets the digital component of the RX data path. Connect to the Transceiver PHY Reset Controller IP core.
PMA Ports		
rx_set_locktoref[2:0]	Input	When asserted, programs the RX CDR to lock to reference mode manually. The lock to reference mode enables you to control the reset sequence using rx_set_locktoref and rx_set_locktodata. The Multirate Reconfiguration Controller (RX) sets this port to 1 if oversampling mode is required. Otherwise, this port is set to 0.

continued...

PMA Ports		
		Refer "Transceiver Reset Sequence" in Transceiver Reset Control in Arria V/Stratix V Devices for more information about manual control of the reset sequence.
`rx_set_locktodata[2:0]`	Input	Always driven to 0. When `rx_set_locktoref` is driven to 1, the CDR is configured to `lock-to-reference` mode. Otherwise, the CDR is configured to `lock-to-data` mode.
`rx_is_lockedtoref[2:0]`	Output	When asserted, the CDR is locked to the incoming reference clock. Connect this port to `rx_is_lockedtodata` port of the Transceiver PHY Reset Controller IP core when `rx_set_locktoref` is 1.
`rx_is_lockedtodata[2:0]`	Output	When asserted, the CDR is locked to the incoming data. Connect this port to `rx_is_lockedtodata` port of Transceiver PHY Reset Controller IP core when `rx_set_locktoref` is 0.
`rx_serial_data[2:0]`	Input	RX differential serial input data.

PCS Ports		
`unused_rx_parallel_data`	Output	Leave unconnected.
`rx_parallel_data[S*3*10-1:0]`	Output	PCS RX parallel data. *Note:* S=Symbols per clock.

Calibration Status Port		
`rx_cal_busy[2:0]`	Output	When asserted, indicates that the initial RX calibration is in progress. This port is also asserted if the reconfiguration controller is reset. Connect to the Transceiver PHY Reset Controller IP core.

Reconfiguration Ports		
`reconfig_to_xcvr[209:0]`	Input	Reconfiguration signals from the Transceiver Reconfiguration Controller.
`reconfig_from_xcvr[137:0]`	Output	Reconfiguration signals to the Transceiver Reconfiguration Controller.

4.2.1.2. PLL Intel FPGA IP Cores

Use the PLL Intel FPGA IP core as the HDMI PLL to generate reference clock for RX or TX transceiver, link speed, and video clocks for the HDMI RX or TX IP core.

The HDMI PLL is referenced by the arbitrary TMDS clock. For HDMI source, you can reference the HDMI PLL by a separate clock source in the VIP passthrough design, which contains frame buffer. The HDMI PLL for TX has the same desired output frequencies as RX across symbols per clock and color depth.

- For TMDS bit rates ranging from 3,400 Mbps to 6,000 Mbps (HDMI 2.0), the TMDS clock rate is 1/40 of the TMDS bit rate. The HDMI PLL generates reference clock for RX/TX transceiver at 4 times the TMDS clock.
- For TMDS bit rates below 3,400 Mbps (HDMI 1.4b), the TMDS clock rate is 1/10 of the TMDS bit rate. The HDMI PLL generates reference clock for RX/TX transceiver at identical rate as the TMDS clock.

If the TMDS link operates at TMDS bit rates below the minimum RX/TX transceiver link rate, your design requires oversampling and a factor of 5 is chosen. The minimum link rate of the RX/TX transceiver vary across device families and symbols per clock. The HDMI PLL generates reference clock for RX/TX transceiver at 5 times the TMDS clock.

Note: Place the PLL Intel FPGA block on the transmit path (`pll_hdmi_tx`) in the physical location next to the transceiver PLL.

Table 10. HDMI PLL Desired Output Frequencies for 8-bpc Video

This table shows an example of HDMI PLL desired output frequencies across various TMDS clock rates and symbols per clock for all supported device families using 8-bpc video.

Device Family	Symbols Per Clock	Minimum Link Rate (Mbps)	TMDS Bit Rate (Mbps)	Oversampling (5x) Required	TMDS Clock Rate (MHz)	RX/TX Transceiver Refclk (MHz)	RX/TX Link Speed Clock (MHz)	RX/TX Video Clock (MHz)
Arria V	2	611	270	Yes	27	135	13.5	13.5
			742.5	No	74.25	74.25	37.125	37.125
			1,485	No	148.5	148.5	74.25	74.25
			2,970	No	297	297	148.5	148.5
	4	1,000	270	Yes	27	135	6.75	6.75
			742.5	Yes	74.25	371.25	18.5625	18.5625
			1,485	No	148.5	148.5	37.125	37.125
			5,940	No	148.5	594	148.5	148.5
Stratix V	2	611	540	Yes	54	270	27	27
			1,620	No	162	162	81	81
			5,934	No	296.7	593.4	296.7	296.7

The color depths greater than 8 bpc or 24 bpp are defined to be deep color. For a color depth of 8 bpc, the core carries the pixels at a rate of one pixel per TMDS clock. At deeper color depths, the TMDS clock runs faster than the source pixel clock to provide the extra bandwidth for the additional bits.

The TMDS clock rate is increased by the ratio of the pixel size to 8 bits:

- 8 bits mode—TMDS clock = 1.0 × pixel or video clock (1:1)
- 10 bits mode—TMDS clock = 1.25 × pixel or video clock (5:4)
- 12 bits mode—TMDS clock = 1.5 × pixel or video clock (3:2)
- 16 bits mode—TMDS clock = 2 × pixel or video clock (2:1)

Table 11. HDMI PLL Desired Output Frequencies for Deep Color Video

This table shows an example of HDMI PLL desired output frequencies across symbols per clock and color depths.

Symbols Per Clock	Oversampling (5x) Required	Bits Per Component	TMDS Bit Rate (Mbps)	TMDS Clock Rate (MHz)	RX/TX Transceiver Refclk (MHz)	RX/TX Link Speed Clock (MHz)	RX/TX Video Clock (MHz)
2	Yes	8	270	27	135	13.5	13.5
		10 (3)	337.5	33.75	168.75	16.875	13.5

continued...

Symbols Per Clock	Oversampling (5x) Required	Bits Per Component	TMDS Bit Rate (Mbps)	TMDS Clock Rate (MHz)	RX/TX Transceiver Refclk (MHz)	RX/TX Link Speed Clock (MHz)	RX/TX Video Clock (MHz)
		12 (3)	405	40.5	202.5	20.25	13.5
		16 (3)	540	54	270	27	13.5
4	No	8	1,485	148.5	148.5	37.125	37.125
		10 (3)	1,856.25	185.625	185.625	46.40625	37.125
		12 (3)	2,227.5	222.75	222.75	55.6875	37.125
		16 (3)	2,970	297	297	74.25	37.125

The default frequency setting of the HDMI PLL is fixed at possible maximum value for each clock for appropriate timing analysis.

Note: This default combination is not valid for any HDMI resolution. The core will reconfigure to the appropriate settings upon power up.

4.2.1.3. PLL Reconfig Intel FPGA IP Core

The PLL Reconfig Intel FPGA IP core facilitates dynamic real-time reconfiguration of PLLs in Intel FPGAs.

Use the IP core to update the output clock frequency, PLL bandwidth in real-time, without reconfiguring the entire FPGA.

You can run this IP core at 100 MHz in Stratix V devices. In Arria V devices, you need to run at 75 MHz for timing closure. To simplify clocking in Arria V devices, the entire management clock domain is capped at 75 MHz.

4.2.1.4. Multirate Reconfig Controller (RX)

The Multirate Reconfig Controller implements rate detection circuitry with the HDMI PLL to drive the RX transceiver to operate at any arbitrary link rates ranging from 250 Mbps to 6,000 Mbps. Link rate of 6,000 Mbps is not the absolute maximum but the intention is to support HDMI 2.0b link rate.

The Multirate Reconfig Controller performs rate detection on the HDMI PLL arbitrary reference clock, which is also the TMDS clock, to determine the clock frequency band. Based on the detected clock frequency band, the circuitry dynamically reconfigures the HDMI PLL and transceiver settings to accommodate for the link rate change.

(3) For this release, deep color video is only demonstrated in VIP bypass mode. It is not available in VIP passthrough mode.