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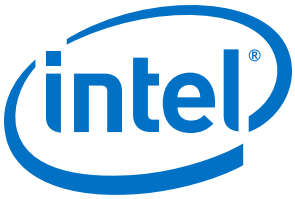

JESD204B Intel FPGA IP User Guide

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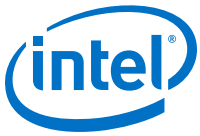


1. JESD204B IP Core Quick Reference

The JESD204B Intel FPGA IP is a high-speed point-to-point serial interface intellectual property (IP).

Note: For system requirements and installation instructions, refer to *Intel FPGA Software Installation & Licensing*.

Table 1. Brief Information About the JESD204B IP Core

Item		Description
Release Information	Version	18.0
	Release Date	May 2018
	Ordering Code	IP-JESD204B
	Product ID	0116
	Vendor ID	6AF7
IP Core Information	Protocol Features	• Joint Electron Device Engineering Council (JEDEC) JESD204B.01, 2012 standard release specification • Device subclass: — Subclass 0—Backwards compatible to JESD204A. — Subclass 1—Uses *SYSREF* signal to support deterministic latency. — Subclass 2—Uses *SYNC_N* detection to support deterministic latency.
IP Core Information	Core Features	• Run-time configuration of parameters L,M, and F • Data rates up to 12.5 gigabits per second (Gbps)—per JESD204B specification • Data rates of up to 16.0 Gbps—not certified per JESD204B specification (uncharacterized support) • Single or multiple lanes (up to 8 lanes per link) • Serial lane alignment and monitoring • Lane synchronization • Modular design that supports multidevice synchronization • MAC and PHY partitioning • Deterministic latency support • 8B/10B encoding • Scrambling/Descrambling • Avalon® Streaming (Avalon-ST) interface for transmit and receive datapaths • Avalon Memory-Mapped (Avalon-MM) interface for Configuration and Status registers (CSR) • Dynamic generation of simulation testbench

continued...

Item		Description
	Typical Application	• Wireless communication equipment • Broadcast equipment • Military equipment • Medical equipment • Test and measurement equipment
	Device Family Support	• Intel Cyclone® 10 GX FPGA devices • Intel Stratix® 10 FPGA devices • Intel Arria® 10 FPGA devices • Stratix V FPGA devices • Arria V FPGA devices • Arria V GZ FPGA devices • Cyclone V FPGA devices
	Design Tools	• Platform Designer parameter editor in the Intel Quartus® Prime software for design creation and compilation • Timing Analyzer in the Intel Quartus Prime software for timing analysis • ModelSim-Intel FPGA, Aldec Riviera-PRO*, Synopsys VCS/VCS MX, Cadence NCSim, and Cadence Xcelium* Parallel simulator software for design simulation or synthesis

Related Information

- Design Examples for JESD204B IP Core User Guide
  Provides information about design examples for Arria V, Cyclone V, Stratix V, and Intel Arria 10 devices using Intel Quartus Prime Standard Edition software.
- JESD204B Intel Arria 10 FPGA IP Design Example User Guide
- JESD204B Intel Stratix 10 FPGA IP Design Example User Guide
- JESD204B Intel Cyclone 10 GX FPGA IP Design Example User Guide
- Intel FPGA Software Installation and Licensing
- What's New in Intel FPGA IP
- JESD204B IP Core Release Notes
- Errata for JESD204B IP Core in the Knowledge Base
- AN803: Implementing ADC-Intel Arria 10 Multi-Link Design with JESD204B RX IP Core
- AN804: Implementing ADC-Intel Stratix 10 Multi-Link Design with JESD204B RX IP Core
- JESD204B Intel FPGA IP Document Archives on page 115
  Provides a list of user guides for previous versions of the JESD204B IP core.

2. About the JESD204B

The JESD204B Intel FPGA IP is a high-speed point-to-point serial interface for digital-to-analog (DAC) or analog-to-digital (ADC) converters to transfer data to FPGA devices. This unidirectional serial interface runs at a maximum data rate of 16.0 Gbps. This protocol offers higher bandwidth, low I/O count and supports scalability in both number of lanes and data rates. The JESD204B Intel FPGA IP addresses multi-device synchronization by introducing Subclass 1 and Subclass 2 to achieve deterministic latency.

Note: The full product name, JESD204B Intel FPGA IP, is shortened to JESD204B IP core in this document.

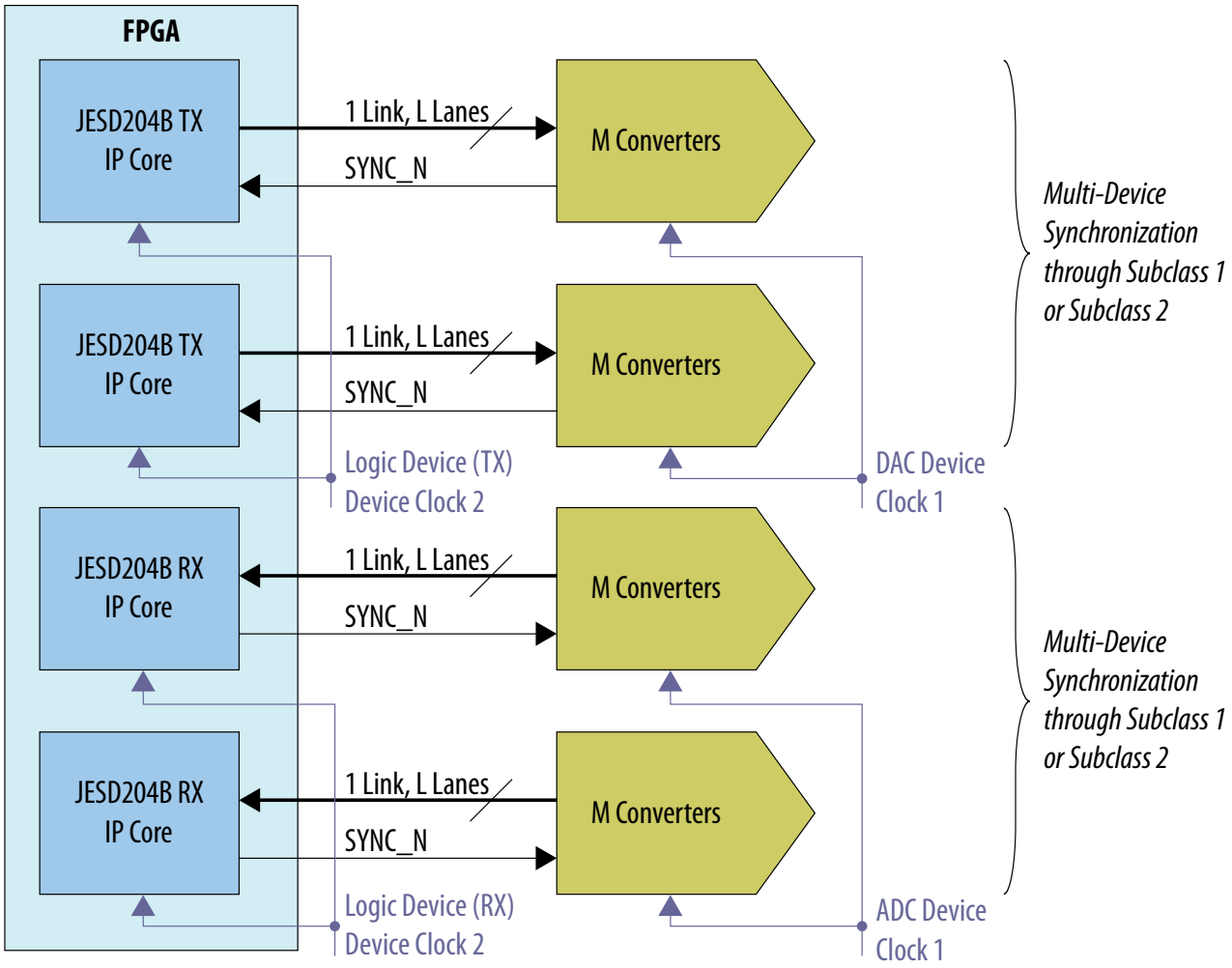
The JESD204B IP core incorporates:

- Media access control (MAC)—data link layer (DLL) block that controls the link states and character replacement.
- Physical layer (PHY)—physical coding sublayer (PCS) and physical media attachment (PMA) block.

The JESD204B IP core does not incorporate the Transport Layer (TL) that controls the frame assembly and disassembly. The TL and test components are provided as part of a design example component where you can customize the design for different converter devices.

Figure 1. Typical System Application for JESD204B IP Core

The JESD204B IP core uses the Avalon-ST source and sink interfaces, with unidirectional flow of data, to transmit and receive data on the FPGA fabric interface.



Key features of the JESD204B IP core:

- Data rate of up to 16.0 Gbps (characterization up to 12.5G)
- Run-time JESD204B parameter configuration (L, M, F, S, N, K, CS, CF)
- MAC and PHY partitioning for portability
- Subclass 0 mode for backward compatibility to JESD204A
- Subclass 1 mode for deterministic latency support (using *SYSREF*) between the ADC/DAC and logic device
- Subclass 2 mode for deterministic latency support (using *SYNC_N*) between the ADC/DAC and logic device
- Multi-device synchronization

Related Information

- V-Series Transceiver PHY User Guide
- Intel Arria 10 Transceiver PHY User Guide
- Intel Cyclone 10 GX Transceiver PHY User Guide
- Intel Stratix 10 E-Tile Transceiver PHY User Guide
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
- Intel Stratix 10 GX 2800 L-Tile ES-1 Transceiver PHY User Guide
- Intel Stratix 10 Device Datasheet
- Intel Arria 10 Device Datasheet

2.1. Datapath Modes

The JESD204B IP core supports TX-only, RX-only, and Duplex (TX and RX) mode. The IP core is a unidirectional protocol where interfacing to ADC utilizes the transceiver RX path and interfacing to DAC utilizes the transceiver TX path.

The JESD204B IP core generates a single link with a single lane and up to a maximum of 8 lanes. If there are two ADC links that need to be synchronized, you have to generate two JESD204B IP cores and then manage the deterministic latency and synchronization signals, like *SYSREF* and *SYNC_N*, at your custom wrapper level.

The JESD204B IP core supports duplex mode only if the LMF configuration for ADC (RX) is the same as DAC (TX) and with the same data rate. This use case is mainly for prototyping with internal serial loopback mode. This is because typically as a unidirectional protocol, the LMF configuration of converter devices for both DAC and ADC are not identical.

2.2. IP Core Variation

The JESD204B IP core has three core variations:

- JESD204B MAC only
- JESD204B PHY only
- JESD204B MAC and PHY

In a subsystem where there are multiple ADC and DAC converters, you need to use the Intel Quartus Prime software to merge the transceivers and group them into the transceiver architecture. For example, to create two instances of the JESD204B TX IP core with four lanes each and four instances of the JESD204 RX IP core with two lanes each, you can apply one of the following options:

- MAC and PHY option
  1. Generate JESD204B TX IP core with four lanes and JESD204B RX IP core with two lanes.
  2. Instantiate the desired components.
  3. Use the Intel Quartus Prime software to merge the PHY lanes.
- MAC only and PHY only option—based on the configuration above, there are a total of eight lanes in duplex mode.
  1. Generate the JESD204B Duplex PHY with a total of eight lanes. (TX skew is reduced in this configuration as the channels are bonded).
  2. Generate the JESD204B TX MAC with four lanes and instantiate it two times.
  3. Generate the JESD204B RX MAC with two lanes and instantiate it four times.
  4. Create a wrapper to connect the JESD204B TX MAC and RX MAC with the JESD204B Duplex PHY.

Note: If the data rate for TX and RX is different, the transceiver does not allow duplex mode to generate a duplex PHY. In this case, you have to generate a RX-only PHY on the RX data rate and a TX-only PHY on the TX data rate.

2.3. JESD204B IP Core Configuration

Table 3. JESD204B IP Core Configuration

Symbol	Description	Value
L	Number of lanes per converter device	1-8
M	Number of converters per device	1-256
F	Number of octets per frame	1, 2, 4-256
S	Number of transmitted samples per converter per frame	1-32
N	Number of conversion bits per converter	1-32
N'	Number of transmitted bits per sample (JESD204 word size, which is in nibble group)	1-32
K	Number of frames per multiframe	17/F ≤ K ≤ 32 ; 1-32
CS	Number of control bits per conversion sample	0-3
CF	Number of control words per frame clock period per link	0-32
HD	High Density user data format	0 or 1
LMFC	Local multiframe clock	(F × K /4) link clock counts (1)

(1) The value of F x K must be divisible by 4.

2.3.1. Run-Time Configuration

The JESD204B IP core allows run-time configuration of LMF parameters in all supported devices except for Intel Stratix 10. For Intel Stratix 10 devices, the JESD204B IP core must be parameterized according to your target converter device with the IP configurations shown in *JESD204B Configurations Tab* of Table 13 on page 35

Note: For Intel Stratix 10 devices, run-time access for certain registers have been disabled. Refer to the TX and RX register map for more information.

The most critical parameters that must be set correctly during IP generation are the L and F parameters. Parameter L denotes the maximum lanes supported while parameter F denotes the size of the deskew buffer needed for deterministic latency. The hardware generates during parameterization, which means that run-time programmability can only fall back from the parameterized and generated hardware, but not beyond the parameterized IP core.

You can use run-time configuration for prototyping or evaluating the performance of converter devices with various LMF configurations. However, in actual production,Intel recommends that you generate the JESD204B IP core with the intended LMF to get an optimized gate count.

For example, if a converter device supports LMF = 442 and LMF = 222, to check the performance for both configurations, you need to generate the JESD204B IP core with maximum F and L, which is L = 4 and F = 2. During operation, you can use the fall back configuration to disable the lanes that are not used in LMF = 222 mode. You must ensure that other JESD204B configurations like M, N, S, CS, CF, and HD do not violate the parameter F setting. You can access the Configuration and Status Register (CSR) space to modify other configurations such as:

- K (multiframe)
- device and lane IDs
- enable or disable scrambler
- enable or disable character replacement

F Parameter

This parameter indicates how many octets per frame per lane that the JESD204B link is operating in. You must set the F parameter according to the JESD204B IP Specification for a correct data mapping.

To support the High Density (HD) data format, the JESD204B IP core tracks the start of frame and end of frame because F can be either an odd or even number. The start of frame and start of multiframe wrap around the 32-bits data width architecture. The RX IP core outputs the start of frame (`sof[3:0]`) and start of multiframe (`somf[3:0]`), which act as markers, using the Avalon-ST data stream. Based on these markers, the transport layer build the frames.

In a simpler system where the HD data format is set to 0, the F will always be 1, 2, 4, 6, 8, and so forth. This simplifies the transport layer design, so you do not need to use the `sof[3:0]` and `somf[3:0]` markers.

Related Information

- JESD204B RX Address Map and Register Definitions

- JESD204B TX Address Map and Register Definitions

2.4. Channel Bonding

The JESD204B IP core supports channel bonding—bonded (PMA bonding for Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX) and non-bonded modes.

The channel bonding mode that you select may contribute to the transmitter channel-to-channel skew. A bonded transmitter datapath clocking provides low channel-to-channel skew as compared to non-bonded channel configurations.

For Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices, refer to PMA Bonding chapter of the respective *Transceiver PHY User Guide* , about how to connect the ATX PLL and fPLL in bonded configuration and non-bonded configuration. For the non-bonded configuration, refer to *Implementing Multi-Channel xN Non-Bonded Configuration*. For bonded configuration, refer to *Implementing x6/xN Bonding Mode*.

- In PHY-only mode, you can generate up to 32 channels, provided that the channels are on the same side. In MAC and PHY integrated mode, you can generate up to 8 channels.
- In bonded channel configuration, the lower transceiver clock skew for all channels result in a lower channel-to-channel skew.
  - For Stratix V, Arria V, and Cyclone V devices, you must use contiguous channels when you select bonded mode. The JESD204B IP core automatically selects between ×6, ×N or feedback compensation (fb_compensation) bonding depending on the number of transceiver channels you set.
  - For Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 devices, you do not have to place the channels in bonded group contiguously. Refer to Table 5 on page 12 for the clock network selection. Refer to *Channel Bonding* section of the respective *Transceiver PHY User Guide* for more information about PMA Bonding.
- In non-bonded channel configuration, the transceiver clock skew is higher and latency is unequal in the transmitter phase compensation FIFO for each channel. This may result in a higher channel-to-channel skew.

Table 4. Maximum Number of Lanes (L) Supported in Bonded and Non-Bonded Mode

Device Family	Core Variation	Bonding Mode Configuration	Maximum Number of Lanes (L)
Intel Stratix 10 Intel Arria 10 Intel Cyclone 10 GX Stratix V Arria V GZ Cyclone V	PHY only	Bonded	32 (2)
		Non-bonded	32 (2)
	MAC and PHY	Bonded	8
		Non-bonded	8
Arria V	PHY only	Bonded	32 (2)

continued...

(2) The maximum lanes listed here is for configuration simplicity. Refer to the *Intel FPGA Transceiver PHY User Guide* for the actual number of channels supported.

Device Family	Core Variation	Bonding Mode Configuration	Maximum Number of Lanes (L)
		Non-bonded	32 (2)
	MAC and PHY	Bonded	6
		Non-bonded	8

Table 5. Clock Network Selection for Bonded Mode

Device Family	L ≤ 6	L > 6
Intel Stratix 10 Intel Arria 10 Intel Cyclone 10 GX	×6	×N (3)
Stratix V	×6	feedback compensation
Arria V	×N	×N
Arria V GZ	×6	feedback compensation
Cyclone V	×N	×N

Related Information

- V-Series Transceiver PHY User Guide
- Intel Arria 10 Transceiver PHY User Guide
- Intel Cyclone 10 GX Transceiver PHY User Guide
- Intel Stratix 10 E-Tile Transceiver PHY User Guide
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
- Intel Stratix 10 GX 2800 L-Tile ES-1 Transceiver PHY User Guide
- Intel Stratix 10 Device Datasheet
- Intel Arria 10 Device Datasheet

(3) Bonded mode is not supported for data rate > 15 Gbps. Refer to the respective datasheet for the maximum data rate and channel span supported by the ×N clock network and the transceiver power supply operating condition for your device.

2.5. Performance and Resource Utilization

Table 6. JESD204B IP Core FPGA Performance

Device Family	PMA Speed Grade	FPGA Fabric Speed Grade	Data Rate		Link Clock F_{MAX} (MHz)
			Enable Hard PCS (Gbps)	Enable Soft PCS (Gbps) [4]	
Intel Stratix 10	1	1	2.0 to 12.0	2.0 to 16.0[6]	data_rate/40
		2	2.0 to 12.0	2.0 to 13.5	data_rate/40
	2	1	2.0 to 9.83	2.0 to 16.0[6]	data_rate/40
		2	2.0 to 9.83	2.0 to 13.5	data_rate/40
	3	1	2.0 to 9.83	2.0 to 16.0[6]	data_rate/40
		2	2.0 to 9.83	2.0 to 13.5	data_rate/40
		3	2.0 to 9.83	2.0 to 12.5	data_rate/40
Intel Arria 10	1	1	2.0 to 12.0	2.0 to 15.0 [6][5]	data rate/40
	2	1	2.0 to 12.0	2.0 to 15.0 [6] [5]	data rate/40
	2	2	2.0 to 9.83	2.0 to 15.0 [6] [5]	data rate/40
	3	1	2.0 to 12.0	2.0 to 14.2 [6] [7]	data rate/40
	3	2	2.0 to 9.83	2.0 to 14.2 [6] [8]	data rate/40
	4	3	2.0 to 8.83	2.0 to 12.5[9]	data rate/40

continued...

(4) Select `Enable Soft PCS` to achieve maximum data rate. For the TX IP core, enabling soft PCS incurs an additional 3–8% increase in resource utilization. For the RX IP core, enabling soft PCS incurs an additional 10–20% increase in resource utilization.

(5) When using Soft PCS mode at 15.0 Gbps, the timing margin is very limited. You are advised to enable high fitter effort, register duplication, and register retiming to improve timing performance.

(6) Refer to the Intel Arria 10 and Intel Stratix 10 Device Datasheet for the maximum data rate supported across transceiver speed grades and transceiver power supply operating conditions.

(7) For Intel Arria 10 GX 160, SX 160, GX 220 and SX 220 devices, the supported data rate is up to 12.288 Gbps.

(8) For Intel Arria 10 GX 160, SX 160, GX 220 and SX 220 devices, the supported data rate is 11.0 Gbps.

Device Family	PMA Speed Grade	FPGA Fabric Speed Grade	Data Rate		Link Clock F_{MAX} (MHz)
			Enable Hard PCS (Gbps)	Enable Soft PCS (Gbps) (4)	
Intel Cyclone 10 GX	*<Any supported speed grade>*	*<Any supported speed grade>*	2.0 to 6.25	2.0 to 6.25	data rate/40
Stratix V	1	1 or 2	2.0 to 12.2	2.0 to 12.5	data rate/40
	2	1 or 2	2.0 to 12.2	2.0 to 12.5	data rate/40
	2	3	2.0 to 9.8	2.0 to 12.5 (10)	data rate/40
	3	1, 2, 3, or 4	2.0 to 8.5	2.0 to 8.5	data rate/40
Arria V GX/SX	*<Any supported speed grade>*	*<Any supported speed grade>*	1.0 to 6.55	— (11)	data rate/40
Arria V GT/ST	*<Any supported speed grade>*	*<Any supported speed grade>*	1.0 to 6.55	4.0 to 7.5 (PMA direct) (11)	data rate/40
Arria V GZ	2	3	2.0 to 9.9	— (11)	data rate/40
	3	4	2.0 to 8.8	— (11)	data rate/40
Cyclone V	5	*<Any supported speed grade>*	1.0 to 5.0	—	data rate/40
	6	6 or 7	1.0 to 3.125	—	data rate/40

The following table lists the resources and expected performance of the JESD204B IP core. These results are obtained using the Intel Quartus Prime software targeting the following Intel FPGA devices:

- Cyclone V: 5CGTFD9E5F31I7
- Arria V: 5AGXFB3H4F35C5
- Arria V GZ: 5AGZME5K2F40C3
- Intel Arria 10: 10AX115H2F34I2SGES

(4) Select `Enable Soft PCS` to achieve maximum data rate. For the TX IP core, enabling soft PCS incurs an additional 3–8% increase in resource utilization. For the RX IP core, enabling soft PCS incurs an additional 10–20% increase in resource utilization.

(9) For Intel Arria 10 GX 160, SX 160, GX 220 and SX 220 devices, the supported data rate is 10.0 Gbps.

(10) When using Soft PCS mode at 12.5 Gbps, the timing margin is very limited. You are advised to enable high fitter effort, register duplication, and register retiming to improve timing performance.

(11) Enabling Soft PCS does not increase the data rate for the device family and speed grade. You are recommended to select the *Enable Hard PCS* option.

- Stratix V: 5SGXEA7H3F35C3
- Intel Stratix 10: 1SG280LN3F43E3VG
- Intel Cyclone 10 GX: 10CX105YF672I6G

All the variations for resource utilization are configured with the following parameter settings:

Table 7. Parameter Settings To Obtain the Resource Utilization Data

Parameter	Setting
JESD204B Wrapper	Base and PHY
JESD204B Subclass	1
Data Rate	5 Gbps
PCS Option	Enabled Hard PCS
PLL Type	• ATX (for 10 series devices) • CMU (for V series devices)
Bonding Mode	Non-bonded
Reference Clock Frequency	125.0 MHz
Octets per frame (F)	1
Enable Scrambler (SCR)	Off
Enable Error Code Correction (ECC_EN)	Off

Table 8. JESD204B IP Core Resource Utilization

The numbers of ALMs and logic registers in this table are rounded up to the nearest 10.

Note: The resource utilization data are extracted from a full design which includes the Intel FPGA Transceiver PHY Reset Controller IP core. Thus, the actual resource utilization for the JESD204B IP core should be smaller by about 15 ALMs and 20 registers.

Device Family	Data Path	Number of Lanes (L)	ALMs	ALUTs	Logic Registers	Memory Block (M10K/M20K) (12) (13)
Intel Stratix 10	RX	1	873.1	1225	1307	1
		2	1344.4	1838	2018	2
		4	2293.2	3057	3474	4
		8	4412.4	5921	6576	8
	TX	1	556.5	707	890	0
		2	757.4	1059	1099	0
		4	1041.9	1532	1541	0

continued...

(12) M10K for Arria V, Cyclone V devices, M20K for Arria V GZ, Stratix V, Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 devices.

(13) The Intel Quartus Prime software may auto-fit to use MLAB when the memory size is too small. Conversion from MLAB to M20K or M10K was performed for the numbers listed above.

Device Family	Data Path	Number of Lanes (L)	ALMs	ALUTs	Logic Registers	Memory Block (M10K/M20K) (12) (13)
		8	1469.9	1950	2479	0
Intel Arria 10	RX	1	1034.8	1488	1215	0
		2	1553	2216	1839	0
		4	2688	3767	3089	0
		8	5293.5	7132	5579	0
	TX	1	726	1116	948	0
		2	895	1376	1068	0
		4	1248	1893	1308	0
		8	1923.5	2971	1787	0
Intel Cyclone 10 GX	RX	1	1011.5	1488	1207	1
		2	1512	3767	1821	2
		4	2613.5	3767	3054	4
		8	5142	7132	5515	8
	TX	1	716.5	1116	948	0
		2	892	1376	1067	0
		4	1243	1893	1308	0
		8	1925	2971	1788	0
Stratix V	RX	1	1047.2	1530	1226	0
		2	1608.7	2322	1871	0
		4	2897.2	4037	3164	0
		8	5412.5	7506	5743	0
	TX	1	711	1152	948	0
		2	926.7	1491	1086	0
		4	1345.7	2134	1359	0
		8	2114.7	3358	1907	0
Arria V	RX	1	1024.5	1516	1208	1
		2	1555.5	2302	1841	2
		4	2769.5	3951	3099	4
		8	5189	7399	5620	8
	TX	1	711.7	1149	948	0

continued...

(12) M10K for Arria V, Cyclone V devices, M20K for Arria V GZ, Stratix V, Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 devices.

(13) The Intel Quartus Prime software may auto-fit to use MLAB when the memory size is too small. Conversion from MLAB to M20K or M10K was performed for the numbers listed above.

Device Family	Data Path	Number of Lanes (L)	ALMs	ALUTs	Logic Registers	Memory Block (M10K/M20K) (12) (13)
		2	860.5	1418	1065	0
		4	1188.7	1932	1300	0
		8	1721	2854	1768	0
Arria V GZ	RX	1	1048.7	1530	1228	0
		2	1601.5	2322	1871	0
		4	2894	4037	3162	0
		8	5400.5	7506	5745	0
	TX	1	712.2	1152	948	0
		2	926.5	1491	1087	0
		4	1349.2	2134	1359	0
		8	2104.7	3358	1907	0
Cyclone V	RX	1	1022	1516	1210	1
		2	1555.5	2302	1841	2
		4	2777.5	3951	3099	4
		8	5195	7399	5622	8
	TX	1	713.5	1149	949	0
		2	867	1418	1065	0
		4	1198	1932	1301	0
		8	1709.2	2838	1768	0

Related Information

JESD204B IP Core Parameters on page 35

(12) M10K for Arria V, Cyclone V devices, M20K for Arria V GZ, Stratix V, Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 devices.

(13) The Intel Quartus Prime software may auto-fit to use MLAB when the memory size is too small. Conversion from MLAB to M20K or M10K was performed for the numbers listed above.

3. Getting Started

Related Information

- Intel FPGA Software Installation & Licensing
- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Platform Designer Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

3.1. Introduction to Intel FPGA IP Cores

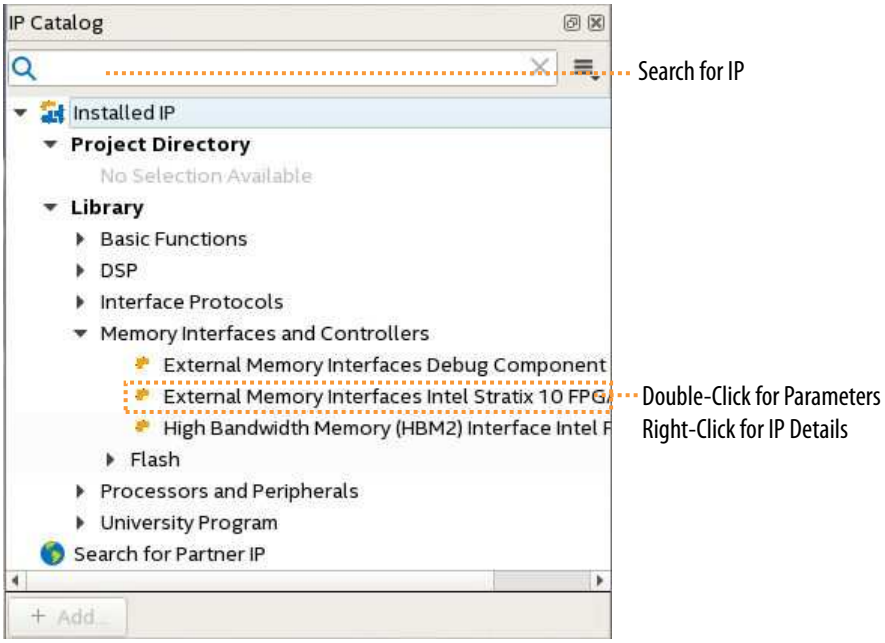
Intel and strategic IP partners offer a broad portfolio of configurable IP cores optimized for Intel FPGA devices.

The Intel Quartus Prime software installation includes the Intel FPGA IP library. Integrate optimized and verified Intel FPGA IP cores into your design to shorten design cycles and maximize performance. The Intel Quartus Prime software also supports integration of IP cores from other sources. Use the IP Catalog (**Tools ➤ IP Catalog**) to efficiently parameterize and generate synthesis and simulation files for your custom IP variation. The Intel FPGA IP library includes the following types of IP cores:

- Basic functions
- DSP functions
- Interface protocols
- Low power functions
- Memory interfaces and controllers
- Processors and peripherals

This document provides basic information about parameterizing, generating, upgrading, and simulating stand-alone IP cores in the Intel Quartus Prime software.

Figure 2. IP Catalog



3.2. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 3. IP Core Installation Path

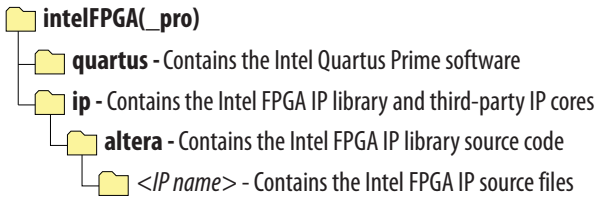


Table 9. IP Core Installation Locations

Location	Software	Platform
<*drive*>:\intelFPGA_pro\quartus\ip\altera	Intel Quartus Prime Pro Edition	Windows*
<*drive*>:\intelFPGA\quartus\ip\altera	Intel Quartus Prime Standard Edition	Windows
<*home directory*>:/intelFPGA_pro/quartus/ip/altera	Intel Quartus Prime Pro Edition	Linux*
<*home directory*>:/intelFPGA/quartus/ip/altera	Intel Quartus Prime Standard Edition	Linux

3.3. Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

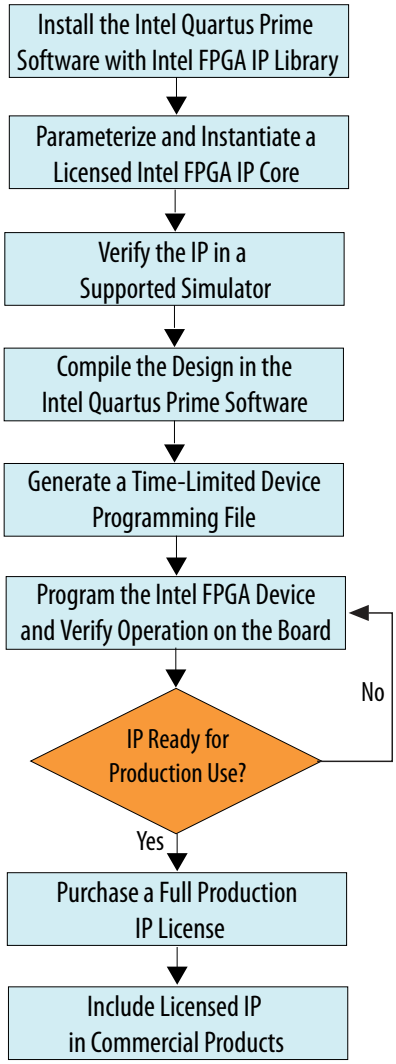
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (<*project name*>_time_limited.sof) that expires at the time limit.

Figure 4. Intel FPGA IP Evaluation Mode Flow



Note: Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the Self-Service Licensing Center or contact your local Intel FPGA representative.

The Intel FPGA Software License Agreements govern the installation and use of licensed IP cores, the Intel Quartus Prime design software, and all unlicensed IP cores.

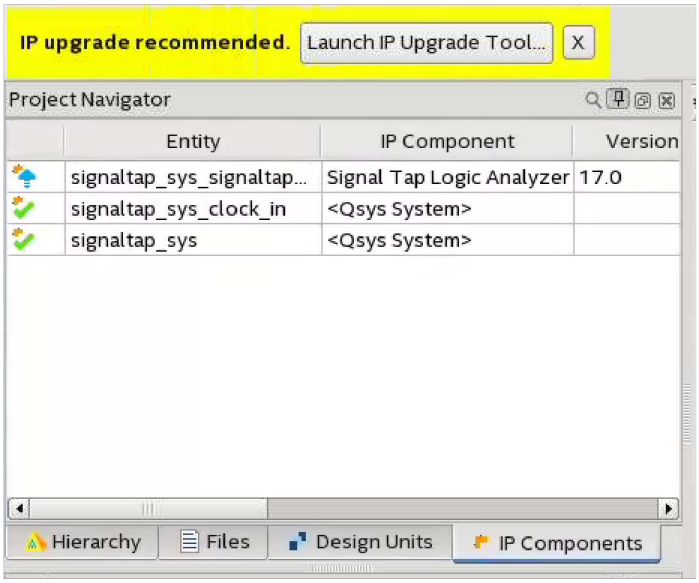
Related Information

- Intel Quartus Prime Licensing Site
- Intel FPGA Software Installation and Licensing

3.4. Upgrading IP Cores

Any Intel FPGA IP variations that you generate from a previous version or different edition of the Intel Quartus Prime software, may require upgrade before compilation in the current software edition or version. The Project Navigator displays a banner indicating the IP upgrade status. Click **Launch IP Upgrade Tool** or **Project ➤ Upgrade IP Components** to upgrade outdated IP cores.

Figure 5. IP Upgrade Alert in Project Navigator



Icons in the **Upgrade IP Components** dialog box indicate when IP upgrade is required, optional, or unsupported for an IP variation in the project. Upgrade IP variations that require upgrade before compilation in the current version of the Intel Quartus Prime software.

Note: Upgrading IP cores may append a unique identifier to the original IP core entity names, without similarly modifying the IP instance name. There is no requirement to update these entity references in any supporting Intel Quartus Prime file, such as the Intel Quartus Prime Settings File (`.qsf`), Synopsys* Design Constraints File (`.sdc`), or Signal Tap File (`.stp`), if these files contain instance names. The Intel Quartus Prime software reads only the instance name and ignores the entity name in paths that specify both names. Use only instance names in assignments.

Table 10. IP Core Upgrade Status

IP Core Status	Description
IP Upgraded 	Indicates that your IP variation uses the latest version of the Intel FPGA IP core.
IP Component Outdated 	Indicates that your IP variation uses an outdated version of the IP core.
IP Upgrade Optional 	Indicates that upgrade is optional for this IP variation in the current version of the Intel Quartus Prime software. You can upgrade this IP variation to take advantage of the latest development of this IP core. Alternatively, you can retain previous IP core characteristics by declining to upgrade. Refer to the Description for details about IP core version differences. If you do not upgrade the IP, the IP variation synthesis and simulation files are unchanged and you cannot modify parameters until upgrading.
IP Upgrade Required 	Indicates that you must upgrade the IP variation before compiling in the current version of the Intel Quartus Prime software. Refer to the Description for details about IP core version differences.
IP Upgrade Unsupported 	Indicates that upgrade of the IP variation is not supported in the current version of the Intel Quartus Prime software due to incompatibility with the current version of the Intel Quartus Prime software. The Intel Quartus Prime software prompts you to replace the unsupported IP core with a supported equivalent IP core from the IP Catalog. Refer to the Description for details about IP core version differences and links to Release Notes.
IP End of Life 	Indicates that Intel designates the IP core as end-of-life status. You may or may not be able to edit the IP core in the parameter editor. Support for this IP core discontinues in future releases of the Intel Quartus Prime software.
IP Upgrade Mismatch Warning 	Provides warning of non-critical IP core differences in migrating IP to another device family.
IP has incompatible subcores 	Indicates that the current version of the Intel Quartus Prime software does not support compilation of your IP variation, because the IP has incompatible subcores

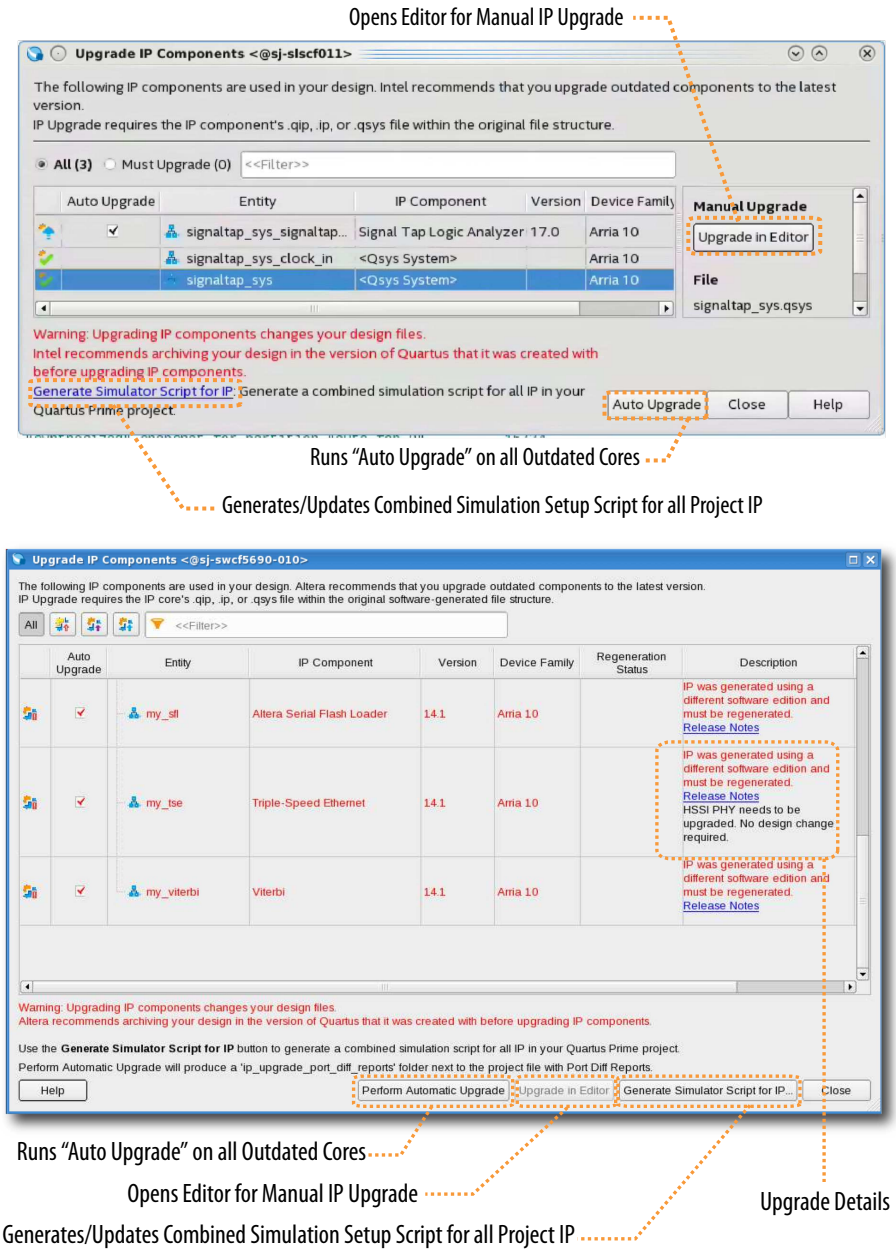
continued...

IP Core Status	Description
Compilation of IP Not Supported 	Indicates that the current version of the Intel Quartus Prime software does not support compilation of your IP variation. This can occur if another edition of the Intel Quartus Prime software, such as the Intel Quartus Prime Standard Edition, generated this IP. Replace this IP component with a compatible component in the current edition.

Follow these steps to upgrade IP cores:

1. In the latest version of the Intel Quartus Prime software, open the Intel Quartus Prime project containing an outdated IP core variation. The **Upgrade IP Components** dialog box automatically displays the status of IP cores in your project, along with instructions for upgrading each core. To access this dialog box manually, click **Project ➤ Upgrade IP Components**.
2. To upgrade one or more IP cores that support automatic upgrade, ensure that you turn on the **Auto Upgrade** option for the IP cores, and click **Auto Upgrade**. The **Status** and **Version** columns update when upgrade is complete. Example designs that any Intel FPGA IP core provides regenerate automatically whenever you upgrade an IP core.
3. To manually upgrade an individual IP core, select the IP core and click **Upgrade in Editor** (or simply double-click the IP core name). The parameter editor opens, allowing you to adjust parameters and regenerate the latest version of the IP core.

Figure 6. Upgrading IP Cores



Note: Intel FPGA IP cores older than Intel Quartus Prime software version 12.0 do not support upgrade. Intel verifies that the current version of the Intel Quartus Prime software compiles the previous two versions of each IP core. The *Intel FPGA IP Core Release Notes* reports any verification exceptions for Intel FPGA IP cores. Intel does not verify compilation for IP cores older than the previous two releases.

Related Information

Intel FPGA IP Core Release Notes