A 10/100 BASE-TX/ 100 BASE-FX Converter

(Port Mirror/Recovery, OAM Monitor/Control, OAM PHY & RS232 Exentender)

Features

Built in 3 MACs
- One external MII I/F port (P03)
- One external SMII/MII/RS232 I/F or internal MII I/F port (P02)
- One external SMII/MII/RS232 I/F or internal MII I/F port (P01)

Built in a 10/100BASE-TX/100BASE-FX Transceiver
Built in a PHY for 100BASE-FX
Built in a 3-port switch
- Non-blocking architecture
- 288Kb packet buffer
- 1K MAC address (or pass without address look up)
- Pass all packets with/without CRC check (optional)
- Pass PAUSE frame (optional)
- Support modified cut through frame forwarding for low latency
- Converter mode with auto-change mode function
- Support flow control for full duplex (symmetric/asymmetric) and half duplex (collision/carrier base) operation
- Bandwidth control (32K or 512Kbps x N)
- Forward 2046 bytes (max.) packets in switch mode
- 16 802.1Q tag VLANs (port base TAG insertion/ removal)
- OoS priority support (port or tag base)
- Port mirroring
- Link aggregation (support recovery)
- Offload setting for CPU port

Support Pass Through mode for extreme low latency data forwarding
- Pass all frames including OAM/ fragment
- Support 9K jumbo packets

Support RS232-like interface to TP/Fiber extension mode
- 2 independent pairs support
- Six MODEM control pins (RTS, CTS, DTR, DSR, DC and SI)
- Auto Baud rate detection (max. baud rate up to 500K bps)

Support special tag
Support TS-1000
- TS-1000 std. version 2
- IP113A/M/C/F maintenance frame compatible
- Variable and flexible auto loop back test
- OAM frame TX. /Rx. controllable
- OAM frame receiving notification

Support two wires serial CPU interface for management
- Configure local and remote IP113S LF through local SMI
- Monitor local and remote IP113S LF through local SMI
- PHY MII registers accessible
- Support loop back test (In-band or out-band)
- The OAM frame is compatible to TS-1000 standard (the Telecommunication Technology Committee, TTC)

Support RMON MIB Counters
- Ethernet statistics, Ethernet History, Alarm, Even groups
- Overflow interrupt supported

Support auto MDI-MDIX function (optional)
Support link fault pass through function between P01 and P02
Support far end fault function (FEF pattern or OAM)
Built in power abnormal detection
LED display
- 4 modes selectable
- 4 blinking speed selectable
- Loop back test result display

Support EEPROM Configuration
0.25u technology, 2.5/3.3V power
Support Lead Free package (Please refer to the Order Information)

General Description

IP113S LF built in a 3-port switch controller, an OAM engine, a fast Ethernet transceiver, a PHY for 100BASE-FX and three MII I/F. Two of these MII can be configured as SMII or RS232 I/F. The powerful switch engine supports flow contol, VLAN, QoS, port mirroring, and trunking, etc. The transceivers in IP113S LF are designed in DSP approach with advance 0.25um technology; this results in high noise immunity and robust performance.

IP113S LF can be a 10/100BASE-TX to 100BASE-FX converter with an MII to connect to an external PHY for back up fiber application or an external MAC for web management application. IP113S LF forwards packets with length up to 2046 bytes in store and forward mode and modified cut through mode and it can support jumbo frame (up to 9K bytes) in pure converter mode and pass through mode to meet requirement of extra long packets.

IP113S LF supports remote access function and loop back test function defined in TS-1000 standard version 2 (*). Local IP113S LF can access the registers of remote IP113S LF by programming local IP113S LF's registers via SMI connection. IP113S LF implements the management function using the maintenance frame defined in TS-1000 spec.

IP113S LF supports SMII to connect to a switch controller to build up a multiple-port fiber switch, which supports TS-1000. IP113S LF is a two-port 100BASE-FX PHY with TS-1000 function in this application.

IP113S LF can be used as a six-pin RS232 extender, RTS, CTS, DTR, DSR, DC and SI, when it works as a RS232 to Ethernet converter. The limitation in distance of RS232 is extended to the distance of Ethenet 100BASE-TX or 100BASE-FX.

* The Telecommunication Technology Committee owns the copyright of TS-1000.

Table of Contents

Revision History

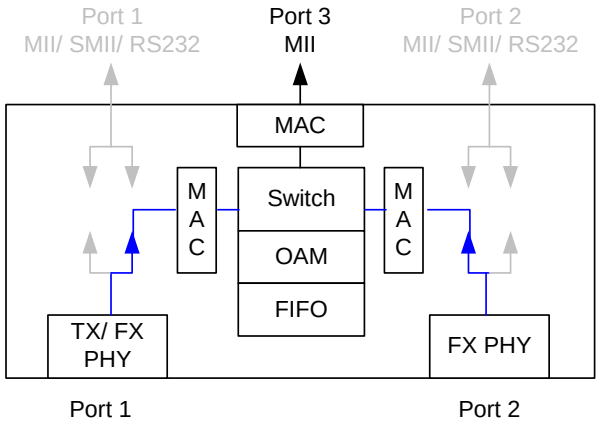
Revision #	Change Description
IP113S LF-DS-R01	Initial release.

1 Applications & Block diagram

1.1 Managed TX/FX converter, FX/FX repeater

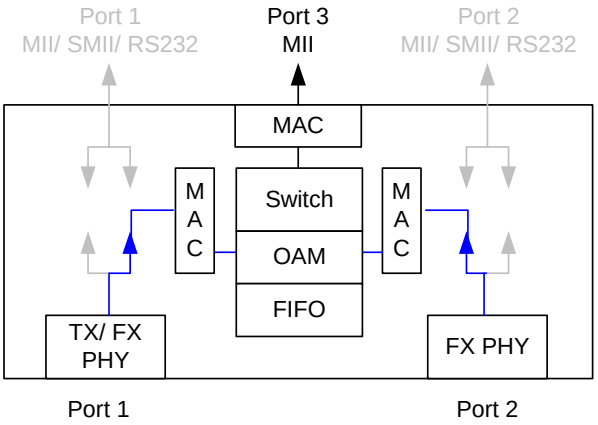
1.1.1 Store and forward / modified cut-through mode with internal PHY

Function	Setting	Pin setting	Register value
OP Mode	Switch / Modified cut-through mode	PassDis =1 CFG_CutThrDis =don't care CFG_CnvDis =1	0B[2] = 0 0B[1:0] = 00 / 10
Dual PHY mode	Disabled	DulPHYDis = 1	0A[8] = 0
Ext. MAC I/F	Disabled	ExtIFDis1 = 1 ExtIFDis2 = 1 Port1IFMd[1:0] = don't care Port2IFMd[1:0] = don't care	0A[5:4] = 00 0A[3:0] = xxxx



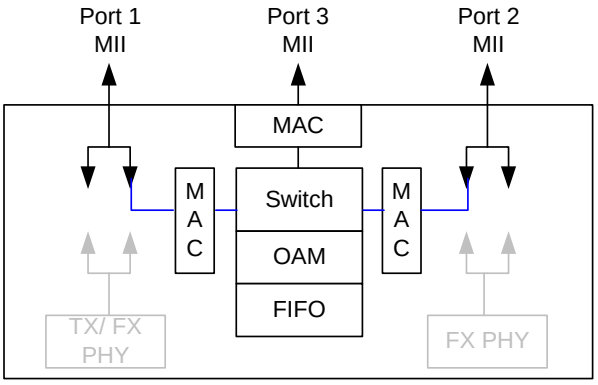
1.1.2 Converter mode with internal PHY

Function	Setting	Pin setting	Register value
OP Mode	Converter mode	PassDis = 1 CFG_CutThrDis = don't care CFG_CnvDis = 0	0B[2] = 0 0B[1:0] = 01 / 11
Dual PHY mode	Disabled	DulPHYDis = 1	0A[8] = 0
Ext. MAC I/F	Disabled	ExtIFDis1 = 1 ExtIFDis2 = 1 Port1IFMd[1:0] = don't care Port2IFMd[1:0] = don't care	0A[5:4] = 00 0A[3:0] = xxxx



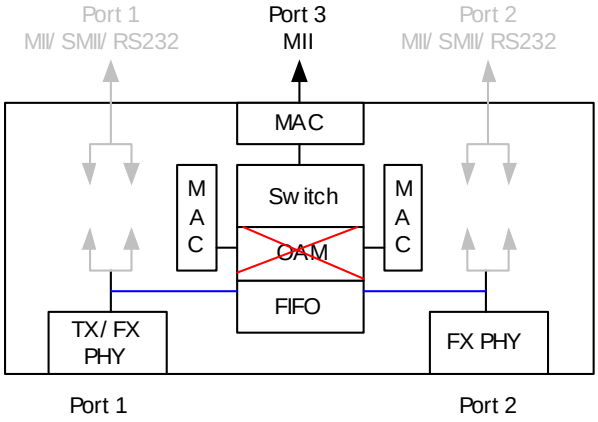
1.1.3 Store and forward / modified cut-through mode with external PHY

Function	Setting	Pin setting	Register value
OP Mode	Switch / Modified cut-through mode	PassDis = 1 CFG_CutThrDis = don't care CFG_CnvDis = 1	0Bh[2] = 0 0Bh[1:0] = 00 / 10
Dual PHY mode	Disabled	DulPHYDis = 1	0Ah[8] = 0
Ext. MAC I/F	MII	ExtIFDis1 = 0 ExtIFDis2 = 0 Port1IFMd[1:0] = 11 Port2IFMd[1:0] = 11	0Ah[5:4] = 11 0Ah[3:0]=1111



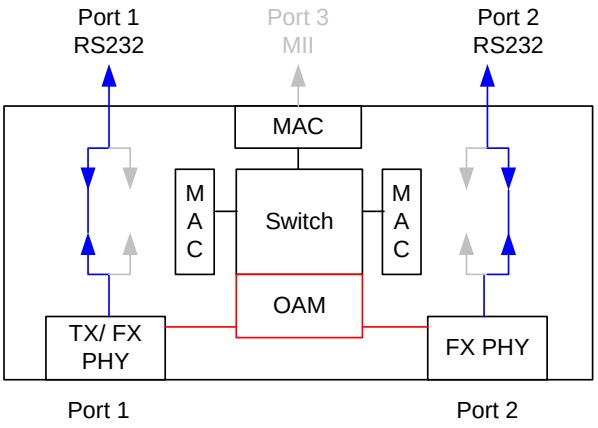
1.1.4 Pass through mode (pure conerter without TS1000 function)

Function	Setting	Pin setting	Register value
OP Mode	Pass through mode (pure converter, no OAM)	PassDis = 0 CFG_CutThrDis = don't care CFG_CnvDis = don't care	0B[2] = 1 0B[1:0] = xx
Dual PHY mode	Disabled	DulPHYDis = 1	0A[8] = 0
Ext. MAC I/F	Disabled	ExtIFDis1=1 ExtIFDis2=1 Port1IFMd[1:0]= don't care Port2IFMd[1:0]= don't care	0A[5:4]=00 0A[3:0]=xxxx



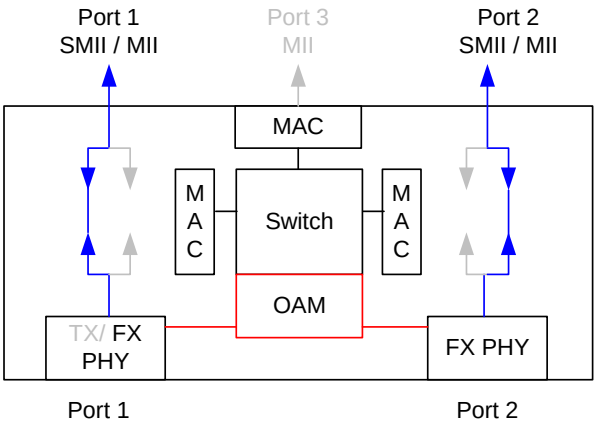
1.2 Dual Ethernet to RS232 converter

Function	Setting	Pin setting	Register value
OP Mode	Converter mode	PassDis = 1 CFG_CutThrDis = don't care CFG_CnvDis = 0	0Bh[2] = 0 0Bh[1:0] = 00 / 10
Dual PHY mode	Enabled	DulPHYDis = 0	0Ah[8] = 1
Ext. MAC I/F	RS232	ExtIFDis1=0 ExtIFDis2=0 Port1IFMd[1:0]=00 Port2IFMd[1:0]=00	0Ah[5:4]=11 0Ah[3:0]=0000

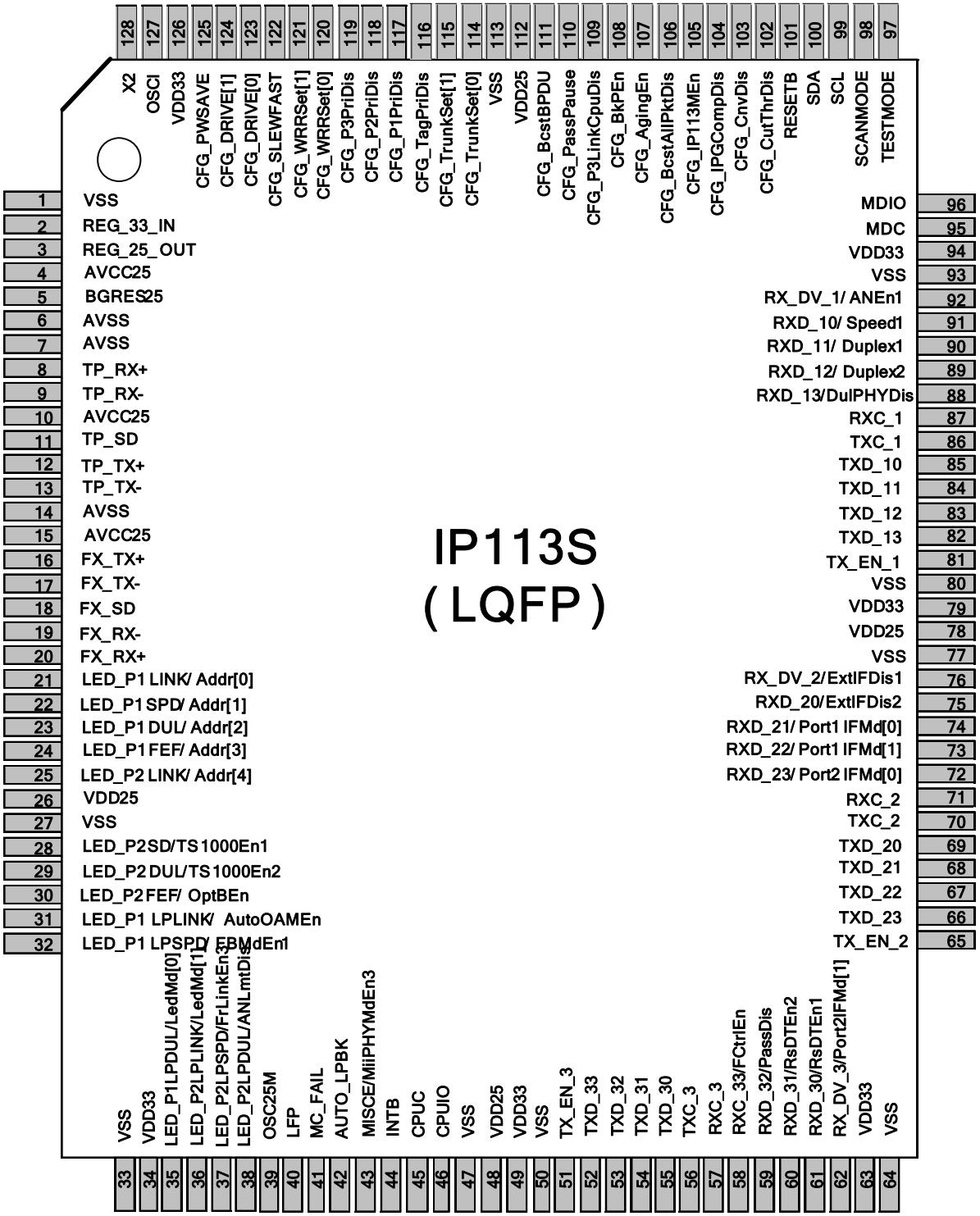


1.3 Dual PHY with OAM functions and MII or SMII I/F

Function	Setting	Pin setting	Register value
OP Mode	Converter mode	PassDis = 1 CFG_CutThrDis = don't care CFG_CnvDis = 0	0B[2] = 0 0B[1:0] = 00 / 10
Dual PHY mode	Enabled	DulPHYDis = 0	0A[8] = 1
Ext. MAC I/F	SMII/ Rev MII/ MII	ExtIFDis1=0 ExtIFDis2=0 Port1IFMd[1:0]=01,10,11 Port2IFMd[1:0]=01,10,11	0A[5:4]=11 0A[1:0]=01, 10, 11 0A[3:2]=01, 10, 11



2 Pin Diagram



Pin description

Type	Description
P	Power or ground
I; O	I: Input pin; O:Output pin
IL	Input latched upon reset

Type	Description
PD	PD: Pulled down with internal resistor
PU	PU: Pulled up with internal resistor
I/O	Bi-direction Input/Output

Pin no.	Label	Type	Description
P1 MII/SMII/RS232 I/F (The following settings are latched at the end of power on Reset)			
86	TXC_1	I/O	**MII TXCLK / SMII TXC**
81	TX_EN_1	I, PD	**MII TXEN / SMII SYNC / RS232 RD_1**
85	TXD_10	I, PD	**MII TXD0 / SMII TXD1 / RS232 CTS_1**
84	TXD_11	I, PD	**MII TXD1/ RS232 DSR_1**
83	TXD_12	I/O, PD	**MII TXD2 / RS232 CD_1** CD_1 is an output pin if RsDTEn1 is pulled low. Otherwise, it is an input pin.
82	TXD_13	I/O, PD	**MII TXD3 / RS232 RI_1** RI_1 is an output pin if RsDTEn1 is pulled low. Otherwise, it is an input pin.
87	RXC_1	I/O	**MII RXCLK / SMII RXC**

Pin no.	Label	Type	Description
P1 MII/SMII/RS232 I/F (The following settings are latched at the end of power on Reset)			
92	RX_DV_1/ANEn1	I/O, PU	**MII RXDV /SMII RXSYNC/ RS232 TD_1** **P1 nway enable** 0: nway disabled 1: nway enabled (default) The setting can be updated by writing 4Eh[2].
91	RXD_10/Speed1	I/O, PU	**MII RXD0 / SMII RXD1 / RS232 RTS_1** **P1 speed mode** 0: 10Mb speed 1: 100Mb speed (default) The setting can be updated by writing 4Eh[3].
90	RXD_11/Duplex1	I/O, PU	**MII RXD1 / RS232 DTR_1** **P1 duplex mode** 0: half duplex 1: full duplex (default) The setting can be updated by writing 4Eh[4].
89	RXD_12/Duplex2	I/O, PU	**MII RXD2** **P2 duplex mode** 0: half duplex 1: full duplex (default) The setting can be updated by writing 4Eh[8].
88	RXD_13/DulPHYDis	I/O, PU	**MII RXD3** **IP113S LF Dul PHY mode disable** 0: P1 and p2 work as two independent PHY with OAM function 1: P1and p2 are interconnected through internal switch engine or FIFO (default) The setting can be updated by writing 0Ah[8]

Pin no.	Label	Type	Description
P2 MII/SMII/RS232 I/F (The following settings are latched at the end of power on Reset)			
70	TXC_2	I/O	**MII TXCLK**
65	TX_EN_2	I, PD	**MII TXEN / RS232 RD_2**
69	TXD_20	I, PD	**MII TXD0 / SMII TXD2/ RS232 CTS_2**
68	TXD_21	I, PD	**MII TXD1 / RS232 DSR_2**
67	TXD_22	I/O, PD	**MII TXD2 / RS232 CD_2** CD_2 is an output pin if RsDTEn2 is pulled low. Otherwise, it is an input pin.
66	TXD_23	I/O, PD	**MII TXD3 / RS232 RI_2** RI_2 is an output pin if RsDTEn2 is pulled low. Otherwise, it is an input pin.
71	RXC_2	I/O	**SMII RXC**

Pin no.	Label	Type	Description
P2 MII/SMII/RS232 I/F (The following settings are latched at the end of power on Reset)			
76	RX_DV_2/ExtIFDis1	I/O, PU	**MII RXDV / RS232 TD_2** **P1 external I/F disable** 0: external MAC interface enable. Using external MII or SMII or RS232 interface defined in bit[3:0]. 1: using internal MII interface connected to internal PHY (default) The setting can be updated by writing 0Ah[4]
75	RXD_20/ExtIFDis2	I/O, PU	**MII RXD0 / SMII RXD2/ RS232 RTS_2** **P2 external I/F disable** 0: external MAC interface enable. Using external MII or SMII or RS232 interface 1: using internal MII interface connected to internal PHY (default) The setting can be updated by writing 0Ah[3]
74	RXD_21/Port1IFMd[0]	I/O, PU	**MII RXD1/ RS232 DTR_2** **P1 external I/F mode[0]**
73	RXD_22/Port1IFMd[1]	I/O, PU	**MII RXD2** **P1 external I/F mode[1]** **Port1IFMd[1:0]** 00: RS232 01: SMII 10: reversed MII 11: MII (default) Note: Only MII/reversed-MII interface can connected to internal PHY or MAC, others to PHY only. The setting can be updated by writing 0Ah[1:0]
72	RXD_23/Port2IFMd[0]	I/O, PU	**MII RXD3** **P2 external I/F mode[0]** **Port2IFMd[1:0]** 00: RS232 01: SMII 10: reversed MII 11: MII (default) Note: Only MII/reversed-MII interface can connected to internal PHY or MAC, others to PHY only. The setting can be updated by writing 0Ah[3:2]

Pin no.	Label	Type	Description
P3 MII I/F (The following settings are latched at the end of power on Reset)			
56	TXC_3	I/O	**MII TXCLK**
51	TX_EN_3	I, PD	**MII TXEN**
55	TXD_30	I, PD	**MII TXD0**
54	TXD_31	I, PD	**MII TXD1**
53	TXD_32	I, PD	**MII TXD2**
52	TXD_33	I, PD	**MII TXD3**
57	RXC_3	I/O	**MII RXC**
62	RX_DV_3/Port2IFMd[1]	I/O, PU	**MII RXDV** **P2 external I/F mode[1]** Please refer to RXD_23/Port2IFMd[0].
61	RXD_30/RsDTEn1	I/O, PU	**MII RXD0** **P1 RS232 DTE mode enable** 0: RS232 is in DCE mode. CD_1 and RI_1 are outputs. 1: RS232 is in DTE mode. CD_1 and RI_1 are inputs. **P1 SMII RXD delay** 1: SMII RXD delay 4ns (default) 0: no delay The setting can be updated by writing 0Ah[6]
60	RXD_31/RsDTEn2	I/O, PU	**MII RXD1** **P2 RS232 DTE mode enable** 0: RS232 is in DCE mode. CD_2 and RI_2 are outputs. 1: RS232 is in DTE mode. CD_2 and RI_2 are inputs. **P2 SMII RXD delay** 1: SMII RXD delay 4ns (default) 0: no delay The setting can be updated by writing 0Ah[7]
59	RXD_32/PassDis	I/O, PU	**MII RXD2** **Pass through mode diable** 0: Pass through mode enable 1: Pass through mode disable (default) The setting can be updated by writing 0BH[2]
58	RXD_33/FCtrlEn	I/O, PU	**MII RXD3** **IP113S LF flow control enable** 0: disable 1: enable (default) The setting can be updated by writing 33H[5:0]

Pin no.	Label	Type	Description
LED display (The following settings are latched at the end of power on Reset)			
21	LED_P1LINK/Addr[0]	I/O, PD	**P1 LINK/ACT LED** **P1 PHY_addr[0]** (default = 0)
22	LED_P1SPD/Addr[1]	I/O, PD	**P1 Speed/SD LED** **P1 PHY_addr[1]** (default = 0)
23	LED_P1DUL/Addr[2]	I/O, PD	**P1 Duplex/Col LED** **P1 PHY_addr[2]** (default = 0)
24	LED_P1FEF/Addr[3]	I/O, PD	**P1 FEF/Loop Back LED** **P1 PHY_addr[3]** (default = 0)
25	LED_P2LINK/Addr[4]	I/O, PD	**P2 LINK/ACT LED** **P1 PHY_addr[4]** (default = 0)
	P2 PHY_addr[4:0] = P1 PHY_addr[4:0] + 1 P3 PHY_addr[4:0] = P1 PHY_addr[4:0] + 2		
28	LED_P2SD/TS1000En1	I/O, PU	**P2 fiber Signal Detect LED** **P1 TS1000 enable** 0: disable 1: enable (default) The setting can be updated by writing 39h[0]
29	LED_P2DUL/TS1000En2	I/O, PU	**P2 Duplex/Col LED** **P2 TS1000 enable** 0: disable 1: enable (default) The setting can be updated by writing 39h[1]
30	LED_P2FEF/OptBEn	I/O, PU	**P2 FEF/ Loop back LED** **Option B enable** 0: disable 1: enable **(**default) The setting can be updated by writing 39h[2]
31	LED_P1LPLINK/AutoOAM En	I/O, PU	**P1 Link Partner's Link/Test** **Auto send enable** 0: enable 1: disable (default). The setting can be updated by writing 39h[3]

<table>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">LED display (The following settings are latched at the end of power on Reset)</td></tr>
<tr><td>32</td><td>LED_P1LPSPD/FBMdEn1</td><td>I/O, PU</td><td>P1 Link Partner’s Speed/Test Done

TP port fiber mode eable
0: enable
1: disable (default).</td></tr>
<tr><td>35</td><td>LED_P1LPDUL/LedMd[0]</td><td>I/O, PU</td><td rowspan="2">P1 Link Partner’s Duplex LED/Test OK LED mode[0]

P2 Link Partner’s Link LED /Test LED mode[1]

LED mode[1:0]
<table><tr><td>00</td><td>Bi-colors speed mode* / duplex(col) / FEF(loop)</td></tr><tr><td>01</td><td>Link100(act)/ link10(act)/ duplex/ FEF</td></tr><tr><td>10</td><td>Link100(act)/ link10(act)/ duplex(col)/ FEF(loop)</td></tr><tr><td>11</td><td>Link(act)/ speed/ duplex(col)/ FEF(loop) (default)</td></tr></table>
The setting can be updated by writing 01h[12:11]
* : when bi-color mode enabled, first two LED signals are combined to drive the bi-color LEDs. Link100(act)-> color one, Link10(act) or FEF (in fiber)-> color two.</td></tr>
<tr><td>36</td><td>LED_P2LPLINK/LedMd[1]</td><td>I/O, PU</td></tr>
<tr><td></td><td colspan="3"></td></tr>
<tr><td>37</td><td>LED_P2LPSPD/FrLinkEn3</td><td>I/O, PU</td><td>P2 Link Partner’s Speed /Test Done

P3 force link enable
0: enable
1: disable (default)
The setting can be updated by writing 35h[7]</td></tr>
<tr><td>38</td><td>LED_P2LPDUL/ANLmtDis</td><td>I/O, PU</td><td>P2 Link Partner’s Duplex /Test OK

Nway capability limited disable
0: limited
1: not limited (default)
The setting can be updated by writing 30h[3]</td></tr>
</table>

LED functions

	LED Mode			
LED pin	00	01	10	11 (default)
LED_P1LINK	**Dual color mode**	On: Link 100M Off: Unlink Flash: 100M Act	On: Link 100M Off: Unlink Flash: 100MAct	On: Link Off: Unlink Flash: Act
LED_P1SPD		On: Link 10M Off: Unlink Flash: 10MAct	On: Link 10M Off: Unlink Flash: 10M Act	On: 100M Off: 10M
LED_P1DUL	On: Full Off: Half Flash: Collision	On: Full Off: Half	On: Full Off: Half Flash: Collision	On: Full Off: Half Flash: Collision
LED_P1FEF	On: FEF detected Off: No FEF Flash: Enter loop back mode	On: FEF detected Off: No FEF	On: FEF detected Off: No FEF Flash: Enter loop back mode	On: FEF detected Off: No FEF Flash: Enter loop back mode
LED_P2LINK	Dual color mode	On: Link 100M Off: Unlink Flash: 100M Act	On: Link 100M Off: Unlink Flash: 100MAct	On: Link Off: Unlink Flash: Act
LED_P2SD		On: Link 10M Off: Unlink Flash: 10MAct	On: Link 10M Off: Unlink Flash: 10M Act	On: 100M Off: 10M
LED_P2DUL	On: Full Off: Half Flash: Collision	On: Full Off: Half	On: Full Off: Half Flash: Collision	On: Full Off: Half Flash: Collision
LED_P2FEF	On: FEF detected Off: No FEF Flash: Enter loop back mode	On: FEF detected Off: No FEF	On: FEF detected Off: No FEF Flash: Enter loop back mode	On: FEF detected Off: No FEF Flash: Enter loop back mode
	Normal operation		**When performing Auto Loop Back test**	
LED_P1LPLINK	On: Link partner Link ok Off: Link partner Unlink		Flash: Auto loop test enable. IP113S LF asks link partner to enter loop back mode.	
LED_P1LPSPD	On: Link partner is 100M Off: Link partner is 10M		On: Loop back test complete Off: Under loop back test	
LED_P1LPDUL	On: Link partner is Full Off: Link partner is Half		On: Pass Loop back test Off: Fail Loop back test	
LED_P2LPLINK	On: Link partner Link ok Off: Link partner Unlink		Flash: Auto loop test enable. IP113S LF asks link partner to enter loop back mode.	
LED_P2LPSPD	On: Link partner is 100M Off: Link partner is 10M		On: Loop back test complete Off: Under loop back test	
LED_P2LPDUL	On: Link partner is Full Off: Link partner is Half		On: Pass Loop back test Off: Fail Loop back test	

Dual color mode LED

	LED_P1LINK (LED_P2LINK)	LED_P1SPEED (LED_P2SPD)
Link off	1	1
100M link	1	0
100M link/Active	Flash	0
10M link	0	1
10M link/Active	0	Flash

<table>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Configuration (The following settings are latched at the end of power on Reset)</td></tr>
<tr><td>102</td><td>CFG_CutThrDis</td><td>I, PU</td><td rowspan="2">Modified Cut through mode disable
Converter mode disable

<table><tr><th>CFG_CutThrDis</th><th>CFG_CnvDis</th><th>Function</th></tr><tr><td>1</td><td>1</td><td>Store and forward mode (default)</td></tr><tr><td>0</td><td>1</td><td>Modified cut-through mode</td></tr><tr><td>1</td><td>0</td><td>Converter mode</td></tr><tr><td>0</td><td>0</td><td>Converter mode if duplex and speed of P01 equal P02, otherwise modified cut-through mode</td></tr></table>
The setting can be updated by writing 0Bh[1:0]</td></tr>
<tr><td>103</td><td>CFG_CnvDis</td><td>I, PU</td></tr>
<tr><td>104</td><td>CFG_IPGCompDis</td><td>I, PU</td><td>IPG compensation disable
0: Tx.IPG+80ppm
1: Tx.IPG+0ppm (default)
The setting can be updated by writing 01h[3]</td></tr>
<tr><td>105</td><td>CFG_IP113MEn</td><td>I, PU</td><td>IP113S LF can recognize IP113A/M OAM
0: disable
1: enable (default)
The setting can be updated by writing 39h[4]</td></tr>
<tr><td>106</td><td>CFG_BcstAllPktDis</td><td>I, PU</td><td>Broadcast all received frame disable
0: enable
1: disable (default)</td></tr>
<tr><td>107</td><td>CFG_AgingEn</td><td>I, PU</td><td>MAC address table aging enable
0: disable
1: enable (default)
The setting can be updated by writing 12H[1]</td></tr>
<tr><td>108</td><td>CFG_BkPEn</td><td>I, PU</td><td>Half duplex back pressure enable
0: disable
1: enable (default)
The setting can be updated by writing 34h[2:0]</td></tr>
<tr><td>109</td><td>CFG_P3LinkCpuDis</td><td>I, PU</td><td>P3 link to CPU disable
0: enable
1: disable (default)
The setting can be updated by writing 12h[3]</td></tr>
<tr><td>110</td><td>CFG_PassPause</td><td>I, PU</td><td>Pass PAUSE frame disable
0: enable
1: disable (default)
The setting can be updated by writing 33h[5:0]</td></tr>
</table>

Pin no.	Label	Type	Description
Configuration (The following settings are latched at the end of power on Reset)			
111	CFG_BcstBPDU	I, PU	**Broadcast BPDU frames** 0: discarded 1: broadcasting (default) The setting can be updated by writing 01H[4]
114	CFG_TrunkSet[0]	I, PU	**Trunk setting [1:0]** CFG_TrunkSet[1:0] 00:Port2 and Port3 Trunk 01:Port1 and Port3 Trunk 10:Port1 and Port2 Trunk 11:No Trunk (default)
115	CFG_TrunkSet[1]	I, PU	
116	CFG_TagPriDis	I, PU	**TAG priority disable** 0: enable 1: disable (default) The setting can be updated by writing 08H[4]
117	CFG_P1PriDis	I, PU	**P1 port based priority disable** 0:enable 1: disable (default) The setting can be updated by writing 08H[0]
118	CFG_P2PriDis	I, PU	**P2 port based priority disable** 0: enable 1: disable (default) The setting can be updated by writing 08H[1]
119	CFG_P3PriDis	I, PU	**P3 port based priority disable** 0: enable 1: disable (default) The setting can be updated by writing 08H[2]
120	CFG_WRRSet[0]	I, PD	**WRR Ratio[1:0]** 00:First in first out (default) 01:High priority: Low priority = 2:1 10:High priority: Low priority = 4:1 11:High priority: Low priority = 8:1
121	CFG_WRRSet[1]	I, PD	
122	CFG_SLEWFAST	I, PD	**PAD slew rate fast enable** 0: enable (default) 1: disable
123	CFG_DRIVE[0]	I, PD	**PAD output driving current [1:0]** CFG_DRIVE[1:0] 00: 2mA (default) 01: 4mA 10: 8mA 11: 12mA
124	CFG_DRIVE[1]	I, PD	
125	CFG_PWSAVE	I, PD	**Power saving mode enable** 0: enable (default) 1: disable

Pin no.	Label	Type	Description
Configuration (Real time setting)			
40	LFP	I, PD	**Linlk fault pass through** 0: disable (default) 1:enable Link status of one port is forwarded to the other port. This pin is real time setting instead of the latched value at the end of reset. The setting can be updated by writing 39H[15]
41	MC_FAIL	I, PD	**Media converter fails** 0: normal (default) 1: fail The setting can be updated by writing 39H[8]
42	AUTO_LPBK	I, PD	**Auto loop back test** 0: disable (default) 1:enable A port will perform loop back test for once if its corresponding TS1000En pin is pulled high and there is a low-to-high transition on this pin. The corresponding LED pin LED_PxLPLINK is always flashing if this pin stays at high. It provides an easy way to instruct IP113M performing loop back test without programming registers. The setting can be updated by writing 40H[4]
43	MISCE/MiiPHYMdEn3	I/O, PU	**P3 MII I/F PHY mode_enable** 0: MAC mode 1: PHY mode (default)

Pin no.	Label	Type	Description
MDI			
8	TP_RX+	I	**TP receive pair**
9	TP_RX-	I	**TP receive pair**
11	TP_SD	I	**100Base-FX signal detect** In two-fiber mode, IP113S LF's TP_SD should be connected to SD pin of fiber Transceiver. When TP_SD is lower than 1.95V, link is downand far end fault patterns are generated on TP_TX+/TP_TX-. When TP_SD is higher than 2.15V, fiber signal is detected.
12	TP_TX+	O	**TP transmit pair**
13	TP_TX-	O	**TP transmit pair**
16	FX_TX+	O	**Fiber transmit pair**
17	FX_TX-	O	**Fiber transmit pair**
18	FX_SD	I	**100Base-FX signal detect** IP113S LF's FX_SD should be connected to SD pin of fiber Transceiver. When FX_SD is lower than 1.95V, link is down and far end fault patterns are generated on FX_TX+/FX_TX-. When FX_SD is higher than 2.15V, fiber signal is detected.
19	FX_RX+	I	**Fiber receive pair**
20	FX_RX-	I	**Fiber receive pair**

Pin no.	Label	Type	Description
SMI			
95	MDC	I/O	**Clock for serial management bus.** It's recommended to add a 30pf capacitor to ground for noise filetrring.
96	MDIO	I/O	**I/O data for serial manment bus**. It shoud be connected to VDD33 through a 1.5K pull up resistor. MDIO is an open drain
EEPROM Interface			
99	SCL	I/O, PU	**Serial EEPROM clock output**
100	SDA	I/O, PU	**Serial EEPROM data**
CPU Interface			
45	CPUC	I	**Serial CPU access clock input.** Please see the section of "Programming the Internal Register" for the usage of CPUC and CPUIO.
46	CPUIO	I/O, PU	**Serial CPU data**
44	INTB	O, PU	**Interrupt** 0: an interrupt happens. 1: no interrupt.

Pin no.	Label	Type	Description
Miscellaneous			
101	RESETB	I	**System reset (low active).** **It should be kept at "low" for at least 10 microseconds.**
127	OSCI	I	**Crystal/ Oscillator 25MHz input**
128	X2	O	**Crystal output**
39	OSC25M	O	**A 25Mhz reference clock output for other devices**
5	BGRES25	I	**Band gap resister** It is connected to GND throught a 6.19k(1%) resistor in application citcuit
2	REG_33_IN	I	**3.3V Power**
3	REG_25_OUT	O	**Regulat output** The interal linear regulator uses this pin to control external transistor to generates a voltages source 2.5V
Test mode			
97	TESTMODE	I, PD	**TEST pin** This pin shold be left open or connected to ground for normal operation
98	SCANMODE	I, PD	**Scan pin** This pin shold be left open or connected to ground for normal operation

Pin no.	Label	Type	Description
Power			
4 10 15	AVCC25		**Analog Power**
26 48 78 112	VDD25		**Digital Power**
34 49 63 94 79 126	VDD33		**Digital Power**
1 27 33 47 50 64 77 80 93 113	VSS		
6 7 14	AVSS		

3 Functional Description

3.1 Data forwarding

Related registers	0Bh[1:0].

IP113S LF supports four types of data forwarding mode, store & forward mode, modified cut-through mode, converter mode and pure converter mode. User can select one of the modes by programming register 0Bh[1:0].

3.2 Store & forward mode

Related registers	01h[5]

When IP113S LF works in “store & forward” mode, it begins to forward a packet to a destination port after the entire packet is received. The latency depends on the packet length. The maximum packet length is up to 2046 bytes in this mode. Different from a normal switch chip, IP113S LF supports options to forward IEEE802.3x pause frame. These options are default off and can be turned on by programming register 01h[5].

3.3 Modified cut-through mode

IP113S LF begins to forward the received data when it receives the first 64 bytes of the frame. The latency is about 512 bits time width. The maximum packet length is up to 2046 bytes in this mode. IP113S LF filters OAM frames in this mode. Please refer to pin description of pin 102 CFG_CutThrDis and pin 103 CFG_CnvDis or register 0Bh[1:0] for configuration information.

3.4 Converter mode

IP113S LF operates with small latency in this mode. The transmission flow does not wait until entire frame is ready, but instead it forwards the received data immediately after the data being received. Both transceivers in IP113S LF are interconnected via OAM engine and the internal switch engine and data buffer are not used. IP113S LF filters OAM farms and supports 9KB jumbo packet in this mode. Please refer to pin description of 102 CFG_CutThrDis and pin 103 CFG_CnvDis or register 0Bh[1:0] for configuration information. The switch engine in IP113S LF is disabled in this mode.

3.5 Pass through mode

IP113S LF operates with the minimum latency in this mode. Both transceivers in IP113S LF are interconnected via internal MIIs and the internal switch engine and data buffer are not used. IP113S LF pass all frames including OAM farms and supports 9KB jumbo packet in this mode. Please refer to pin description of PassDis or register 0Bh[2] for configuration information. The switch engine in IP113S LF is disabled in this mode. IP113S LF doesn’t support TS1000 when working in this mode.

In converter mode or pass through mode, it is strongly recommended that both TP port and fiber port of IP113S LF should work at 100M full duplex.

3.6 Operation mode summary

0Bh [2]	0Bh [1:0]	Modes	Packet forwarding	Latency	Switch & buffer	Max length	Note
1	X	Pure converter mode	OAM: pass Error: pass Good: pass Pause: pass	Min	Un-used	9KB	
0	00	Switch mode	OAM: filter Error: filter Good: pass Pause: option	Ethernet Packet length	Used	2046B	Forward pause frame options: Register 01h[5].
0	01	Converter mode	OAM: filter Error: pass Good: pass Pause: pass	OAM packet length	Un-used	9KB	
0	10	Modified cut-through mode	OAM: filter Error: pass Good: pass Pause: option	64 bytes	Used	2046B	Forward pause frame options: Register 01h[5].
0	11	Auto Converter mode	OAM: filter Error: pass Good: pass Pause: pass	OAM packet length	Un-used	9KB	Change to modified cut-through mode automatically, if duplex or speed of port 1 and port 2 are not equal.

3.7 Switch engine and queue management

3.7.1 Address learning and hashing

Related registers	12h[0]

IP113S LF's switch engine can handle up to 1024 MAC address entries. And it provides two kinds of hash method to maintain the MAC address table; one is the direct mapping and the other is the CRC-12 algorithm. When the direct mapping method is selected, register 12h[0] set to "1", IP113S LF recognizes the least significant 12 bits of the MAC address. When the CRC-12 algorithm is used, register 12h[0] set to "0"; IP113S LF executes the following equation to decide the address (location) in the MAC address table.

CRC-12 equation: X^12+X^11+X^3+X^2+X+1

Packets with the following conditions will not be stored in MAC address table.

- Erroneous packet
- 802.3x pause packet
- 802.1D Reserved Group packet
- Multicast source MAC address

3.7.2 Aging

Related registers	12h[1], 13h[7:0]

IP113S LF supports programmable aging time to meet various the system requirement, ranging from 384 sec to 98304sec ± 6.7%. User can program aging time by writing register 13h[7:0]. The address aging function can be disabled by programming register 12h[1].

3.7.3 Special packet handling

IP113S LF recognize the following type of packets by examining the field listed in the following table. Port 3 can be defined as a CPU port by writing "1" to register 12h[4].

					Action	
	DA	SA	Type	Register	12h[4]=1	12h[4]=0
Broadcast, Multicast	FF-FF-FF-FF-FF-FF 01-XX-XX-XX-XX-XX	--	--	12h[3]	0: can be sent to CPU port 1: can't be sent to CPU port except ARP	broadcast
STP	01-80-C2-00-00-**00**	--	--	01h[10]	0: broadcast 1: to CPU port	broadcast
802.3x Pause	01-80-C2-00-00-**01**	--	--	01h[5]	0: drop 1: broadcast	
Slow protocol	01-80-C2-00-00-**02**	--	--	01h[8]	0: drop 1: to CPU port	0: drop 1: broadcast
802.1x	01-80-C2-00-00-**03**	--	--	01h[9]	0: see 01h[4] 1: send to CPU port if 01[4]=0, otherwise broadcast	0: see 01h[4] 1: broadcast
BPDU	01-80-C2-00-00-**03~0F**	--	--	01h[4]	0: drop 1: broadcast	
ARP	--	--	0806			

Note:
1. "--" means don't care.

3.7.4 Inter frame gap compensation

Related registers	01h[3]

IP113S LF supports an option to transmit a packet with IPG shorter than min value defined IEEE802.3 for 80 ppm after 1ms transmission at 100Mbps or 10ms at 10Mbps. This function can be turned on by writing "1" to register 01h[3].

3.7.5 Packet buffer re-allocation

Related registers	0Ch~0Eh

IP113S LF uses internal packet buffer to store and forward packets. The default setting of port 1 and port 2 is bigger than port 3 (port 3 is assumed to connect to CPU usually). IP113S LF allows user to re-arrange the buffer allocation to fully utilize the memory resource. User can defined the size of shared area and per port's dedicate area by programming register 0Ch ~ 0Eh with the unit in pages. A page consists of f 64 bytes. It is note that the total page of the three ports can't exceed 426.

3.7.6 Flow Control

Related registers	10h~11h, 33h~34h, 01h[2], 01h[0]

IP113S LF supports two kinds of flow control mechanisms, backpressure for half duplex operation and IEEE 802.3x for full duplex operation.

3.7.6.1 IEEE802.3x

When operating in full duplex mode, IP113S LF supports IEEE802.3x flow control. Each port's flow control function can be enabled individually by programming register 33h[5:0]. When the packet count in buffer reaches the PAUSE Off threshold, IP113S LF generates a "Xoff" pause packet immediately or right after the current packet has been transmitted. When receiving a pause packet, the link partner stops transmission for a period of time defined in the pause packet. This prevents the buffer of IP113S LF from overrun. When the packet count in buffer is lower than the PAUSE On threshold, IP113S LF generates a "Xon" pause packet to notify the link partner the receiving buffer is available.

3.7.6.2 Back pressure

When operating in half duplex mode, the IP113S LF supports backpressure flow control. Each port's backpressure function can be enabled individually by programming register 34h[2:0]. When the packet count in buffer reaches the PAUSE On threshold, IP113S LF generates a jam pattern to back off the link partner.

IP113S LF supports collision_based and carrier-based backpressure to back off the link partner. When the collision_based backpressure is enabled, register 01h[2] set to "0"; IP113S LF generates a jam pattern only when the link partner is transmitting data. When detecting a collision on line, the link partner stops transmission until a back off time expires. The backpressure mechanism follows the CSMA/CD behavior defined in IEEE802.3. When the carrier_based backpressure is enabled, register 01h[2] set to "1", IP113S LF transmits null packets continuously to prevent link partner's transmission when the buffer is not available.

To prevent the packet loss due to excessive collision caused by backpressure mechanism, user can clear bit 0 of register 01h to disable the drop function due to 16 consecutive collisions defined in IEEE802.3.

3.7.7 Broadcast Storm Control

Related registers	12h[2], 13h[14:8]

To prevent the broadcast storm, the IP113S LF implement a broadcast storm control mechanism. When this function is enabled, a port begins to drop incoming broadcast packets if the received broadcast packet counts reach the threshold defined in register 13h[14:8]. User can enable the broadcast storm protection function by writing "1" to register 12h[2].

3.7.8 SMII, MII

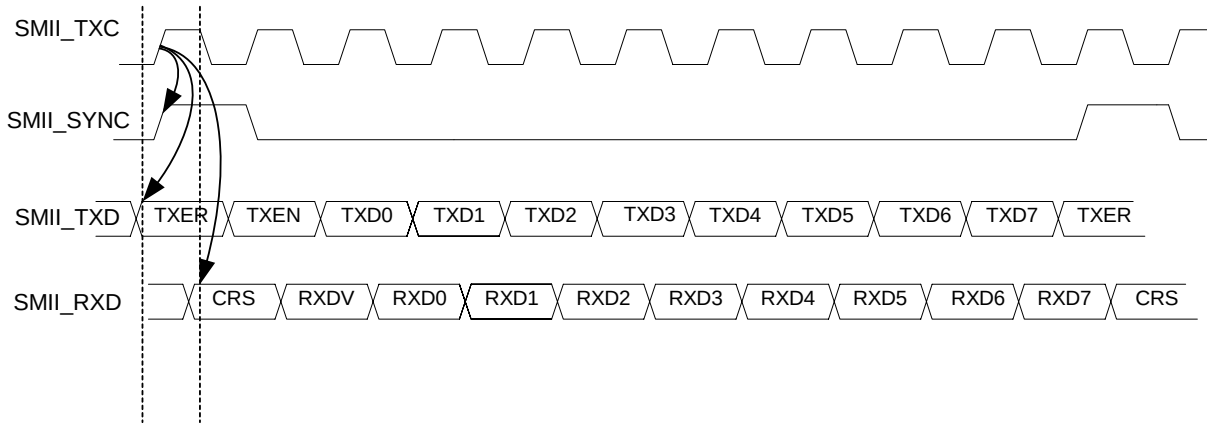
Related registers	F7h~F8h

3.7.8.1 SMII I/F

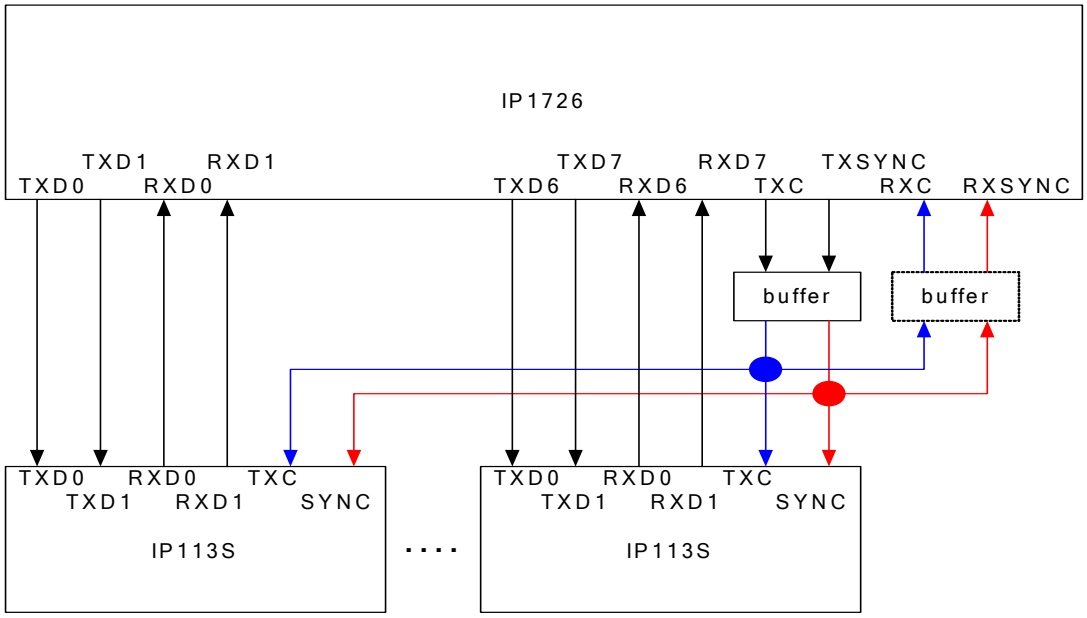
IP113S LF sends out data on SMII_RXD at the rising edge of SMII_TXC and uses SMII_SYNC to indicate the start of a 10-bit frame. By recognizing the high pulse of the SMII_SYNC, a MAC can capture the correct data stream.

A MAC sends out data on SMII_TXD at the rising edge of SMII_TXC and uses SMII_SYNC to indicate the start of a 10-bit frame. By recognizing the high pulse of the SMII_SYNC, IP113S LF samples the correct data at the rising edge of SMII_TXC.

Accompanied by the high pulse of SMII_SYNC, the TXEN, TX_ER and 8-bit TX data are present on the TXD pin. For the RX part of SMII, the CRS, RXDV, and 8-bit RX data are present on the RXD pin.



It is note that both SMII_SYNC and SMII_TXC are input signals and are shared with all IP113S LF as shown in the following figure.



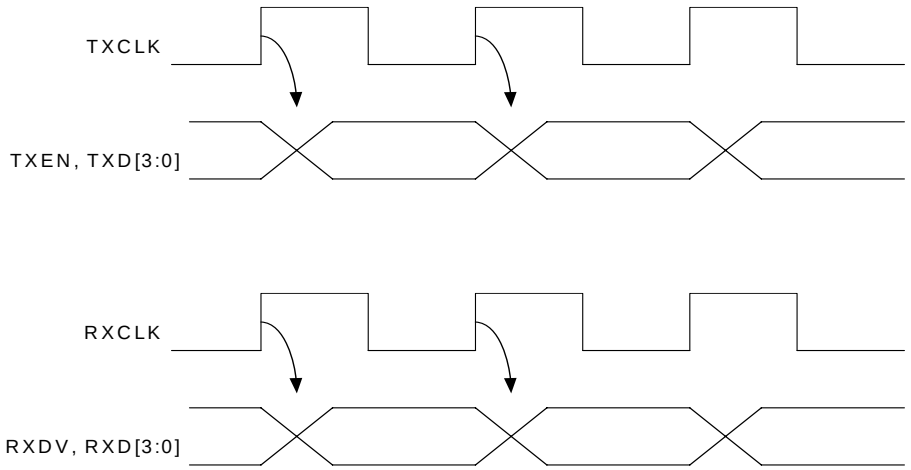
3.7.8.2 MII I/F

IP113S LF sends out data RXDV and RXD[3:0] at the rising or falling edge (reversed-MII) of RXCLK. By recognizing the RXDV and RXD[3:0], an external CPU can capture the correct data stream.

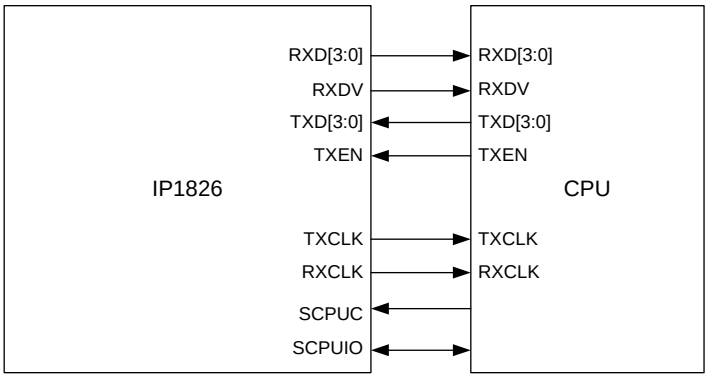
An external CPU sends out data TXD[3:0] and control signal TXEN at the rising edge of TXCLK. By recognizing the TXEN, TXD[7:0], IP113S LF can capture the correct data stream. IP113S LF samples the correct data at the rising edge of TXCLK.

Both TXCLK and RXCLK are sent out from IP113S LF. To fit the timing requirement, the delay on TXCLK and RXCLK can be adjusted by programming register F8h[6:7].

MII



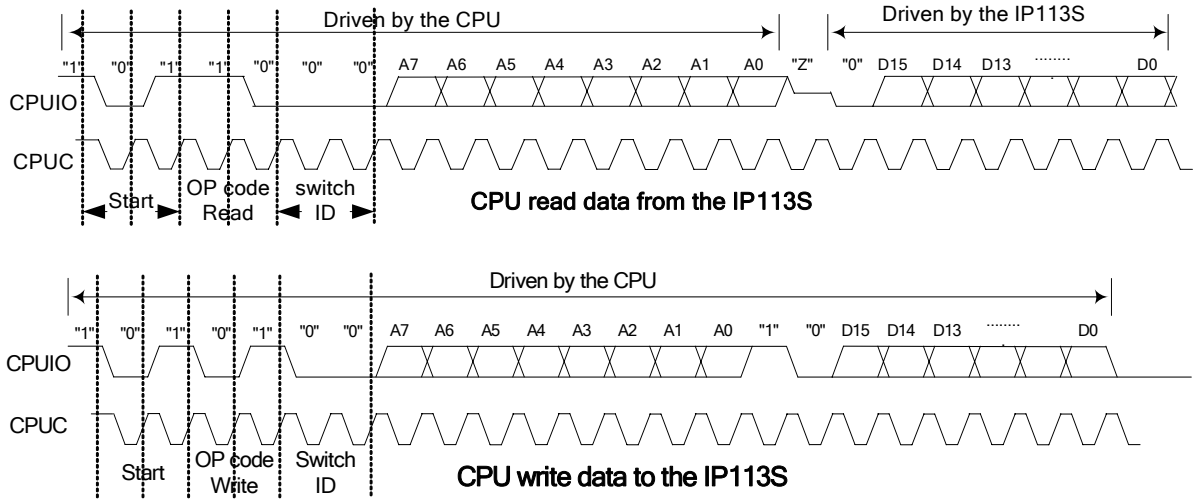
MII



3.7.9 CPU interface

There is no need to program the register of the IP113S LF for the generic application. However it's probably necessary to program the internal register to fit some special applications. The interface between the IP113S LF and the CPU is a serial bus, which comprises a clock and an I/O signal. Like the access cycle of the serial management interface, the serial interface comprises the switch ID, the read/write command, the address and the data. The access cycle is depicted as below.

The access cycle is much like the access cycle of MDC, MDIO. Care should be taken that the switch ID is 2-bit wide rather than 5-bit wide. The maximum frequency of CPUC is 2.5MHz.



3.7.10 Configure / access the port properties

Related registers	30h~34h, 38h, D0h[11]

User can configure the property of each port through CPU I/F. The property of each port can be configured individually. User can set the auto-negotiation, speed, and duplex function by writing register 30h~ 32h. When auto-negotiation is disabled, the speed and duplex depend on the setting in register 31h and 32h. When auto-negotiation is enabled, user can instruct a port to advertise all capability or the specific capability in register 31h and 32h by writing register 30h[3]. When auto MDI/MDIX is disabled (register D0h[11]=1), user can the MDI in MDI or MDIX mode by writing register 30h[4]. Because port 2 is a fiber port, its auto-negotiation function should be disabled. (If an external PHY of port 2 is used, auto-negotiation function is settable…)

The following table is an configuration example of port 1.

Nway	Nway limited	Speed	Duplex	Operation mode
30h[0]	30h[3]	31h[0]	32h[0]	
0	X	0	0	Force 10M half
0	X	0	1	Force 10M full
0	X	1	0	Force 100M half
0	X	1	1	Force 100M full
1	0	0	0	Auto-negotiation with 10M half capability
1	0	0	1	Auto-negotiation with 10M full/half capability
1	0	1	0	Auto-negotiation with 100M/10M half capability
1	0	1	1	Auto-negotiation with 100M/10M full/half capability
1	1	0	0	Auto-negotiation with 10M half capability
1	1	0	1	Auto-negotiation with 10M full capability
1	1	1	0	Auto-negotiation with 100M half capability
1	1	1	1	Auto-negotiation with 100M full capability

User can get the status of each port by reading register 38h. The registers provide the status of asyn pause function, syn pause function, duplex, speed and link of each port.

There is only two internal PHY for port 1 and port2. If user configures the properties of port3, IP113S LF will update the external PHY connected to port 3 through MDC/MDIO.

3.7.11 Force link

Related registers	35h[7:5]

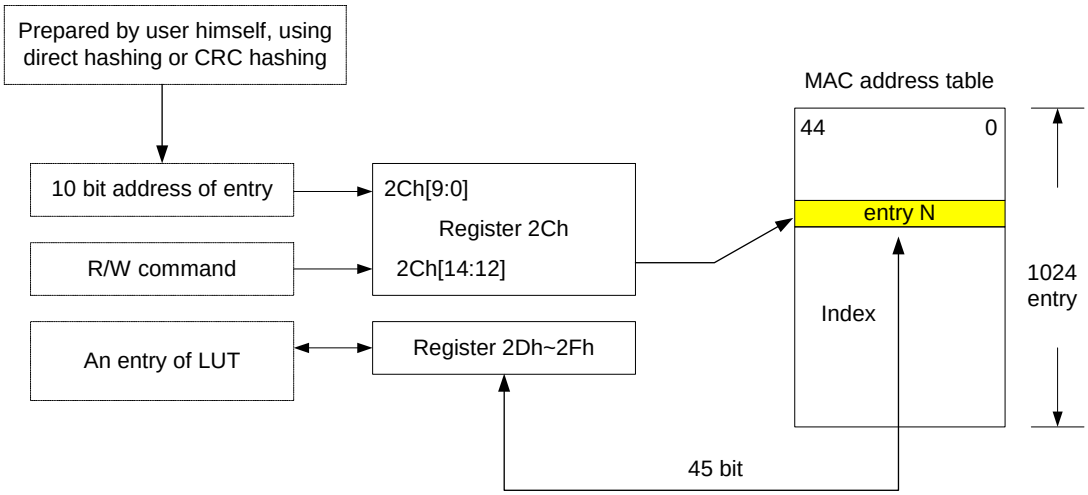
If an external PHY doesn't support SMI, a MAC can't set or get the status of the PHY and port is always link down. To prevent this situation, IP113S LF supports force-link function for an external PHY without SMI. User can force a port of IP113S LF to be link ok by programming register 35h[7:5].

3.7.12 Read / write MAC address table (LUT)

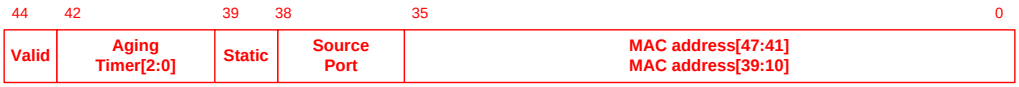
Related registers	2Ch~2Fh

User can access IP113S LF's MAC address table. The address space is 1K, from 0~1023. To write an entry to the MAC address table, user has to fill the 45-bit data to register 2Dh~2Fh, specify the address of the entry in register and issues a write command by programming register 2Ch. To read an entry from MAC address table, user has to specify the address of the entry and issues a read command by programming register 2Ch. The entry can be read from register 2Dh~2Fh. It is note that the bit 13~ 15 of register 2Fh is invalid, because of entry is 45-bit wide only.

Because IP113S LF builds and accesses the MAC address table with the address derived with hashing algorithm, user has to calculate the address of an entry in the same way before accessing the table. That is, if direct hashing is selected, register 12h[0] equal to 1, the address of an entry is the 12 lsb of a MAC address. If CRC hashing is selected, register 12h[0] equal to 0, the address of an entry is the 12 lsb of CRC result of a MAC address.



The format of MAC address table



3.7.13 Read / write PHY registers

Related registers	35h~37h, C0h~C6h, D7h

User can access the register of IP113S LF through CPU I/F. To read a register of PHY, user has to specify the address of the PHY, address of the register, and issue a read command by programming register 36h. User can poll the register 36h[13] to see if the access is completed. The content of the register can be read from register 37h.

To write a register of PHY, user has to fulfill the written data to register 37h in advance. And then, user has to specify the address of the PHY, address of the register, and issue a write command by programming register 36h

The associated PHY addresses from port 1 to port 3 are defined in register 35h[4:0].

IP113S LF supports an alternative to access the registers. Register C0h~C6h are mapped to register 0~6 of internal PHY of port 01. Register D7h is mapped to MII register 0 of internal PHY of port 02.

3.7.14 EEPROM interface

IP113S LF supports EEPROM I/F to access 24C04/08/16. At the end of reset, IP113S LF begins to download the content of EEPROM. Being an EEPROM master, IP113S LF downloads all the content of EEPROM only if the first two bytes in EEPROM are “1131h”. After reading EEPROM, the EEPROM I/F of IP113S LF becomes input pins.

The register address of IP113S LF should comply with the address of EEPROM. The mapping relationship between the IP113S LF registers and the EEPROM address are depicted in the following table.

EEPROM address	EEPROM content	IP113S LF’s Register
00h	11h	11h
01h	31h	31h
02h	Expected value	01h[15:8]
03h	Expected value	01h[7:0]
04h	Expected value	02h[15:8]
05h	Expected value	02h[7:0]
•••••• ••••••	•••••• ••••••	•••••• ••••••
FEh	Expected value	3Fh[15:8]
FFh	Expected value	3Fh[8:0]

Note:

1. The EEPROM ID should be set to “3’b000”; i.e. A2=0; A1=0; A0=0
2. IP113S LF downloads the content of the EEPROM ranging from address 00h to FFh; i.e. the register beyond this range is not recognized by IP113S LF.

3.7.15 MIBs counters

Related registers	5Dh~A3h

IP113S LF supports 2 groups of MIB counters. Each one consists of 17 statistic 32-bit counters and can be assigned to calculate the events on any one of the 3 ports by programming register 5Dh. User can read the counter from the read-only-and-clear registers in the following table.

		MIB group 1	MIB group 2
		5Dh[1:0] 00: for port 01 01: for port 02 10: for port 03 11: for port 03	5Dh[5:4] 00: for port 01 01: for port 02 10: for port 03 11: for port 03
		Low word, high word	Low word, high word
0	Rx byte count	60h, 61h	82h, 83h
1	Dropped packet event	62h, 63h	84h, 85h
2	Rx packet count	64h, 65h	86h, 87h
3	Rx broadcast packet count	66h, 67h	88h, 89h
4	Rx multicast packet count	68h, 69h	8Ah, 8Bh
5	Rx CRC/Align error packet count	6Ah, 6Bh	8Ch, 8Dh
6	Rx under size packet count (<64 bytes, CRC ok)	6Ch, 6Dh	8Eh, 8Fh
7	Rx over size packet count (>1522 bytes, CRC ok)	6Eh, 6Fh	90h, 91h
8	Rx fragment packet count (<64 bytes, bad CRC)	70h, 71h	92h, 93h
9	Rx jabber packet count (>1522 bytes, bad CRC)	72h, 73h	94h, 95h
10	Collision count	74h, 75h	96h, 97h
11	Rx 64 byte packet count	76h, 77h	98h, 99h
12	Rx 65-127 byte packet count	78h, 79h	9Ah, 9Bh
13	Rx 128-255 byte packet count	7Ah, 7Bh	9Ch, 9Dh
14	Rx 256-511 byte packet count	7Ch, 7Dh	9Eh, 9Fh
15	Rx 512-1023 byte packet count	7Eh, 7Fh	A0h, A1h
16	Rx 1024-1522 byte packet count	80h, 81h	A2h, A3h

3.7.16 Interrupt

Related registers	Mask register 35h[9:8], 43h[11:8], 5Dh; Status register 53h; D1h

IP113S LF supports one interrupt pin to indicate status change. When one of the following conditions happens, IP113S LF will assert the interrupt pins if the corresponding mask is disabled.

1. Link status changes on any port (mask: register 35h[9]; status: 53h[1])
2. A CPU read/write register command is completed (mask: register 35h[8]; status: 53h[0])
3. Link partner power abnormal (mask: register 43h[11:10]; status: 53h[5], 53h[4])
4. An OAM frame is received (mask: register 43h[9:8]; status: 53h[3], 53h[2])
5. MIB counter group pre-overflow (mask: register 5Dh[6], 5Dh[2]; status: 53h[7], 53h[6])

User can read register 53h[7:0] and D1h to identify the interrupt source. The polarity of interrupt pin is always low active and can't be configured.
When MIB counters pre-overflow interrupt indicates, user should read MIB counters in 20 sec.

3.7.17 Reset

Related registers	07h, 52h

There are several ways to reset IP113S LF, chip reset, software reset and MAC reset. To assert low on RESETB pin or writing "1" to register 52h[1] resets IP113S LF. The input should be kept at "0" for more than 1.6 microseconds after power up. IP113S LF supports software reset, user can reset IP113S LF by writing "1" to register 52h[0]. Besides reset whole chip, IP113S LF supports MAC reset function. User can reset MAC of each port individually by writing "1" to register 07h[2:0].

3.7.18 LED

Related registers	01h

IP113S LF supports 4 LED display modes as shown in the following table. User can configure the LED mode by setting pin 35/36 or programming register 01h[12:11]. The flash period is programmable. User can configure the flash period by programming register 01h[14:13].

	LED Mode			
LED pin name	00	01	10	11 (default)
LED_P1LINK	**Dual color mode**	On: Link 100M Off: Unlink Flash: 100M Act	On: Link 100M Off: Unlink Flash: 100MAct	On: Link Off: Unlink Flash: Act
LED_P1SPD		On: Link 10M Off: Unlink Flash: 10MAct	On: Link 10M Off: Unlink Flash: 10M Act	On: 100M Off: 10M
LED_P1DUL	On: Full Off: Half Flash: Collision	On: Full Off: Half	On: Full Off: Half Flash: Collision	On: Full Off: Half Flash: Collision
LED_P1FEF	On: FEF detected Off: No FEF Flash: Enter loop back mode	On: FEF detected Off: No FEF	On: FEF detected Off: No FEF Flash: Enter loop back mode	On: FEF detected Off: No FEF Flash: Enter loop back mode
LED_P2LINK	Dual color mode	On: Link 100M Off: Unlink Flash: 100M Act	On: Link 100M Off: Unlink Flash: 100MAct	On: Link Off: Unlink Flash: Act
LED_P2SD		On: Link 10M Off: Unlink Flash: 10MAct	On: Link 10M Off: Unlink Flash: 10M Act	On: 100M Off: 10M
LED_P2DUL	On: Full Off: Half Flash: Collision	On: Full Off: Half	On: Full Off: Half Flash: Collision	On: Full Off: Half Flash: Collision
LED_P2FEF	On: FEF detected Off: No FEF Flash: Enter loop back mode	On: FEF detected Off: No FEF	On: FEF detected Off: No FEF Flash: Enter loop back mode	On: FEF detected Off: No FEF Flash: Enter loop back mode

Dual color mode LED

	LED_P1LINK (LED_P2LINK)	**LED_P1SPEED (LED_P2SPD)**
Link off	**1**	**1**
100M link	**1**	**0**
100M link/Active	**Flash**	**0**
10M link	**0**	**1**
10M link/Active	**0**	**Flash**

The follwing LED pins show the status of remote IP113S LF in normal operation. When IP113S LF performs a loop back test, LED_PxLPLINK becomes flash and the other pins show the status of loop back test.

LED pin name	**Normal operation**	**When performing Auto Loop Back test**
LED_P1LPLINK	On: Link partner Link ok Off: Link partner Unlink	Flash: Auto loop test enable. IP113S LF asks link partner to enter loop back mode.
LED_P1LPSPD	On: Link partner is 100M Off: Link partner is 10M	On: Loop back test complete Off: Under loop back test
LED_P1LPDUL	On: Link partner is Full Off: Link partner is Half	On: Pass Loop back test Off: Fail Loop back test
LED_P2LPLINK	On: Link partner Link ok Off: Link partner Unlink	Flash: Auto loop test enable. IP113S LF asks link partner to enter loop back mode.
LED_P2LPSPD	On: Link partner is 100M Off: Link partner is 10M	On: Loop back test complete Off: Under loop back test
LED_P2LPDUL	On: Link partner is Full Off: Link partner is Half	On: Pass Loop back test Off: Fail Loop back test

3.8 Bandwidth Control

Related registers	02h~05h

IP113S LF implements a sophisticated data rate control mechanism, which is very useful for the bandwidth-limited network. By controlling both the ingress and the egress data rate, IP113S LF provides a variety of the bandwidth configuration. It limits the maximum byte counts, which a port can send or receive in a period of time. If the sending byte counts or receiving byte counts of a port in a period of time reaches a pre-defined data rate, it will stop transmitting or receiving data.

Each port's egress/ingress data rate can be programmed individually. The egress/ ingress rate of port1~port 3 are defined in register 02h~05h. The detail configuration is shown in the following tables. It is note that if maximum data rate is selected, for example 512kbps X (N=FF), IP113S LF disables the rate control mechanism and support wire speed data forwarding.

Egress bandwidth

	Port 1		Port 2		Port 3	
	Register 02h[0]=0	Register 02h[0]=1	Register 02h[1]=0	Register 02h[1]=1	Register 02h[2]=0	Register 02h[2]=1
Rate	32kbps x N	512kbps x N	32kbps x N	512kbps x N	32kbps x N	512kbps x N
N	Register 03h[7:0]		Register 04h[7:0]		Register 05h[7:0]	

Ingress bandwidth

	Port 1		Port 2		Port 3	
	Register 02h[8]=0	Register 02h[8]=1	Register 02h[9]=0	Register 02h[9]=1	Register 02h[10]=0	Register 02h[10]=1
Rate	32kbps x N	512kbps x N	32kbps x N	512kbps x N	32kbps x N	512kbps x N
N	Register 03h[15:8]		Register 04h[15:8]		Register 05h[15:8]	

3.9 VLAN

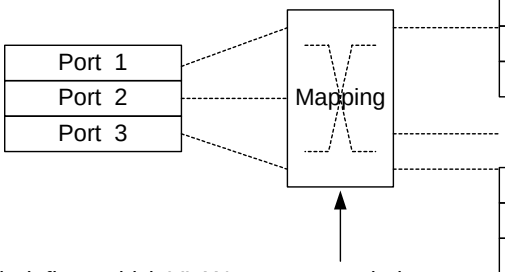
Related registers	1Ah~2Bh

IP113S LF supports port_based VLAN and tag_based VLAN. User can program register 1Bh[0] to select one of the VLAN.

3.9.1 Port_based VLAN

User can enable port_based VLAN function by writing 0 to register 1Bh bit 0. Each port uses four bit in registers 1Ah to select one of 16 port_base VLAN configuration defined in register 1Ch~2Bh. That is, a set of ports allowed to be forwarded from the source port. When a packet is received, IP113S LF forwards the packet according to MAC address and the VLAN members of the source port.

Take the following example for the detailed description. The data incoming from port 1 will be forwarded to the corresponding port defined in register 1Dh[14:12] if register 1Ah[3:0] is fulfilled with 0001. Similarly, The data incoming from port 2 will be forwarded to the corresponding port defined in register 2Ah[14:12] if register 1Ah[7:4] is fulfilled with 1110. The data incoming from port 3 will be forwarded to the corresponding port defined in register 1Fh[14:12] if register 2Bh[11:8] is fulfilled with 1111.



Index	Definition	Register
0000	VLAN member 0	1Ch[14:12]
0001	VLAN member 1	1Dh[14:12]
0010	VLAN member 2	1Eh[14:12]
.....		
1100	VLAN member 12	28h[14:12]
1101	VLAN member 13	29h[14:12]
1110	VLAN member 14	2Ah[14:12]
1111	VLAN member 15	2Bh[14:12]

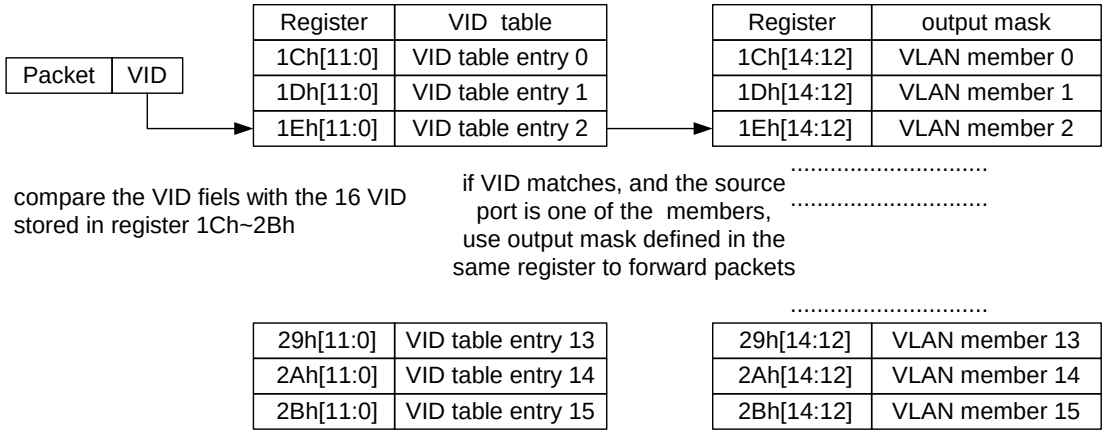
Register 1Ah defines which VLAN group a port belongs to.
1Ah[11:8]: port 3, 1Ah[7:4]: port 2, 1Ah[3:0]: port 1

3.9.2 Tag_based VLAN

IP113S LF supports a 16-entry VLAN table, VID table entry 0~15, to provide 16 active VLANs out of 4096 VLANs defined in IEEE802.1Q. User defines the 16 VID entries in the VID table, selects one VID from the table for each port and enables the tag VLAN function by programming register 1Ch~2Bh, 1Ah and register 1Bh bit 0.

When a tagged packet is received, IP113S LF compares the VID field in the packet with the VID stored in the register 1Ch~2Bh. If there is no matched VID, IP113S LF drops the packet. If it is matched and the source port is one of the members of the VID, IP113S LF uses the VLAN members defined in the same register as an output port mask to forward the packet. That is, a set of ports, to which the packet can be forwarded. IP113S LF forwards the packet according to MAC address and the output port mask. It is note that register 1Ch~ 2Bh define port_base VLAN configuration and tag_based VLAN table entry.

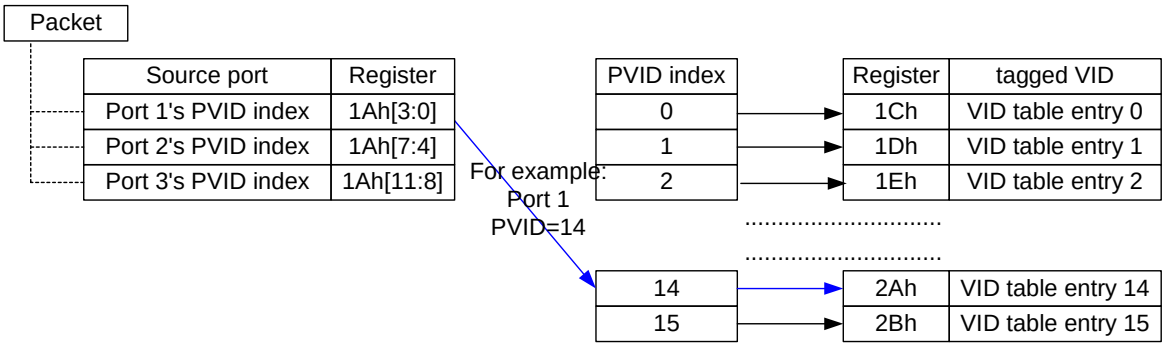
When an un-tagged packet is received, IP113S LF uses the default VID for the source port as the VID of the packet. One of the 16 VID entries is chosen as the default VID for a port according to the setting in the register 1Ah. IP113S LF forwards the packet in the same way as mentioned above. A tagged packet with VID equal to “000” is handled as an un-tagged packet.



3.9.3 Add/ Remove/ Modify VLAN tag

Related registers	1Bh

IP113S LF inserts or removes a tag of a frame if tagging/ un-tagging function is enabled. Tagging function of a port is enabled if the corresponding bit in register 1Bh[4:2] is set to “1”. A tag port always adds a tag to a forwarded packet with the VID selected by PVID. The tag information VID is defined in register 1Ch~2Bh and the PVID for each source port is defined in register 1Ah. A packet with VID equal to 12’b0 will be handled as un-tag frame. Un-tagging function of a port is enabled if the corresponding bit in register 1Bh[7:5] is set to “1”. A un-tag port always removes a tag from a forwarded packet. The operation is illustrated as follows. It is note that the VID defined in register 1Ch~2Bh for tagging is also used for 802.1Q tag_based VLAN.



Frame type of the received packet	The operation of a port which forwards the packet	
	Forward to a untagged filed	**Forward to a tagged field**
Untagged	Forward the packet without modification	1. Insert a tag using the default VLAN tag value of the source port 2. Calculate new CRC 3. The default VLAN tag value is defined in the register 1Ch~2Bh.
Priority-tagged (VLAN ID=0)	1. Strip tag 2. Calculate new CRC	1. Keep priority field. 2. Replace the tag with the default VLAN tag value of the source port 3. Calculate new CRC 4. The default VLAN tag value is defined in the register 1Ch~2Bh.
VLAN-tagged	1. Strip tag 2. Calculate new CRC	Forward the packet without modification

3.9.4 Packet across a VLAN

Related registers	1Bh[1]

Usually, a packet is not allowed to be forwarded across a VLAN. That is, if the destination port does not belong to the same VLAN, the packet is dropped. IP113S LF provides a leaky VLAN option to allow uni-cast packets to stride across a VLAN. This function is enabled by set bit 1 of register 1Bh.

3.10 Class of Service

Related registers	0Fh

IP113S LF implements two levels of priority queues, high priority and low priority. The priority for each packet is based on the following schemes:

1. Physical port
2. 802.1Q VLAN tag

Each incoming packet is mapped to either a high priority queue or a low priority queue. When no CoS function is enabled, the first-in/ first-out forwarding method is used. The output schedule mode and weight function for the ratio of high/low priorities is defined in register 0Fh[7:0].

When multiple CoS schemes are enabled, the data packet is treated as the high priority as long as any one of three CoS schemes is mapped to “high”.

Take the following example for detail explanation.

If a port is set as a low priority port, when it receives a packet, which embeds with high priority VLAN tag, this packet will be forwarded as a high priority packet. In the other words, the priority of a packet would be set to high if any of two CoS schemes is interpreted as the high priority.

3.10.1 Port based CoS

Related registers	08h[2:0]

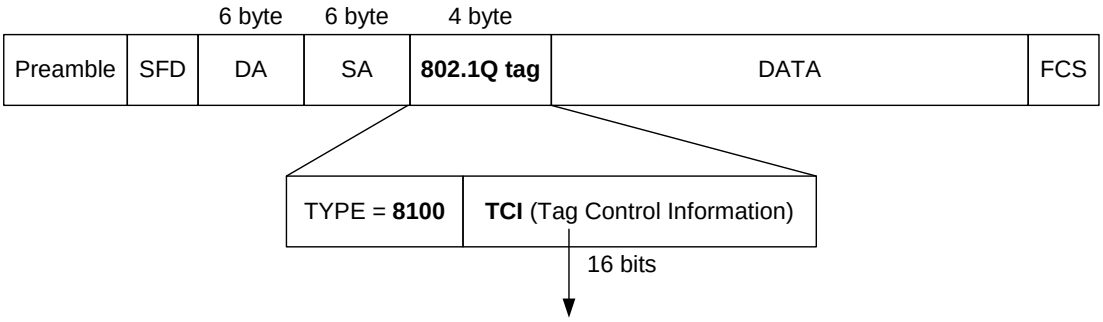
The port-based priority only concerns the physical port location in IP113S LF. A packet received by a high priority port is handled as a high priority packet. Each port of IP113S LF can be configured as a high priority port individually by programming registers 08h[2:0]. The bit 0~2 of register 08h corresponds to port 1 ~ port 3.

3.10.2 802.1Q priority tag based CoS

Related registers	08h[4]

When the CoS for 802.1Q VLAN tag is enabled, the IP113S LF will examine the 3 bits of priority field carried by a VLAN tag and map it to the corresponding priority. A packet with priority field ranging from 0 to 3 will be treated as a low priority packet, and will be stored in low priority queue. A packet with priority field ranging from 4 to 7 will be treated as a high priority packet, and will be stored in high priority queue. The CoS function of each port can be enabled by writing “1” to register 08h[4].

802.1Q priority tag based CoS



Bit[15:13]: Priority
IP1826 uses these bits to define priority.
Low priority: 000~011
High priority: 100~111

Bit 12: Canonical Format Indicator (CFI)
Bit[11~0]: VLAN ID.

3.11 MAC address based Security

Related registers	17h, 16h[2:0], 12h[4]

IP113S LF supports MAC address based security function. When IP113S LF receives a packet with un-known SA (a SA not found in the address table), it drops, broadcasts, or forwards to CPU port according to the setting in the register 17h. This function is valid only if the address learning function is disabled by clear the corresponding bits in register 16h[2:0]. User has to build up MAC address table through CPU I/F by programming 2Ch~2Fh in advance for IP113S LF to perform security function. Please refer to the section “Read / write MAC address table (LUT)”.

If user want IP113S LF to forward un-known SA packet to CPU, he has to defined port 3 as a CPU port by writing “1” to register 12h[4].

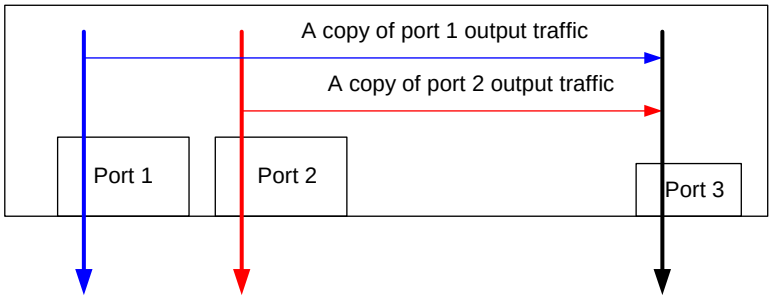
3.12 Port Mirroring (sniffer)

Related registers	19h

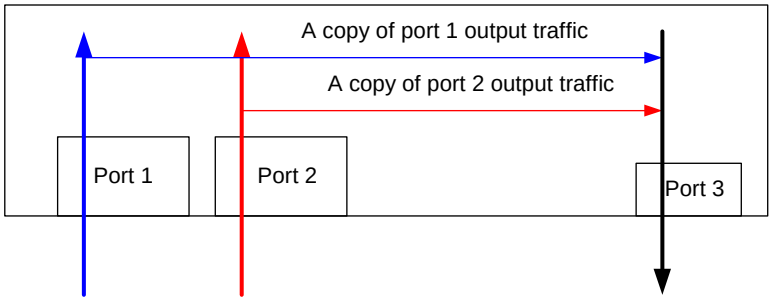
In some circumstances, the network administrator requires to monitor the network status. The port mirroring function helps the network administrator diagnose the network.

IP113S LF supports port mirroring function by adding the traffic of monitored ports (source ports) to the output traffic of snooping ports (destination ports). IP113S LF supports two kinds of mirroring methods: the ingress and the egress. The registers 19h[5:0] define the monitored ports (source port) and its corresponding monitor method. The register 19h[8:6] specifies the snooping ports (destination port).

For example, if user wants to monitor the output traffic of port 1 and port 2 from port 3 as shown in the following figure. He has to write “100” to register 19h[8:6] to choose port 3 as a monitoring port and write “000101”to register 19h[5:0] to make the output traffic of port 1 and 2 to be monitored. IP113S LF will copy the traffic out of port 1 and port 2 to port 3.



If user wants to monitor the input traffic of port 1 and port 2 from port 3 as shown in the following figure. He has to write “100” to register 19h[8:6] to choose port 3 as a monitoring port and write “001010”to register 19h[5:0] to make the input traffic of port 1 and 2 to be monitored. IP113S LF copy the input traffic of port 1 and port 2 to port 3.

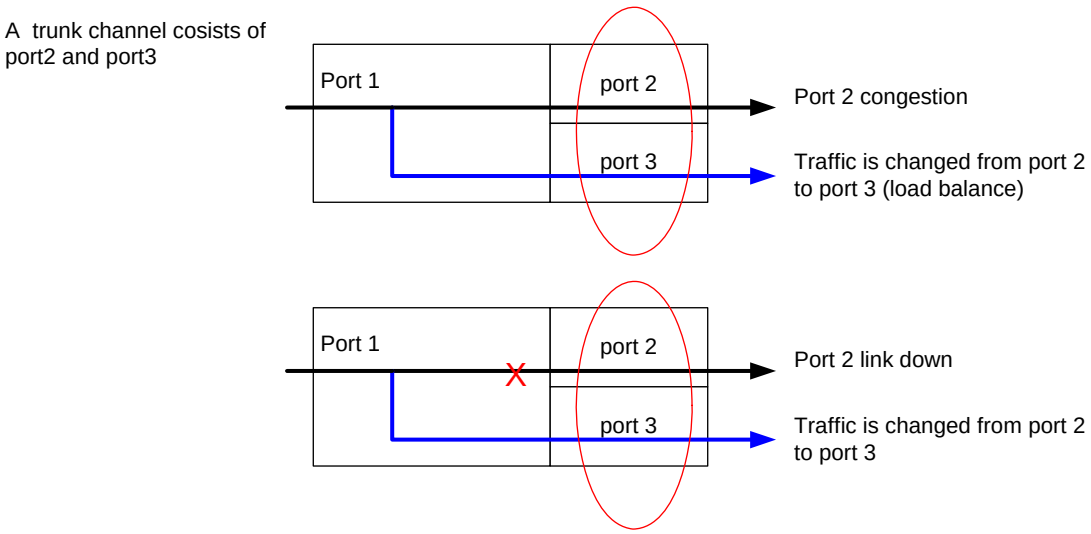


3.13 Trunk Channel

Related registers	18h

3.13.1 Trunk channel behavior

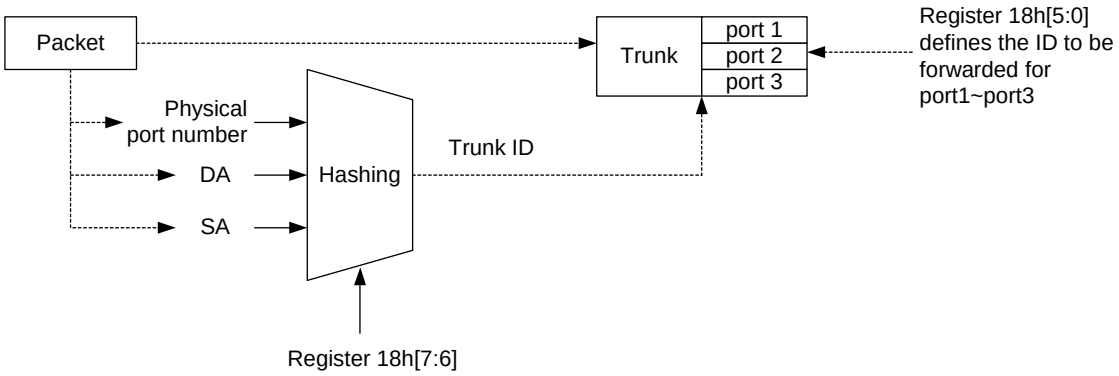
IP113S LF supports one trunk channel, which consists of each 2 of the 3 ports. A trunk channel works as if a “big” port with multiple times of bandwidth. IP113S LF supports auto-recover function. If the destination port of a packet is link down, IP113S LF forwards the packet to the other port of the trunk. User can specify the trunk ports by programming register 18h[5:0].



3.13.2 Load balance

To fully utilize the bandwidth in a trunk channel, IP113S LF supports load balance function. A physical port of a trunk can forward the packet of the trunk only if the trunk ID of the packet matches the setting in the registers 18h. When a packet is forwarded to a port in a trunk, its destination port is according to trunk ID. For example, if register 18h[1:0] is written with 01, only the packet with ID equal to 0 will be forwarded by port 1. If register 18h[3:2] is written with 10, only the packet with ID equal to 1 will be forwarded by port 2.

User can select a hashing mode for IP113S LF to use physical port number, DA, or SA to calculate trunk ID by programming registers 18h[7:6].

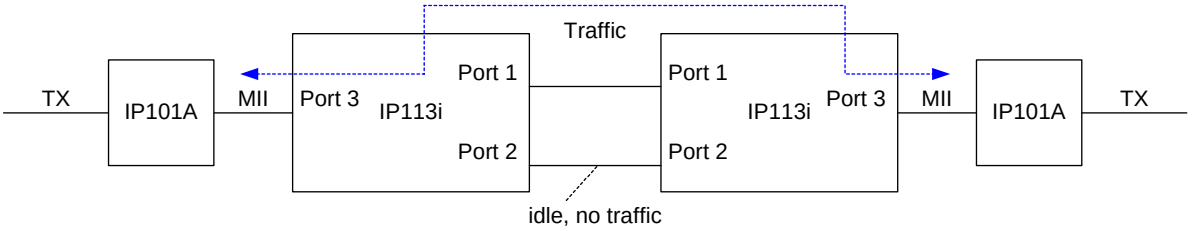


3.13.3 Use trunk channel function to implement redundant fiber channel

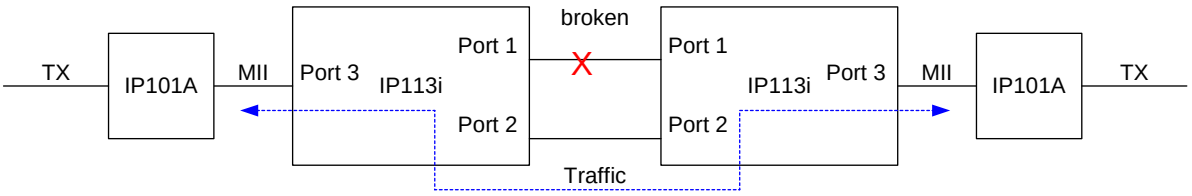
In the following example, port 1 and port 2 are trunked and port ID is used as trunk ID, by writing "0000_1001" to register 18h. In normal operation, there is no traffic on port 2 because of frames from port 3 always have trunk ID equal to "0". IP113S LF always forwards the frames from port 3 to port 1. (i.e. the port ID of port 1/2/3 is 0/1/0)

When the link status is down on port1, IP113S LF forwards the frames from port 3 to port2 due to the auto-recover function of IP113S LF. This achieves the requirement of redundant fiber channel.

Normal operation (assume port 1 is active)



If the fibers on port 1 is broken, traffic is switched from port 1 to port 2 automatically

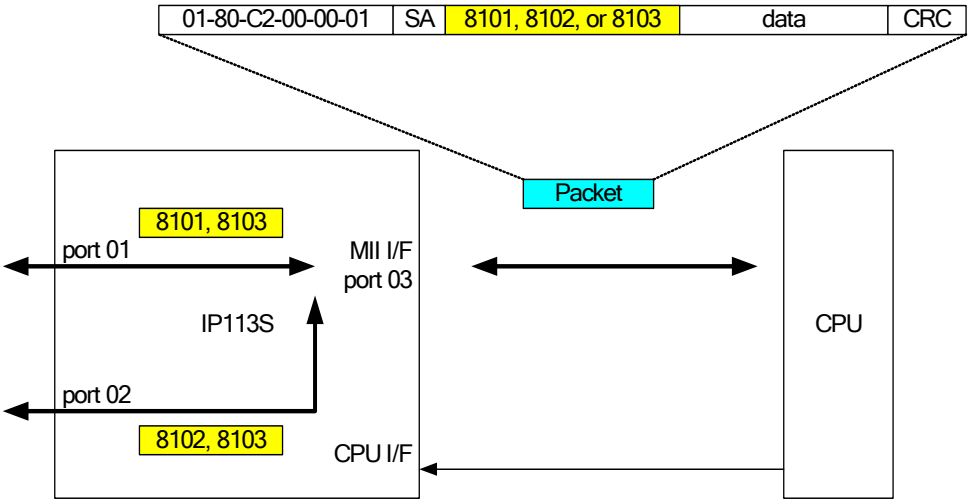


3.14 Special tag

Related registers	12h[5]

IP113S LF supports special tag function on port 03. If register 12h[5] is written with '1', the function is enabled. IP113S LF will behave as follows:

1. Add tag "8101" to a packet forwarded to port 03, if the packet is received from port 01.
2. Add tag "8102" to a packet forwarded to port 03, if the packet is received from port 02.
3. Forward a packet from port 03 to port 01 if the tag of the packet is "8101".
4. Forward a packet from port 03 to port 02 if the tag of the packet is "8102".
5. Forward a packet from port 03 to port 01 and port 02 if the tag of the packet is "8103".



3.15 Remote management

IP113S LF supports remote monitor, loop back test, and remote register R/W function. IP113S LF implement the function by exchanging OAM frames between two IP113S LFs. An OAM frames can be forwarded to/from port 1 or port 2 according to the setting in the register 39h ~3Fh. It is note that port1 doesn't support OAM frame when it works in 10BASE_T mode.

3.15.1 OAM frame

3.15.1.1 Frame format

IP113S LF supports two types of OAM frames, TS-1000 standard frame and ICplus proprietary. The only differences between the two frames are definitions of bit M24-M47. A TS-1000 OAM frame only defines the remote monitor and loop back test function. To implement remote register R/W function, IP113S LF supports ICplus proprietary OAM frames, which utilizes M24-M47 to carry the instruction and information. It is different from IP113M, which uses C8-C15 to implement remote register R/W function. The OAM frame format is shown below:

F0	F4	C0	C4	C8	C12	S0	S4	S8	S12	M0	M4	M8	M12	M16	M20	M24	M28	M32	M36	M40	M44	E0	E4
F1	F5	C1	C5	C9	C13	S1	S5	S9	S13	M1	M5	M9	M13	M17	M21	M25	M29	M33	M37	M41	M45	E1	E5
F2	F6	C2	C6	C10	C14	S2	S6	S10	S14	M2	M6	M10	M14	M18	M22	M26	M30	M34	M38	M42	M46	E2	E6
F3	F7	C3	C7	C11	C15	S3	S7	S11	S15	M3	M7	M11	M15	M19	M23	M27	M31	M35	M39	M43	M47	E3	E7

3.15.1.2 Bit definition of OAM frame and its corresponding registers (3Ah~3Eh)

<table>
<tr><th>Bit</th><th>Item</th><th>Description</th><th>Note</th></tr>
<tr><td>F7 – F0</td><td>Preamble</td><td>01010101</td><td></td></tr>
<tr><td>C0</td><td>Discriminator for the maintenance signal</td><td>0</td><td rowspan="5">Reg 3Eh</td></tr>
<tr><td>C1</td><td>Direction</td><td>0: terminal MC → central MC
1: central MC → terminal MC
(MC: media converter)</td></tr>
<tr><td>C3 – C2</td><td>Command</td><td>00: Reserved
10: Indication
01: Request
11: Acknowledge</td></tr>
<tr><td>C7 – C4</td><td>Version</td><td>0000</td></tr>
<tr><td>C15 – C8</td><td>Control signal</td><td>IP113S LF use M[47:24] to implement the function of read/write link partner's registers, instead of C[15:8]. But it can recognize the command of read/write link partner's registers issued by IP113M using C[15:8].
<table>
<tr><th colspan="8">C15~C8</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>01</td><td>Loop test start</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td><td>Loop test finished</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10</td><td>Status indication</td></tr>
<tr><td colspan="7"></td><td>11</td><td>Reserved</td></tr>
</table>
Definition in IP113M
<table>
<tr><th colspan="6">C15~C8</th><th>Function</th></tr>
<tr><td colspan="5">Address [4:0]</td><td>R/W</td><td>11</td><td>Remote R/W</td></tr>
</table>
</td></tr>
</table>

Bit	Item	Description	Note
S0	Condition of power	0: normal, 1: power off	Reg 3Dh
S1	Situation of receiving optical power	0: normal, 1: abnormal	
S2	Terminal/ network side link	0: link up, 1: link down If S11="1", S2="X"	
S3	MC (media converter) fails	0: normal, 1: abnormal	
S4	Informing way for optical receiving power off	0: OAM frame 1: Far end fault indication	
S5	Status indication for loop test	0: normal mode, 1: under loop test	
S6	Information for notice of terminal link status (Available for option B or not)	0: terminal IP113S LF does not support option B. 1: terminal IP113S LF supports option B, which can inform speed, duplex, and auto-negotiation in terminal IP113S LF. If S11 = "1", S6="X'	
S8 – S7	Terminal link speed	00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: others It is valid, if S6 = "1". If S2 or S11 = "1", S7, S8 = {X, X}	
S9	Duplex for the terminal side	1: full duplex, 0: half duplex It is valid, if S6 = "1". If S6 ="0", S9="0". If {S7, S8} = {1,1}, S9="X" If S2 or S11 = "1", S9="X"	
S10	Auto-negotiation capability for the terminal side	1: available, 0: un-available It is valid, if S6 = "1". If S6 ="0", S10="0". If {S7, S8} = {1,1}, S10="X" If S11 = "1", S10="X"	
S11	Number of interface in Terminal/ network side	0: one UTP 1: more than one UTP	
S15 – S12	Reserved		
E7 – E0	FCS	CRC – 8 FCS calculation area: C0 - M47	

Bit	Item	Description	Note
M23 – M0	Vender code	Vender code for TTC standard It is C30900h.	Reg 3Ah Reg 3Bh[7:0]
Definition of M47-24 in IP113S LF when M[25:24]=11 (ICplus proprietary, not TS-1000 standard)			
M47 – M40	Byte data	Data written to terminal side or read back from terminal side	Reg 3Bh[15:8] Reg 3Ch
M39 – M32	Address	Address of controllable registers of terminal side	
M31 – M30	Model	Model name 01: for IP113S LF Others: reserved	
M29 – M28	Version	Version control 00 (default)	
M27	Read/write	Read/ write control 0: read command 1: write command	
M26	H/L	High / low byte indication for M47~M40 0: low byte of accessed register 1: high byte of accessed register	
M25~M24	OP	Operation mode 00: Normal mode 01: Extend mode (for remote control) 10: reserved 11: reserved Note: Extend mode checks M[23:0], too.	
Definition of M47-24 of IP113S LF when M[25:24]=00, compatible to IP113M (TS-1000 standard)			
M47 – M24	Model number	Specified by vender It is 000000h.	Reg 3Bh[15:8] Reg 3Ch

	OAM Remote Control Frame Format							
	M47 - M40	M39 - M32	M31 - M24					M23 - M0
TS-1000 Standard	Model Number							Vender Code
ICplus proprietary	Byte data	Address	Model	Ver.	R/W	H/L	OP	Vender Code

3.15.2 Remote monitor

Related registers	3Eh~3Fh, 44h~4Dh, 4Fh~50h

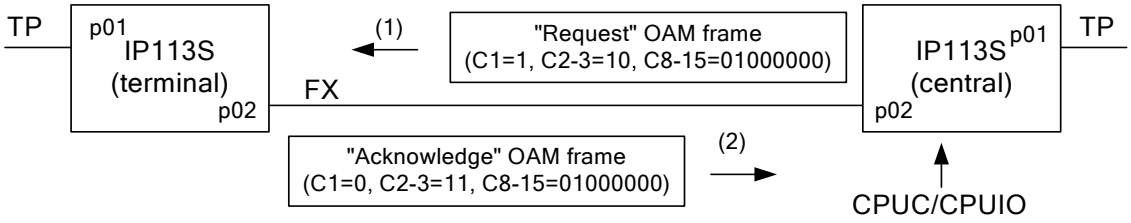
Remote monitor is a function defined in TS-1000 standard. Refer to the diagram below; two IP113S LF are connected through port2, users can instruct central IP113S LF, on the right, to issue a status request frame defined in TS-1000 to get status of terminal IP113S LF. User has to write “0206h” to register 3Eh and write “0003h” to register 3Fh to trigger a status request OAM frame. The M field in the frame is ICplus’s VID and is independent of the setting in register 3Ah~3Ch.

The terminal IP113S LF, on the left, receives the status request frame and sends out a acknowledge frame, which carries its current status when it is available. The central IP113S LF receives the acknowledge frame and stores the status of terminal IP113S LF to register 50h (or 4Fh, OAM frame is received from port1 of central IP113S LF). The information of bit 5, 8, and 15 of register 50h (4Fh) are supported by ICplus proprietary OAM of IP113M only. The entire acknowledge OAM frame is store to register 49h~4Dh(or 44h~48h, if OAM frame is received from port1 of central IP113S LF). The status of terminal IP113S LF is shown on the LEDs of central IP113S LF.

An interrupt will be generated when an OAM frame is received if the corresponding bit in register 43h[9:8] is set to “1”. User can identify the types of received OAM frames from port 02 (port 01) by reading register 43h[7:4] (register 43h[3:0]).

Although M field is not defined in TS-1000 for the remote monitor function, a terminal IP113S LF always sends out an acknowledge OAM frame with a M field with no remote read/write command defined in IP113S LF. Because IP113S LF always checks all field of an OAM frame.

Or, you can just enable the auto indication function of terminal IP113S LF. Any status changes defined in TS-1000 will auto send out an indication OAM from terminal IP113S LF.



Step 1: Central IP113S LF’s written registers and issued OAM frame								
Register	Reg 3Fh [3:0]	Reg 3Eh			Reg 3Dh	Reg 3Ch	Reg 3Bh	Reg 3Ah
OAM frame		C1	C2~C3	C8~C15	S0-16	M32- 47	M16-31	M0-15
	0011	1	10	0100-0000	--	--	--	--
Step 2: Central IP113S LF’s received OAM frame and stored registers								
OAM frame		C1	C2~C3	C8~C15	S0-16	M32- 47	M16-31	M0-15
		0	11	0100-0000	Valid status	--	--	--
From P2		Reg 49h			Reg 50h, 4Ah	Reg 4Dh	Reg 4Ch	Reg 4Bh
From P1		Reg 44h			Reg 4Fh, 45h	Reg 48h	Reg 47h	Reg 46h

“--”: Means don’t care

3.15.3 Remote control read/write

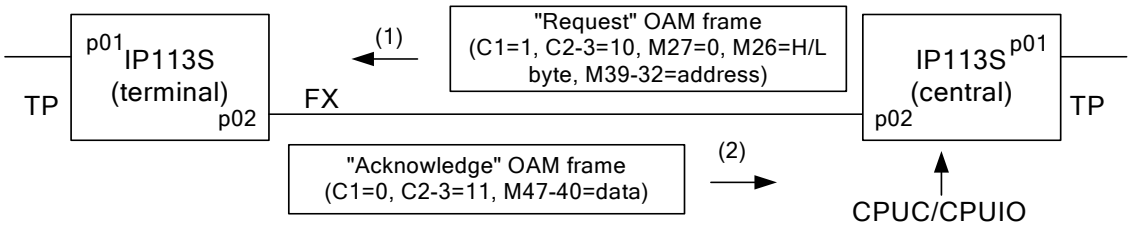
3.15.3.1 Remote control read

Related registers	3Ah~3Fh, 44h~4Dh

Remote control read function is not defined in TS-1000 standard; it is a proprietary function. Users can instruct central IP113S LF to issue a remote control read frame to read the register of terminal IP113S LF by programming register 3Bh~3Ch. The register 3Ch[7:0] are filled with the address of accessed register and register 3Bh[15:8] are filled with “41h” for low byte access (or “45h” for high byte access). Then, user has to write “0206h” to register 3Eh and write “0003h” to register 3Fh to trigger a status request OAM frame.

The terminal IP113S LF receives the frame and sends out the content of the register to central IP113S LF when it is available. The central IP113S LF receives the frame and stores the data to register 4Dh [15:8]. The entire acknowledge OAM frame is store to register 49h~4Dh(or 44h~48h, if OAM frame is received from port1 of central IP113S LF). The status of terminal IP113S LF is shown on LED of central IP113S LF.

As mentioned in the section of remote monitor, user can identify the types of received OAM frames from port 02 (port 01) by reading register 43h[7:4] (register 43h[3:0]).



Step 1: Central IP113S LF’s written registers and issued OAM frame								
Register	Reg 3Fh [3:0]	Reg 3Eh			Reg 3Dh	Reg 3Ch	Reg 3Bh	Reg 3Ah
OAM frame		C1	C2~C3	C8~C15	S0-16	M32- 47	M16-31	M0-15
	0011	1	10	0100-0000 C[8:9] can’t be “11”	--	M27=0, read; M26=H/L, M29-32= Address		ICplus VID[15:0]
Step 2: Central IP113S LF’s received OAM frame and stored registers								
OAM frame		C1	C2~C3	C8~C15	S0-16	M32- 47	M16-31	M0-15
		0	11	0100-0000	Valid status	M40-47=Data		--
From P1		Reg 44h			Reg 4Fh, 45h	Reg 48h	Reg 47h	Reg 46h
From P2		Reg 49h			Reg 50h, 4Ah	Reg 4Dh	Reg 4Ch	Reg 4Bh

“--”: Means don’t care

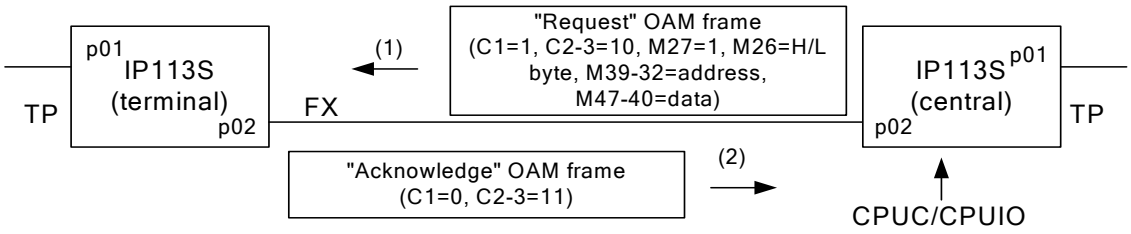
3.15.3.2 Remote control write

Related registers	3Ah~3Fh, 44h~4Dh

Remote control write function is not defined in TS-1000 standard; it is a proprietary function. Users can instruct central IP113S LF to issue a remote control write frame to write the register of terminal IP113S LF by programming register 3Bh~3Ch. The register 3Ch[7:0] are filled with the address of accessed register, 3Ch[15:8] are filled with the data, and register 3Bh[15:8] are filled with "49" for low byte access (or "4D" for high byte access). Then, user has to write "0206h" to register 3Eh and write "0003h" to register 3Fh to trigger a status request OAM frame.

The terminal IP113S LF receives the frame; write the specific register according to the content of the frame and sends out an acknowledge frame with its current status when it is available. The central IP113S LF receives the frame to make sure the operation is completed. The entire acknowledge OAM frame is store to register 49h~4Dh(or 44h~48h, if OAM frame is received from port1 of central IP113S LF). The status of terminal IP113S LF is shown on LED of central IP113S LF.

As mentioned in the section of remote monitor, user can identify the types of received OAM frames from port 02 (port 01) by reading register 43h[7:4] (register 43h[3:0]).



Step 1: Central IP113S LF's written registers and issued OAM frame								
Register	Reg 3Fh [3:0]	Reg 3Eh			Reg 3Dh	Reg 3Ch	Reg 3Bh	Reg 3Ah
OAM frame		C1	C2~C3	C8~C15	S0-16	M32- 47	M16-31	M0-15
	0011	1	10	0100-0000 C[8:9] can't be "11"	--	M27=1, write;M26=H/L, M29-32=Address M40-47=Data		ICplus VID[15:0]
Step 2: Terminal IP113S LF acknowledgement								
OAM frame		C1	C2~C3	C8~C15	S0-16	M32- 47	M16-31	M0-15
		0	11	0100-0000	Valid status	--	--	--
From P1		Reg 44h			Reg 4Fh, 45h	Reg 48h	Reg 47h	Reg 46h
From P2		Reg 49h			Reg 50h, 4Ah	Reg 4Dh	Reg 4Ch	Reg 4Bh

"--": Means don't care

If a remote control OAM is received and processing, any local register's r/w action will interrupt this process!! The register read/write priority is as follows:

Local CPU r/w > OAM received from P02 > OAM received from P01 > EEPROM > PIN initial setting

3.15.3.3 Response to a remote R/W command issued by IP113M

Related registers	39h[4]

Besides responses to a remote control frames issued from a remote IP113S LF, IP113S LF supports an option to recognize a remote control frames issued by IP113M. This option is enabled by set register 39h[4].

For an IP113S LF OAM frame, remote R/W command is embedded in M[47:24]. For an IP113M OAM frame, command is embedded in C[15:8] with C[9:8] equal to 2'b11. IP113S LF only responses to the IP113M remote R/W commands which access register 0~18d, 20d, 22d, 23d, and 31d (0~12h, 14h, 16h, 17h and 1Fh) if the option is enabled. Register 0~12h in IP113M are mapped to register C0h~D2h in IP113S LF. For register 14h, 16h, 17h and 1Fh in IP113M, there is no direct mapping registers in IP113S LF. IP113S LF will translate the request to the appropriate registers. This makes IP113S LF interoperable with IP113M.

IP113S LF doesn't response to OAM frame issued from IP113M if the option is disabled or the accessed register is not supported in IP113S LF.

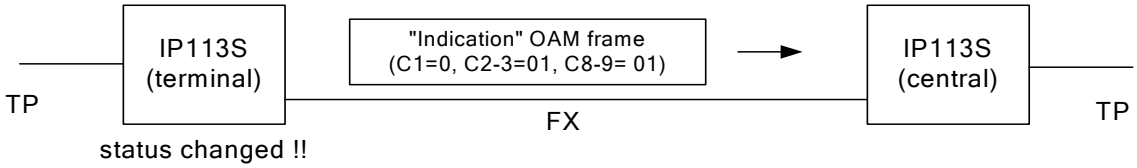
3.15.4 Auto sends (Status change notice)

Related registers	39h, 44h~4Dh, 4Fh~50h

IP113S LF sends out status frame automatically, without receiving status request frame if pin AUTO_SEND is pulled high or register 39h[3] is set. It sends out the first status frame to a port when the link status of the port is established (it's FX port in the following diagram). It sends out status frames when the status on the other port has changed (it's TP port in the following diagram). IP113S LF uses a standard TS-1000 OAM frame to implement the function. Central IP113S LF uses the mechanism to get the status of the remote IP113S LF without SMI programming. IP113S LF doesn't send out proprietary OAM supported in IP113M.

There are two options for auto send function, option B and non-option B. The default setting is option B. User can write "0" to register 39h[2] for selecting non-option B.

Refer to the following diagrams, a terminal IP113S LF, AUTO SEND function is enabled and it sends indication frames to central IP113S LF if its status is changed.



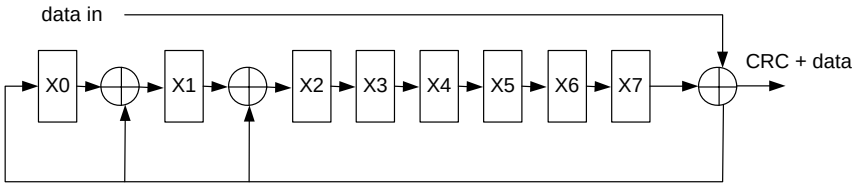
Terminal IP113S LF supports option B, which can inform speed, duplex, and auto-negotiation in terminal IP113S LF. In another words, the information of speed, duplex and auto-negotiation will be replaced by masked data, if terminal IP113S LF is operating in non-option B.

IP113S LF's issued OAM frame							
Register	Reg 39h[3]=1						
OAM frame	C1	C2~C3	C8~C15	S0-16	M32- 47	M16-31	M0-15
	0	10	0100-0000	Status Indication	Model no. and Vender ID		

(Status Indication: Please refer to 3.15.1.2 Bit definition of OAM frame)

The IP113S LF, on the other side, receives the status indication frame and stores the status to register 50h (or 4Fh, OAM frame is received from port1 of central IP113S LF). The information of bit 5, 8, and 15 of register 50h (4Fh) are supported by ICplus proprietary OAM of IP113M only. The entire OAM frame is store to register 49h~4Dh(or 44h~48h, if OAM frame is received from port1 of central IP113S LF). The status of terminal IP113S LF is shown on the LEDs of central IP113S LF. Besides TS-1000 standard auto-send frames, IP113S LF can recognize proprietary auto-send frames issued by IP113M.

CRC polynomial for OAM frame: X8 + X2 + X + 1



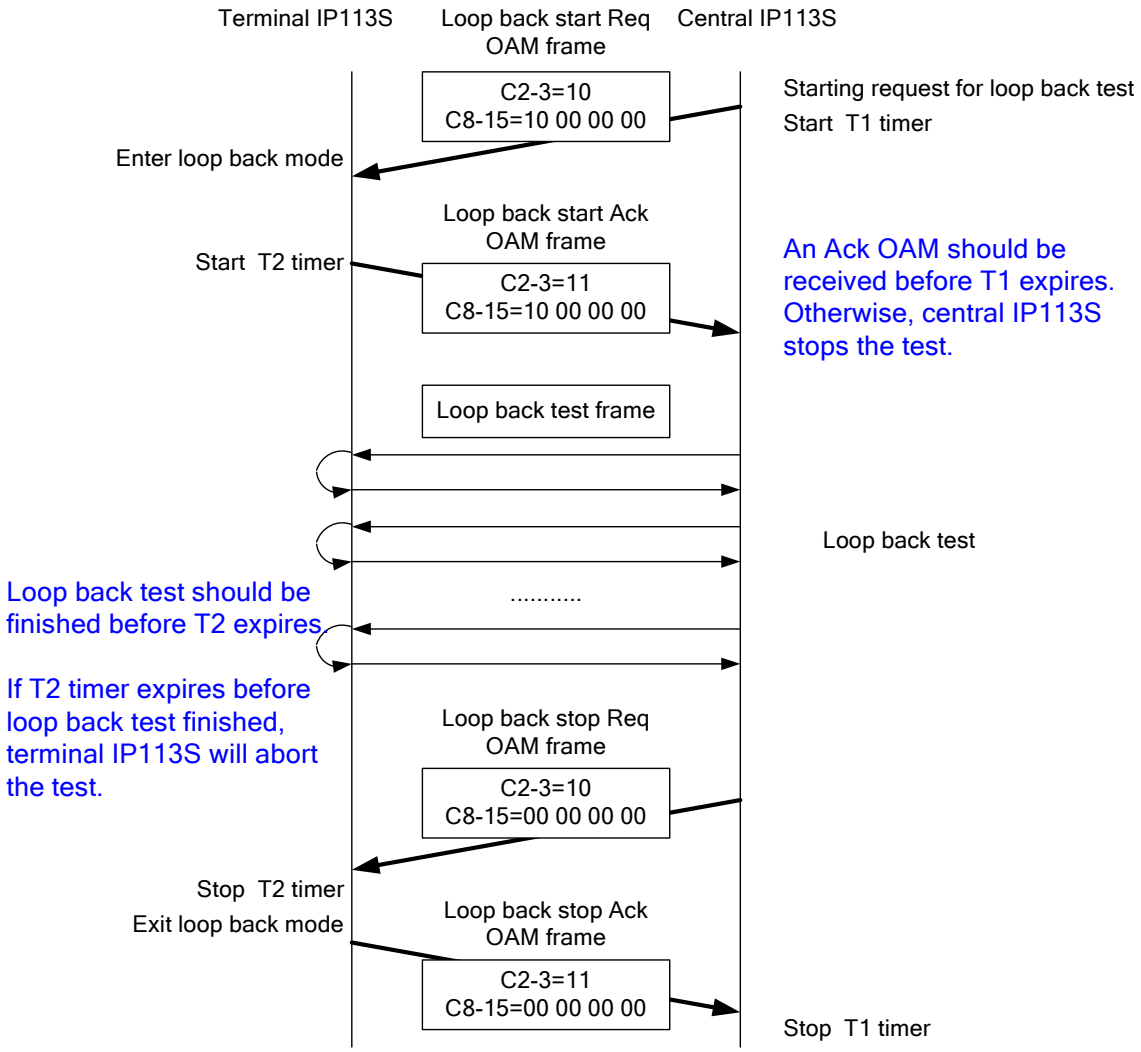
CRC calculation

3.15.5 Loop back test

3.15.5.1 Loop back test sequence defined in TS-1000

The following diagram shows the loop back sequence defined in TS-1000 standard. User can program the register of central IP113S LF to start and to end the test by exchanging OAM frame with the terminal IP113S LF. T1 and T2 timers are used to abort the test automatically when error happens during the test period.

IP113S LF supports two kind of loop back test function, in-band loop back test and out-band loop back test. For an out-band loop back test, the loop back test packet is generated by an external packet source; for an in-band loop back test, the loop back test packet is generated by central IP113S LF.



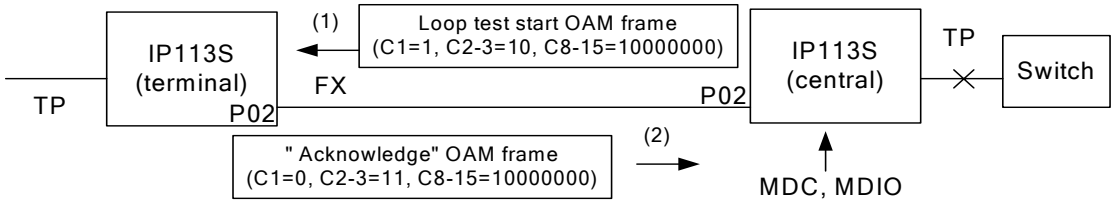
3.15.5.2 Out-band loop back test

Users can instruct central IP113S LF to issue an OAM frame to request a loop back test. User has to write “8006h” to register 3Eh and write “0003h” to register 3Fh to trigger a loop back test start OAM frame. The M field in the frame is ICplus’s VID and is independent of the setting in register 3Ah~3Ch. T1 timer in central IP113S LF begins to count when it issues a loop back test request OAM to terminal IP113S LF. An acknowledge OAM frame should be received before T1 expires, otherwise central IP113S LF releases from the loop back test.

After receiving the loop test start OAM frame, the terminal IP113S LF starts its T2 timer and becomes in loop back mode. Once the terminal IP113S LF entry the Loop back mode, the port which is not on the Loop back path will be turned off automatically. User also can disable this function by writing “1” to Reg39[9] before IP113S LF entry the Loop back mode, to keep the port’s existing status.The Loop back test should be finished before T2 timer expires. If the expected test time exceeds T2, user has to instruct central IP113S LF to issue a remote write OAM to disable T2 timer of terminal IP113S LF to make sure the test not aborted by terminal IP113S LF.

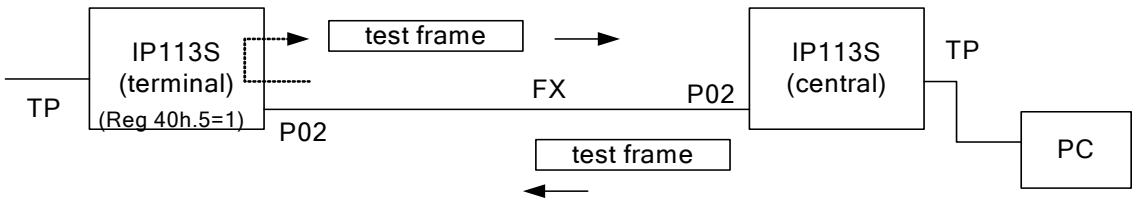
Users can feed packet with an external packet source, such as a PC. After finishing loop back test, user has to write “0006h” to register 3Eh and write “0003h” to register 3Fh to trigger a loop back test finish OAM frame. After receiving the loop back test finished OAM frame, the terminal IP113S LF stops its T2 timer and becomes in normal mode. The procedure is illustrated in the following diagrams. T1 timer in central IP113S LF stops when it receives an acknowledge OAM from of loop back test finished from terminal IP113S LF.

1. Disconnect switch port and instruct the terminal IP113S to perform loop testand disable terminal T2 timer by programming central IP113S through SMI



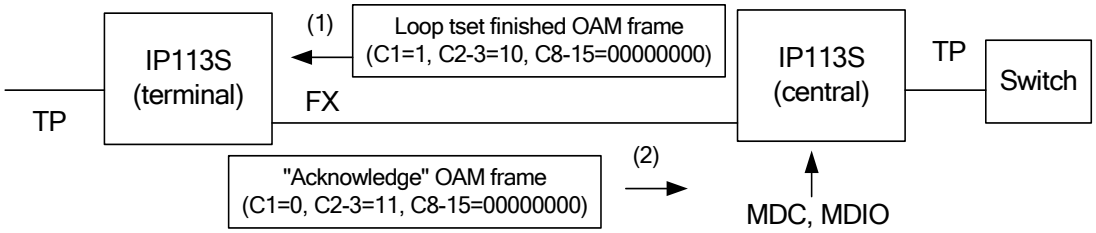
2. Terminal IP113S runs at loop back mode

3. PC forces test frames to central IP113S and terminal IP113S loops back the frames.



4. PC reports the loop back test result after sending all test frames.

5. Reconnect switch and instruct the central IP113S to end loop back test and enable T2 timer.



3.15.5.3 Auto in-band loop back test

Besides performing the loop back test with an external packet source, IP113S LF supports an alternative, auto in-band loop back test. IP113S LF sends out IEEE802.3 standard frame to do loop back test. User doesn't have to maintain the OAM exchange behavior, all he has to do is to specify the DA, data format, packet length and packet counts by programming register 09h and 41h in advance and then trigger an auto in-band loop back test by writing register 40h[4] (or 40h[0]). The signals of these two bits toggle from "0" to "1" will trigger auto loop back test once.

The procedure is illustrated in the following example, port 01 is a TP port and port 02 is a fiber port, which connects two IP113S LF.

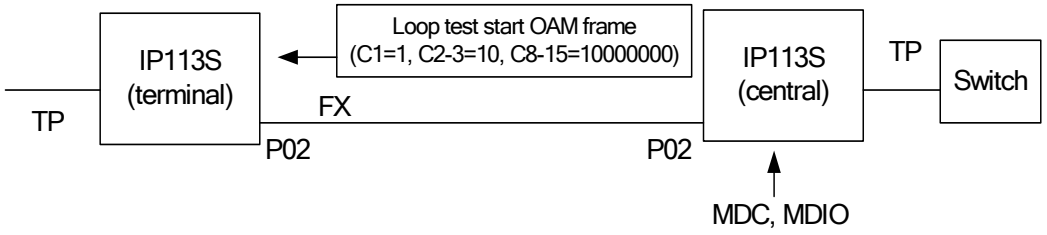
After writing "1" to register 40h[4], T1 timer in central IP113S LF begins to count when it issues a loop back test request OAM to terminal IP113S LF. An acknowledge OAM frame should be received before T1 expires, otherwise central IP113S LF releases from the loop back test.

After receiving the loop test start OAM frame, the terminal IP113S LF starts its T2 timer and becomes in loop back mode.Once the terminal IP113S LF entry the Loop back mode, the port which is not on the Loop back path will be turned off automatically. User also can disable this function by writing "1" to Reg39[9] before IP113S LF entry the Loop back mode, to keep the port's existing status.Loop back test should be finished before T2 timer expires. The expected in-band loop back test time is shorter than T2; because the maximum loop back packet count is 255, which spends less than T2. It is different from IP113M, which has to disable terminal T2 timer. Because the packet count of in-band loop back test in IP113M is not limited.

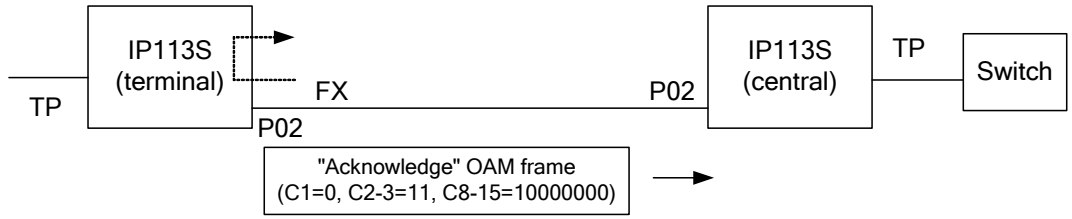
After acknowledged, central IP113S LF sends out the pre-defined frames onto port 02 to perform loop back test. After finishing loop back test, central IP113S LF sends out a loop back test finished OAM frame. After receiving the loop back test finished OAM frame, the terminal IP113S LF stops its T2 timer and quits loop back mode. T1 timer in central IP113S LF stops when it receives an acknowledge OAM from of loop back test finished from terminal IP113S LF. User can poll register 40h[6] to see if the test is completed and get the test result by reading register 40h[7].

The procedure is illustrated in the following diagrams.

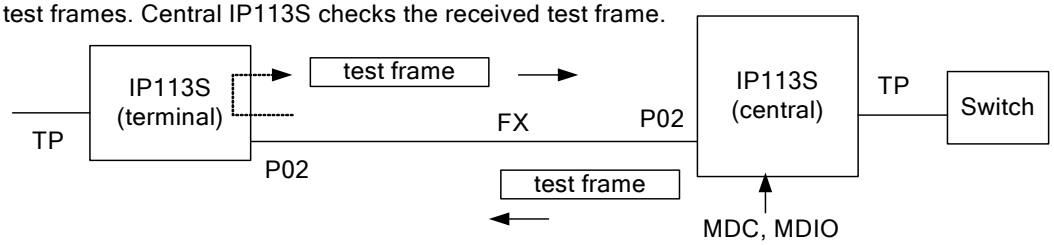
1. Specify test packets and instruct central IP113S to perform in-band loop back test



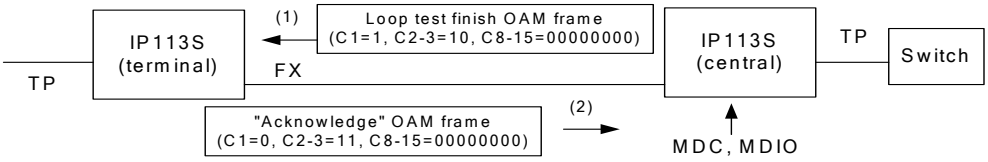
2. Terminal IP113S runs at loop back mode and acknowledges with maintenance frame



3. Central IP113S forces test frames to terminal IP113S and terminal IP113S loops back the test frames. Central IP113S checks the received test frame.



4. Central IP113S ends loop back test enables receive function of TP port and enable T2 timer of terminal IP113S.



5. To get test result by reading register 40h[7]. All user has to do is step 1 and step 5. From step 2 to step 4 are performed by IP113S automatically.

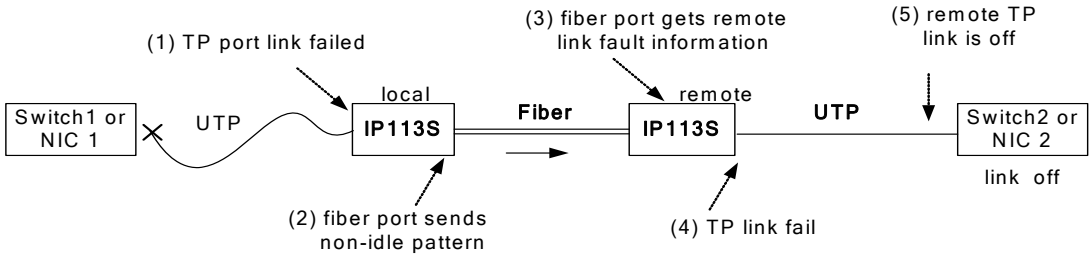
3.15.5.4 Start an auto in-band loop back test without programming (by pin)

IP113S LF supports another way to trigger auto in-band loop back test mentioned in the previous paragraph without register programming. All user has to do is to pull high AUTO_TEST pin. IP113S LF will perform auto in-band loop back test using the packet of default setting. The signal toggled from “0” to “1” will trigger auto loop back test once.

Step	Description
1	Set pin AUTO_TEST to “1” (The following step is executed automatically by IP113S LF)
1.1	Central IP113S LF sends loop back start request to terminal IP113S LF and goes to CST2 state.
1.2	Terminal IP113S LF sends loop back start acknowledge to central IP113S LF and enters loop back test mode.
1.3	Central IP113S LF goes to CST1 state and begins sending frames defined in register 09h and 41h.
1.4	Terminal IP113S LF loops back the received frames at the TP port’s PMD sub-layer.
1.5	Central IP113S LF checks the loop back frames and reports the result.
2	The LED pin LED_P1LPLINK and LED_P2LPLINK are Flash (on 80ms / off 20ms) during the auto loop back test period (AUTO_TEST is “1”).
3	The LED pin LED_P1LPSPD and LED_P2LPSPD indicates the loop back test complete (on) (when AUTO_TEST is “1”). The LED pin LED_P1LPDULand LED_P2LPDUL indicates the loop back test ok (on) (when AUTO_TEST is “1”)
4	If another auto loop back test is needed, set AUTO_TEST to “0” and then “1”. That is, AUTO_TEST is triggered whenever there is a low-to-high transition on this pin.

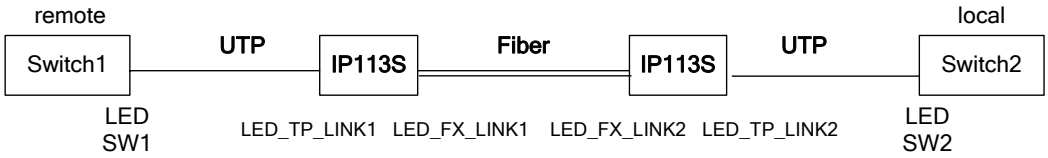
3.16 Link fault pass through

When link fault pass through function is enabled, link status on TX port will inform the FX port of the same device and vice versa. From the link fault pass through procedure illustrates in the figure below, if link fail happens on IP113S LF's TX port (1), the local FX port sends non-idle pattern to notice the remote FX port (2). The remote FX port then forces its TX port to link failed after receiving the non-idle pattern (4). In other words, this mechanism will alert the link fault status of local TX port to the remote converter's TX port, and the link status of the remote TX port will become off. Link status LED will also be off for both IP113S LF and its link partner. This function can be enabled by writing "1" to register 39h bit 15.



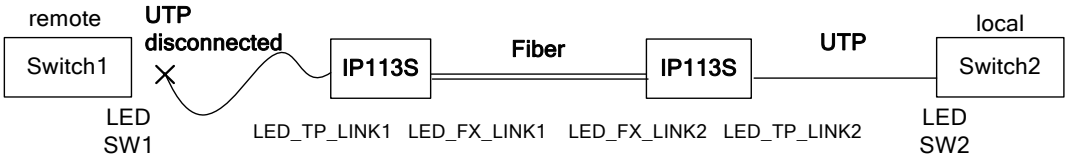
The procedure of link fault pass through

3.16.1 Normal case



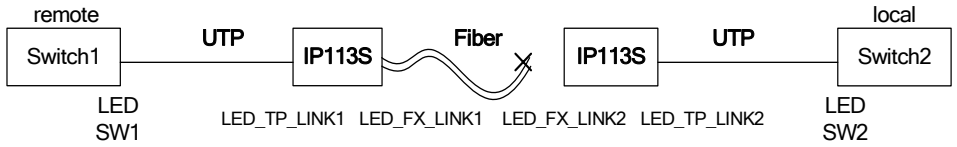
Link LED on SW1	LED_TP_LINK1	LED_FX_LINK1	LED_FX_LINK2	LED_TP_LINK2	Link LED on SW2
ON	ON	ON	ON	ON	ON

3.16.2 Remote TP port disconnected



Link LED on SW1	LED_TP_LINK1	LED_FX_LINK1	LED_FX_LINK2	LED_TP_LINK2	Link LED on SW2
Off	Off	Off	Off	Off	Off

3.16.3 FX port disconnected



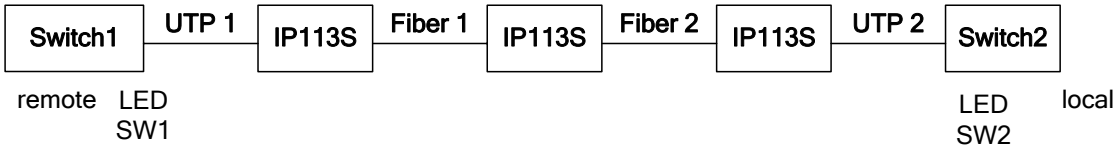
Link LED on SW1	LED_TP_LINK1	LED_FX_LINK1	LED_FX_LINK2	LED_TP_LINK2	Link LED on SW2
Off	Off	Off	Off	Off	Off

3.16.4 LED diagnostic functions for fault indication

LED_TP_LINK	LED_FX_LINK	LED_FX_SD	LED_FX_FEF_DET	Status
On	On	On	Off	Link ok
Flash	Flash	On	Off	Link ok & activity
Off	Off	On	Off	Remote TP link off
Off	Off	Off	Off	Fiber RX off, Fiber TX/ RX off
Off	Off	On	On	Fiber TX off

Note
Flash: flash period can be modified from 01h[14:13]
Link fault pass through is enabled.

3.16.5 Link fault pass through in FX to FX application



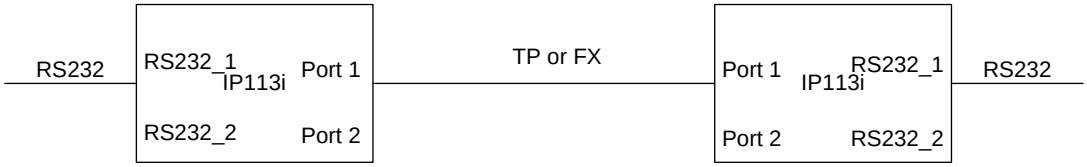
LED SW1 and LED SW2 are both off, if either UTP1, Fiber1, Fiber2 or UTP2 is broken and link fault pass through is enabled. That is, if link status is ok on switch port then all segments are guaranteed link good.

3.17 RS232 extension

IP113S LF can be configured as two independent Ethernet to RS232 converters as shown in the following table. Each is useful in the application of extending the length of RS232 cable. The distance between two RS232 devices is extended to the limitation of UTP or fiber of Ethernet.

Function	Setting	Register value
OP Mode	Converter mode	0Bh[2:0]=010 / 011
Dual PHY mode	Enabled	0Ah[8]= 1
Ext. MAC I/F	RS232	0Ah[5:4]=11 0Ah[3:0]=0000

User can use TS-1000 loop back test function to test the interconnection between both IP113S LF in this mode. Although IP113S LF supports dual RS232-Ethernet but they are two independent pathes and it doesn't support back up function.



4 Register Map

R = Read; W = Write; R/W = Read/Write

Address (Hex)	Description	Control
0x00	ID of IP113S LF	Switch
0x01	MAC miscellaneous configuration	Switch
0x02~0x05	Bandwidth width control	Switch
0x06	MAC receive enable	Switch
0x07	MAC reset control	Switch
0x08	Priority setting	Switch
0x09	MAC TS-1000 auto loop-back test frame format setting	Switch
0x0A	MAC data path flow setting	Switch
0x0B	Switch operation mode	Switch
0x0C~0x0E	Memory page setting	Switch
0x0F	Output queue schedule control	Switch
0x10~0x11	Flow control threshold	Switch
0x12	ARL miscellaneous configuration	Switch
0x13	Broadcast storm and LUT aging timer setting	Switch
0x14	Forward data frame setting	Switch
0x15	MAC transmit enable	Switch
0x16	ARL learning mode	Switch
0x17	Security configuration	Switch
0x18	Port trunk configuration	Switch
0x19	Port mirroring configuration	Switch
0x1A	Port VID index setting	Switch
0x1B	VLAN operation configuration	Switch
0x1C~0x2B	VLAN table entry 0~15 configuration	Switch
0x2C	CPU access LUT control	Switch
0x2D~0x2F	CPU access LUT data	Switch
0x30	Auto-negotiation setting	Switch
0x31	Speed setting	Switch
0x32	Duplex setting	Switch
0x33	802.3x flow control setting	Switch
0x34	Backpressure flow control setting	Switch
0x35	SMI miscellaneous configuration	Switch
0x36	CPU access PHY's registers control	Switch
0x37	CPU access PHY's registers data	Switch
0x38	Port link status	Switch
0x39	OAM miscellaneous configuration	Switch
0x3A~3C	OAM vendor code and model number M[47:0] for Tx.	Switch
0x3D	OAM status data S[15:0] for Tx.	Switch

Address (Hex)	Description	Control
0x3E	OAM control signals and instruction identifier C[15:0] for Tx.	Switch
0x3F	Remote control OAM frame transmitting configuration	Switch
0x40	TS-1000auto loop back test configuration	Switch
0x41	Packet number for TS-1000 auto loop back test	Switch
0x42	Auto loop back test result counter	Switch
0x43	OAM frame receiving configuration	Switch
0x44	P01 Link partner's control signals and instruction identifier C[15:0]	Switch
0x45	P01 Link partner's status data S[15:0]	Switch
0x46~0x48	P01 Link partner's vendor code and model number M[47:0]	Switch
0x49	P02 Link partner's control signals and instruction identifier C[15:0]	Switch
0x4A	P02 Link partner's status data S[15:0]	Switch
0x4B~0x4D	P02 Link partner's vendor code and model number M[47:0]	Switch
0x4E	Local status	Switch
0x4F	P01 Link partner status	Switch
0x50	P02 Link partner status	Switch
0x51	(Reserved)	Switch
0x52	Chip miscellaneous configuration	Switch
0x53	Chip interrupt status report	Switch
0x54~0x58	(Reserved)	Switch
0x59	(Reserved)	Switch
0x5A	Analog macro configuration	Switch
0x5B~0x5C	(Reserved)	Switch
0x5D	RMON MIBs configuration	Switch
0x5E~0x5F	(Reserved)	Switch
0x60~0x81	RMON MIBs group1	Switch
0x82~0A3	RMON MIBs group2	Switch
0xC0	MII Control Register for P01 :MII register 0	Nway
0xC1	MII Status Register for P01 :MII register 1	Nway
0xC2	MII PHY identifier Register 1 for P01 :MII register 2	Nway
0xC3	MII PHY identifier Register 2 for P01 :MII register 3	Nway
0xC4	MII AN Advertisement Register for P01 :MII register 4	Nway
0xC5	MII AN Link Partner Base Page Ability Register for P01 :MII register 5	Nway
0xC6	MII AN Expansion Register for P01 :MII register 6	Nway
0xC7~0xC8	(Not used)	
0xC9~0xCF	(Reserved)	Dsp
0xD0	MII Special Control Register for P01 :MII register 16	Nway
0xD1	MII interrupt Control Register for P01 :MII register 17	Nway
0xD2	MII Extended Status Register for P01 :MII register 18	Nway
0xD3~0xD6	(Not used)	
0xD7	MII Control Register for P02 :MII register 0	Nway

4.1 MAC Control Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
00H	00H 01H	IP113S LF's ID	RO	0x1131
01H	02H 03H	MAC miscellaneous configuration: bit[14:13] : LED blinking speed selection 00: 50ms/50ms on/off 01: 100ms/100ms on/off (default) 10: 150ms/150ms on/off 11: 200ms/200ms on/off bit[12:11] : LED display modes selection 00: bi-colors speed mode/duplex(col)/FEF(loop) 01: link100(act)/link10(act)/duplex/FEF 10: link100(act)/link10(act)/duplex(col)/FEF(loop) 11: link(act)/speed/duplex(col)/FEF(loop) (default) bit[10] : STP packet filtering setting (DA=0x0180c2000000) 0: broadcast to all ports (default) 1: forwarded to CPU port (port 3) only if 12.[4] = 1, otherwise broadcasting bit[9] : 802.1x packet filtering setting (DA=0x0180c2000003) 0: depending on bit 1.[4] (default) 1: forwarded to CPU port (port 3) only if 12.[4] =1, and 1.[4] = 0, otherwise depending on bit 1.[4] bit[8] : Slow protocol packet filtering setting(DA=0x0180c2000002) 0: discarded (default) 1: forwarded to CPU port only if 12.[4] = 1, otherwise broadcasting bit[7] : (reserved for test) 1: (default) bit[6] : (reserved for test) 0: (default) bit[5] : 802.3x PAUSE frame filtering setting 0: filtered and handled by IP113S LF (default) 1: broadcasting bit[4] : BPDU packets filtering setting (DA= 0x0180c2000003~0x0180c200000F) 0: discarded 1: broadcasting (default) bit[3] : Tx. IPG compensation enable, used to compensate the frequency between Tx. and Rx. 0: Tx. IPG +0ppm (default) 1: Tx. IPG +80ppm	R/W	0x3892

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		bit[2] : Half duplex back pressure method selection 0: Collision base (default) 1: Carrier Sense base bit[1] : Half duplex collision back off enable 0: disable 1: enable (default) bit[0] : Half duplex collision 16 times drop enable 0: disable (default) 1: enable		
02H	04H 05H	Ingress / egress bandwidth control mode bit[10] : Ingress bandwidth control mode for P03 0: 32Kbps x N 1: 512Kbps x N (default) N refers to rgister 0x03 bit[9] : Ingress bandwidth control mode for P02 0: 32Kbps x N 1: 512Kbps x N (default) N refers to rgister 0x04 bit[8] : Ingress bandwidth control mode for P01 0: 32Kbps x N 1: 512Kbps x N (default) N refers to rgister 0x05 bit[2] : egress bandwidth control mode for P03 0: 32Kbps x N 1: 512Kbps x N (default) N refers to rgister 0x03 bit[1] : egress bandwidth control mode for P02 0: 32Kbps x N 1: 512Kbps x N (default) N refers to rgister 0x04 bit[0] : egress bandwidth control mode for P01 0: 32Kbps x N 1: 512Kbps x N (default) N refers to rgister 0x05	R/W	0x0707
03H	06H 07H	Ingress/ egress bandwidth setting for P01 bit[15:8] : ingress rate setting (N) for P01 0x00~0xFF (default) bit[7:0] : egress rate setting (N) for P01 0x00~0xFF (default)	R/W	0xFFFF

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
04H	08H 09H	Ingress/ egress bandwidth setting for P02 bit[15:8] : ingress rate setting (N) for P02 0x00~0xFF **(**default) bit[7:0] : egress rate setting (N) for P02 0x00~0xFF (default)	R/W	0xFFFF
05H	0AH 0BH	Ingress/ egress bandwidth setting for P03 bit[15:8] : ingress rate setting (N) for P03 0x00~0xFF (default) bit[7:0] : egress rate setting (N) for P03 0x00~0xFF (default)	R/W	0xFFFF
06H	0CH 0DH	MAC receiving enable for [P03, P02, P01], 1 bit per port bit[2:0] : enable the MAC receiving ability 0: disable 1: enable (default)	R/W	0x0007
07H	0EH 0FH	Reserved		0xFFFF
08H	10H 11H	Priority setting bit[2:0] : port base priority enable for [P03, P02, P01], 1 bit per port 0: disable port base priority (default) 1: packet received by this port is high priority bit[4] : TAG base priority enable 0: disable TAG priority (default) 1: packet's priority depends on TAG information Note: these two conditions are "OR" together	R/W	0x0000
09H	12H 13H	Auto loop back test frames format setting bit[7] : DA is broadcast or unicast 0: DA = 0x0090C3000002 (default) 1: DA = 0Xffffffffffff bit[6:4] : Data format 000: 0x55AA(default) 100: 0x00FF 001: 0x5555 101: 0x0000 010: 0xAAAA 110: 0xFFFF 011: 0x5A5A 111: 0x0F0F bit[3] : Sending packet length node 0: packet length is fixed (default) 1: packet length will add "1" after sending a packet bit[2:0] : packet length setting 000: 64 (default) 100: 768 001: 128 101: 1024 010: 256 110: 1280 011: 512 111: 1518	R/W	0x0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
0AH	14H 15H	MAC data path setting bit[8] : Dual PHY mode 0: IP113S LF can forward data between port 1 and port2. (default) 1: IP113S LF' is partitioned as two PHYs bit[7:6] : DCE or DTC mode of RS232 interface for [P02,P01], 1 bit per port 0: RS232 is in DCE mode, CD and RI signals are outputs. 1: RS232 is in DTE mode, CD and RI signals are inputs. (default) bit[5:4] : external MAC interface enable for [P02,P01], 1 bit per port 0: using internal MII interface connected to internal PHY (default) 1: external MAC interface enable. Using external MII or SMII or RS232 interface defined in bit[3:0]. bit[3:0] : External interface selection for [P02,P01], 2 bit per port 00: RS232 01: SMII 10: reversed MII 11: MII (default) Note: Only MII/reversed-MII interface can connected to internal PHY or MAC, others to PHY only.	R/W	0x00CF

4.2 DMA Control register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
0BH	16H 17H	Switch operation mode setting/monitoring bit[7:6] : switch operation monitoring 00: switch function OK (default) x1: P01's switch function is fail 1x: P02's switch function is fail bit[5] : the Built-In-Self-Test (BIST) result 0: BIST is fail 1: BIST is pass (default) bit[4] : the BIST procedure indication 0: BIST is complete (default) 1: BIST is under going bit[3] : Embedded memory BIST test 0: disable the BIST procedure 1: enable the BIST procedure (default) Note: 0 changes to 1 will trigger BIST again bit[2] : Pass through mode enable 0: operation mode is follow bit[1:0] (default) 1: enter Pass through mode (pure converter, no OAM supported) bit[1:0] : converter/cut-through/store-forward 00: store and forward mode (default) 01: converter mode 10: modified cut-through mode 11: converter mode if duplex and speed of P01 equal P02, otherwise modified cut-through mode	 RO R/W	0x0028
0CH	18H 19H	p01 memory page allocation bit[7:0] : memory allocation 142: (default) Note: Total pages of three ports plus together can not exceed 426	R/W	0x00A0
0DH	1AH 1BH	p02 memory page allocation bit[7:0] : memory allocation 142: (default)	R/W	0x00A0
0EH	1CH 1DH	p03 memory page allocation bit[7:0] : memory allocation 142: (default)	R/W	0x006A

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
0FH	1EH 1FH	Output queue schedule mode bit[7:5] : High priority queue weight number when WRR mode is selected. 000: (default) bit[4:2] : Low priority queue weight number when WRR mode is selected. 000: (default) Note: When bit[7:5] and bit[4:2] are set to “000”, the weight number will be interpreted as “8” bit[1:0] : output queues schedule mode 00: First in first out (default) 01: Strict priority, the IP113S LF will always forward packets in high priority queue until the queue is empty. 10: Weighted-and-round-Robin scheme. The high/low packets ratio is based on bit[7:2] 11: Undefined	R/W	0x0000
10H	20H 21H	Reserved. The default value should be adopted for normal operation.	R/W	0x0030
11H	22H 23H	Reserved. The default value should be adopted for normal operation.	R/W	0x003C

4.3 ARL Control Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
12H	24H 25H	Address resolution miscellaneous setting bit[5] : special tag 0: disabled 1:enabled bit[4] : Indicate the p03 connected to CPU 0: P03 is a normal port (default) 1: P03 is connected to CPU bit[3] : Blocking the broadcast/multi-case/unknown broadcast packet to CPU. 0: Broadcast frames send to CPU (default) 1: Broadcast frames do not send to CPU except ARP packets bit[2] : broadcast storm control enable 0: broadcast storm control disabled (default) 1: broadcast storm control enabled bit[1] : Look-up-table aging function disable 0: aging function enabled (default) 1: aging function disabled bit[0] : Look-up-table hash algorithm selection 0: CRC hashing (default) 1: direct address hashing	R/W	0x0000
13H	26H 27H	Broadcast storm threshold and aging timer setting bit[14:8] : the broadcast frames allowed in one period. one period is 1ms for 100Mb speed and 10ms for 10Mb. bit[7:0] : the aging timer of LUT the aging timer = (mg_aging_timer + 1) x 384s +/- 6.7	R/W	0x7F00
14H	28H 29H	ARL forward the data frames setting (used for STP protocol) bit[2:0] : ARL forward the data frame, 1 bit per port 0: only control frames are forwarded (STP and slow protocol should be enable, reg01) 1: all good frames are forwarded (default)	R/W	0x0007
15H	2AH 2BH	MAC transmit enable setting bit[2:0] : transmit enable for [P03, P02, P01], 1 bit per port 0: transmit disabled 1: transmit enabled (default)	R/W	0x0007

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
16H	2CH 2DH	ARL learning mode bit[15:13] : out going destination port of P03 when bit[12] = 1 000: not forwarded (default) xx1: forwarded to P01 x1x: forwarded to P02 1xx: not forwarded to P03 because local traffic bit[12] : P03 static route enable 0: using LUT to check out going destination ports (default) 1: using bit[15:13] as out going destination ports bit[11:9] : out going destination port of P02 when bit[8] = 1 000: not forwarded (default) xx1: forwarded to P01 x1x: not forwarded to P02 because local traffic 1xx: forwarded to P03 bit[8] : P02 static route enable 0: using LUT to check out going destination ports (default) 1: using bit[11:9] as out going destination ports bit[7:5] : out going destination port of P01 when bit[11] = 1 000: not forwarded (default) xx1: not forwarded to P01 because local traffic x1x: forwarded to P02 1xx: forwarded to P03 bit[4] : P01 static route enable 0: using LUT to check out going destination ports (default) 1: using bit[7:5] as out going destination ports bit[3] : (reserved) bit[2:0] : LUT SA learning disable setting, 1 bit per port 0: learning enabled (default) 1: learning disabled	R/W	0x0000
17H	2EH 2FH	LUT security configuration bit[1:0] : forward unknown SA frame policy 00: broadcast (default) 01: broadcast 10: filtering 11: forward to CPU	R/W	0x0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
18H	30H 31H	Trunk group setting bit[7:6] : Hash mode setting for frame trunk ID 00: port base (default) 01: SA base 10: DA base 11: SA xor DA base bit[5:4] : Trunk group configuration for P03 00: P03 is not trunked (default) 01: P03 is trunked and pass the frame with trunk ID = 0 10: P03 is trunked and pass the frame with trunk ID = 1 11: not allowed bit[3:2] : Trunk group configuration for P02 bit[1:0] : Trunk group configuration for P01 Note: (a) You can trunk 2 ports together only (any combination). (b) If trunked, bit[4]/[2]/[0] should be set carefully for only 1 bit =1 same as bit[5]/[3]/[1] . Example: Trunk P03, P01 together, bit[5:0] should be 100001 or 0100	R/W	0x0000
19H	32H 33H	Port mirroring configuration bit[8:6] : the snooping port set (destination), 1 bit per port 0: the monitored frames are not forwarded to this port (default) 1: the monitored frames are forwarded to this port bit[5:4] : P03 monitored mode set 00: not be monitored (default) x1: egress frames be monitored 1x: ingress frames be monitored bit[3:2] : P02 monitored mode set 00: not be monitored (default) x1: egress frames be monitored 1x: ingress frames be monitored bit[1:0] : P01 monitored mode set 00: not be monitored (default) x1: egress frames be monitored 1x: ingress frames be monitored	R/W	0x0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
1AH	34H 35H	PVID index setting bit[11:8] : PVID index configuration for P03, indicates the default VID of P03 is put in which VID entry for a un-tag packet. If port base VLAN is enable, IP113S LF use index 2 to check VLAN group, whatever this setting is. (16 entries selectable) 2: (default) bit[7:4] : PVID index configuration for P02, indicates the default VID of P02 is put in which VID entry for a un-tag packet. If port base VLAN is enable, IP113S LF use index 1 to check VLAN group, whatever this setting is. (16 entries selectable) 1: (default) bit[3:0] : PVID index configuration for P01, indicates the default VID of P01 is put in which VID entry for a un-tag packet. If port base VLAN is enable, IP113S LF use index 0 to check VLAN group, whatever this setting is. (16 entries selectable) 0: (default)	R/W	0x0210
1BH	36H 37H	VLAN configuration bit[7:5] : Egress removing TAG setting for [P03,P02,P01],1 bit per port. 0: Do not care the frame is tagged or not (default) 1: Remove the TAG of tagged frame. bit[4:2] : Egress inserting TAG setting for [P03,P02,P01], 1 bit per port 0: Do not care the frame is tagged or not (default) 1: Insert the TAG for non-tagged frame and modified the TAG for tagged frame bit[1] : Leaky VLAN setting 0: drop the frame if source port is not in the VLAN group (default) 1: Forward the uni-cast frame even if source port is not in the VLAN group bit[0] : port base VLAN or TAG base VLAN selection. 0: port base VLAN (default) 1: TAG base VLAN	R/W	0x0000
1CH	38H 39H	VLAN table entry 0 configuration bit[14:12] : VLAN members for this VID, 1 bit per port. 0: port not in this VID group 1: port in this VID group (default) bit[11:0] : VID for this entry 1: (default)	R/W	0x7001
1DH	3AH 3BH	VLAN table entry 1 configuration (definition is the same with reg.1CH except default value)	R/W	0x7002

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
1EH	3CH 3DH	VLAN table entry 2 configuration (The definition is the same with reg.1CH except default value)	R/W	0x7003
1FH	3EH 3FH	VLAN table entry 3 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
20H	40H 41H	VLAN table entry 4 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
21H	42H 43H	VLAN table entry 5 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
22H	44H 45H	VLAN table entry 6 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
23H	46H 47H	VLAN table entry 7 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
24H	48H 49H	VLAN table entry 8 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
25H	4AH 4BH	VLAN table entry 9 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
26H	4CH 4DH	VLAN table entry 10 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
27H	4EH 4FH	VLAN table entry 11 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
28H	50H 51H	VLAN table entry 12 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
29H	52H 53H	VLAN table entry 13 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
2AH	54H 55H	VLAN table entry 14 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000
2BH	56H 57H	VLAN table entry 15 configuration (The definition is the same with reg.1CH except default value)	R/W	0x0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
2CH	58H 59H	CPU access LUT control bit[14] : CPU read/write command trigger 0: disable (default) 1: trigger a CPU read/write LUT command bit[13] : CPU data (from reg.2D to reg.2F) content index 0: the data is read back data from LUT (default) 1: the data is what CPU write into reg.2D~reg.2F bit[12] : CPU read/write LUT mode 0: read command (default) 1: write command bit[11:10] : (reserved) bit[9:0] : 1K memory access address for LUT 0: (default) Note: the LUT data format should be got from contact window.	R/W	0x0000
2DH	5AH 5BH	CPU access LUT DATA bit[15:0] bit[15:0] : CPU read/write LUT DATA [15:0] (1) If read, when reg.2C[13] = 0: show the last read back data from LUT. when reg.2C[13] = 1: show the data, which you wrote into this register. (2) If write, this is the data want to write into LUT	R/W	0x0000
2EH	5CH 5DH	CPU access LUT DATA bit[31:16] bit[15:0] : CPU read/write LUT DATA [31:16] (1) If read, when reg.2C[13] = 0: show the last read back data from LUT. when reg.2C[13] = 1: show the data which you wrote into this register (2) If write, this is the data want to write into LUT	R/W	0x0000
2FH	5EH 5FH	CPU access LUT DATA bit[44:32] bit[12:0] : CPU read/write LUT DATA [44:32] (1) If read, when reg.2C[13] = 0: show the last read back data from LUT. when reg.2C[13] = 1: show the data, which you wrote into this register. (2) If write, this is the data want to write into LUT.	R/W	0x0000

4.4 SMI Control Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
30H	60H 61H	Auto negotiation configuration bit[4] : MDI/MDIX force setting when auto crossover disable (D0h[11]=1) 0: MDI (default) 1: MDIX bit[3] : auto negotiation ability limitation 0: advertisement MII register is not limited (default) 1: advertisement MII register is limited to one ability only (depends on what speed and what duplex) bit[2:0] : auto negotiation enable for [P03,P02,P01], 1 bit per port 0: auto negotiation is disabled (force mode) 1: auto negotiation is enabled (default: 101) Note: P02 should fix to no-auto negotiation mode.	R/W	0x0005
31H	62H 63H	Speed configuration bit[2:0] : speed selection for [P03,P02,P01], 1 bit per port 0: 10Mb speed 1: 100Mb speed (default)	R/W	0x0007
32H	64H 65H	Duplex configuration bit[2:0] : duplex selection for [P03,P02,P01], 1 bit per port 0: half duplex 1: full duplex (default)	R/W	0x0007
33H	66H 67H	802.3x flow control configuration bit[5:0] : flow control selection for [P03,P02,P01], 2 bit per port The advertisement MII register bit[11:10] set. [ASM_DIR, PAUSE] 00: No PAUSE 01: Symmetric PAUSE 10: Asymmetric PAUSE toward link partner 11: Both symmetric and asymmetric PAUSE toward local device (default)	R/W	0x003F
34H	68H 69H	Backpressure configuration bit[2:0] : half duplex backpressure flow control for [P03,P02,P01], 1 bit per port. 0: backpressure disabled 1: backpressure enabled (default)	R/W	0x0007

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
35H	6AH 6BH	SMI miscellaneous setting bit[9] : The interrupt notification enable when link status changed. (any one of three ports, refer to reg.53) 0: Interrupt disabled (default) 1: Interrupt enabled bit[8] : The interrupt enable which indicates CPU read/write PHY MII registers command complete 0: Interrupt disabled (default) 1: Interrupt enabled bit[7:5] : Force link setting for [P03,P02,P01], 1 bit per port 0: Link status depends on PHY's MII registers.(default) 1: forced to link bit[4:0] : address setting for IP113S LF polling PHY P01 port's address = mg_phy_addr[4:0]. P02 port's address = mg_phy_addr[4:0] + 1. P03 port's address = mg_phy_addr[4:0] + 2 (default = 0)	R/W	0x0000
36H	6CH 6DH	CPU read/write PHY's MII registers command bit[15] : the read/write command trigger 0: IDLE or command complete (default) 1: Issue a command bit[14] : read or write command 0: read command (default) 1: write command bit[13] : read/write command completed 0: not yet 1: command completed bit[12:11] : (not used) bit[10] : CPU data (reg.37) content index 0: the data is read back data from PHY (default) 1: the data is what CPU write into reg.37 bit[9:5] : MII register address 0: (default) bit[4:0] : PHY address 0: (default)	 R/W, SC R/W RO R/W	0x0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
37H	6EH 6FH	CPU access PHY MII register data[15:0] bit[15:0] : CPU read/write PHY MII register data [15:0] (1) If read, show the read back data from PHY if reg. 36[10] = 0, otherwise the write data. (2) If write, this is the data want to write into PHY	R/W	0x0000
38H	70H 71H	Port status for [P03,P02,P01], 5 bits per port : [rx_pause, tx_pause, duplex, speed, link] bit[14:10] : The link status and operation mode for P03 bit[14] : flow control ability for Rx. path 0: disable (default) 1: enable bit[13] : flow control ability for Tx. path 0: disable (default) 1: enable bit[12] : duplex mode 0: half duplex (default) 1: full duplex bit[11] : speed mode 0: 10Mb speed (default) 1: 100Mb speed bit[10] : link status 0: link off (default) 1: link on bit[9:5] : The link status and operation mode for P02. bit[4:0] : The link status and operation mode for P01.	RO	0x0000

4.5 OAM Control Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
39H	72H 73H	OAM miscellaneous configuration bit[15] : Link fault pass through (LFP) function between P02 and P01 0: LFP function disabled 1: LFP function enable bit[14:10] : (not used) bit[9] : Keep P01 (the port not to be tested) link when loop back test is processing 0: link will disconnect when loop back path enable 1: keep link status unchange when loop back path enable bit[8] : MC status of IP113S LF 0: normal (default) 1: fail Note: this bit can be configuration from PIN, CPU I/F and internal watchdog mechanism. bit[7] : power fail detection disable 0: detect the power whether it is under the threshold or not. (default) 1: power detection function disabled. bit[6:5] : Loss-of-optical-signal notification way for [P02,P01],1 bit per port 0: with OAM frame 1: with alarm FEFI (default: 01) bit[4] : IP113A/M/C/F OAM command acceptable 0: do not care the remote control command issued by IP113M. 1: accept the remote control commands issued by IP113M which want to remote control the following registers defined in IP113M. (default) IP113M reg.0 ~ reg.18, reg.20, reg.22, reg.23 and reg.31 supported. OUT IP113M reg.19, reg20.3d, reg20.10d reg23.7d (change the definition) reg.21 and reg.24~reg.30 not supported. bit[3] : Auto notify and response TS-1000 OAM frames	R/W	0x0077

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		0: disable auto sending indication and does not response to any OAM frames. (default). It is note that a received OAM is always stored to 43h~4Dh even if this bit is set to “0”. 1: auto sending indication and responding OAM frames. bit[2] : support for notification of status for the terminal-side 0: option B not supported 1: option B supported **(**default) bit[1:0] : TS-1000 function enable for [P02,P01],1 bit per port 0: IP113S LF can not Tx./Rx. TS-1000 OAM frames 1: IP113S LF can Tx./Rx. TS-1000 OAM frames.(default:11) It is note that port1 doesn’t support OAM frame when it works in 10BASE_T mode.		
3AH	74H 75H	Vendor Code M[15:0] used by OAM frames bit[15:0] : M[15:0], the 1st through 16th bits of an OUI of the vendor. (default: 0x0900)	R/W	0x0900
3BH	76H 77H	Model number M[31:24] and Vendor Code M[23:16] used by OAM Frames. bit[15:8] : M[31:24], Vendor can assign the model number M[31:24] without informing TTC. (default: 0x40)	R/W	0x40C3
		If these bits are used to remote control command, it’s definition is as follows.(cooperation with “request” OAM frame) M[31:30] : Model name 01: IP113S LF others: not defined M[29:28] : Version control M[27] : read/ write control 0: read 1: write M[26] : Upper byte indication 0: applied command to lower byte of a word. 1: applied command to upper byte of a word. M[25:24] : operation mode 00: normal mode 01: extended mode (for remote control) others: undefined		
		bit[7:0] : M[23:16], The 17th through 32th bits of an OUI of the vendor.(default: 0xC3)		

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
3CH	78H 79H	Model number M[47:32] used by OAM frames bit[15:0] : M[47:32], Vendor can assign the model number M[47:32] without informing TTC. (default: 0x0000) If these bits are used to remote control command, it's definition is as follows.(cooperation with "request" OAM frame) M[47:40] : registers data M[39:32] : registers address	R/W	0x0000
3DH	7AH 7BH	S[15:0] data used by OAM frames or remote control write data. (IP113M) bit[15:0] : when issuing an OAM frame via reg.3F, this content will be embedded into S[15:0] of an OAM frame. So, it my be local status read from reg.4E or remote control write data defined by IP113M.(0: default)	R/W	0x0000
3EH	7CH 7DH	C[15:0] control signal and instruction identifier used by OAM frames or remote control write data.(IP113M) bit[15:0] : when issuing an OAM frame via reg.3F, this content will be embedded into C[15:0] of an OAM frame.(0: default)	R/W	0x0000
3FH	7EH 7FH	Remote control OAM frame transmitting configuration bit[3:2] : M[47:0] operation mode selection 00: IP113S LF auto Response/Indication OAM frames using Icplus's VID to be M[47:0], other types OAM frames using M[47:0] defined in reg.3A~reg.3C. (default) 01: All OAM frames including auto or issued, use M[47:0] defined in reg.3A~reg.3C to send. others: (undefined) bit[1] : the issued OAM frame is sending to P01 or P020 0: P01 1: P02 (default) bit[0] : Remote control OAM frame trigger set 0: idle (default) 1: trigger an OAM frame which format is defined in reg.3A~reg.3F	R/W	0x0002

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
40H	80H 81H	TS-1000 Loop back test configuration bit[8] : TS-1000 loop back test T2 timer enable setting 0: T2 timer disabled 1: T2 timer enabled. If T2 timer expires, an loop back test ending indication OAM will be sent.(default) bit[7] : P02's auto loop back test result 0: fail (default) 1: good bit[6] : P02's auto loop back test is completed 0: not completed (default) 1: completed bit[5] : set P02's data path into loop back mode 0: normal Tx./Rx. path (default) 1: be loop back test path bit[4] : set P02 issue auto loop back test request to terminal-side 0: not perform auto loop back test.(default) 1: start an auto loop back test procedure. This bit toggled from “0” to “1” will trigger auto loop back test once. bit[3] : P01's auto loop back test result indication 0: fail (default) 1: good bit[2] : P01's auto loop back test is completed 0: not completed (default) 1: completed bit[1] : set P01's data path into loop back mode 0: normal Tx./Rx. path (default) 1: be loop back test path. bit[0] : set P01 issue auto loop back test request to terminal-side. 0: not perform auto loop back test.(default) 1: start an auto loop back test procedure. This bit toggled from “0” to “1” will trigger auto loop back test once.	 R/W RO RO R/W RO RO R/W	0x0100
41H	82H 83H	Packet number for TS-1000 Loop back test sending. bit[7:0] : Number of loop back test packet to send 0~255: (default 16) Note: The loop back packet’s format is defined in reg.09	R/W	0x0040

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
42H	84H 85H	Loop back result counter bit[15:8] : Number of good looped-back packet received of P02. bit[7:0] : Number of good looped-back packet received of P01. Note: these counters will be cleared when a new auto loop back test procedure is issued.	RO	0x00000
43H	86H 87H	OAM frame receiving configuration bit[11:10] : Link partner power abnormal interrupt enable for [P02,P01], 1 bit per port (refer to reg.52) 0: interrupt disabled (default) 1: issue an interrupt when link partner power status changes. bit[9:8] : OAM frame received interrupt enable for [P02,P01], 1 bit per port (refer to reg.52) 0: interrupt disabled (default) 1: issue an interrupt when an OAM frame received. bit[7:6] : P02 received OAM Instruction 00: undefined 01: request 10: indication 11: response bit[5] : P02 received OAM is CRC error 0: good crc (default) 1: crc error bit[4] : P02 received OAM frame 0: no OAM frame received (default) 1: an OAM frame has been received bit[3:2] : P01 received OAM Instruction 00: undefined 01: request 10: indication 11: response bit[1] : P01 received OAM is CRC error 0: good crc (default) 1: crc error bit[0] : P01 received OAM frame 0: no OAM frame received (default) 1: an OAM frame has been received	 R/W RO RO RC RO RC RO RO RC RO RC	0x00000
44H	88H 89H	C[15:0] of P01's received OAM frame bit[15:0] : received OAM's C[15:0]	RO	0x00000
45H	8AH 8BH	S[15:0] of P01's received OAM frame bit[15:0] : received OAM's S[15:0]	RO	0x00000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
46H	8CH 8DH	M[15:0] of P01's received OAM frame bit[15:0] : received OAM's M[15:0]	RO	0x00000
47H	8EH 8FH	M[31:16] of P01's received OAM frame bit[15:0] : received OAM's M[31:16]	RO	0x00000
48H	90H 91H	M[47:32] of P01's received OAM frame bit[15:0] : received OAM's M[47:32]	RO	0x00000
49H	92H 93H	C[15:0] of P02's received OAM frame bit[15:0] : received OAM's C[15:0]	RO	0x00000
4AH	94H 95H	S[15:0] of P02's received OAM frame bit[15:0] : received OAM's S[15:0]	RO	0x00000
4BH	96H 97H	M[15:0] of P02's received OAM frame bit[15:0] : received OAM's M[15:0]	RO	0x00000
4CH	98H 99H	M[31:16] of P02's received OAM frame bit[15:0] : received OAM's M[31:16]	RO	0x00000
4DH	9AH 9BH	M[47:32] of P02's received OAM frame bit[15:0] : received OAM's M[47:32]	RO	0x00000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
4EH	9CH 9DH	Local status of IP113S LF bit[15] : Indicates the IP113S LF is in LFP mode 0: normal mode (default) 1: LFP function is enabled bit[14] : P01 FEF detect 0: no FEF detected (default) 1: FEF pattern or OAM detected bit[13] : P01 signal detect (SD) 0: SD is not detected (default) 1: SD is detected bit[12] : P02 link status 0: link off (default) 1: link on bit[11] : Data path of P02 is set into loop back mode 0: normal tx./rx. path (default) 1: looped-back data path bit[10] : P02 FEF detection 0: no FEF detected (default) 1: FEF pattern or OAM detected bit[9] : P02 signal detect (SD) 0: SD is not detected (default) 1: SD is detected bit[8] : P02 duplex mode 0: half duplex 1: full duplex (default) bit[7] : P02 flow control enable 0: flow control disabled 1: flow control enabled (default) bit[6] : P01 link status 0: link off (default) 1: link on bit[5] : P01 flow control enable 0: flow control disabled 1: flow control enabled (default) bit[4] : P01 duplex mode 0: half duplex 1: full duplex (default) bit[3] : P01 speed mode 0: 10Mb speed 1: 100Mb speed (default) bit[2] : P01 auto negotiation enable 0: nway disabled 1: nway enabled (default) bit[1] : P01 status report available 0: P01 status is not valid (default) 1: P01 status is valid bit[0] : Data path of P01 is set into loop back mode 0: normal tx./rx. path (default) 1: looped-back data path	RO	0x01BC

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
4FH	9EH 9FH	Link partner status of P01 bit[15] : Link partner is in LFP mode (Note*) 0: normal mode (default) 1: LFP function is enabled bit[14] : Link partner support multi-port UTP 0: one (default) 1: greater than one bit[13] : Link partner loss-of-optical-signal notification method 0: OAM frame 1: FEFI (default) bit[12] : Link partner MC status 0: normal (default) 1: failure bit[11] : Link partner power supply status 0: normal (default) 1: power supply failure bit[10] : OAM indication format 0: TS-1000 OAM (default) 1: Icplus OAM, supported by IP113M only bit[9] : Link partner optical signal detect (SD) 0: normal (default) 1: abnormal bit[8] : Link partner duplex mode (Note*) 0: half duplex 1: full duplex (default) bit[7] : Local optical link indication 0: link abnormal, status report not ready! (default) 1: link on, and the parameters reported in this register are meaningful. bit[6] : Link partner network-side link status 0: established 1: not established (default) bit[5] : Link partner network-side flow control (Note*) 0: flow control disabled (default) 1: flow control enabled bit[4] : Link partner network-side duplex mode 0: half duplex (default) 1: full duplex bit[3] : Link partner network-side speed 0: 10Mb speed (default) 1: 100Mb speed bit[2] : Link partner network-side auto negotiation enable 0: nway disabled (default) 1: nway enabled bit[1] : Link partner option B supported 0: not supported (default) 1: support bit[0] : Link partner operation status 0: under ordinary operation (default) 1: under loop back test Note*: these bits are valid only when bit[10] = 1.	RO	0x2040

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
50H	A0H A1H	Link partner status of P02 (The same definition with reg.4F)	RO	0x2040
51H	A2H A3H	(Reserved)		

4.6 Miscellaneous Control Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
52H	A4H A5H	Chip miscellaneous configuration bit[2] : Set IP113S LF into fast test mode, this bit is reserved for testing only! 0: normal operation 1: speed up all counters in IP113S LF bit[1] : Chip reset, all registers in IP113S LF will reset to power on default value. 0: not reset 1: reset bit[0] : software reset, reset IP113S LF without updating the content of registers 0: not reset 1: reset	 R/W R/W, SC R/W, SC	0x0000
53H	A6H A7H	Chip interrupt status report bit[7] : Any one of the second MIBs counters group pre-overflow indication 0: counters are not overflow (default) 1: counters will overflow (had better read MIBs in 20 sec.) bit[6] : Any one of the first MIBs counters group pre-overflow indication 0: counters are not overflow (default) 1: counters will overflow (had better read MIBs in 20 sec.) bit[5] : P02 has detected a power stable change in its link partner 0: not detect (default) 1: detected bit[4] : P01 has detected a power stable change in its link partner 0: not detect (default) 1: detected bit[3] : P02 has received an OAM frame 0: not received (default) 1: received an OAM frame bit[2] : P01 has received an OAM frame 0: not received (default) 1: received an OAM frame bit[1] : One of three port's link status changed 0: Link status not changed (default) 1: link status changed bit[0] : Indicates the command issued from CPU to PHY via MDC/MDIO has been completed. 0: not completed (default) 1: completed	RO, RC	0x0000
59H	B2H B3H	(Reserved)		

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
5AH	5AH~ 5BH	Analog Macro performance configuration I. (Reserved)	R/W	0x0000
5BH	5CH~ 5DH	Analog Macro performance configuration II. (Reserved)	R/W	0x0000
5CH	B4H~ B9H	(Reserved)		

4.7 MIB Control Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
5DH	BAH BBH	MIBs counters configuration bit[7] : (reserved) bit[6] : Overflow Interrupt indication enable for MIBs group 2 . Please refer to register 53h 0: interrupt disabled (default) 1: interrupt enabled bit[5:4] : MIBs group 2 counting base. (i.e. these MIBs counters is calculating based on which port's information) 00: P01 01: P02 (default) 1x: P03 bit[3] : (reserved) bit[2] : Overflow Interrupt indication enable for MIBs group 1 . Please refer to register .53h 0: interrupt disabled (default) 1: interrupt enabled bit[1:0] : MIBs group 1 counting base. (i.e. these MIBs counters is calculating based on which port's information) 00: P01 (default) 01: P02 1x: P03	R/W	0x0010
5EH 5FH		(reserved)		
60H		MIBs group 1.0 - **etherStatesOctets**, (lower word) The total number of octets of data (including those in bad packets) received on the network (excluding framing bits but including FCS octets)	RO, RC	
61H		MIBs group 1.0 - **etherStatesOctets**, (upper word)	RO, RC	
62H		MIBs group 1.1 - **etherStatesDropEvents**, (lower word) The total number of events in which packets were dropped by the probe due to lack of resources. Note that this number is not necessarily the number of the packets dropped; it is just the number of times this condition has been detected.	RO, RC	
63H		MIBs group 1.1 - **etherStatesDropEvents**, (upper word)	RO, RC	
64H		MIBs group 1.2 - **etherStatesPkts**, (lower word) The total number of packets (including bad packets, broadcast packets, and multicast packets) received.	RO, RC	
65H		MIBs group 1.2 - **etherStatesPKts**, (upper word)	RO, RC	

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
66H		MIBs group 1.3 - **etherStatesBroadcastPkts**, (lower word) The total number of good packets received that were directed to the broadcast address. Note that this does not include multicast packets.	RO, RC	
67H		MIBs group 1.3 - **etherStatesBroadcastPkts**, (upper word)	RO, RC	
68H		MIBs group 1.4 - **etherStatesMulticastPkts**, (lower word) The total number of good packets received that were directed to a multicast address. Note that this number does not include packets directed to the broadcast address.	RO, RC	
69H		MIBs group 1.4 - **etherStatesMulticastPkts**, (upper word)	RO, RC	
6AH		MIBs group 1.5 - **etheStatesCRCAlignErrors**, (lower word) The total number of packets received that had a length (excluding framing bits, but including FCS octets) of between 64 and 1518 octets, inclusive, but had either a bad FCS with an integral number of octets or a bad FCS with a non-integral number of octets (Alignment error).	RO, RC	
6BH		MIBs group 1.5 - **etheStatesCRCAlignErrors**, (upper word)	RO, RC	
6CH		MIBs group 1.6 - **etherStatesUndersizePkts**, (lower word) The total number of good packets received that were less than 64 octets long (excluding framing bits, but including good FCS octets) and were otherwise well formed.	RO, RC	
6DH		MIBs group 1.6 - **etherStatesUndersizePkts**, (upper word)	RO, RC	
6EH		MIBs group 1.7 - **etheStatesOversizePkts**, (lower word) The total number of packets received that were longer than 1522 octets and were otherwise well formed.	RO, RC	
6FH		MIBs group 1.7 - **etheStatesOversizePkts**, (upper word)	RO, RC	
70H		MIBs group 1.8 - **etherStatesFragments**, (lower word) The total number of good packets received that were less than 64 octets long and had a bad FCS with integral number of octets or a bad FCS with a non-integral number of octets (Alignment error).	RO, RC	
71H		MIBs group 1.8 - **etherStatesFragments**, (upper word)	RO, RC	
72H		MIBs group 1.9 - **etheStatesJabbers**, (lower word) The total number of packets received that were longer than 1522 octets and had either a bad FCS with integral number of octets or a bad FCS with a non-integral number of octets (Alignment error).	RO, RC	
73H		MIBs group 1.9 - **etheStatesJabbers**, (upper word)	RO, RC	

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
74H		MIBs group 1.10 - **etherStatesCollisions**, (lower word) The best estimate of the total number of collisions on this Ethernet segment.	RO, RC	
75H		MIBs group 1.10 - **etherStatesCollisions**, (upper word)	RO, RC	
76H		MIBs group 1.11 - **etheStatesPkts64Octets**, (lower word) The total number of packets (including bad packets) received that were 64 octets in length.	RO, RC	
77H		MIBs group 1.11 - **etheStatesPkts64Octets**, (upper word)	RO, RC	
78H		MIBs group 1.12 - **etherStatesPkts65to127Octets**, (lower word) The total number of packets (including bad packets) received that were between 65 and 127 octets in length inclusive.	RO, RC	
79H		MIBs group 1.12 - **etherStatesPkts65to127Octets**, (upper word)	RO, RC	
7AH		MIBs group 1.13 - **etheStatesPkts128to255Octets**, (lower word) The total number of packets (including bad packets) received that were between 128 and 255 octets in length inclusive.	RO, RC	
7BH		MIBs group 1.13 - **etheStatesPkts128to255Octets**, (upper word)	RO, RC	
7CH		MIBs group 1.14 - **etherStatesPkts256to511Octets**, (lower word) The total number of packets (including bad packets) received that were between 256 and 511 octets in length inclusive.	RO, RC	
7DH		MIBs group 1.14 - **etherStatesPkts256to511Octets**, (upper word)	RO, RC	
7EH		MIBs group 1.15 - **etheStatesPkts512to1023Octets**, (lower word) The total number of packets (including bad packets) received that were between 512 and 1023 octets in length inclusive.	RO, RC	
7FH		MIBs group 1.15 - **etheStatesPkts512to1023Octets**, (upper word)	RO, RC	
80H		MIBs group 1.16 - **etherStatesPkts1024to1522Octets**, (lower word). The total number of packets (including bad packets) received that were between 1024 and 1522 octets in length inclusive.	RO, RC	
81H		MIBs group 1.16 - **etherStatesPkts1024to1522Octets**, (upper word)	RO, RC	
82H		MIBs group 2.0 - **etherStatesOctets**, (lower word)	RO, RC	
83H		MIBs group 2.0 - **etherStatesOctets**, (upper word)	RO, RC	
84H		MIBs group 2.1 - **etherStatesDropEvents**, (lower word)	RO, RC	
85H		MIBs group 2.1 - **etherStatesDropEvents**, (upper word)	RO, RC	
86H		MIBs group 2.2 - **etherStatesPkts**, (lower word)	RO, RC	

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
87H		MIBs group 2.2 - **etherStatesPKts**, (upper word)	RO, RC	
88H		MIBs group 2.3 - **etherStatesBroadcastPkts**, (lower word)	RO, RC	
89H		MIBs group 2.3 - **etherStatesBroadcastPkts**, (upper word)	RO, RC	
8AH		MIBs group 2.4 - **etherStatesMulticastPkts**, (lower word)	RO, RC	
8BH		MIBs group 2.4 - **etherStatesMulticastPkts**, (upper word)	RO, RC	
8CH		MIBs group 2.5 - **etheStatesCRCAlignErrors**, (lower word)	RO, RC	
8DH		MIBs group 2.5 - **etheStatesCRCAlignErrors**, (upper word)	RO, RC	
8EH		MIBs group 2.6 - **etherStatesUndersizePkts**, (lower word)	RO, RC	
8FH		MIBs group 2.6 - **etherStatesUndersizePkts**, (upper word)	RO, RC	
90H		MIBs group 2.7 - **etheStatesOversizePkts**, (lower word)	RO, RC	
91H		MIBs group 2.7 - **etheStatesOversizePkts**, (upper word)	RO, RC	
92H		MIBs group 2.8 - **etherStatesFragments**, (lower word)	RO, RC	
93H		MIBs group 2.8 - **etherStatesFragments**, (upper word)	RO, RC	
94H		MIBs group 2.9 - **etheStatesJabbers**, (lower word)	RO, RC	
95H		MIBs group 2.9 - **etheStatesJabbers**, (upper word)	RO, RC	
96H		MIBs group 2.10 - **etherStatesCollisions**, (lower word)	RO, RC	
97H		MIBs group 2.10 - **etherStatesCollisions**, (upper word)	RO, RC	
98H		MIBs group 2.11 - **etheStatesPkts64Octets**, (lower word)	RO, RC	
99H		MIBs group 2.11 - **etheStatesPkts64Octets**, (upper word)	RO, RC	
9AH		MIBs group 2.12 - **etherStatesPkts65to127Octets**, (lower word)	RO, RC	
9BH		MIBs group 2.12 - **etherStatesPkts65to127Octets**, (upper word)	RO, RC	
9CH		MIBs group 2.13 - **etheStatesPkts128to255Octets**, (lower word)	RO, RC	

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
9DH		MIBs group 2.13 - **etheStatesPkts128to255Octets**, (upper word)	RO, RC	
9EH		MIBs group 2.14 - **etherStatesPkts256to511Octets**, (lower word)	RO, RC	
9FH		MIBs group 2.14 - **etherStatesPkts256to511Octets**, (upper word)	RO, RC	
A0H		MIBs group 2.15 - **etheStatesPkts512to1023Octets**, (lower word)	RO, RC	
A1H		MIBs group 2.15 - **etheStatesPkts512to1023Octets**, (upper word)	RO, RC	
A2H		MIBs group 2.16 - **etherStatesPkts1024to1522Octets**, (lower word)	RO, RC	
A3H		MIBs group 2.16 - **etherStatesPkts1024to1522Octets**, (upper word)	RO, RC	

4.8 PHY Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
C0H	00H	MII control register of P01 PHY: **MII register 0** bit[15] : 1 = PHY reset 0 = normal operation (default) This bit is self-clearing, IP113M will return a value of 1 before reset process is completed, and will not accept any write transaction of MII Management within reset process. bit[14] : 1 = Loopback mode 0 = normal operation **(**default) When this bit set, IP113M will be isolated from the network media, and the assertion of TXEN at the MII will not transmit data on the network. All MII transmit data path will return to MII receive data path in response to the assertion of TXEN. MII COL signal will remain de-asserted at all times, unless bit 0.7 (Collision Test) is set. bit[13] : 1 = 100Mbps (default) 0 = 10Mbps It is valid only if bit[12] is set to be 0. If bit[12] =1, the operation speed is selected by regC4(reg4) and regC5(reg5). Or you can read the value from reg38 directly. bit[12] : 1 = Auto-Negotiation Enable **(**default) 0 = Auto-Negotiation Disable regD0.11(reg16.11) auto-MDI/MDIX should be disabled if auto negotiation is disabled. bit[11] : 1 = power down 0 = normal operation (default) Setting this bit to 1 will cause IP113S LF TP port's PHY into power down mode, but still respond to management transactions. bit[10] : 1 = electrically isolate PHY from MII 0 = normal operation (default) When this bit is setting to 1, IP113M will be isolated from RMII, and not respond to the TXD[3:0] and TXEN and keep CRS, RXDV and RXD[3:0] in high impedance, but will respond to management transactions. If PHY address of IP113S LF is setting to 0 at power-on reset, this bit will be set to 1, otherwise will be set to 0. bit[9] : 1 = re-starting Auto-Negotiation 0 = Auto-Negotiation re-start complete (default)	R/W, SC R/W	0x3100

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		Setting this bit to logic high will cause TP port's PHY to restart an Auto-Negotiation cycle, but depend on the value of bit[12] (Auto-Negotiation Enable). If bit [12] is cleared then this bit has no effect, and change to Read Only. When an Auto-Negotiation cycle is being processed, write 0 into this bit has no effect. This bit is self-clearing after Auto-Negotiation process is completed. bit[8] : 1 = full duplex **(**default) 0 = half duplex It is valid only if bit [12] is set to be 0. bit[7] : 1 = enable the collision test 0 = disable the collision test (default) If setting this bit to logic 1, when MII TXEN signal is asserted, IP113M will assert the MII COL signal within 512BT (Bit Time, depend on 10Mbps or 100Mbps). When MII TXEN is de-asserted, then TP110 will assert MII COL signal within 4BT. Clearing this bit to logic 0 for normal operation. bit[6:0] : (reserved)	RO	
C1H	01H	MII status register of P01 PHY: **MII register 1** bit[15] : 1 = 100Base-T4 capable 0 = not 100Base-T4 capable (default) IP113S LF does not support 100Base-T4. This bit is fixed to be 0. bit[14] : 1 = 100Base-X full duplex capable (default) 0 = not 100Base-X full duplex capable bit[13] : 1 = 100Base-X half duplex capable (default) 0 = not 100Base-X half duplex capable bit[12] : 1 = 10Base-T full duplex capable (default) 0 = not 10Base-T full duplex capable bit[11] : 1 = 10Base-T half duplex capable (default) 0 = not 10Base-T half duplex capable bit[10:7] :Ignore on read bit[6] : 1 = preamble may be suppressed **(**default) 0 = preamble always required	RO	0x7845

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		bit[5] : 1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress (default) When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4, 5, 6 and 7 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4, 5, 6 and 7 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0. bit[4] : 1 = remote fault detected 0 = not remote fault detected **(**default) When read as logic 1, indicates that IP113S LF has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP113S LF reset. bit[3] : 1 = Auto-Negotiation capable (default) 0 = not Auto-Negotiation capable When read as logic 1, indicates that IP113S LF has the ability to perform Auto-Negotiation. The value of this bit will depend on the external mode setting of IP113S LF operation mode. bit[2] : 1 = Link Pass 0 = Link Fail (default) When read as logic 1, indicates that IP113S LF has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers. bit[1] : 1 = jabber condition detected 0 = no jabber condition detected (default) When read as logic 1, indicates that IP113S LF has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP113S LF reset. This bit is set until jabber condition is cleared and reading the contents of the register. bit[0] : 1 = Extended register capabilities **(**default) 0 = No extended register capabilities IP113S LF has extended register capabilities.		

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
C2H	02H	MII identifier register of P01 PHY: **MII register 2** bit[15:0] : IP113S LF OUI (Organizationally Unique Identifier) ID, the msb is 3rd bit of IP113S LF OUI ID, and the lsb is 18th bit of IP113S LF OUI ID. IP113S LF OUI is 0x0090C3.	RO	0x0243
C3H	03H	MII identifier register of P01 PHY: **MII register 3** bit[15:10] : IP113S LF OUI ID, the msb is 19th bit of IP113S LF OUI ID, and lsb is 24th bit of IP113S LF OUI ID. bit[9:4] : (IP113S LF model number) bit[3:0] : (IP113M revision number)	RO	0x0C50

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
C4H	04H	MII advertisement register of P01 PHY: **MII register 4** bit[15] : 1 = Next Page ability is supported 0 = Next Page ability is not supported (default) IP113M does not support next page, this bit is fixed to be 0. bit[14] :Reserved by IEEE, write as 0, ignore on read. bit[13] : 1 = Advertises that this device has detected a remote fault. 0 = No remote fault detected (default) bit[12] :Reserved for future IEEE use, write as 0, ignore on read. bit[11] : 1 = Asymmetric pause operation for full duplex 0 = No asymmetric pause function supported (default) bit[10] : 1 = Advertises that this device has implemented function.(default) 0 = No pause function supported bit[9] : 1 = 100BASE-T4 is supported 0 = 100BASE-T4 is not supported (default) bit[8] : 1 = 100BASE-TX full duplex is supported (default) 0 = 100BASE-TX full duplex is not supported bit[7] : 1 = 100BASE-TX is supported (default) 0 = 100BASE-TX is not supported bit[6] : 1 = 10BASE-T full duplex is supported (default) 0 = 10BASE-T full duplex is not supported bit[5] : 1 = 10BASE-T is supported (default) 0 = 10BASE-T is not supported bit[4:0] Use to identify the type of message being sent by Auto-Negotiation. (default = 0x01)		

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
C5H	05H	MII auto-negotiation link partner basic page ability of P01 PHY: **MII register 5** bit[15] : 1 = Next Page ability is supported by link partner. 0 = Next Page ability is not supported by link partner. bit[14] : 1 = Link partner has received the ability data word. 0 = Not acknowledge. bit[13] : 1 = Link partner indicates a remote fault. 0 = No remote fault indicate by link partner. If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic1. bit[12] :Reserved by IEEE for future use, write as 0, read as 0. bit[11] : 1 = Link partner supports asymmetric pause. 0 = Link partner does not support asymmetric pause. bit[10] : 1 = Link partner supports pause function. 0 = Link partner does not support pause function. bit[9] : 1 = Link partner support 100BASE-T4. 0 = Link partner is not support 100BASE-T4. bit[8] : 1 = Link partner support 100BASE-TX full duplex. 0 = Link partner is not support 100BASE-TX full duplex. bit[7] : 1 = Link partner support 100BASE-TX. 0 = Link partner is not support 100BASE-TX. bit[6] : 1 = Link partner support 10BASE-T full duplex. 0 = Link partner is not support 10BASE-T full duplex. bit[5] : 1 = Link partner support 10BASE-T. 0 = Link partner is not support 10BASE-T. bit[4:0] :Protocol selector of the link partner.	RO	0x0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
C6H	06H	MII auto-negotiation expansion register of P01 PHY: **MII register 6** bit[15:5] :Reserved by IEEE, writes as 0, ignore on read. bit[4] : 1 = A fault has been detected via Parallel Detection function. 0 = A fault has not detected via Parallel Detection function. (default) bit[3] : 1 = Link Partner is Next Page able. 0 = Link Partner is not Next Page able. (default) bit[2] : 1 = Local Device is Next Page able. (default) 0 = Local Device is not Next Page able. bit[1] : 1 = A New Page has been received. 0 = A New Page has not been received. (default) bit[0] : 1 = Link Partner is Auto-Negotiation able. 0 = Link Partner is not Auto-Negotiation able. (default)	 RO RO,IH RO RO,IH	0x0004
C7H C8H		(not used)		
C9H~ CFH	09H~ 0FH	MII registers reserved for P01 DSP:		

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
D0H	10H	MII specific control register of P01 PHY: bit[15:12] :This bit should be “0” for normal operation. bit[11] : Auto Crossover function disable. 1: disable, 0: enable (default) It should be disabled if MII register 0.12 auto-negotiation is disabled. bit[10] : Heart Beat function enable. 1: enable, 0:disable (default) The default value is recommended to adopt. bit[9] : Jabber function enable. 1: enable, 0:disable (default) The default value is recommended to adopt. bit[8] : Far-End-Fault function disable. 1: disable, 0: enable (default) The default value is recommended to adopt. bit[7] : Analog power save mode disable 1: disable, 0: enable (default) The default value is recommended to adopt. bit[6] : 10Mb transmit NLP disable. 1: disable, 0: enable (default) This bit should be “0” for normal operation. bit[5] : Bypass DSP re-start function in PCS. 1: bypass DSP re-start, 0: not bypass (default) This bit should be “0” for normal operation. bit[4] : Bypass PCS 4B/5B coder (It is valid only if bit[15]=1.) 1: bypass 4B/5B, 0: not bypass (default) This bit should be “0” for normal operation. bit[3] : Bypass PCS scrambler (It is valid only if bit[15]=1.) 1: bypass scrambler, 0: not bypass (default) This bit should be “0” for normal operation. bit[2:0] : This bit should be “0” for normal operation.	R/W	0x0000
D1H	11H	MII interrupt register of P01 PHY: bit[15:14] : (reserved) bit[13] : Mask all Interrupt. It enables the all mask bits bit[7]~bit[12]. 1: mask interrupt (default), 0: not mask bit[12] : Reserved		0x3F00

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		bit[11] : Reserved bit[10] : Mask TP port speed mode change Interrupt A mask for bit bit[2]. 1: mask interrupt (default), 0: not mask bit[9] : Mask TP port duplex mode change Interrupt A mask for bit bit[1]. 1: mask interrupt (default), 0: not mask bit[8] :Mask TP port link change Interrupt. A mask for bit bit[0]. 1: mask (default), 0: not mask bit[7] : Remote LP power abnormal interrupt enable. A mask for bit bit[6]. 1: not mask interrupt, 0: mask interrupt (default) bit[6] :Power abnormal It is logic “1” when IP113S LF receives a maintenance frame with link partner's power abnormal message and it will active interrupt pin. It is self-clear after reading the register. 1: remote link partner power abnormal, 0: nothing happen (default) bit[5] : Interrupt status It is logic “OR” of bit bit[0]~bit[4]. 1: any interrupt occur, 0: no interrupt (default) bit[4] : Reserved bit[3] : Reserved bit[2] : Speed mode change It is logic “1” when speed changes on TP port and it will active interrupt pin. It is self-clear after reading the register. 1: speed change interrupt occur, 0: no interrupt (default) bit[1] : Duplex mode change It is logic “1” when duplex status changes on TP port and it will active interrupt pin. It is self-clear after reading the register. 1: duplex status change Interrupt occur, 0: no interrupt (default) bit[0] : Link status change It is logic “1” when link status changes on TP port and it will active interrupt pin. It is self-clear after reading the register. 1: link status change Interrupt occur, 0: no interrupt (default)		

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
D2H	12H	MII extend status register of P01 PHY: bit[15] : (reserved) bit[14] : TP port speed mode (It is valid only if bit[11]=1.) 1: 100M (default), 0: 10M It is a mirror bit of register regC0.13. bit[13] : TP port duplex mode (It is valid only if 8.11=1.) 1: full duplex (default), 0: half duplex It is a mirror bit of regC0.8. bit[12] : (reserved) bit[11] : Resolve complete 1: Auto-negotiation complete, 0: during Auto-negotiation (default) It is a mirror bit of regC1.5. bit[10] : TP port link Status 1: link ok, 0: link fail (default) It is a mirror bit of regC0.2. bit[9] : MDI/MDIX status 0: MDI, TX and RX are normal on TP port. 1: MDIX, TX and RX are crossed over on TP port. bit[8] : Polarity status 1: polarity error, RXIP and RXIM are reversed, 0: polarity ok (default) bit[7] : Jabber status 1: jabber is detected, 0: no jabber (default) It is a mirror bit of regC1.1. bit[6:0] : (reserved)	RO	0x4008
D7H	-	MII control register of P02 PHY: **MII register 0** (P02 do not support auto-negotiation)		

5 Electrical Characteristics

5.1 Absolute Maximum Rating

Permanent device damage may occur if Absolute Maximum Ratings are applied. Functional operation should be restricted to the conditions as specified in the following section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

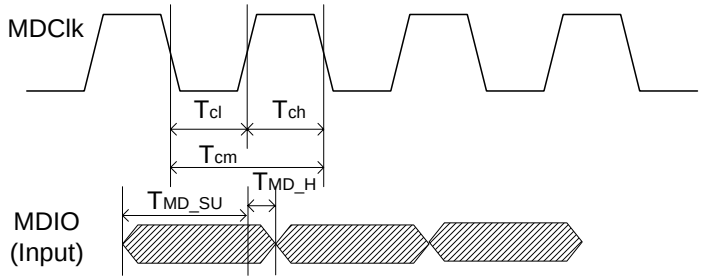
PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	I/O	$V_{DDI/O}$	– 0.5	+3.6V	V
	Core	V_{DDCore}	– 0.5	+1.9V	V
Input Voltage		V_I	– 0.5	$V_{DDI/O}$	V
Output Voltage		V_O	– 0.5	$V_{DDI/O}$	V
Storage Temperature		T_{STG}	-65	+150	°C
Operation Temperature		T_{OPT}	-40	+85	°C

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

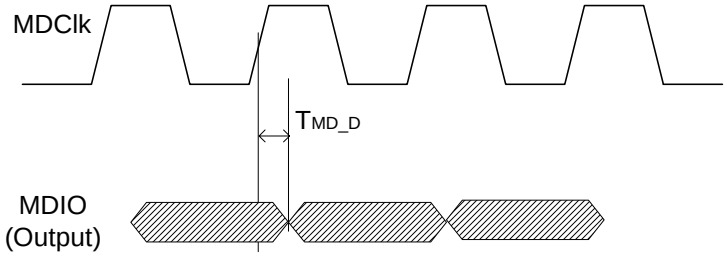
5.2 AC Characteristics

PHY Management (MDIO) Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDCK High Time	-	200	-	ns
T_{cl}	MDCK Low Time	-	200	-	ns
T_{cm}	MDCK cycle time	-	400	-	ns
T_{MD_SU}	MDIO set up time	10	-		ns
T_{MD_H}	MDIO hold time	10	-	-	ns
T_{MD_D}	MDIO output delay time	200	-	210	ns



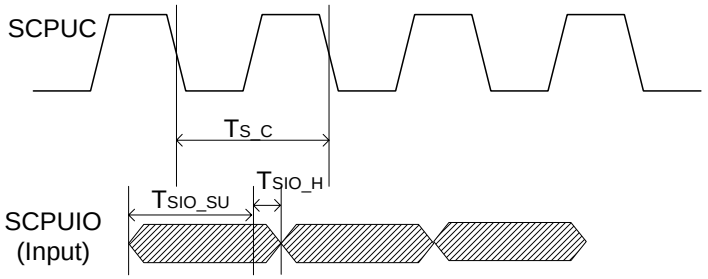
MDIO Input Cycle



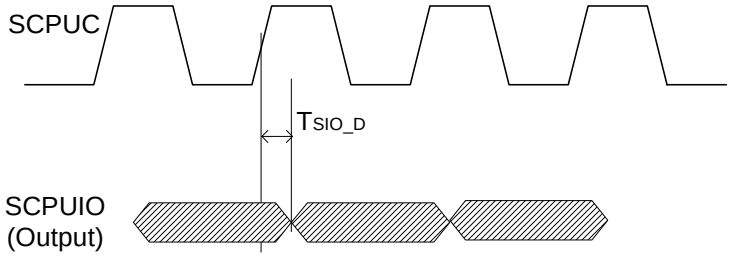
MDIO Output Cicle

CPU Serial Bus Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{S_C}	SCPUC cycle time	400		-	ns
T_{SIO_SU}	Serial I/O set up time	10	-		ns
T_{SIO_H}	Serial I/O hold time	10	-	-	ns
T_{SIO_D}	Serial I/O output delay time		-	20	ns



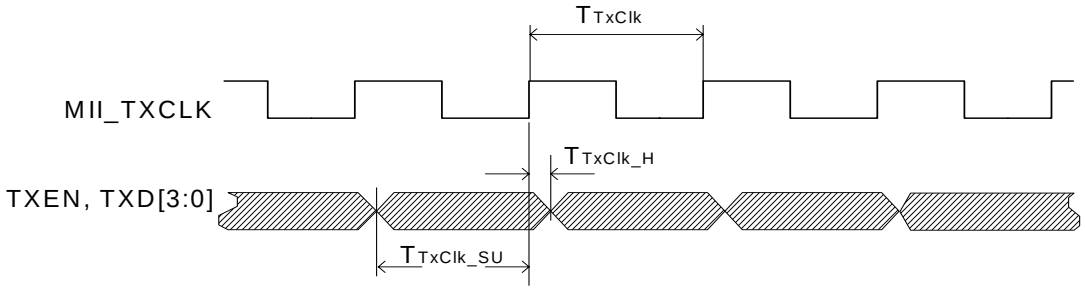
Serial I/O Input Cycle



Serial I/O Output Cycle

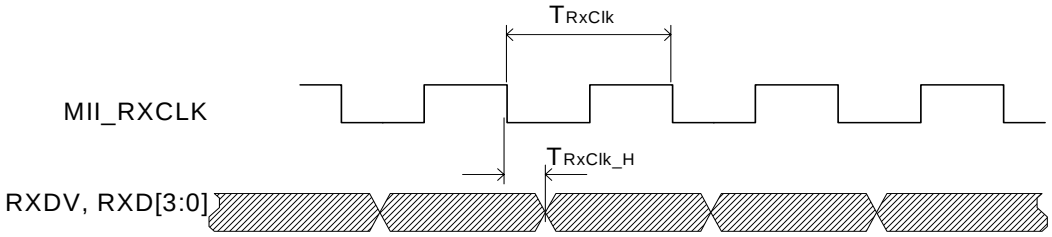
MII Transmit Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100Mbps MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10Mbps MII	-	400	-	ns
T_{TxClk_SU}	TXEN, TXD to MII_TXCLK setup time	2	-	-	ns
T_{TxClk_H}	TXEN, TXD to MII_TXCLK hold time	0.5	-	-	ns



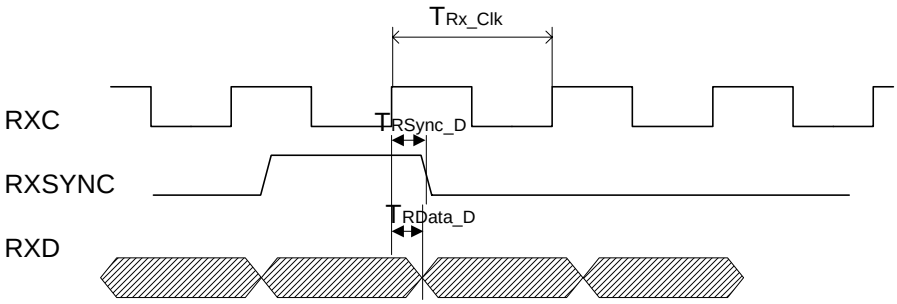
MII Receive Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100Mbps MII	-	40	-	ns
T_{RxClk}	Receive clock period 10Mbps MII	-	400	-	ns
T_{RxClk_D}	MII_RXCLK falling edge to RXDV, RXD	1	-	4	ns



SMII Receive Timing

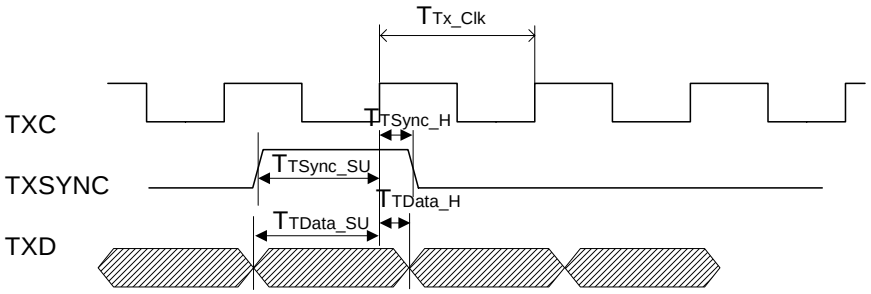
Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rx_Clk}	Receive clock cycle time	-	8	-	ns
T_{RSync_D}	Rx_Clk to RX_Sync output delay	1.0		5.0	ns
T_{RData_D}	Rx_Clk to RXD output delay	1.0	-	5.0	ns



SS-SMII Receive

SMII Transmit Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Tx_Clk}	Transmit clock cycle time	-	8	-	ns
T_{TSync_SU}	Tx_Sync Set up time	2.0			ns
T_{TData_H}	Tx_Sync Hold time	1.0	-		ns
T_{TData_SU}	TxData Set up time	2.0			ns
T_{TData_H}	TxData Hold time	1.0	-		ns



SS-SMII Transmit

5.3 DC Characteristics

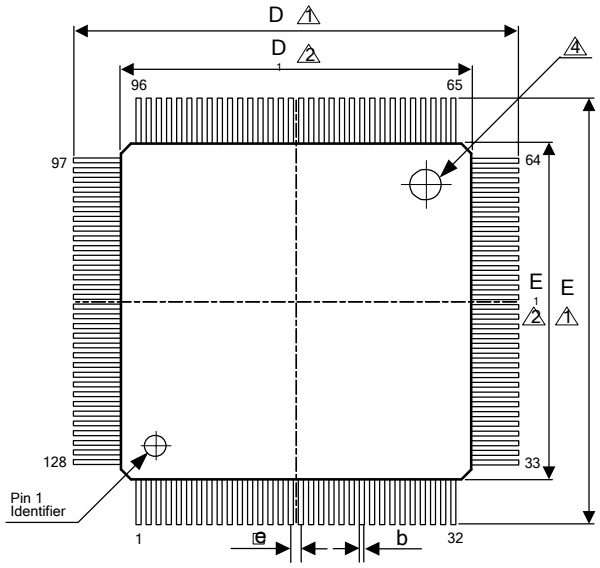
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output low voltage	V_{OL}			0.4	V
Output high voltage (Condition: VDD33 is 3.3 volt)	V_{OH}	3			V
Low level input current	I_{OL}		2		mA
High level output current	I_{OH}		2		mA
VDD33 operation current (Condition: 100M full duplex)			29		mA
VDD25 operation current (Condition: 100M full duplex)			229		mA
VDD33 supply voltage			3.3		V
VDD25 supply voltage			2.5		V
SS-SMII Input Low to High threshold (3.3V operation)	V_{T+}	1.66	1.75	1.79	V
SS-SMII Input High to Low threshold (3.3V operation)	V_{T-}	0.93	1.01	1.06	V
Pull-down resistor	R_{PD}	51		127	KΩ

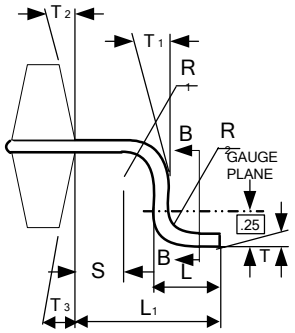
6 Order Information

Part No.	Package	Notice
IP113S LF	128-PIN LQFP	Lead Free

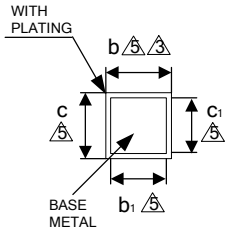
7 Package Detail

LQFP 128 (14mm x 14mm x 1.4mm) Outline Dimensions Unit: inches/mm



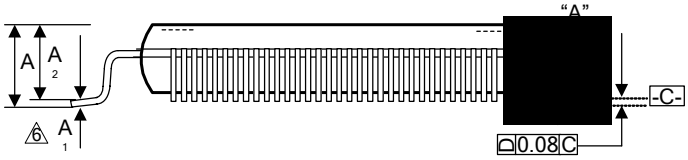


DETAIL "A"



SECTION B-B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	-	0.002	-	-
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	-	0.20	0.004	-	0.008
c1	0.09	-	0.16	0.004	-	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.45	0.018	0.024	0.030
L1	1.00REF			0.039REF		
R1	0.08	-	-	0.003	-	-
R2	0.08	-	0.20	0.030	-	0.008
S	0.20	-	-	0.008	-	-
T	0°	3.5°	7°	0°	3.5°	7°
T1	0°	-	-	0°	-	-
T2	12°TYP			12°TYP		
T3	12°TYP			12°TYP		



Note:

1. To be determined at seating plane -C- .
2. Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Dambar can not be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the Package body.
7. Controlling dimension : Millimeter.