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International
IOR Rectifier

iP1203PbF

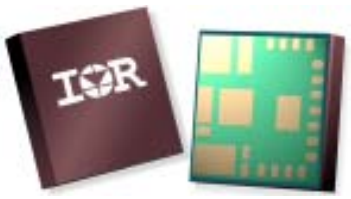
iPOWIR™ TECHNOLOGY

Single Output Full Function Synchronous Buck Power Block

Integrated Power Semiconductors, PWM Control & Passives

Features

- 5.5V to 13.2V Input Voltage
- 0.8V to 8V Output Voltage
- 15A Maximum Load Capability
- 200-400kHz Nominal Switching Frequency
- Over Current Hiccup
- External Synchronization Capable
- Overvoltage Protection
- Over Temperature Protection
- Internal Features Minimize Layout Sensitivity
- Very Small Outline 9mm x 9mm x 2.3mm



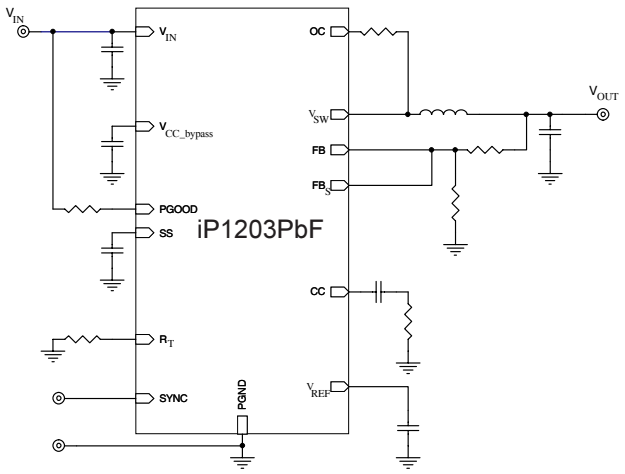
iP1203PbF Power Block

Description

The iP1203PbF is a fully optimized solution for medium current synchronous buck applications requiring up to 15A. It includes full function PWM control, with optimized power semiconductor chipsets and associated passives, achieving high power density. Very few external components are required to create a complete synchronous buck power supply.

iPOWIR™ technology offers designers an innovative space-saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.

iP1203PbF Simplified Application Schematic



PACKAGE DESCRIPTION	INTERFACE CONNECTION	PARTS PER BAG	PARTS PER REEL	T & R ORIENTATION
iP1203PbF	LGA	10	---	Fig 26
iP1203TRPbF	LGA	---	1000	

Pin Number (See Page 18)	Pin Name	Pin Description
1, 23	V_{IN}	Input voltage connection pins
2,3,4,5,7,17,20,21	PGND	Power Ground pins
6	V_{CC_bypass}	PWM controller power supply pin. Internally generated. Requires a 2.2µf external bypass capacitor
8	SS	Soft start pin. External capacitor provides soft start. Pulling soft start pin low will disable the output. Cannot be cycled to unlatch OVP trip
9	CC	Output of the error amplifier
10	FB	Inverting input of the error amplifier
11	FB_s	Output overvoltage sense pin.
12	R_T	Switching frequency setting pin. For R_T selection, refer to Fig.9 of the datasheet
13	PGOOD	Power Good pin. Open collector, requires external pulll-up. If function not needed, pin can be left floating
14	V_{REF}	Non inverting input of the error amplifier (reference Voltage pin). Connect a 100pF cap from this pin to PGND.
15	SYNC	External Clock synchronization pin. Set free running frequency to 80% of the SYNC frequency. When not in use, leave pin floating
16	OCSET	Output overcurrent trip threshold pin
18,19	V_{SW}	Output inductor connection pins
22	V_{SWs}	Test pad, for internal use, short to VSW
24	V_{INs}	Test pad, for internal use, short to V_{IN}

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units	Conditions
V_{IN}	V_{IN}	-0.3	——	15	V	
Feedback	FB	-0.3	——	6		
Output Overvoltage Sense	FB_S	-0.3	——	6		
PGOOD		-0.3	——	15		
Soft Start	SS	-0.3	——	6		
SYNC		-0.3	——	6		
Output RMS Current	$Iout_{VSW}$	——	——	15	A	See Fig.3
Block Temperature	T_{BLK}	-10	——	125	°C	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Voltage Range	V_{IN}	5.5	——	13.2	V	
Output RMS Current	$Iout_{VSW}$	——	——	15	A	T_{PCB} = T_{CASE} = 90°C. See Fig.3
		——	——	11	A	T_{PCB} = 90°C, T_{CASE} = no airflow, no heatsink.
Output Voltage Range	V_{OUT}	0.8	——	8.0	V	For V_{IN} = 12V
		0.8	——	3.3		For V_{IN} = 5.5V

Electrical Specifications @ V_{IN} = 12V

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Power Loss	P_{LOSS}	——	3.75	4.9	W	f_{SW} = 300kHz, V_{IN} = 12V, T_{BLK}= 25°C V_{OUT} = 1.5V, I_{OUT} = 15A, See Fig.10
Over Current Shutdown	I_{OC}	——	25	——	A	V_{IN} = 12V, V_{OUT} = 1.5V f_{SW} = 300KHz, R_{OCSET} = 40.2kΩ
HICCUP Duty Cycle	D_{HICCUP}	——	5	——	%	
Soft Start Time	t_{SS}	——	5	——	ms	V_{IN} = 12V, V_{OUT} = 1.5V, C_{SS}=0.1µF
Reference Voltage	V_{REF}	——	0.8	——	V	
V_{OUT} Accuracy	V_{OUT_ACC1}	-3	——	3	%	T_{BLK} = -10°C to 125°C V_{IN}= 12V, V_{OUT} = 1.5V
	V_{OUT_ACC2}	-2	——	2		T_{BLK} = 0°C to 70°C V_{IN}= 12V, V_{OUT} = 1.5V
Error Amplifier Source/Sink Current	I_{ERR}	——	60	——	µA	
Error Amplifier Transconductance	g_m	——	2000	——	µmho	
Output Overvoltage Shutdown Threshold	OVP	1.1 x V_{OUT}	1.15 x V_{OUT}	1.2 x V_{OUT}	V	
PGOOD Trip Threshold	V_{Th_PGOOD}	——	0.85 x V_{OUT}	——	V	FB ramping down
PGOOD Output Low Voltage	V_{LO_PGOOD}	——	——	0.3	V	I_{SINK}=2mA

Electrical Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Frequency	f_{SW}	170	——	230	kHz	R_T = 48.7kΩ
		255	——	345	kHz	R_T = 30.9kΩ
		340	——	460	kHz	R_T = 21.5kΩ
SYNC Frequency Range	f_{SYNC}	480	——	800	kHz	Free running frequency set 20% below sync frequency
SYNC Pulse Duration	t_{SYNC}	——	200	——	ns	
SYNC, High Level Threshold Voltage		2	——	——	V	
SYNC, Low Level Threshold Voltage		——	——	0.8	V	
V_{IN} Quiescent Current	$I_{IN-LEAKAGE}$	——	25	35	mA	V_{IN} = 12V
Thermal Shutdown	$Temp_{shdn}$	——	140	——	°C	
Max Duty Cycle	D_{MAX}	85	——	——	%	f_{SW}= 200kHz, T_{BLK} = 25°C
V_{IN} Undervoltage Lockout Threshold Voltage	$V_{IN-UVLO}$	——	4.5	——	V	V_{IN} ramping up to 12V
V_{IN} Undervoltage Lockout Hysteresis	$V_{IN-UVLO\ HYST}$	——	0.25	——	V	V_{IN} ramp up and ramp down
Output Disable Voltage Soft Start Low Threshold Voltage	V_{SS-DIS}	——	——	0.25	V	SS Pin Pulled Low
Input Voltage Slew Rate	$V_{IN-SLEW}$	——	——	50	mV/µs	

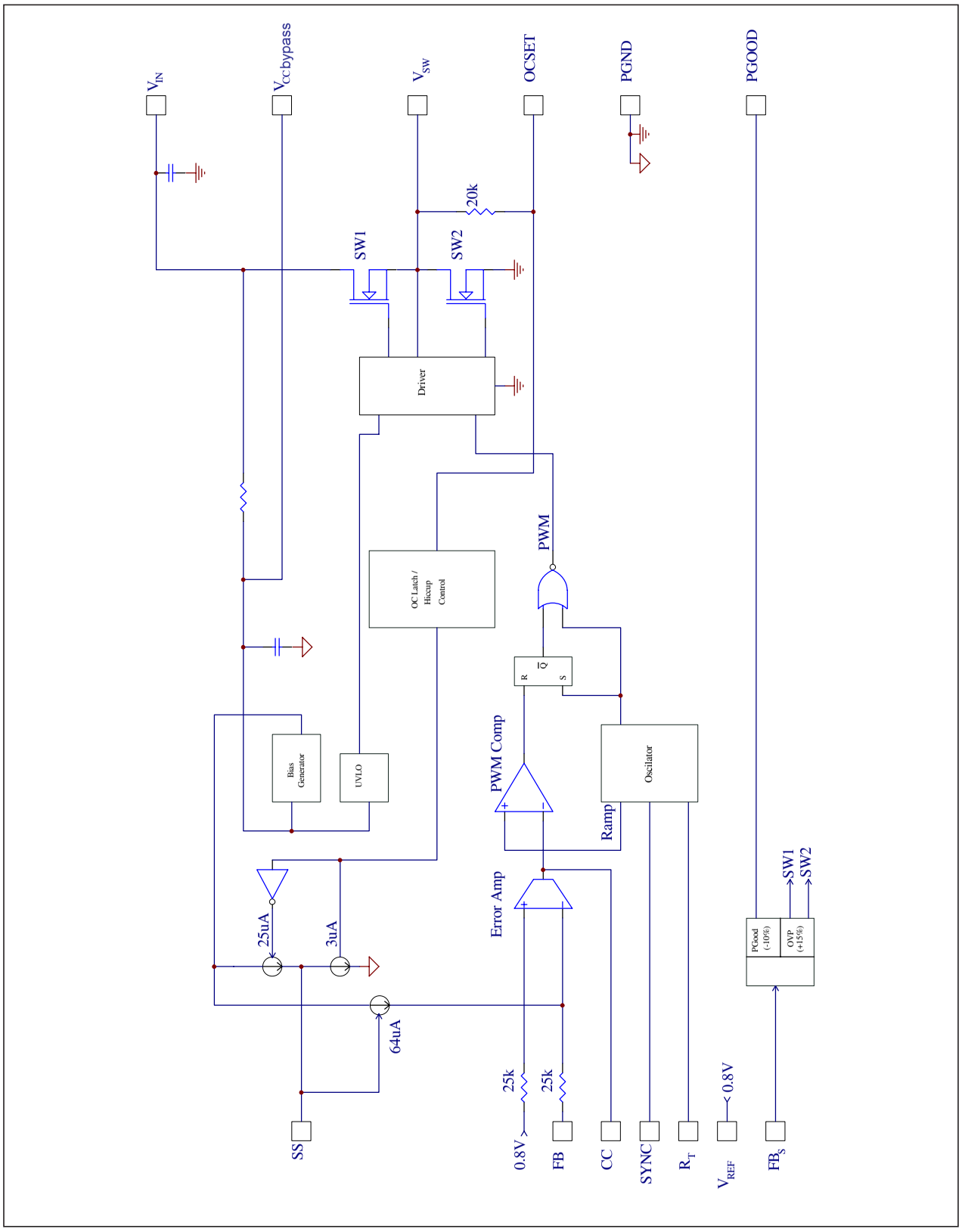


Fig. 1: iP1203PbF Internal Block Diagram

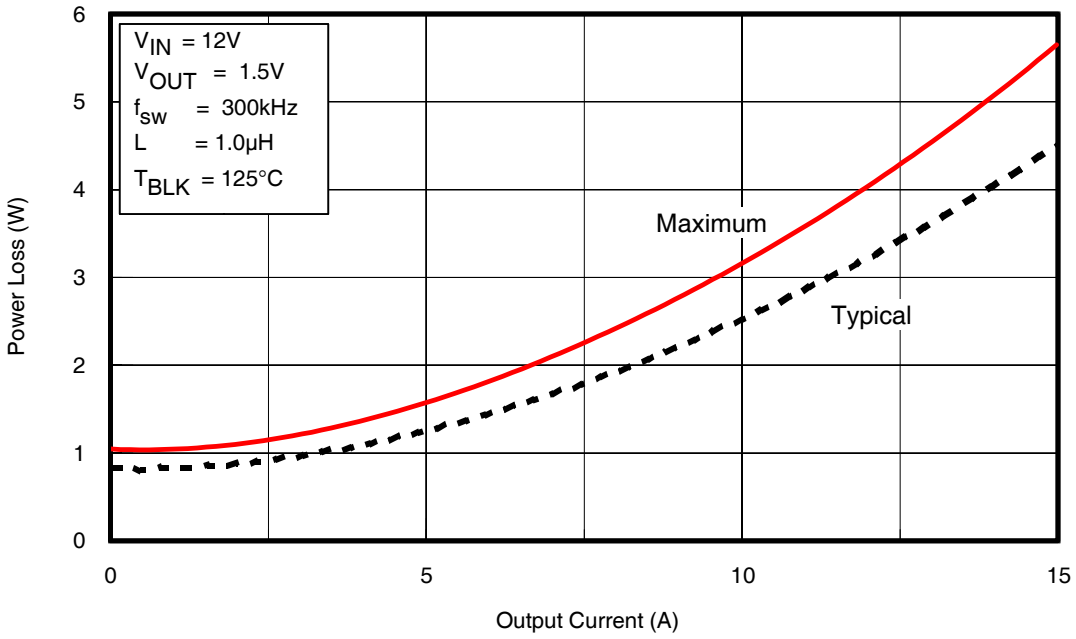


Fig. 2: Power Loss vs. Current

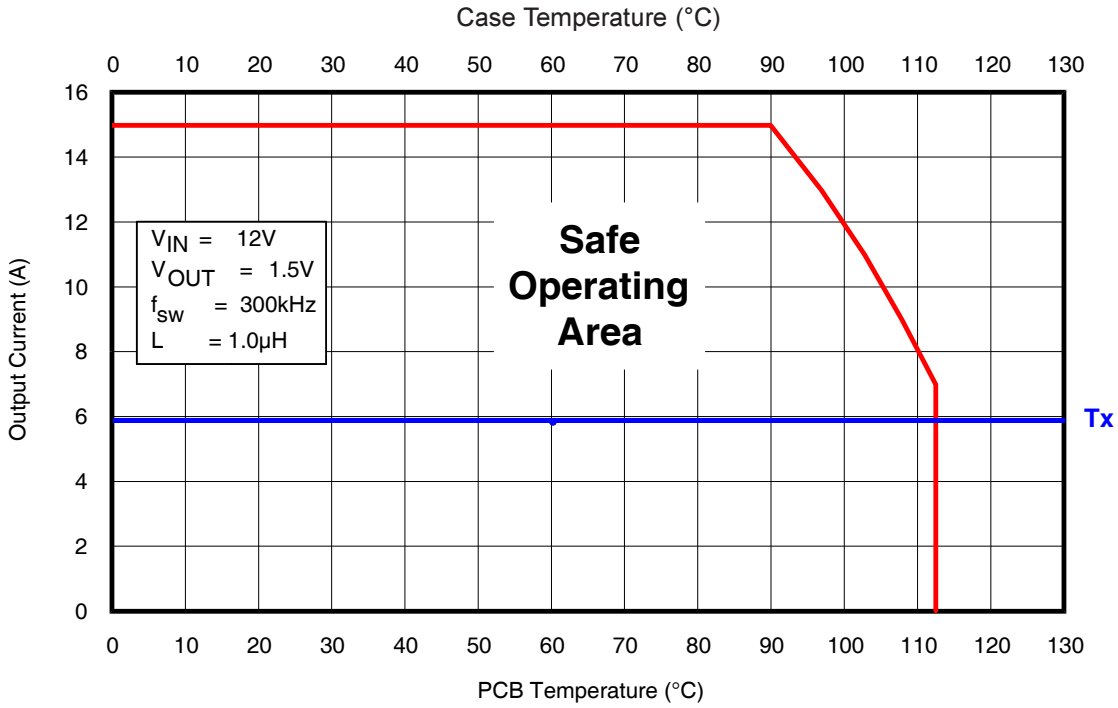


Fig. 3: Safe Operating Area (SOA) vs. T_{PCB} & T_{CASE}

Typical Performance Curves

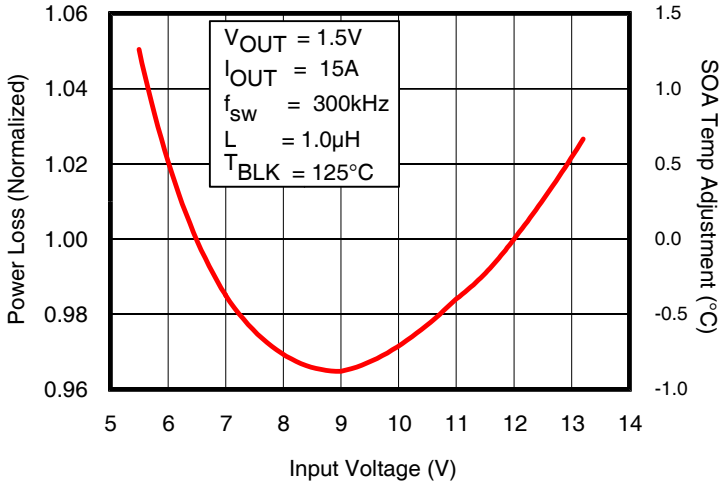


Fig. 4: Normalized Power Loss vs. V_{IN}

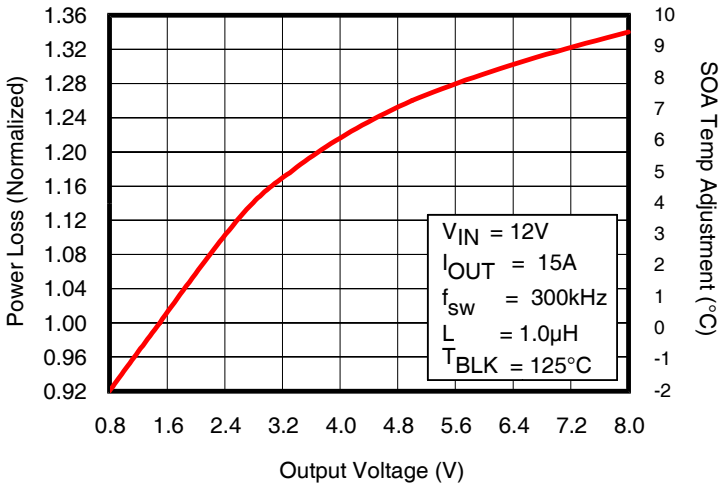


Fig. 5: Normalized Power Loss vs. V_{OUT}

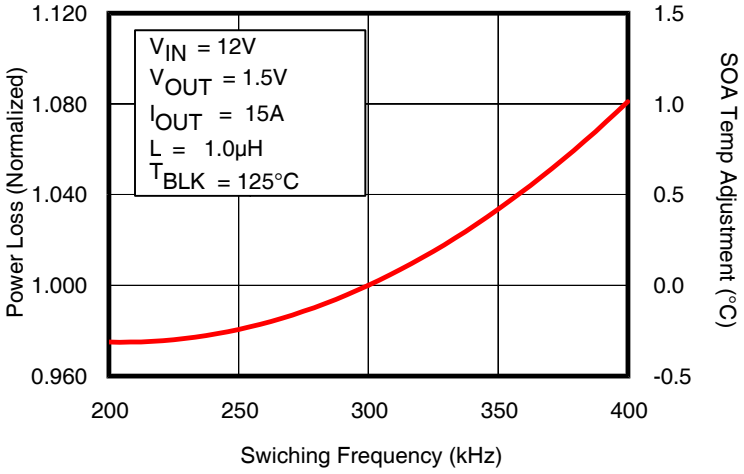


Fig. 6: Normalized Power Loss vs. Frequency

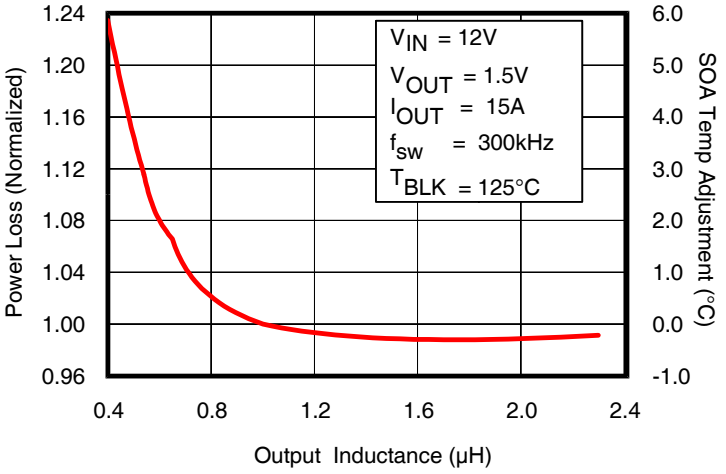


Fig. 7: Normalized Power Loss vs. Inductance

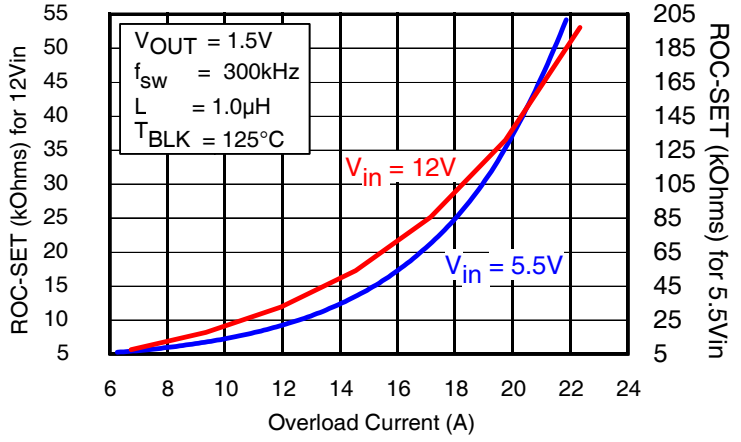


Fig. 8: Nominal Overcurrent Threshold Setting External Resistor Selection

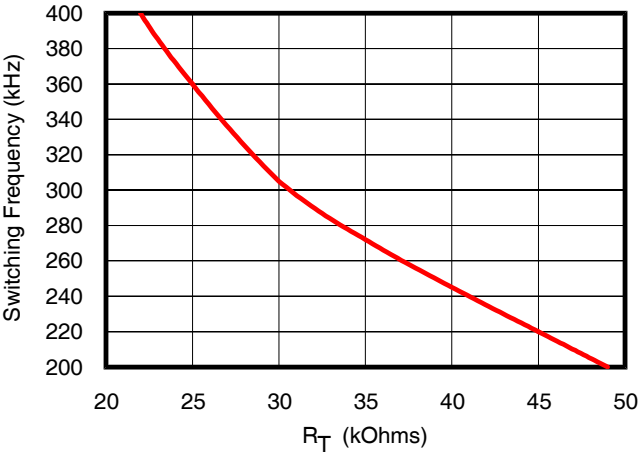


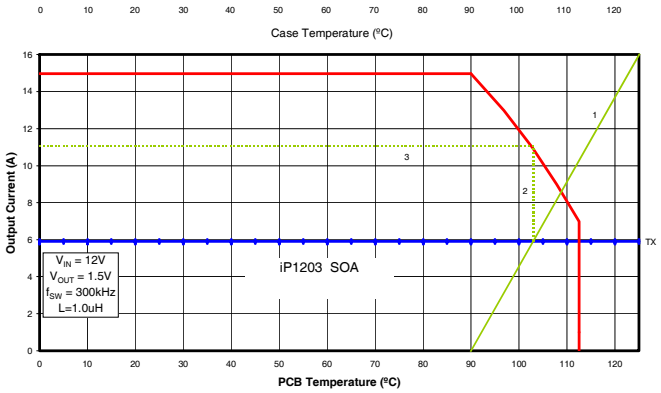
Fig. 9: Switching Frequency vs R_T

Applying the Safe Operating Area (SOA) Curve

The SOA graph incorporates power loss and thermal resistance information in a way that allows one to solve for maximum current capability in a simplified graphical manner. It incorporates the ability to solve thermal problems where heat is drawn out through the printed circuit board and the top of the case.

Procedure

1) Draw a line from Case Temp axis at T_{CASE} to the PCB Temp axis at T_{PCB}.
2) Draw a vertical line from the T_X axis intercept to the SOA curve. (see AN-1047 for further explanation of T_X)
3) Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y axis. The point at which the horizontal line meets the y-axis is the SOA current.
4) If no top sided heatsinking is available, assume T_{CASE} temperature of 125°C for worst case performance.



Adjusting the Power Loss and SOA Curves for Different Operating Conditions

To make adjustments to the power loss curves in Fig. 2, multiply the normalized value obtained from the curves in Figs. 4, 5, 6 or 7 by the value indicated on the power loss curve in Fig. 2. Then if multiple adjustments are required, multiply all of the normalized values together, then multiply that product by the value indicated on the power loss curve in Fig. 2. The resulting product is the final power loss based on all factors. See example no. 1.

To make adjustments to the SOA curve in Fig. 3, determine your maximum PCB Temp & Case Temp at the maximum operating current of each iP1203PbF. Then, add the correction temperature from the normalized curves in Figs. 4, 5, 6 or 7 to the T_X axis intercept (see procedure no. 2 above) in Fig. 3. When multiple adjustments are required, add all of the temperatures together, then add the sum to the T_X axis intercept in Fig. 3. See example no. 2.

Operating Conditions for the following examples:

Output Current = 12A
Output Voltage = 1.2V
Input Voltage = 13.2V
Sw Freq= 400kHz
Inductor = 0.6µH

Example 1) Adjusting for Maximum Power Loss:

(Fig. 2) Maximum power loss = 4.1W
(Fig. 4) Normalized power loss for input voltage ≈ 1.025
(Fig. 5) Normalized power loss for output voltage ≈ 0.97
(Fig. 6) Normalized power loss for frequency ≈ 1.08
(Fig. 7) Normalized power loss for inductor value ≈ 1.08

Adjusted Power Loss = 4.1 x 1.025 x 0.97 x 1.08 x 1.08 ≈ 4.75W

Example 2) Adjusting for SOA Temperature:

Assuming T_{CASE} = 110°C & T_{PCB} = 90°C for both outputs

Output1 (Fig. 4) Normalized SOA Temperature for input voltage ≈ +0.7°C

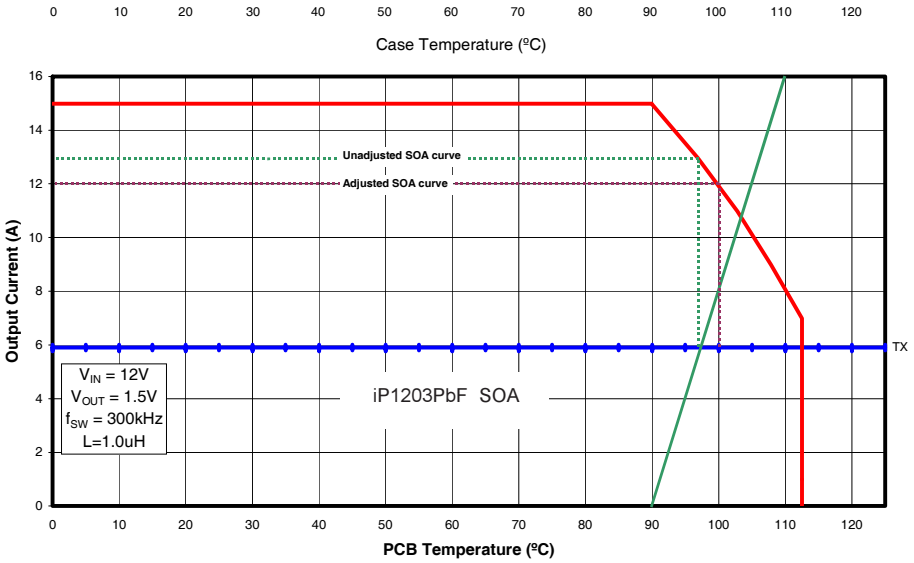
(Fig. 5) Normalized SOA Temperature for output voltage ≈ -0.75°C

(Fig. 6) Normalized SOA Temperature for frequency ≈ +1.0°C

(Fig. 7) Normalized SOA Temperature for inductor value ≈ +2.0°C

T_X axis intercept temp adjustment = +0.5°C - 0.75°C + 1.0°C +2.0°C ≈ +2.75°C

The following example shows how the SOA current is adjusted for a T_X change of +2.75°C and output is **in SOA**



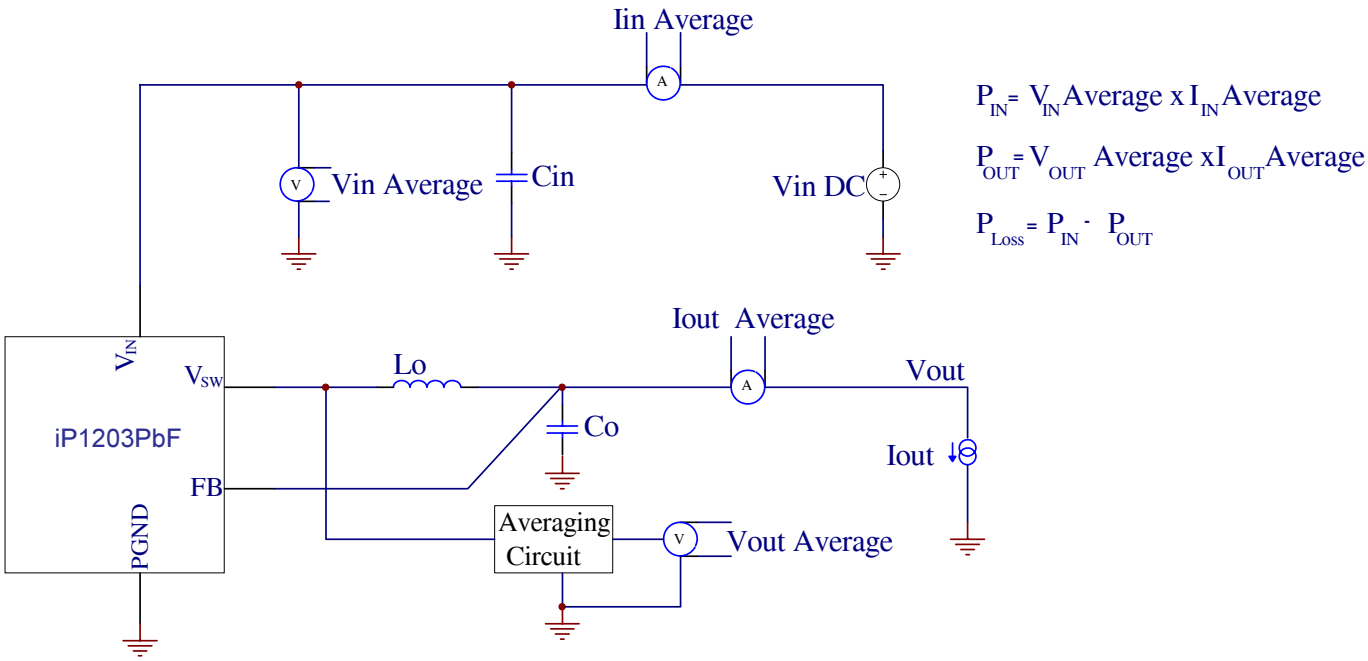


Fig. 10: Power Loss Test Circuit

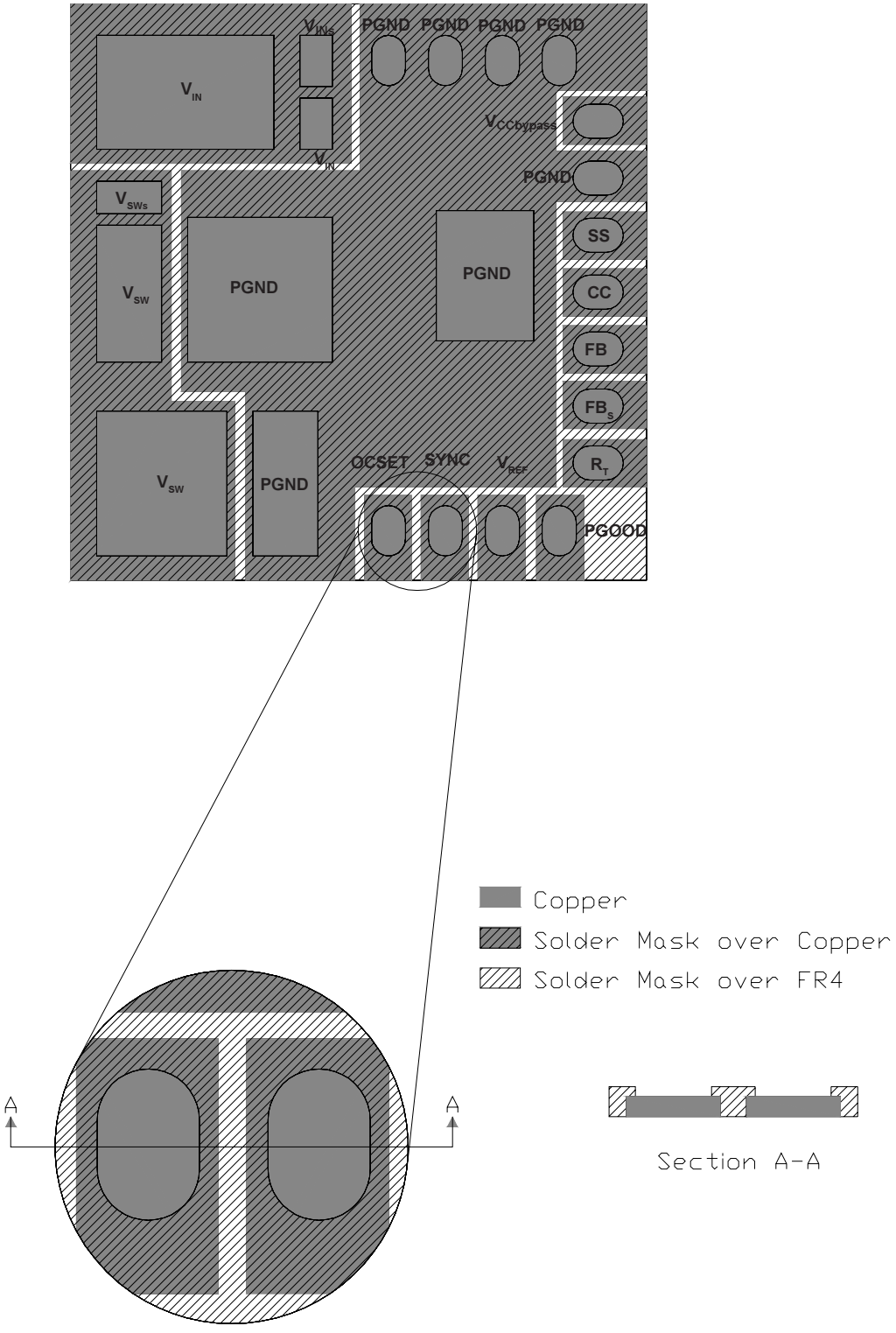


Fig. 11: Recommended PCB Footprint (Top View)

iP1203PbF User's Design Guidelines

The iP1203PbF is a single output 15A power block consisting of optimized power semiconductors, PWM control and its associated passive components. It is based on a synchronous buck topology and offers an optimized solution where space, efficiency and noise caused by parasitics are of concern. The power block operates with fixed frequency voltage mode control. The iP1203PbF components are integrated in a land grid array (LGA) package.

V_{IN} / Enabling the Output

The input operating voltage range of the iP1203PbF is 5.5V to 13.2V.

The iP1203PbF output is turned on upon application of input voltage. The V_{IN} slew rate should not exceed 50mV/µs. The converter can also be turned on and off by releasing or pulling the SS pin low through a logic level MOSFET, the drain of which connects to the soft start pin (see Fig.12). This feature can be useful if sequencing or different start-up timing of different system outputs are required. In situations where the output has undergone a latched shutdown due to overvoltage, cycling Vin will reset the output. Cycling soft start pin will not unlatch the output.

Soft Start

The Soft Start function provides a controlled rise of the output voltage, thus limiting the inrush current. The soft start function has an internal 25µA +/-20% current source that charges the external soft start capacitor C_{ss} up to 3V. During power-up, the output voltage starts ramping up only after the charging voltage across the C_{ss} capacitor has reached a 0.8Vtyp threshold, as shown in Fig. 13.

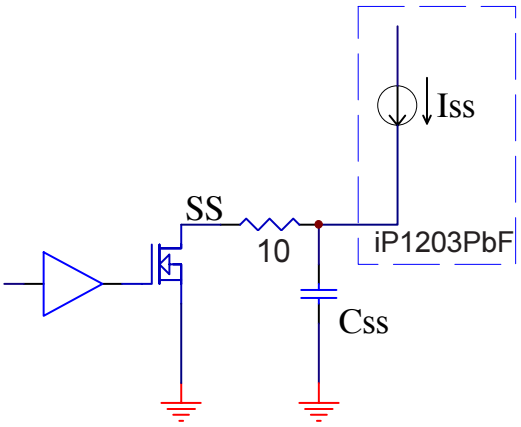


Fig.12: Soft Start/Enable Circuit

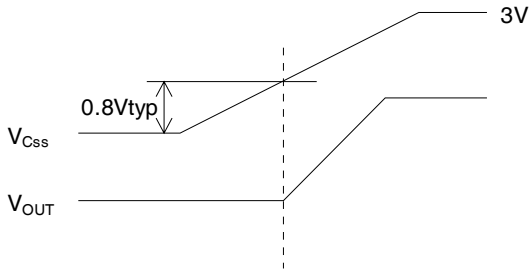


Fig. 13: Power Up Threshold

Frequency and Synchronization

The operating switching frequency (f_{SW}) range of iP1203PbF is 200 kHz to 400 kHz. The desired frequency is set by placing an external resistor to the R_T pin of the iP1203PbF. See Fig. 9 for the proper resistor value.

The iP1203PbF is capable of accepting an external digital synchronization signal. Synchronization will be enabled by the rising edge clock. The free running oscillator frequency is twice the switching frequency. During synchronization, R_T is selected such that the free running frequency is 20% below the synchronization frequency. The maximum synchronization frequency that iP1203PbF can accept is 800kHz. Note that the actual switching frequency is half the synchronization frequency.

Overcurrent Protection HICCUP

The overcurrent protection function of the iP1203PbF offers a hiccup feature. During overloads, when the overcurrent trip threshold is reached, the power supply output shuts down and attempts to restart (output HICCUP mode). The time duration between the shutdown of the output and the restart is determined by the time it takes to discharge the soft start capacitor. Typically, the discharge time of the soft start capacitor is 10 times the charge time. The duty cycle of the hiccup process is typically 5%. The output will stay in hiccup indefinitely until the overload is removed. The typical overcurrent trip threshold of the device is internally set at 30A. The overcurrent shutdown / HICCUP threshold is about ±30% accurate.

The iP1203PbF overcurrent shutdown and HICCUP threshold can be set externally by adding R_{OCSET} resistor from OCSET pin. Refer to Fig.8 for R_{OCSET} selection.

Overvoltage Protection (OVP)

Overvoltage is sensed through output voltage sense pin FB_s. The OVP threshold is set to 115% of the output voltage. Upon overvoltage condition, the OVP forces a latched shutdown. In this mode, the upper FET turns off and the lower FET turns on, thus crowbaring the output. Reset is performed by recycling the input voltage. Overvoltage can be sensed by either connecting FB_s to its corresponding output through a separate output voltage divider resistor network, or it can be connected directly to its corresponding feedback pin FB. For Type III control loop compensation, FB_s should be connected through voltage dividers only.

Refer to the iP1203PbF Design Procedure section on how to set the OVP trip threshold.

PGOOD

This is an output voltage status signal that is open collector and is pulled low when the output voltage falls below 85% of the output voltage. High state indicates that outputs are in regulation. The PGOOD pin can be left floating if not used.

Thermal Shutdown

The iP1203PbF provides thermal shutdown. The threshold typically is set to 140°C. When the trip threshold is exceeded, thermal shutdown turns the output off. Thermal shutdown is not latched and automatic restart is initiated when the sensed temperature drops to the normal range.

iP1203PbF Design Procedure

Only a few external components are required to complete a dual output synchronous buck power supply using iP1203PbF. The following procedure will guide the designer through the design and selection process of these external components.

A typical application for the iP1203 is:
V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 15A, f_{sw} = 300kHz, V_{p-p} = = 50mV

Setting the Output Voltage

The output voltage of the iP1203PbF is set by the 0.8V reference V_{REF} and external voltage dividers.

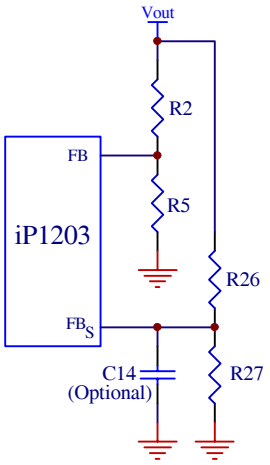


Fig. 14: Typical Scheme for Output Voltage Setting

For Type II compensation,

V_{OUT} is set according to equation (1):

$V_{OUT} = V_{REF} \times (1 + R_2/R_5)$ (see Fig. 14) (1)

Setting R_2 to 1K, V_{OUT} to 1.5V and V_{REF} to 0.8V, will result in R_5= 1.14 Kohms. Final values can be selected according to the desired accuracy of the output.

To set the output voltage for Type III compensation, refer to equation (24) in Type III compensation section.

Setting the Overvoltage Trip

The output of the iP1203 will shut down if it experiences a voltage in the range of 115% of V_{OUT}. The overvoltage sense pin FB_S is connected to the output through voltage dividers, R26 and R27 (Fig. 14), and the trip setpoint is programmed according to equation (1). A separate overvoltage sense pin FB_S is provided to protect the power supply output if for some reason the main feedback loop is lost (for instance, loss of feedback resistors). An optional 100pF capacitor (C14) is used for delay and filtering.

If this redundancy is not required and if a Type II control loop compensation scheme is utilized, FB_S pin can be connected to FB.

Selecting the Soft-Start Capacitor

The soft start capacitor C_{ss} is selected according to equation (2):

$t_{ss} = 40 \times C_{ss}$ (2)

where,
t_{ss} is the output voltage ramp time in milliseconds, and C_{ss} is the soft start capacitor in μF.

A 0.1μF capacitor will provide an output voltage ramp-up time of about 4ms.

Input Capacitor Selection

The switching currents impose RMS current requirements on the input capacitors. Equation (3) allows the selection of the input capacitors.

$$I_{RMS} = I_{out}\sqrt{D(1-D)} \quad (3)$$

where, I_{out} is the output current, and D is the duty cycle and is expressed as:

$D = V_{OUT} / V_{IN}$.

For the above example D= 0.13 and, using equation (3) the capacitor rms current yields 5.0A.

For better efficiency and low input ripple, select low ESR ceramic capacitors. The amount of the capacitors is determined based on the rms rating. In the above example, a total of 3 x 22µF, 2A capacitors will be required to support the input rms current.

Output Capacitor C_o Selection

Selection of the output capacitors depends on two factors:
a. Low effective ESR for ripple and load transient requirements

To support the load transients and to stay within a specified voltage dip ΔV due to the transients, ESR selection should satisfy equation (4):

$$R_{ESR} \leq \Delta V / I_{Loadmax} \quad (4)$$

Where,
$I_{Loadmax}$ is the maximum load current.

If output voltage ripple is required to be maintained at specified levels then the expression in equation (5) should be used to select the output capacitors.

$$R_{ESR} \leq V_{p\text{-}p} / I_{ripple} \quad (5)$$

Where,
$V_{p\text{-}p}$ is the peak to peak output ripple voltage .
I_{ripple} is the inductor peak-to peak ripple current.

In addition, the voltage ripple caused by the output capacitor needs to be significantly smaller than the ripple caused by the ESR of the capacitor. Use equation (6) to satisfy this requirement.

$$C_o > \frac{10}{2\pi \times f_s \times R_{ESR}} \quad (6)$$

If the inductor current ripple I_{ripple} is 30% of $I_{OUT1,}$ the 50mV peak to peak output voltage ripple requirement will be met if the total ESR of the output capacitors is less than 11mΩ. This will require 2 x 470µF POSCAP capacitors. Additional ceramic capacitors can be added in parallel to further reduce the ESR. Care should be given to properly compensate the control loop for low output capacitor ESR values.

When selecting output capacitors, it is important to consider the overshoot performance of the power supply. If the amount of capacitance is not adequate, then, when unloading the output, the magnitude of the overshoot due to stored inductor energy, and depending on the speed of the response of the control loop, can exceed the overvoltage trip threshold of the iP1203PbF and can cause undesirable shutdown of the output. The magnitude of the overshoot should be kept below $1.125V_{OUT}$. To prevent the overshoot from tripping the output a delay can be added by installing capacitor C14 as shown in Fig.14.

b. Stability

The value of the output capacitor ESR zero frequency f_{esr} plays a major role in determining stability. f_{esr} is calculated by the expression in equation (7).

$$f_{ESR} = 1 / (2 \pi \times R_{ESR} \times C_O) \quad (7)$$

Details on how to consider this parameter to design for stability are outlined in the control loop compensation section of this datasheet.

Inductor L_o Selection

Inductor selection is based on trade-offs between size and efficiency. Low inductor values result in smaller sizes, but can cause large ripple currents and lower efficiency. Low inductor values also benefit the transient performance.

The inductor $L_o$is selected according to equation (8):

$$L_O = V_{out} \times (1 - D) / (f_{sw} \times I_{ripple}) \quad (8)$$

For the above example, and for I_{ripple} of 30% of I_{OUT}, L_O is calculated to be 1.0µH.
The core must be selected according to the peak of maximum output current.

Control Loop Compensation

The iP1203PbF feedback control is based on single loop voltage mode control principle.

The goal in the design of the compensator is to achieve the highest unity gain (0 db) crossover frequency with sufficient phase margin for the closed loop transfer function. The LC filter of the power supply introduces a double pole with –40db/dec slope and 180° phase lag. The 180° phase contribution from the LC filter is the source of instabilty.
The resonant frequency of the LC filter is expressed by equation (9):

$$f_{LC} = 1/(2\pi\sqrt{L_0 \times C_0}) \qquad (9)$$

The error amplifier of the iP1203PbF PWM controller is transconductance amplifier, and its output is available for external compensation.

Two types of compensators are studied in this section. The first one is called Type II and it is used to compensate systems the ESR frequency f_{esr} (equation 7) of which is in the midfrequency range and Type III that can be used for any type of output capacitors and have a wide range of f_{esr}.

For output voltage settings less than 1.0V that use low ESR ceramic capacitors, it is recommended that the unity gain crossover frequency be set around 20kHz to maintain stable operation.

Type II

From Fig.15 the transfer function H(s) of the error amplifier is given by (10):

$$H(s) = g_m \times \frac{R_5}{R_5 + R_2} \times \frac{1 + sR_{19}C_9}{sR_{19}C_9} \qquad (10)$$

The term *s* represents the frequency dependence of the transfer function.

The Type II controller introduces a gain and a zero expressed by equations (11) and (12):

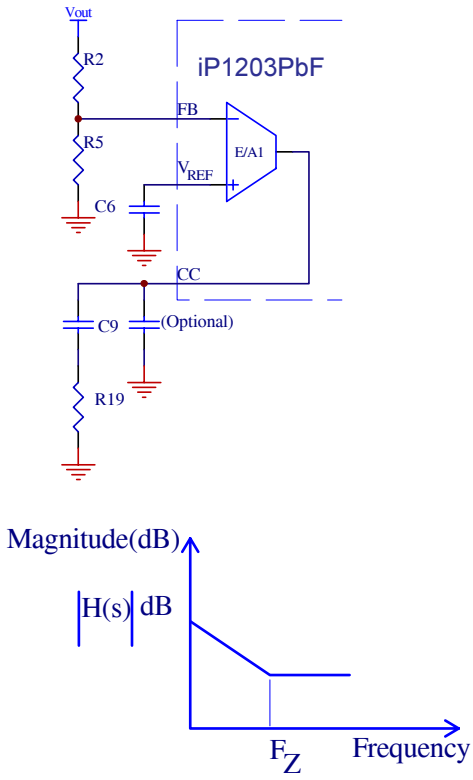


Fig. 15: Typical Type II Compensation and its Gain Plot

$$|H(s)| = g_m \times \frac{R_5}{R_5 + R_2} \times R_{19} \qquad (11)$$

where, g_m is the transconductance of the error amplifier.

$$f_z = \frac{1}{2\pi \times R_{19} \times C_9} \qquad (12)$$

Follow the steps below to determine the feedback loop compensation component values:

1. Select a zero db crossover frequency f_0 in the range of 10% to 20% of the switching frequency f_{sw}.

2. Calculate R_5 using equation (13):

$$R_{19} = V_{ramp} \times \frac{1}{V_{in}} \times \frac{f_0 \times f_{esr}}{f_{LC}^2} \times \frac{R_5 + R_2}{R_5} \times \frac{1}{g_m} \quad (13)$$

Where,
V_{IN} = Maximum input voltage
f_0 = Error amplifier zero crossover frequency
f_{esr} = Output capacitor C_o zero frequency
f_{LC} = Output frequency resonant filter
g_m = Error amplifier transconductance. Use 2mS for g_m.
V_{ramp} = Oscillator ramp voltage.
Use 1.25V for V_{ramp}

3. Place a zero at 75% of f_{LC} to cancel one of the LC filter poles.

$$f_z = 0.75 \times \frac{1}{2\pi\sqrt{L_o \times C_o}} \quad (14)$$

4. Calculate C_9 using equations (12) and (14)

Calculation of the compensation components based on the example above, yields:

f_{LC} = 5.0kHz
f_z = 3.8kHz
f_0 = 45kHz (15% of 300kHz)
f_{esr} = 14kHz, per equation (7) using R_{esr} = 12mΩ.
R_{19} = 2.49K
C_9 = 18nF

Sometimes, a pole f_{p2} is added at half the switching frequency to filter the switching noise. This is done by adding a capacitor C_{opt} in Fig.15 from the output of the error amplifier (CC pin of iP1203PbF) to ground. This pole is given by equation (15):

$$f_{p2} = \frac{1}{2\pi \times R_{19} \times C_{opt}} \quad (15)$$

C_{opt} is found from equation (16) by rearranging the terms in equation (15) and by setting $f_{p2} = f_{sw}/2$:

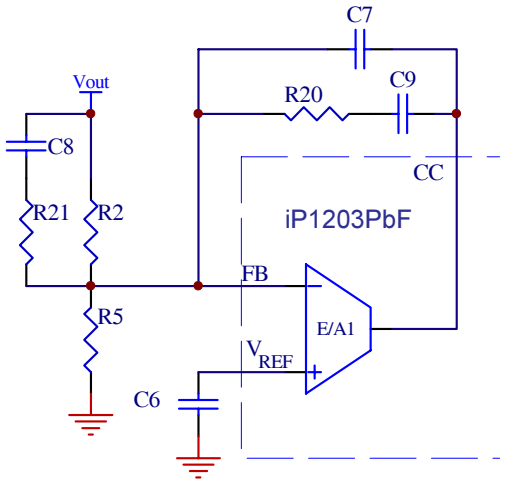
$$C_{opt} = \frac{1}{2\pi \times f_{p2} \times R_{19}} \quad (16)$$

Type III

The Type III compensation scheme allows the use of any type of capacitors with ESR frequency of any range. This scheme suggests a double pole double zero compensation and requires more components around the error amplifier to achieve the desired gain and phase margins. Fig. 13 represents the Type III compensation network for iP1203PbF.

The transfer function of the Type III compensator is given by equation (17)

$$H(s) = \frac{1}{sR_2C_9} \times \frac{(1 + sR_{20}C_9) \times (1 + sR_2C_8)}{(1 + sR_{20}C_7) \times (1 + sR_{21}C_8)} \quad (17)$$



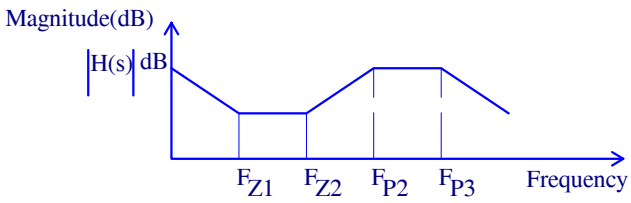


Fig. 16: Typical Type III Compensation and its Gain Plot

The frequencies of the three poles and the two zeros of the Type III compensation scheme are represented by the following equations:

$$f_{p1} = 0 \quad (18)$$

$$f_{p2} = \frac{1}{2\pi \times R_{21} \times C_8} \quad (19)$$

$$f_{p3} = \frac{1}{2\pi \times R_{20} \times C_7} \quad (20)$$

$$f_{z1} = \frac{1}{2\pi \times R_{20} \times C_9} \quad (21)$$

$$f_{z2} = \frac{1}{2\pi \times R_2 \times C_8} \quad (22)$$

The crossover frequency f_0 for Type III compensation is represented by equation (23):

$$f_0 = \frac{1}{V_{ramp}} \times V_{IN} \times R_{20} \times C_8 \times \frac{1}{2\pi \times L_0 \times C_0} \quad (23)$$

Follow the steps below to determine the feedback loop compensation component values:

1. Select a zero db crossover frequency f_0 in the range of 10% to 20% of the switching frequency $f_{sw.}$

2. Select $R_{20} \simeq 10k\Omega$

3. Place the first zero f_{z1} at 75% of the resonant frequency f_{LC} of the output filter.
Determine C_9 from equation (21).

4. Place a third pole f_{P3} at or near the switching frequency f_{SW}.

Select C7 such that $C_7 < \frac{C_9}{10}$

5. Calculate C_8 from equation (23).

6. Place the second zero at 125% of the resonant frequency f_{LC} of the output filter. Calculate R_2 using equation (22).

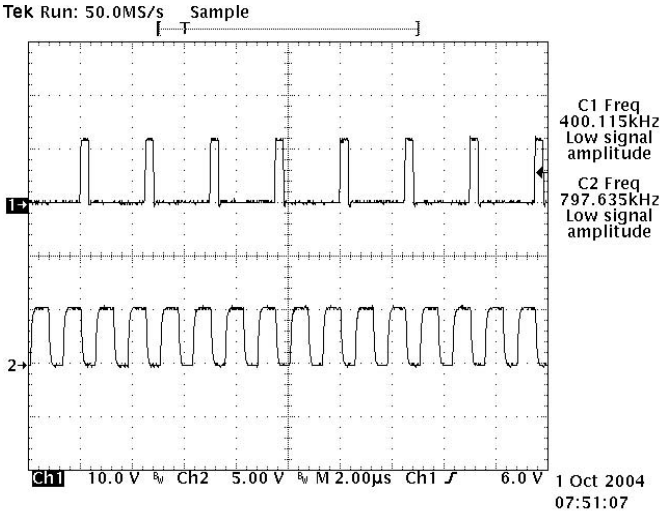
7. Place the second pole f_{p2} at or near f_{esr} of the output capacitor C_o and determine the value of R_{21} from equation (19). Make sure $R_{21} < \frac{R_2}{10}$

8. Use equation (24) to calculate R_5.

$$R_5 = R_2 \times \frac{V_{ref}}{V_o - V_{ref}} \quad (24)$$

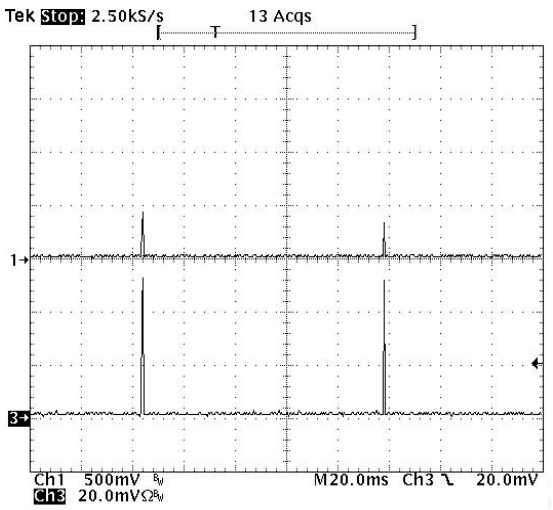
More than one iteration may be required to calculate the values of the compensation components if crossover frequencies higher than the range specified in step 1 are required (for higher bandwidths and faster transient response performance). To ensure stability a phase margin greater than 45° should be achieved. Refer to AN-1043 for more detailed compensation techniques using Transconductance Amplifiers.

Typical Waveforms



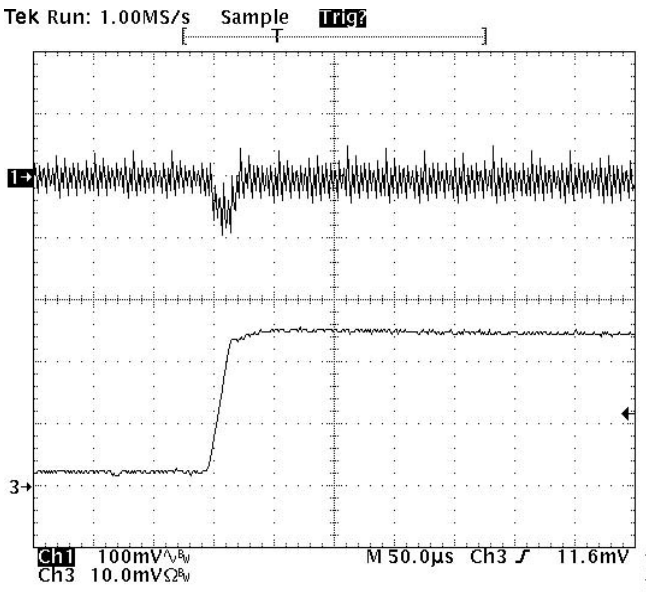
Ch1: Switching node, 400kHz
Ch2: 800kHz external synchronization

Fig. 17: iP1203PbF Outputs Synchronized to 800kHz



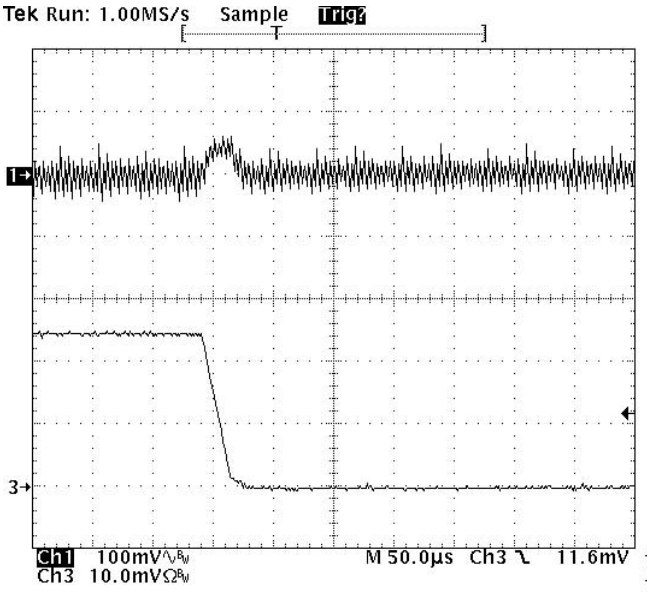
Ch1: Output voltage, 500mV/div
Ch3: Output current, 10A/div

Fig. 18: iP1203PbF Output Hiccup, Due to Overload



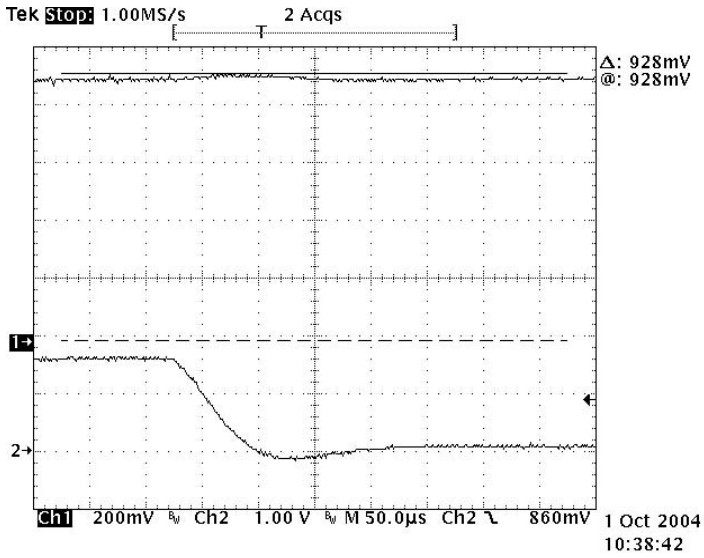
Ch1: Output voltage, 100mV/div ac
Ch3: Load current, 5A/div

Fig. 19: iP1203PbF Transient Response Load Step 1A to 12A



Ch1: Output voltage, 100mV/div ac
Ch3: Load current, 5A/div

Fig. 20: iP1203PbF Transient Response Load Step 12A to 0A



Ch1: FB_s input, 200mV/div
Ch2: Output voltage, 1V/div

Fig. 21: iP1203PbF Overvoltage Trip. Output Voltage Turns Off When Voltage at FB_s Pin Exceeds 15% of FB (0.8V)

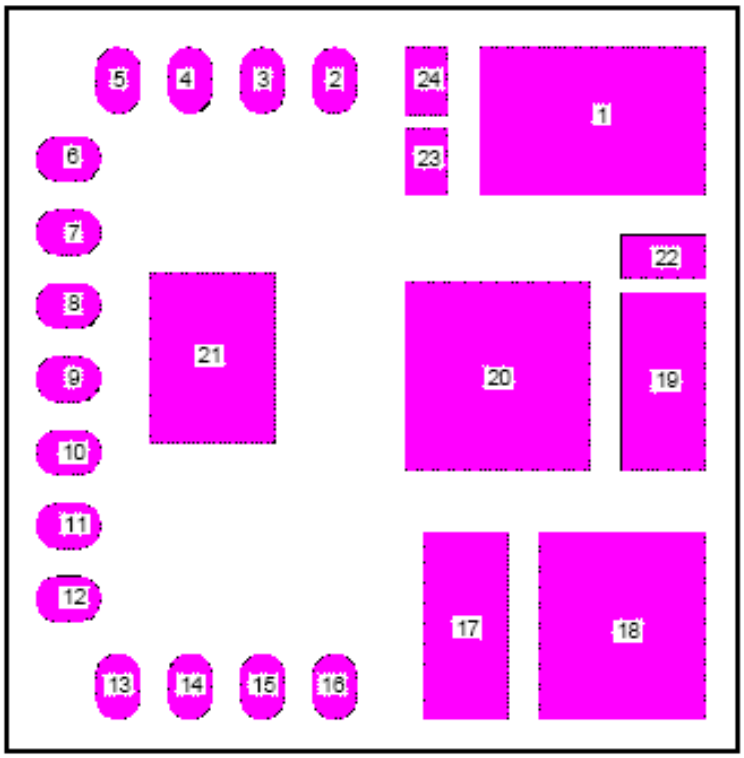


Fig. 22: iP1203PbF Pin Assignment

Layout Guidelines

For stable and noise free operation of the whole power system, it is recommended that the designers use the following guidelines:

1. Follow the layout scheme presented in Fig. 23. Make sure that the output inductor L is placed as close to iP1203PbF as possible to prevent noise propagation that can be caused by switching of power at the switching node Vsw, to sensitive circuits.

2. Provide a mid-layer solid ground plane with connections to the top layer through vias. The PGND pads of iP1203PbF also need to be connected to the same ground plane through vias.

3. To increase power supply noise immunity, place input and output capacitors close to one another, as shown in the layout diagram. This will provide short high current paths that are essential at the ground terminals.

4. Although there is a certain degree of V_{IN} bypassing inside the iP1203PbF, the external input decoupling capacitors should be as close to the device as possible.

5. The feedback track from the output V_{OUT} to FB should be routed as far away from noise generating traces as possible.

6. The compensation components and the Vref bypass capacitor should be placed as close as possible to their corresponding iP1203PbF pins, away from noise generating traces.

7. Refer to IR application note AN-1029 (Optimizing a PCB Layout for an iPOWIR Technology Design) to determine what size vias and copper weight and thickness to use when designing the PCB.

8. Place the overcurrent threshold setting resistors R_{OCSET} close to the iP1203PbF block at the corresponding connection node.

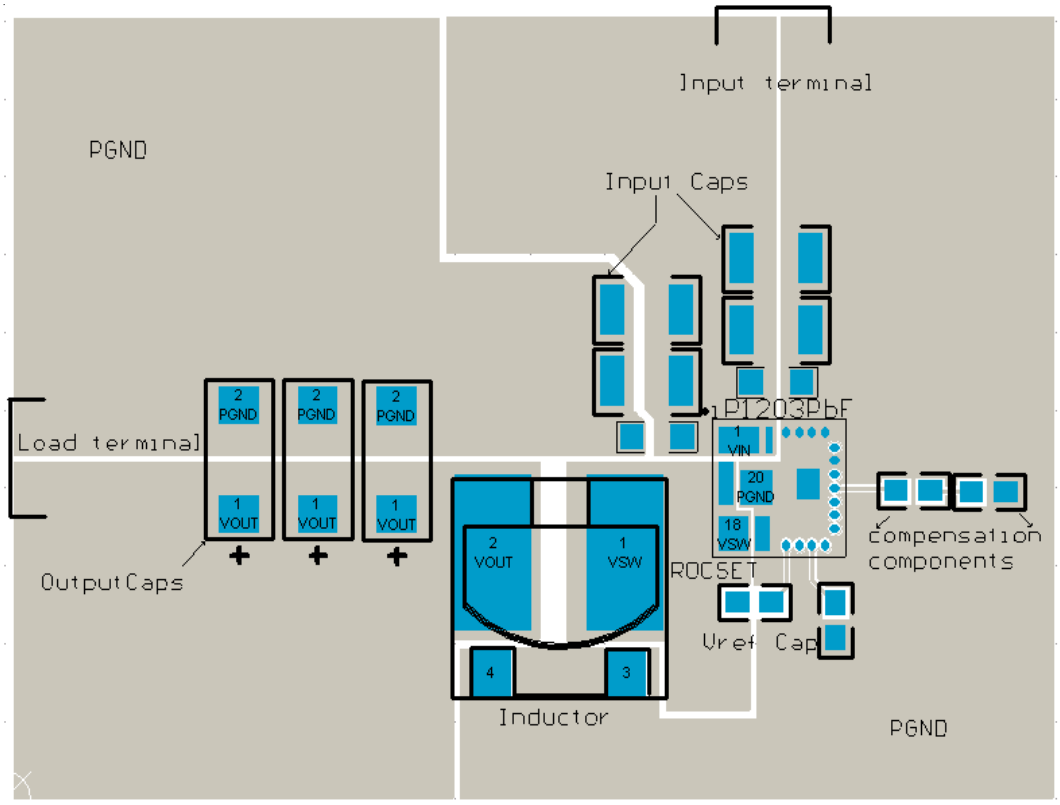


Fig. 23: iP1203PbF Suggested Layout

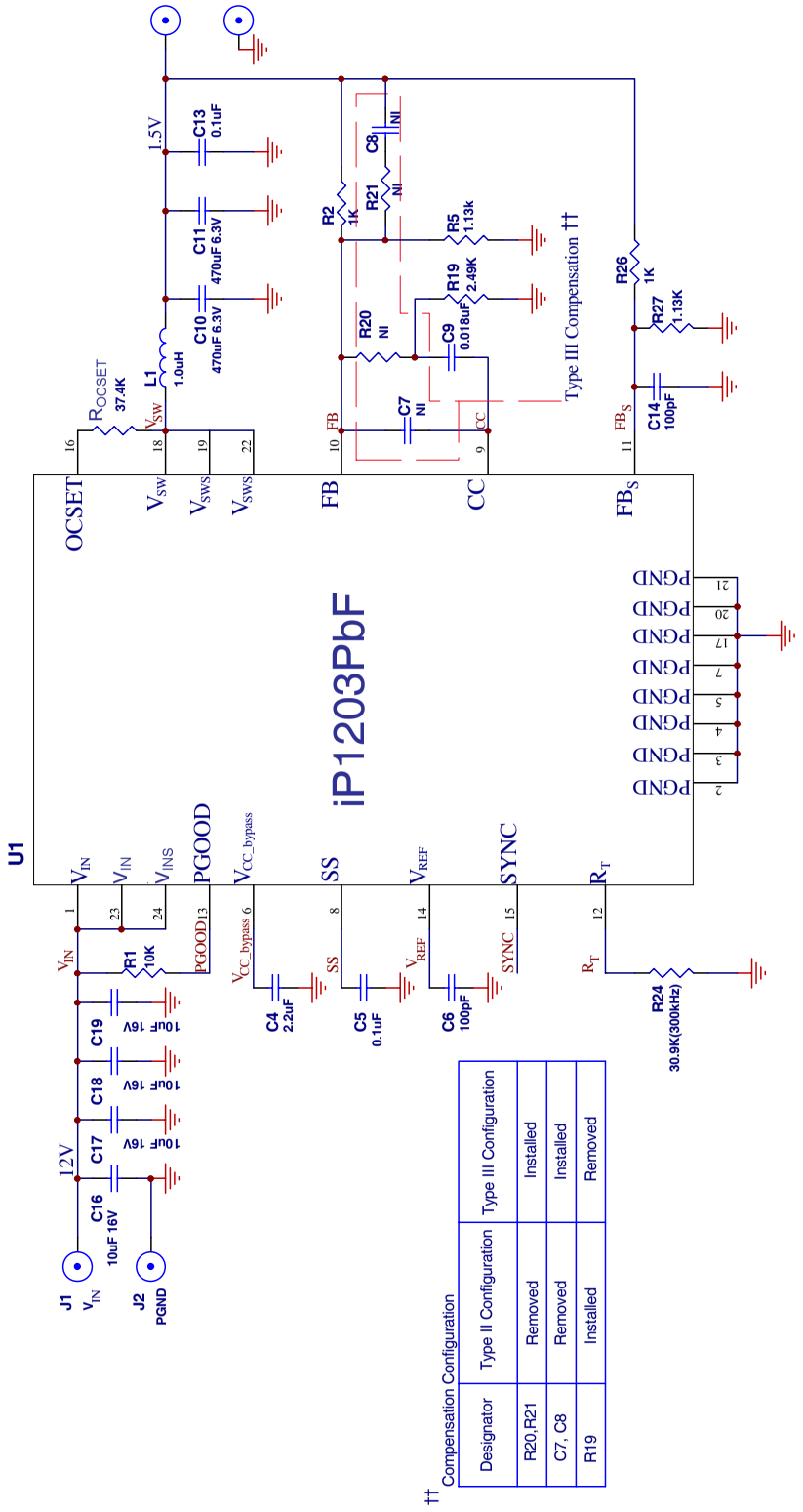
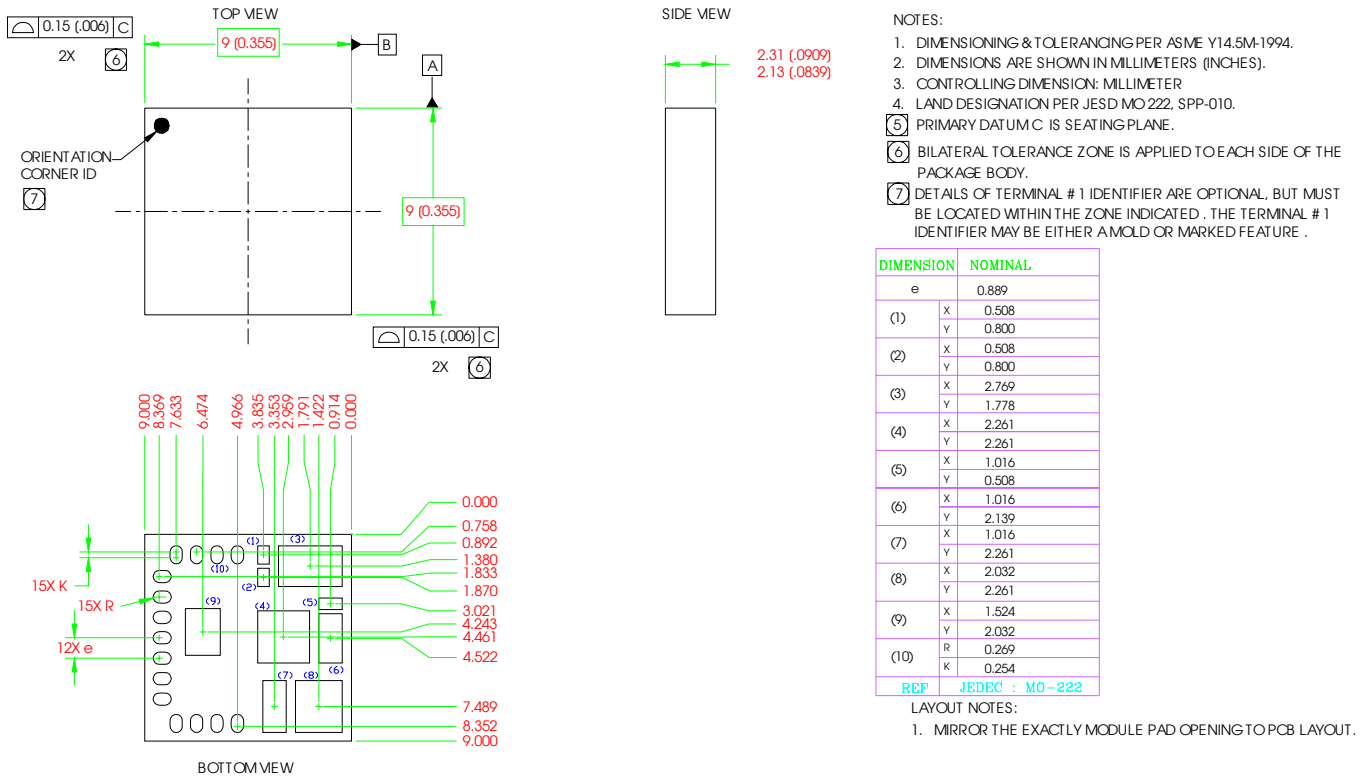


Fig. 24: Typical Application Schematic



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. CONTROLLING DIMENSION: MILLIMETER
4. LAND DESIGNATION PER JESD MO 222, SPP-010.
5. PRIMARY DATUM C IS SEATING PLANE.
6. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
7. DETAILS OF TERMINAL # 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED . THE TERMINAL # 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE .

DIMENSION		NOMINAL
e		0.889
(1)	X	0.508
	Y	0.800
(2)	X	0.508
	Y	0.800
(3)	X	2.769
	Y	1.778
(4)	X	2.261
	Y	2.261
(5)	X	1.016
	Y	0.508
(6)	X	1.016
	Y	2.139
(7)	X	1.016
	Y	2.261
(8)	X	2.032
	Y	2.261
(9)	X	1.524
	Y	2.032
(10)	R	0.269
	K	0.254
REF		JEDEC : MO-222

LAYOUT NOTES:
1. MIRROR THE EXACTLY MODULE PAD OPENING TO PCB LAYOUT.

Fig. 25: Outline Drawing

Refer to the following application notes for detailed guidelines and suggestions when implementing iPOWIR technology products:

AN-1029: Optimizing a PCB Layout for an iPOWIR Technology Design
This paper describes how to optimize the PCB layout design for both thermal and electrical performance. This includes placement, routing, and via interconnect suggestions.

AN-1030: Applying iPOWIR Products in Your Thermal Environment
This paper explains how to use the Power Loss vs Current and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

AN-1043: Stabilize the Buck Converter with Transconductance Amplifier
This paper explains how to stabilize a buck converter for Type II and Type III control loop compensation using transconductance amplifiers.

AN-1047: Graphical solution to two branch heatsinking Safe Operating Area
This paper is a suppliment to AN-1030 and explains how to use the double side Power Loss vs Current and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPOWIR Technology BGA and LGA Packages
This paper discusses optimization of the layout design for mounting iPOWIR BGA and LGA packages on printed circuit boards, accounting for thermal and electrical performance and assembly considerations. Topics discussed includes PCB layout placement, routing, and via interconnect suggestions, as well as soldering, pick and place, reflow, cleaning and reworking recommendations.

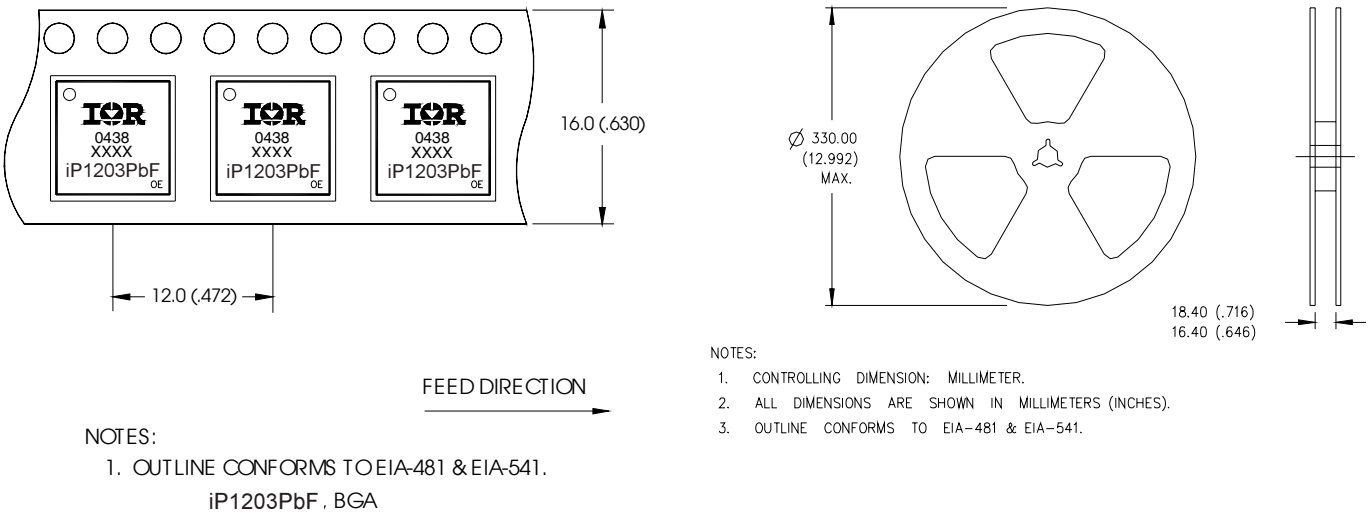


Fig. 26: Tape & Reel Information

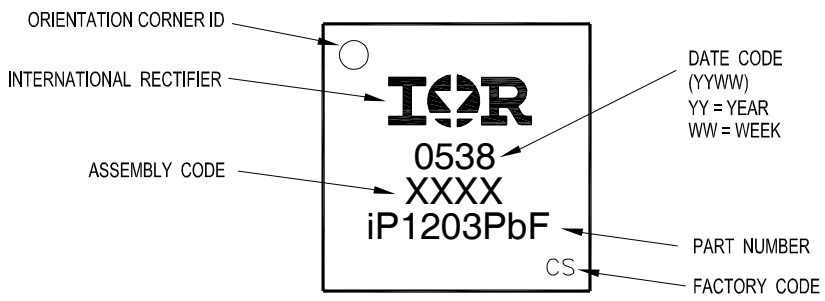
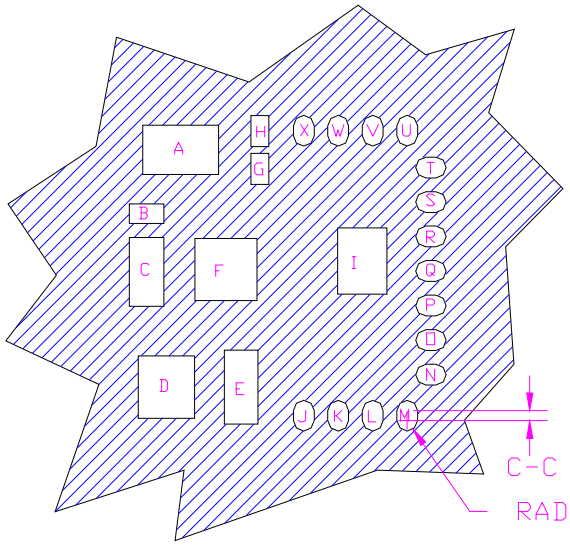


Fig. 27: Part Marking



	SPACE	X	Y
	A	.077	.050
	B	.035	.020
	C	.035	.070
	D	.057	.063
	E	.034	.075
	F	.063	.063
	G	.050	.067
	H	.018	.031
	I	.018	.031
	J~X	0.010(C-C)	0.0105 RAD

SQUEEGEE VIEW
RECOMMENDED STENCIL OPENING
ALL DIMENSIONS IN INCHES

The recommended reflow peak temperature is 260°C. The total furnance time is approximately 5 minutes with approximately 10 seconds at the peak temperature.

Fig.28: Recommended Solder Profile and Stencil Design

This product has been designed and qualified for the industrial market.

International
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