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*i*POWIR™ TECHNOLOGY

SYNCHRONOUS BUCK LGA POWER BLOCK

Features

- 40A Multiphase building block
- No derating up to $T_C = T_{PCB} = 95^oC$
- Optimized for low power loss
- Bias supply range of 4.5V to 6.0V
- Operation up to 1.5MHz
- Over temperature protection
- Bi-directional Current flow
- Under Voltage Lockout
- LGA interface
- 7.7mm x 7.7mm x 2.2mm package

Applications

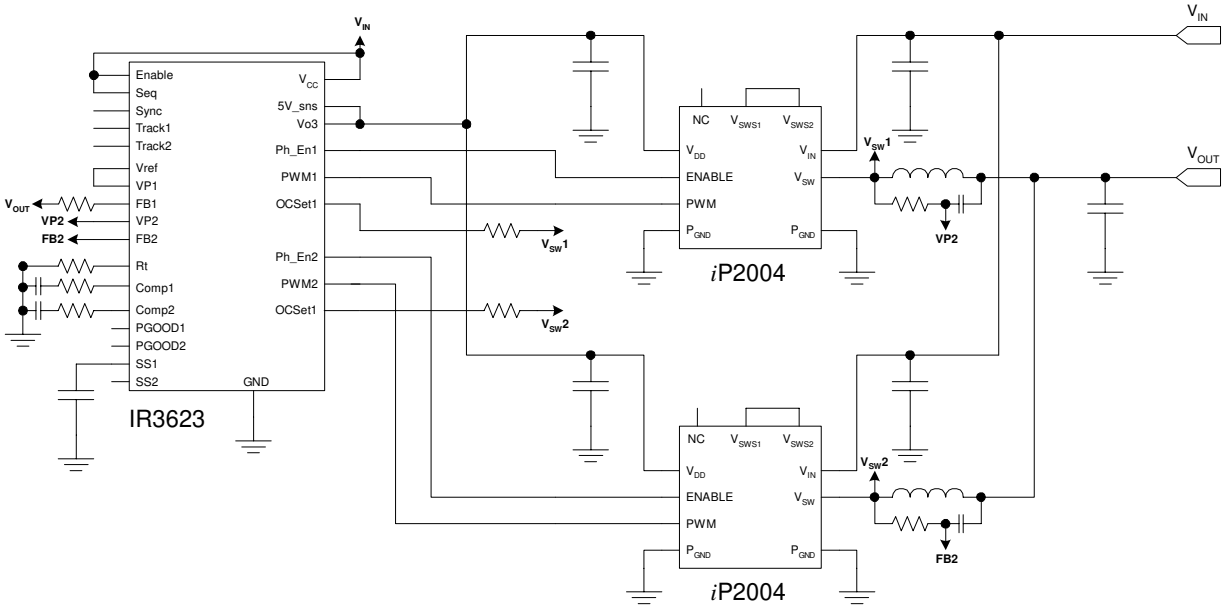
- High frequency, Multi-phase Converters
- Low Duty-Ratio, High Current Microprocessor Power Supplies
- High Frequency Low Profile DC-DC Converters

Description

The iP2004 is a fully optimized solution for high current synchronous buck multiphase applications. Board space and design time are greatly reduced because most of the components required for each phase of a typical discrete-based multiphase circuit are integrated into a single 7.7mm x 7.7mm x 2.2mm power block. The only additional components required for a complete multiphase converter are a PWM controller, the output inductors, and the input and output capacitors.

Package Description	Interface Connection	Standard Quantity	T & R Orientation
iP2004	LGA	10	N/A
iP2004TR	LGA	2000	Figure 18

Typical Application



Absolute Maximum Ratings

V_{IN} to PGND ..... -0.5V to 16V
V_{DD} to PGND ..... -0.5V to 6.5V
PWM to PGND ..... -0.5V to V_{DD} + 0.5V (Note 1)
ENABLE to PGND ..... -0.5V to V_{DD} + 0.5V (Note 1)
Storage Temperature ..... -60ºC to 150ºC
Block Temperature ..... -40ºC to 150ºC (Note 5)
ESD Rating..... HBM Class 1B (500V)
MM Class B (200V)
MSL Rating..... 3

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those listed in the "Recommended Operating Conditions" section of this specification is not implied.

Recommended Operating Conditions

PARAMETER	Min	Typ	Max	Units	Conditions
Supply Voltage (V_{DD})	4.5	-	6.0	V	
Input Voltage (V_{IN})	3.3	-	13.2	V	
Output Voltage (V_{OUT})	-	-	8.0	V	
Output Current (I_{OUT})	-	-	40	A	
Switching Frequency (F_{SW})	250	-	1500	kHz	
On Time Duty Cycle	-	-	85	%	
Minimum V_{SW} On Time	60	-	-	ns	V_{DD} = 5.0V, V_{IN} = 12V
Block Temperature	-40	-	125	ºC	

Electrical Specifications

These specifications apply for T_{BLK} = 0ºC to 125ºC and V_{DD} = 5.0V, unless otherwise specified.

PARAMETER	Min	Typ	Max	Units	Conditions
Ploss					
Power Block Losses	-	7.4	9.1	W	V_{IN} = 12V, V_{DD} = 5.0V, V_{OUT} = 1.3V, I_{OUT} = 40A, F_{SW} = 1MHz, L_{OUT} = 0.3uH, T_A = 25ºC (Note 3)
V_{IN}					
Quiescent Current	-	-	1.0	mA	V_{IN} = 12V, ENABLE = 0V

PARAMETER	Min	Typ	Max	Units	Conditions
VDD					
Supply Current (Stand By)	-	1.1	2.0	mA	V_{DD} = 5.0V, ENABLE = 0V
Supply Current (Operating)	-	70	110	mA	V_{IN} = 12V, V_{DD}= EN ABLE = 5.0V, F_{SW} = 1MHz, 10% DC,
Power-On Reset (POR)					
VCC Rising	3.7	-	4.5	V	
Hysterisis	140	185	230	mV	V_I Rising & Falling
ENABLE INPUT					
Logic Level Low Threshold (V_{IL})	-	-	0.8	V	Schmitt Trigger Input VCC = POR to 6.0V
Logic Level High Threshold (V_{IH})	2.0	-	-	V	
Threshold Hysterisis	-	100	-	mV	
Weak pull-down current	-	10	-	µA	
Rising Propagation Delay (T_{PDH})	-	40	-	ns	
Falling Propagation Delay (T_{PDL})	-	75	-	ns	
PWM INPUT					
Logic Level Low Threshold (V_{IL})	-	-	0.8	V	Schmitt Trigger Input VCC = POR to 6.0V (Note 4)
Logic Level High Threshold (V_{IH})	2.0	-	-	V	
Threshold Hysterisis	-	100	-	mV	
Weak pull-down current	-	2	-	µA	
Rising Propagation Delay (T_{PDH})	-	50	-	ns	
Falling Propagation Delay (T_{PDL})	-	35	-	ns	

Notes:

1. Must not exceed 6.5V.
2. Guaranteed by design, not tested in production.
3. Measurement made with six 10µF (TDK C3225X5R1C106KT or equivalent) ceramic capacitors across V_{IN} to P_{GND} pins (see Figure 9).
4. TPDH and TPDL are not associated with rise and fall times. Does not affect Power Loss (see Figure 10).
5. Block Temperature is defined as any Die temperature within the package.

Power Loss Curve

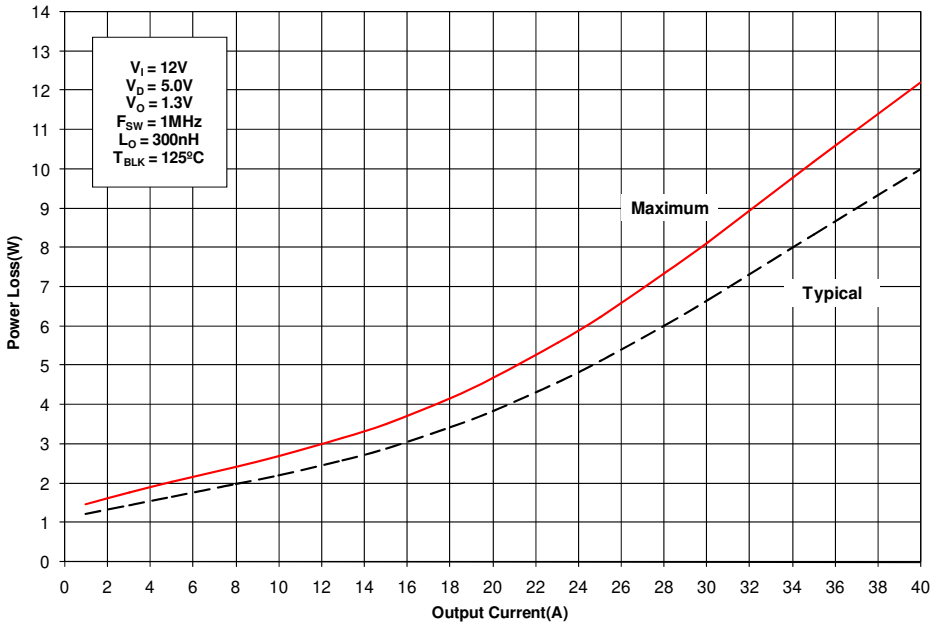


Figure 1Power Loss versus Output Current

SOA Curve

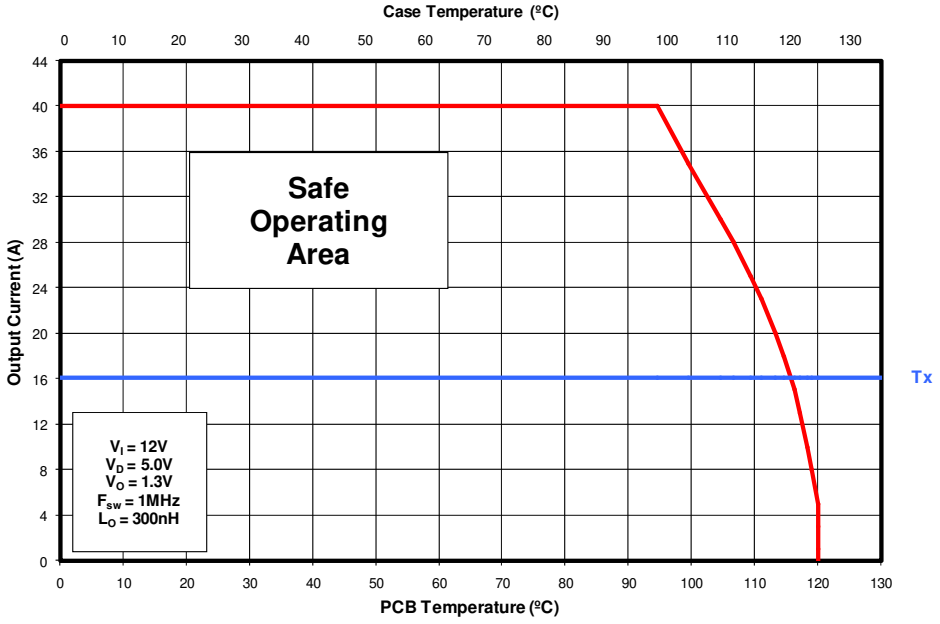


Figure 2 Safe Operating Area (SOA) versus PCB and CASE temperatures (See page 6 for details)

Typical Performance Curves

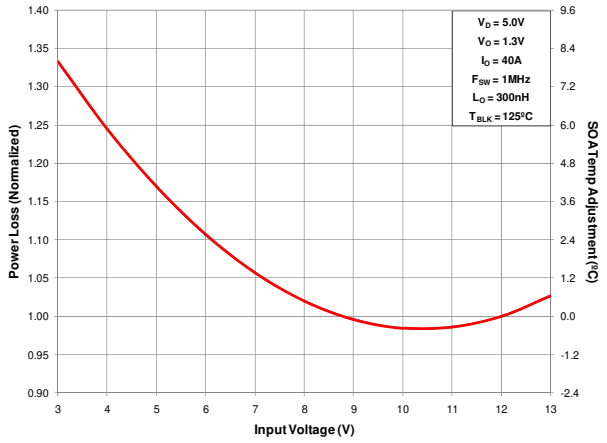


Figure 3 Normalized Power Loss vs. Input Voltage

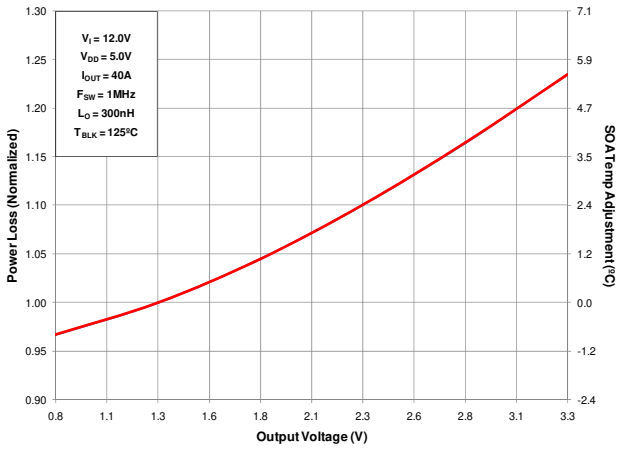


Figure 4 Normalized Power Loss vs. Output Voltage

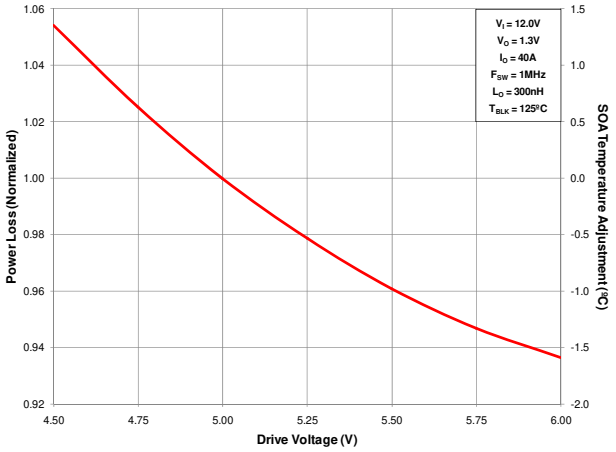


Figure 5 Normalized Power Loss versus Drive Voltage

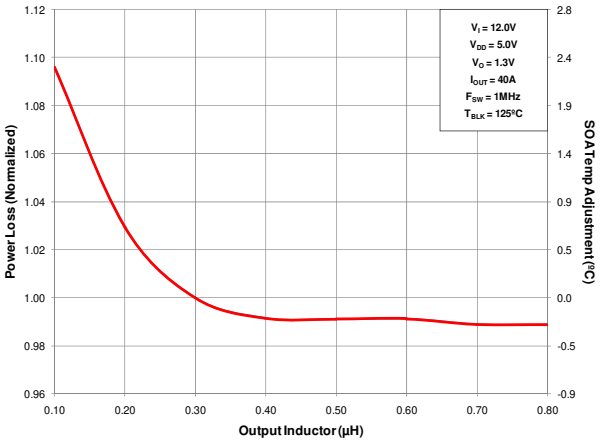


Figure 6 Normalized Power Loss vs. Inductance

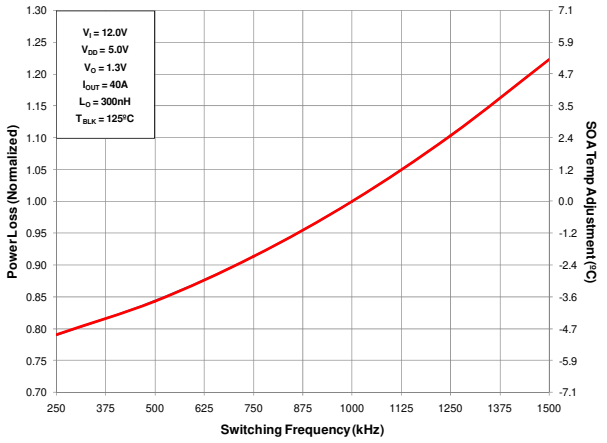


Figure 7 Normalized Power Loss vs. Switching Frequency

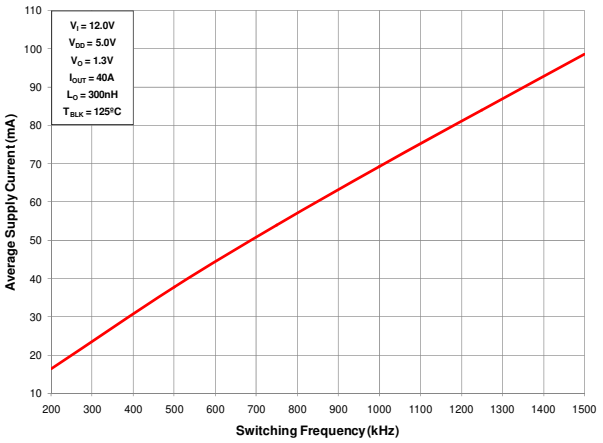


Figure 8 V_{DD} supply current vs. Frequency

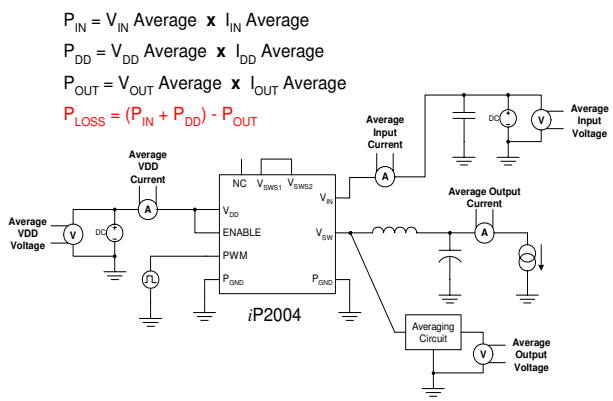


Figure 9 Power Loss Test Circuit

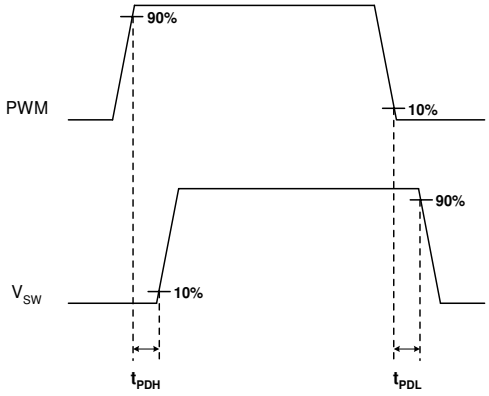


Figure 10 Timing Diagram

Applying the Safe Operating Area (SOA) Curve

The SOA graph incorporates power loss and thermal resistance information in a way that allows one to solve for maximum current capability in a simplified graphical manner. It incorporates the ability to solve thermal problems where heat is drawn out through the printed circuit board and the top of the case. Please refer to International Rectifier Application Note AN1047 for further details on using this SOA curve in your thermal environment.

Procedure

1. Calculate (based on estimated Power Loss) or measure the Case temperature on the device and the Board temperature near the device (1mm from the edge).
2. Draw a line from Case Temperature axis to the PCB Temperature axis.
3. Draw a vertical line from the T_X axis intercept to the SOA curve.
4. Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the SOA continuous current.

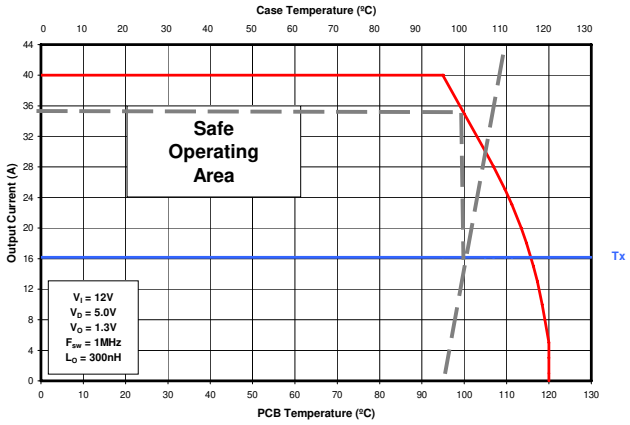


Figure 11 SOA Example, Continuous current ≈ 30A for T_{PCB} = 95°C & T_{CASE} = 110°C

Calculating Power Loss and SOA for Different Operating Conditions

To calculate Power Loss for a given set of operation conditions, the following procedure should be followed:

Power Loss Procedure

1. Determine the maximum current for each iP2004 and obtain the maximum power loss from Figure 1
2. Use the Normalized curves in page 5 to obtain power loss values that match the operating conditions in the Application
3. The maximum power loss under the Application conditions is then the product of the power loss from Figure 1 and the normalized values.

To calculate the Safe Operating Area (SOA) for a given set of operating conditions, the following procedure should be followed:

SOA Procedure

1. Determine the maximum PCB and CASE temperature at the maximum operating current for each iP2004
2. Use the Normalized curves in page 5 to obtain SOA temperature adjustments that match the operating conditions in the Application
3. Then, add the sum of the SOA temperature adjustments to the T_X axis intercept in Figure 2

Design Example

Operating Conditions:

Output Current = 30A	Input Voltage = 10V	Output Voltage = 3.3V
Switching Freq = 750kHz	Inductor = 0.2µH	Drive Voltage (V_{DD}) = 5.5V

Calculating Maximum Power Loss:

(Figure 1) Maximum power loss = 8.0W
(Figure 3) Normalized power loss for input voltage ≈ 0.98
(Figure 4) Normalized power loss for output voltage ≈ 1.23
(Figure 5) Normalized power loss for drive voltage (V_{DD}) ≈ 0.96
(Figure 6) Normalized power loss for output inductor ≈ 1.03
(Figure 7) Normalized power loss for switch frequency ≈ 0.91

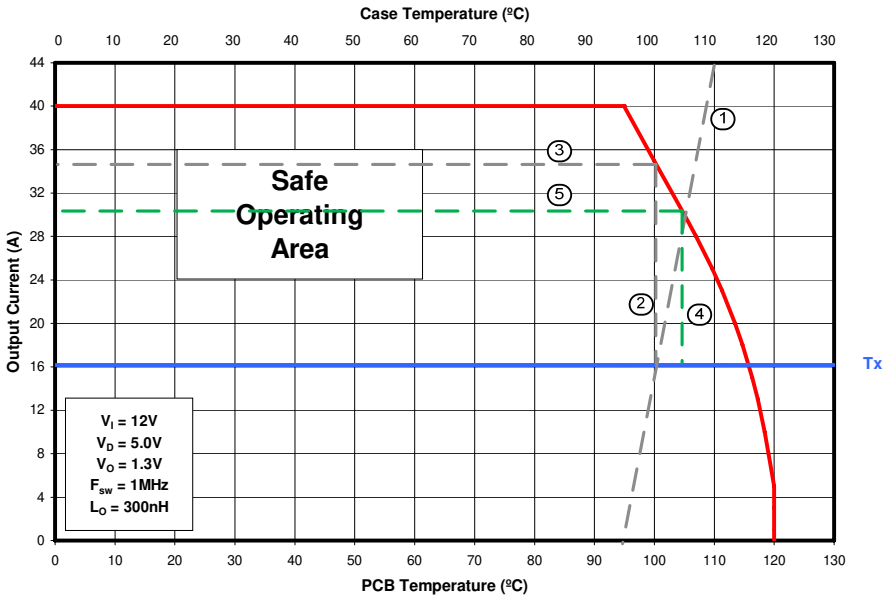
Calculated Maximum Power Loss ≈ 8.0W x 0.98 x 1.23 x 0.96 x 1.03 x 0.91 ≈ 8.68W

Calculating SOA Temperature:

(Figure 3) SOA temperature adjustment for input voltage ≈ -0.5ºC
(Figure 4) SOA temperature adjustment for output voltage ≈ 5.5ºC
(Figure 5) SOA temperature adjustment for drive voltage (V_{DD}) ≈ -0.8 ºC
(Figure 6) SOA temperature adjustment for output inductor ≈ 0.6 ºC
(Figure 7) SOA temperature adjustment for switch frequency ≈ -1.9 ºC

TX axis intercept adjustment ≈ -0.5 ºC + 5.5 ºC - 0.8 ºC + 0.6 ºC - 1.9 ºC ≈ 2.9 ºC

Assuming T_{PCB} = 95ºC & T_{CASE} = 110ºC
The following example shows how the SOA current is adjusted for T_X increase of 2.9ºC



1. Draw a line from Case Temperature axis to the PCB Temperature axis.
2. Draw a vertical line from the T_X axis intercept to the SOA curve.
3. Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the SOA continuous current.
4. Draw a new vertical line from the T_X axis by adding or subtracting the SOA adjustment temperature from the original T_X intercept point.
5. Draw a horizontal line from the intersection of the new vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the new SOA continuous current.

The SOA adjustment indicates the part is still allowed to run at a continuous current of 30A.

Internal Block Diagram

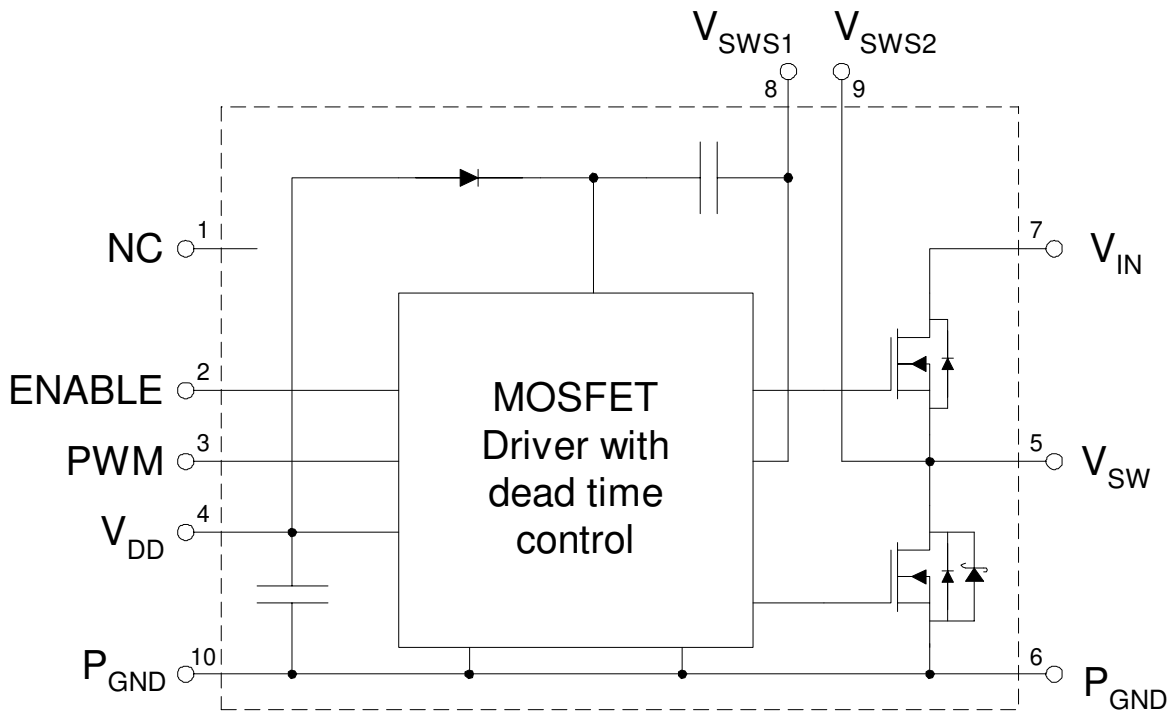


Figure 12 Internal Block Diagram

Pin Description

Pin Number	Pin Name	Description
1	NC	No Connect. This pin is not for electrical connection
2	ENABLE	When set to logic level high, internal circuitry of the device is enabled. When set to logic level low, the Control and Synchronous FETs are turned off.
3	PWM	TTL level input to MOSFET drivers. When PWM is HIGH, the Control FET is on and the Sync FET is off. When PWM is LOW, the Sync FET is on and the Control FET is off.
4	V_{DD}	Supply voltage to internal circuitry.
5	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
6, 10	PGND	Power Ground
7	V_{IN}	Input voltage pin. Connect input capacitors close to this pin.
8	V_{SWS1}	Floating pin. Externally connect to V_{SWS2} only.
9	V_{SWS2}	Floating pin. Externally short to V_{SWS1} only.

Package Pinout Diagram

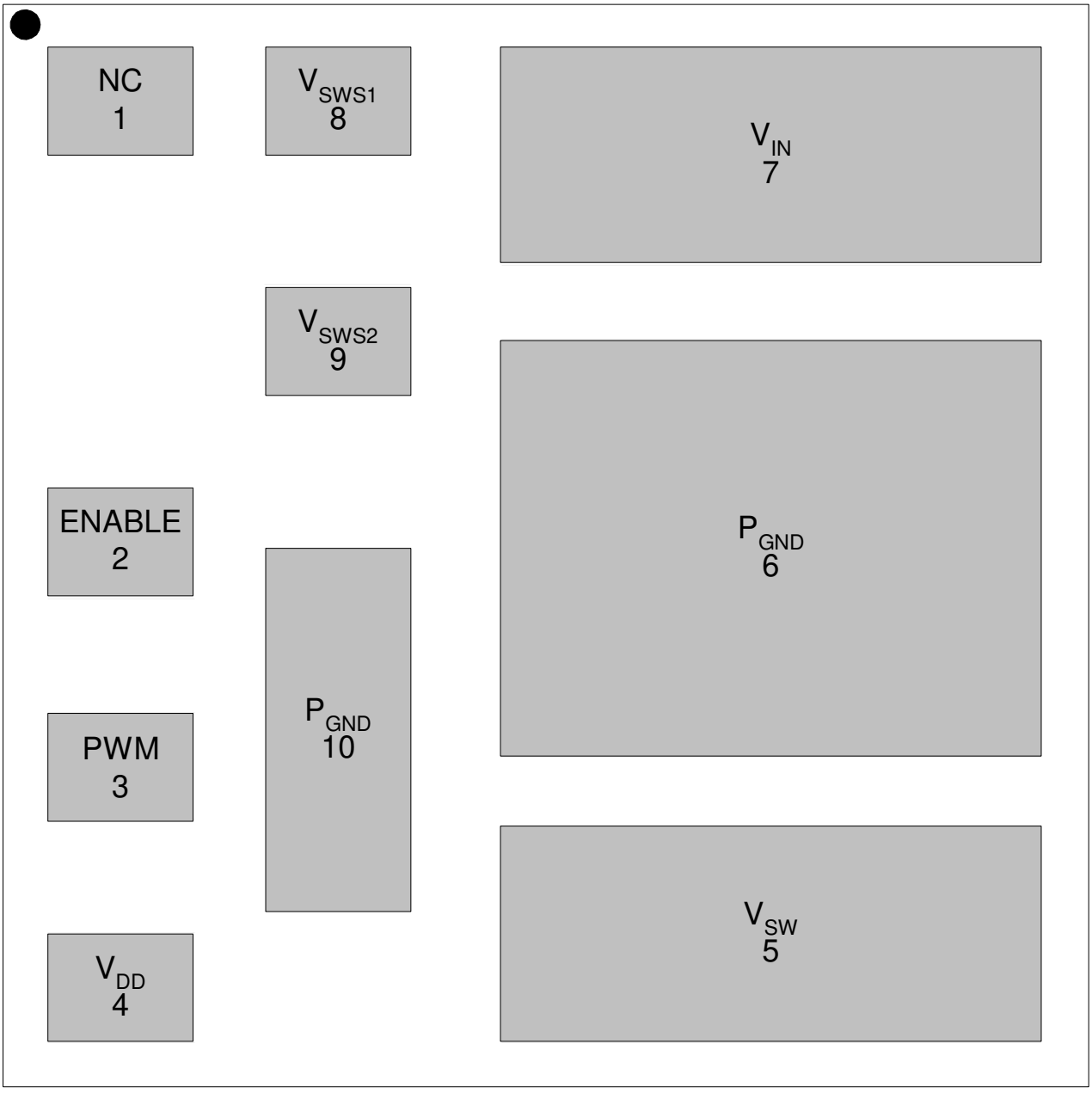


Figure 13 Top Side Transparent View

Recommended PCB Layout

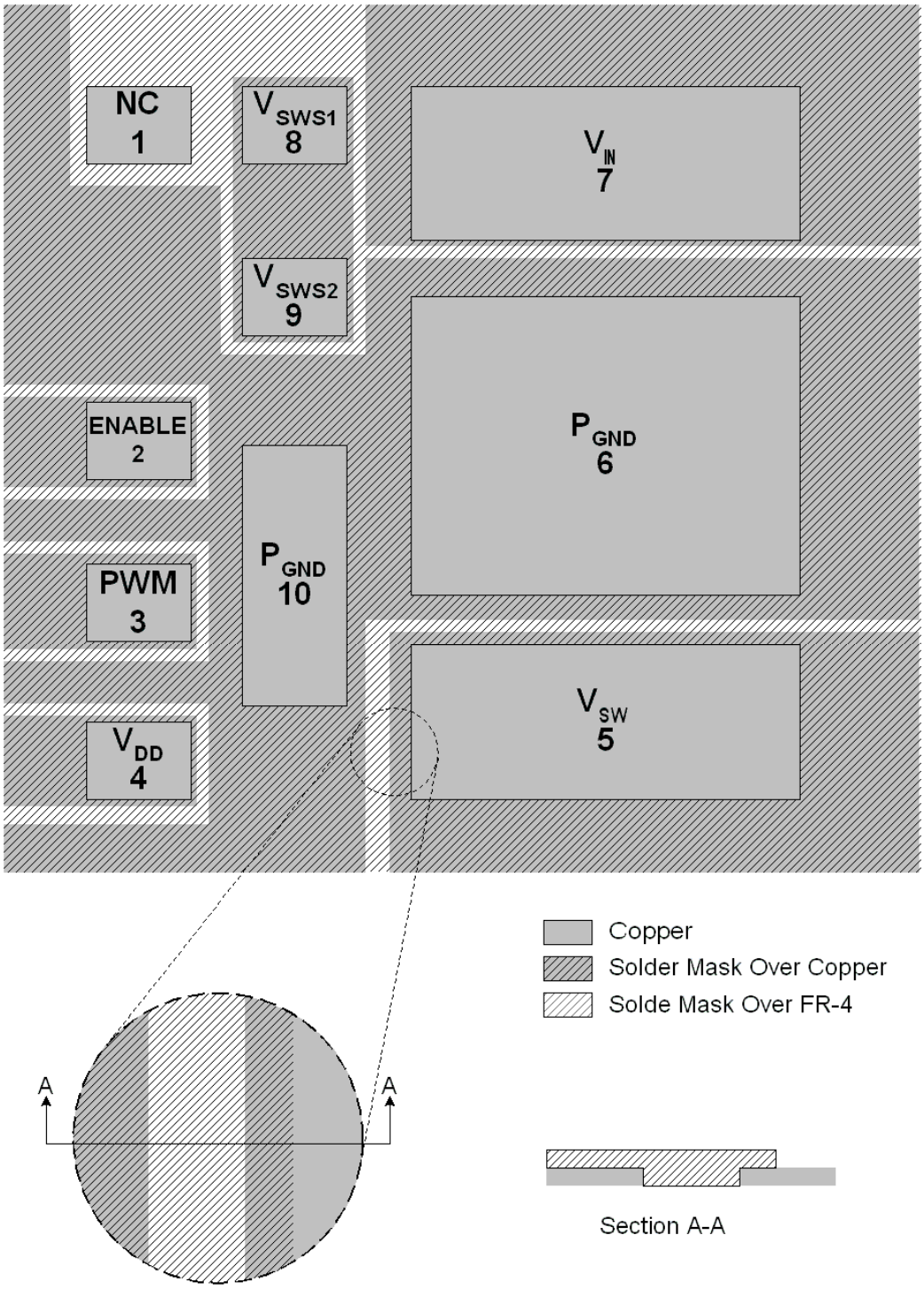


Figure 14 Top copper and Solder-mask layer of PCB layout

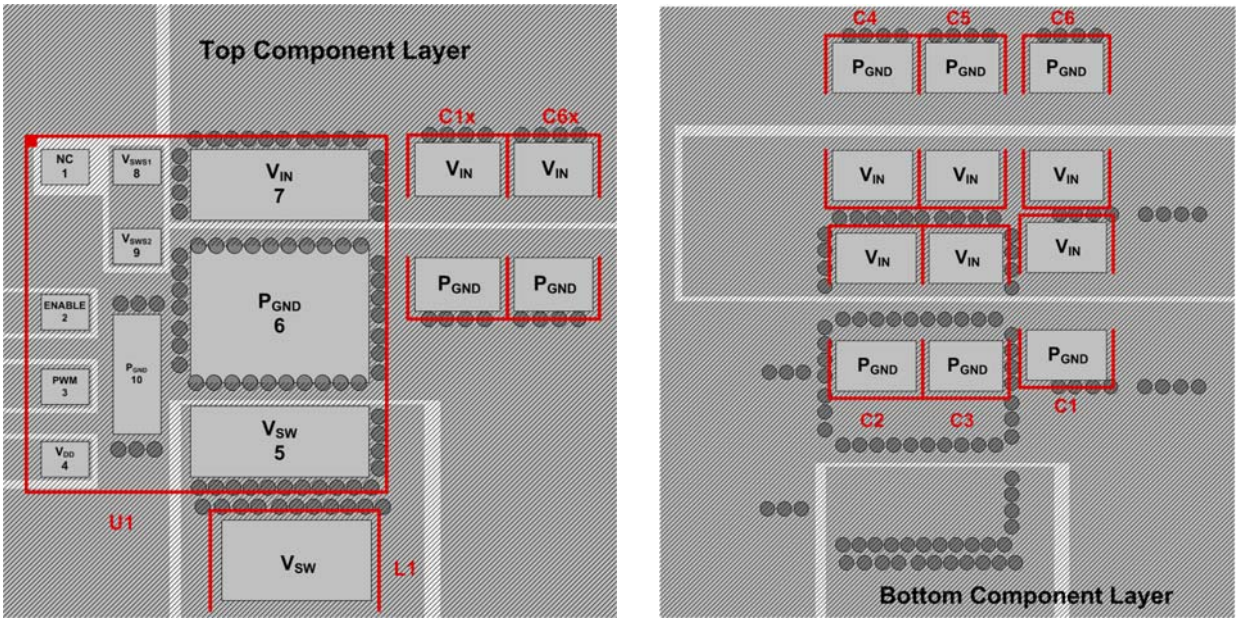


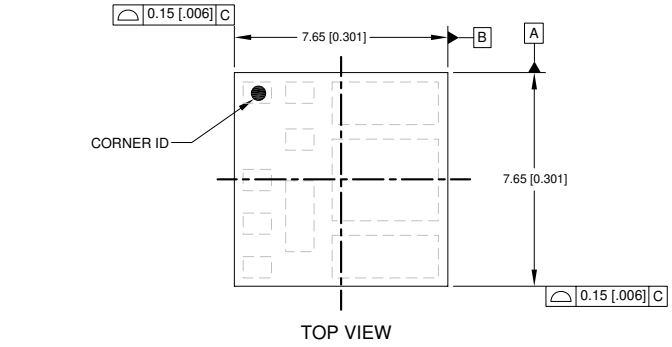
Figure 15 Top & Bottom Component and Via Placement (Topside, Transparent view down)

PCB Layout Guidelines

The following guidelines are recommended to reduce the parasitic values and optimize overall performance.

- All pads on the iP2004 footprint design need to be Solder-mask defined (see Figure 14). Also refer to International Rectifier application notes AN1028 and AN1029 for further footprint design guidance.
- Place as many vias around the Power pads (V_{IN}, V_{SW}, and P_{GND}) for both electrical and optimal thermal performance.
    - Vias in between the different power pads may overlap the pad opening and solder mask edge without the need to plug the via hole. Vias with a 13mil drill hole and 25mil capture pad were used in this example.
- A minimum of six 10µF, X5R, 16V ceramic capacitors per iP2004 are needed for greater than 25A operation. This will result in the lowest loss due to input capacitor ESR.
- Placement of the ceramic input capacitors is critical to optimize switching performance. In cases where there is a heatsink on the case of iP2004, place all six ceramic capacitors right underneath the iP2004 footprint (see Bottom Component Layer). In cases where there is not heatsink, C1 and C6 on the bottom layer may be moved to the C1x and C6x locations (respectively) on the top component layer (see Top Component Layer). In both cases, C2 – C5 need to be placed right underneath the iP2004 PCB footprint.
- Dedicate at least two layer to for PGND only
- Duplicate the Power Nodes on multiple layers (refer to AN1029).

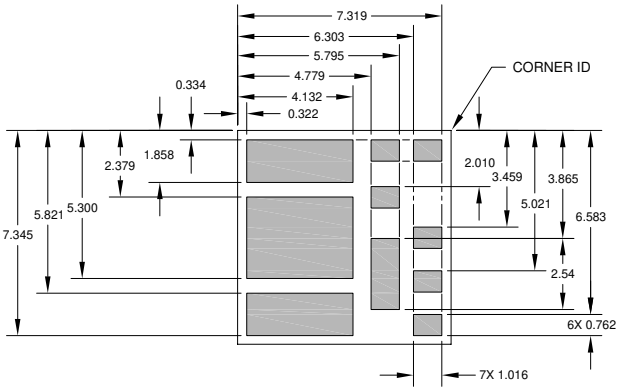
Mechanical Outline Drawing



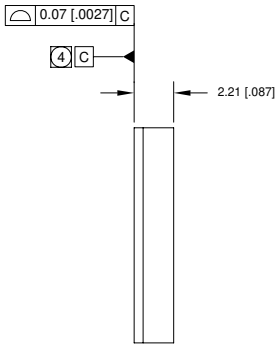
TOP VIEW

NOTES:

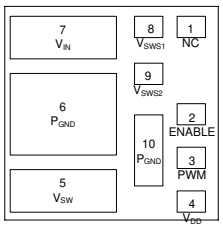
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: MILLIMETER
4. PRIMARY DATUM C (SEATING PLANE) IS DEFINED BY THE SOLDER RESIST OPENING
5. DRAWING NOT TO SCALE.



BOTTOM VIEW



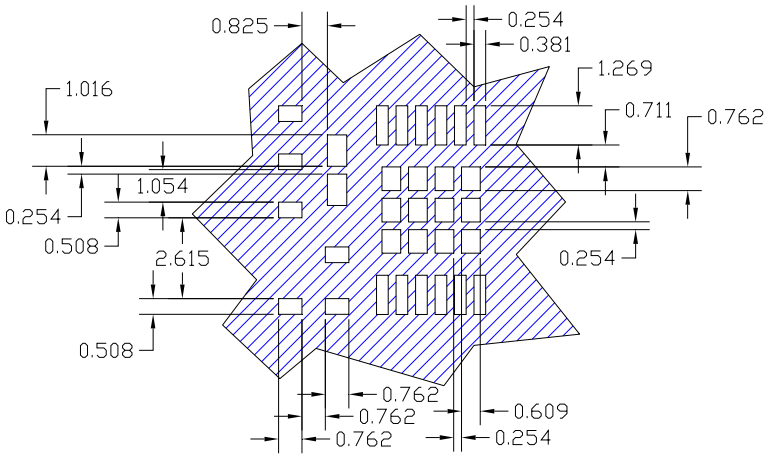
SIDE VIEW



BOTTOM VIEW
ELECTRICAL I/O

Figure 16 Mechanical Outline Drawing

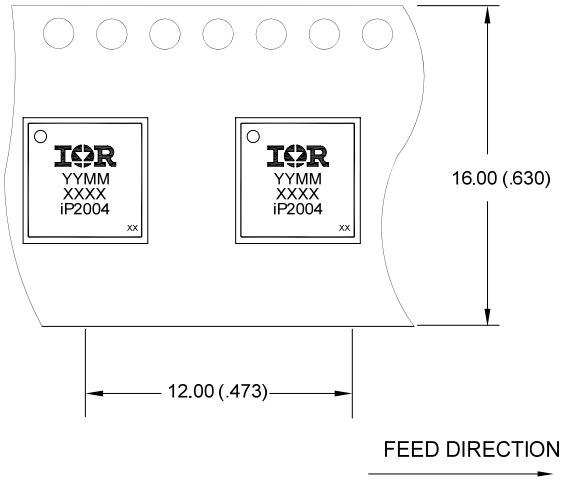
Recommended Solder Paste Stencil Design



NOTES:
1. This view is stencil squeegee view
2. Dimensions are shown in millimeters
3. These openings are based on using a 150 micron thick stencil. If using different thickness stencil, this opening needs to be adjusted accordingly.
4. The recommended reflow peak temperature should not exceed 240°C.
5. The total furnace time is approximately 5 minutes with approximately 10 seconds at the peak temperature.

Figure 17 Solder Paste Stencil Design

Tape and Reel Information



NOTES:
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
iP2004, LGA

Figure 18 Tape & Reel Information

Part Marking

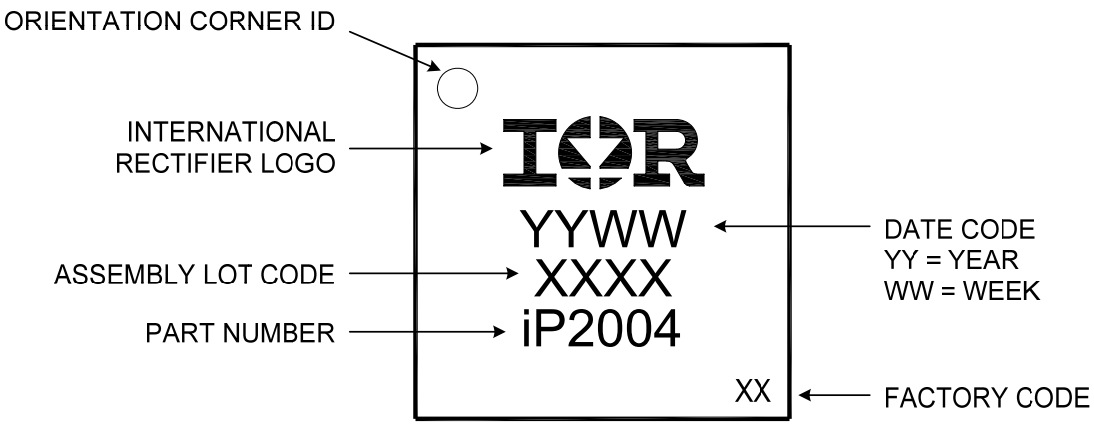


Figure 19 Part Marking

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