Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

IP4786CZ32S

DVI and HDMI interface ESD and overcurrent protection, DDC/CEC buffering, hot plug detect and backdrive protection

Rev. 3 — 7 January 2015 Product data sheet

1. General description

The IP4786CZ32S is designed to protect High-Definition Multimedia Interface (HDMI) transmitter host interfaces. It includes HDMI 5 V overcurrent / overvoltage protection, Display Data Channel (DDC) buffering and decoupling, Hot Plug Detect (HPD), backdrive protection, Consumer Electronic Control (CEC) buffering and decoupling, and ±12 kV contact ElectroStatic Discharge (ESD) protection for all external I/Os in accordance with the IEC 61000-4-2, level 4 standard.

The IP4786CZ32S incorporates Transmission Line Clamping (TLC) technology on the high-speed Transition-Minimized Differential Signaling (TMDS) lines to simplify routing and help reduce impedance discontinuities. All TMDS lines are protected by an impedance-matched diode configuration that minimizes impedance discontinuities caused by typical shunt diodes.

The enhanced 60 mA overcurrent / overvoltage linear regulator guarantees HDMI-compliant 5 V output voltage levels with up to 6.5 V inputs.

The DDC lines use a new buffering concept which decouples the internal capacitive load from the external capacitive load for use with standard Complementary Metal Oxide Semiconductor (CMOS) or Low Voltage Transistor-Transistor Logic (LVTTL) I/O cells down to 1.8 V. This buffering also redrives the DDC and CEC signals, allowing the use of longer or cheaper HDMI cables with a higher capacitance. The internal hot plug detect module simplifies the application of the HDMI transmitter to control the hot plug signal.

All lines provide appropriate integrated pull-ups and pull-downs for HDMI compliance and backdrive protection to guarantee that HDMI interface signals are not pulled down if the system is powered down or enters Standby mode. Only a single external capacitor is required for operation.

2. Features and benefits

- HDMI 2.0 and all backward compatible standards are supported
- 6.0 Gbps TMDS Bit Rate (600 Mcsc TMDS Character Rate) compatible
- Supports Ultra High-Definition (UHD) 4K (2160p) 60 Hz display modes
- Impedance matched 100 Ω differential transmission line ESD protection for TMDS lines (±10 Ω). No Printed-Circuit Board (PCB) pre-compensation required
- Simplified flow-through routing utilizing less overall PCB space
- DDC capacitive decoupling between system side and HDMI connector side and buffering to drive cable with high capacitive load (> 700 pF/25 m)
- All external I/O lines with ESD protection of at least ±12 kV, exceeding the IEC 61000-4-2, level 4 standard

- Hot plug detect module
- CEC buffering and isolation, with integrated backdrive-protected 26 kΩ pull-up
- Robust ESD protection without degradation after repeated ESD strikes
- Highest integration in a small footprint, PCB level, optimized RF routing, 32-pin HVQFN leadless package

3. Applications

- The IP4786CZ32S can be used for a wide range of HDMI source devices, consumer and computing electronics:
  - Tablet and notebook PCs
  - Portable Media Players
  - Digital Still Cameras (DSC)
  - High-Definition (HD) and Standard-Definition (SD) Blu-ray and DVD players
  - Set-top boxes (STB)
  - PC graphic cards
  - Game consoles
  - HDMI picture performance quality enhancer modules
  - Digital Visual Interface (DVI)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
IP4786CZ32S	HXQFN32	plastic thermal enhanced extremely thin quad flat package; no leads; 32 terminals; body 4 × 4 × 0.5 mm	SOT1318-1

5. Functional diagram

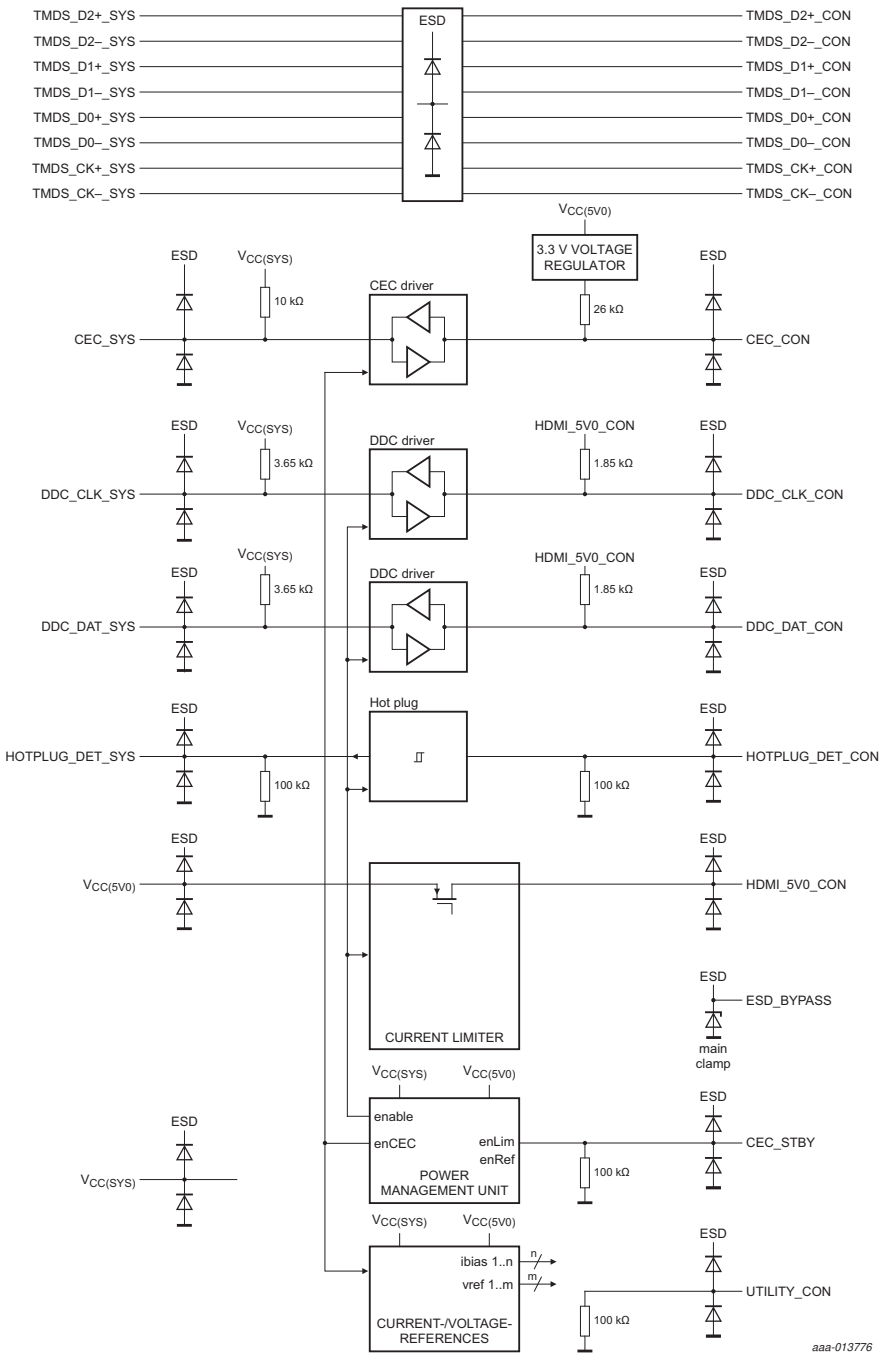


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning

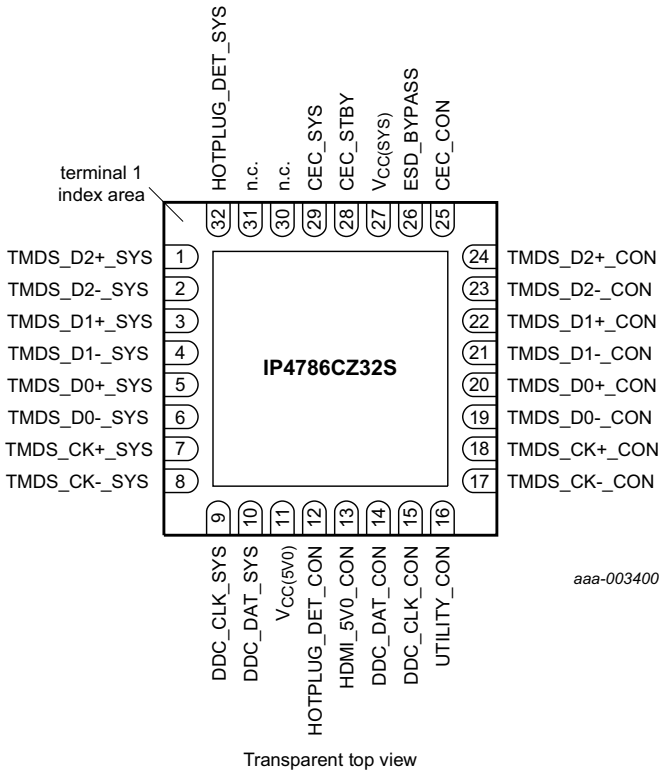


Fig 2. Pin configuration IP4786CZ32S

6.2 Pin description

Table 2. Pin description

Pin	Name	Description
1	TMDS_D2+_SYS	TMDS to ASIC inside system
2	TMDS_D2−_SYS	TMDS to ASIC inside system
3	TMDS_D1+_SYS	TMDS to ASIC inside system
4	TMDS_D1−_SYS	TMDS to ASIC inside system
5	TMDS_D0+_SYS	TMDS to ASIC inside system
6	TMDS_D0−_SYS	TMDS to ASIC inside system
7	TMDS_CK+_SYS	TMDS to ASIC inside system
8	TMDS_CK−_SYS	TMDS to ASIC inside system
9	DDC_CLK_SYS	DDC clock system side
10	DDC_DAT_SYS	DDC data system side
11	$V_{CC(5V0)}$	5 V supply input
12	HOTPLUG_DET_CON	hot plug detect connector side
13	HDMI_5V0_CON	5 V overcurrent out to connector

Table 2. Pin description *...continued*

Pin	Name	Description
14	DDC_DAT_CON	DDC data connector side
15	DDC_CLK_CON	DDC clock connector side
16	UTILITY_CON	utility line ESD protection
17	TMDS_CK−_CON	TMDS ESD protection to connector
18	TMDS_CK+_CON	TMDS ESD protection to connector
19	TMDS_D0−_CON	TMDS ESD protection to connector
20	TMDS_D0+_CON	TMDS ESD protection to connector
21	TMDS_D1−_CON	TMDS ESD protection to connector
22	TMDS_D1+_CON	TMDS ESD protection to connector
23	TMDS_D2−_CON	TMDS ESD protection to connector
24	TMDS_D2+_CON	TMDS ESD protection to connector
25	CEC_CON	CEC signal connector side
26	ESD_BYPASS	ESD bias voltage
27	$V_{CC(SYS)}$	supply voltage for level shifting
28	CEC_STBY	CEC Standby mode control (LOW for lowest power, CEC-only mode)
29	CEC_SYS	CEC I/O signal system side
30	n.c.	not connected
31	n.c.	not connected
32	HOTPLUG_DET_SYS	hot plug detect system side
ground pad	GND	ground

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		GND − 0.5	6.5	V
V_I	input voltage	I/O pins	GND − 0.5	5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4 (contact) [1]	-	±12	kV
		IEC 61000-4-2, level 1 (contact) [2]	-	±2	kV
P_{tot}	total power dissipation	DDC operating at 100 kHz; CEC operating at 1 kHz; 50 % duty cycle; CEC_STBY = HIGH; no current at HDMI_5V0_CON	-	50	mW
		DDC and CEC bus in idle mode; CEC_STBY = HIGH; no current at HDMI_5V0_CON	-	3.0	mW
		DDC and CEC bus in idle mode; CEC_STBY = LOW	-	1.0	mW
T_{amb}	ambient temperature		−25	+85	°C
T_{stg}	storage temperature		−55	+125	°C

[1] Connector-side pins (typically denoted with "_CON" suffix) to ground.

[2] System-side pins: CEC_SYS, DDC_DAT_SYS, DDC_CLK_SYS, HOTPLUG_DET_SYS, CEC_STBY, $V_{CC(SYS)}$ and $V_{CC(5V0)}$.

8. Static characteristics

Table 4. Supplies

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)	[1]	4.5	5.0	6.5	V
$V_{CC(SYS)}$	system supply voltage		1.62	3.3	5.5	V

[1] The IP4786CZ32S contains a 5 V voltage regulator function for higher input voltages. Any input voltage of 4.925 V < $V_{CC(5V0)}$ < 6.50 V provides HDMI-compliant output levels of 4.8 V to 5.3 V on HDMI_5V0_CON.

Table 5. TMDS protection circuit

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS channel						
$Z_{i(dif)}$	differential input impedance	TDR measured; t_r = 200 ps	90	100	110	Ω
C_{eff}	effective capacitance	equivalent shunt capacitance for TDR minimum; t_r = 200 ps [1][2]	-	0.6	-	pF
Protection diode						
V_{BRzd}	Zener diode breakdown voltage	I = 1.0 mA	6.0	-	9.0	V
r_{dyn}	dynamic resistance	surge; I = 1.0 A; IEC 61000-4-5/9				
		positive transient	-	1.0	-	Ω
		negative transient	-	1.0	-	Ω
		TLP [3]				
		positive transient	-	1.0	-	Ω
		negative transient	-	1.0	-	Ω
I_{bck}	back current	$V_{CC(5V0)}$ < $V_{ch(TMDS)}$ [4][5]	-	0.1	1.0	μA
I_{LR}	reverse leakage current	V_I = 3.0 V	-	1.0	-	μA
V_F	forward voltage		-	0.7	-	V
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8.0	-	V

[1] This parameter is guaranteed by design.

[2] Capacitive dip at HDMI Time Domain Reflectometer (TDR) measurement conditions.

[3] ANSI-ESD SP5.5.1-2004, ESD sensitivity testing Transmission Line Pulse (TLP) component level method 50 TDR.

[4] Signal pins:
TMDS_D0+_CON, TMDS_D0−_CON, TMDS_D1+_CON, TMDS_D1−_CON, TMDS_D2+_CON, TMDS_D2−_CON, TMDS_CK+_CON, TMDS_CK−_CON,
TMDS_D0+_SYS, TMDS_D0−_SYS, TMDS_D1+_SYS, TMDS_D1−_SYS, TMDS_D2+_SYS, TMDS_D2−_SYS, TMDS_CK+_SYS and TMDS_CK−_SYS.

[5] Backdrive current from TMDS_x_SYS and TMDS_x_CON pins to local $V_{CC(5V0)}$ bias rail at power-down. Device does not block backdrive current leakage through the device to/from ASIC I/O pins connected to TMDS_x_SYS pins.

Table 6. HDMI_5V0_CON

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
r_{dyn}	dynamic resistance	TLP [1]				
		positive transient	-	1.0	-	Ω
		negative transient	-	1.0	-	Ω
V_{CL}	clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8	-	V
$I_{O(max)}$	maximum output current	$V_{(HDMI\_5V0\_CON)}$ = 4.8 V	55	-	-	mA
I_{bck}	back current	$V_{CC(5V0)} < V_{(HDMI\_5V0\_CON)}$	-	-	10	μA
$I_{O(sc)}$	short-circuit output current	$V_{(HDMI\_5V0\_CON)}$ = 0 V	-	125	175	mA
V_{do}	dropout voltage	4.5 V < $V_{CC(5V0)}$ < 4.925 V; DDC = LOW [2]				
		I_O = 10 mA	-	70	-	mV
		I_O = 55 mA	-	-	125	mV
$V_{O(LDO)}$	LDO output voltage	$I_O \leq$ 55 mA; 4.925 V < $V_{CC(5V0)}$ < 6.5 V; DDC = LOW [2]	4.8	5.05	5.3	V

[1] ANSI-ESD SP5.5.1-2004, ESD sensitivity testing TLP component level method 50 TDR.

[2] The IP4786CZ32S contains a 5 V voltage regulator function for higher input voltages. Any input voltage of 4.925 V < $V_{CC(5V0)}$ < 6.50 V provides HDMI-compliant output levels of 4.8 V to 5.3 V on HDMI_5V0_CON.

Table 7. UTILITY_CON

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies: pins $V_{CC(5V0)}$ and $V_{CC(SYS)}$						
r_{dyn}	dynamic resistance	TLP [1]				
		positive transient	-	1.0	-	Ω
		negative transient	-	1.0	-	Ω
V_{CL}	clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8.0	-	V
C_i	input capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz	-	8.0	10	pF
R_{pd}	pull-down resistance		60	100	140	kΩ

[1] ANSI-ESD SP5.5.1-2004, ESD sensitivity testing TLP component level method 50 TDR.

Table 8. Static characteristics

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDC buffer on connector side[1]						
V_{IH}	HIGH-level input voltage		0.5 × $V_{(HDMI\_5V0\_CON)}$	-	6.5	V
V_{IL}	LOW-level input voltage		−0.5	-	0.3 × $V_{(HDMI\_5V0\_CON)}$	V
V_{OH}	HIGH-level output voltage	[2]	$V_{(HDMI\_5V0\_CON)}$ − 0.02	-	$V_{(HDMI\_5V0\_CON)}$ + 0.02	V
V_{OL}	LOW-level output voltage	internal pull-up and external sink	-	100	200	mV
V_{IK}	input clamping voltage	I_I = −18 mA	-	-	−1.0	V
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 5.0 V; $V_{CC(SYS)}$ = 3.3 V; CEC_STBY = HIGH [2][3]	-	8.0	10	pF
R_{pu}	pull-up resistance		1.6	1.8	2.0	kΩ
DDC buffer on system side[1][4]						
V_{IH}	HIGH-level input voltage	$V_{CC(SYS)}$ = 1.8 V	450	-	-	mV
		$V_{CC(SYS)}$ = 2.5 V	620	-	-	mV
		$V_{CC(SYS)}$ = 3.3 V	760	-	-	mV
		$V_{CC(SYS)}$ = 5.0 V	800	-	-	mV
V_{IL}	LOW-level input voltage	$V_{CC(SYS)}$ = 1.8 V	-	-	330	mV
		$V_{CC(SYS)}$ = 2.5 V	-	-	380	mV
		$V_{CC(SYS)}$ = 3.3 V	-	-	400	mV
		$V_{CC(SYS)}$ = 5.0 V	-	-	420	mV
V_{OH}	HIGH-level output voltage	[2]	$V_{CC(SYS)}$ − 0.02	-	$V_{CC(SYS)}$ + 0.02	V
V_{OL}	LOW-level output voltage	$V_{CC(SYS)}$ = 1.8 V [5]	-	490	500	mV
		$V_{CC(SYS)}$ = 2.5 V [5]	-	640	690	mV
		$V_{CC(SYS)}$ = 3.3 V [5]	-	685	790	mV
		$V_{CC(SYS)}$ = 5.0 V [5]	-	720	820	mV
V_{IK}	input clamping voltage	I_I = −18 mA	-	-	−1.0	V
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz [2]	-	6.0	8.0	pF
R_{pu}	pull-up resistance		3.2	3.65	4.1	kΩ

Table 8. Static characteristics *...continued*

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CEC_CON[1]						
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.80	V
V_{OH}	HIGH-level output voltage		2.88	3.3	3.63	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.5 mA	-	100	200	mV
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 1.65 V; AC input = 2.5 $V_{(p-p)}$; f = 100 kHz [2]	-	8.0	10	pF
R_{pu}	pull-up resistance		23.4	26.0	28.6	kΩ
CEC_SYS[1][4]						
V_{IH}	HIGH-level input voltage	$V_{CC(SYS)}$ = 1.8 V	450	-	-	mV
		$V_{CC(SYS)}$ = 2.5 V	620	-	-	mV
		$V_{CC(SYS)}$ = 3.3 V	760	-	-	mV
		$V_{CC(SYS)}$ = 5.0 V	800	-	-	mV
V_{IL}	LOW-level input voltage	$V_{CC(SYS)}$ = 1.8 V	-	-	330	mV
		$V_{CC(SYS)}$ = 2.5 V	-	-	380	mV
		$V_{CC(SYS)}$ = 3.3 V	-	-	400	mV
		$V_{CC(SYS)}$ = 5.0 V	-	-	420	mV
V_{OH}	HIGH-level output voltage	[2]	$V_{CC(SYS)}$ − 0.02	-	$V_{CC(SYS)}$ + 0.02	V
V_{OL}	LOW-level output voltage	$V_{CC(SYS)}$ = 1.8 V [5]	-	490	500	mV
		$V_{CC(SYS)}$ = 2.5 V [5]	-	640	690	mV
		$V_{CC(SYS)}$ = 3.3 V [5]	-	675	770	mV
		$V_{CC(SYS)}$ = 5.0 V [5]	-	710	800	mV
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 1.65 V; AC input = 2.5 $V_{(p-p)}$; f = 100 kHz [2]	-	6.0	7.0	pF
R_{pu}	pull-up resistance		8.5	10	11.5	kΩ
HOTPLUG_DET_CON[1]						
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
R_{pd}	pull-down resistance		60	100	140	kΩ
C_i	input capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz [2]	-	8.0	10	pF

Table 8. Static characteristics *...continued*

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HOTPLUG_DET_SYS[1]						
V_{OH}	HIGH-level output voltage	I_{OL} = 1 mA	0.7 × $V_{CC(SYS)}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −1 mA	-	200	300	mV
R_{pd}	pull-down resistance		60	100	140	kΩ

[1] The device is active if the input voltage at pin CEC_STBY is above the HIGH level.

[2] This parameter is guaranteed by design.

[3] Capacitive load measured at power-on.

[4] No external pull-up resistor attached.

[5] Typical value at T_{amb} = +25 °C.

Table 9. CEC_STBY power management circuit

$V_{CC(SYS)}$ = 1.62 V to 5.5 V; $V_{CC(5V0)}$ = 4.5 V to 6.5 V; GND = 0 V; T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Board side: input pin CEC_STBY[1]						
V_{IH}	HIGH-level input voltage	HIGH = active [2]	1.2	-	6.5	V
V_{IL}	LOW-level input voltage	LOW = standby [3]	−0.5	-	0.8	V
R_{pd}	pull-down resistance		60	100	140	kΩ
C_i	input capacitance	V_I = 3 V or 0 V	-	6	7	pF

[1] The CEC_STBY pin should be connected permanently to $V_{CC(5V0)}$ or $V_{CC(SYS)}$ if no enable control is needed.

[2] DDC buffers, HPD buffer, and HDMI_5V0_CON out enabled; CEC buffer enabled.

[3] DDC buffers, HPD buffer, and HDMI_5V0_CON out disabled; CEC buffer enabled.

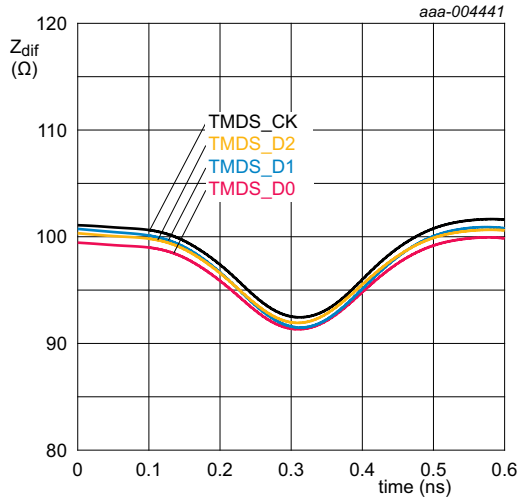
9. Dynamic characteristics

Table 10. Dynamic characteristics

$V_{CC(5V0)}$ = 5.0 V; $V_{CC(SYS)}$ = 1.8 V; GND = 0 V; T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDC_DAT_SYS, DDC_CLK_SYS, DDC_DAT_CON, DDC_CLK_CON[1]						
t_{PLH}	LOW to HIGH propagation delay	system side to connector side Figure 16	-	80	-	ns
t_{PHL}	HIGH to LOW propagation delay	system side to connector side Figure 16	-	60	-	ns
t_{PLH}	LOW to HIGH propagation delay	connector side to system side Figure 17	-	120	-	ns
t_{PHL}	HIGH to LOW propagation delay	connector side to system side Figure 17	-	80	-	ns
t_{TLH}	LOW to HIGH transition time	connector side Figure 18	-	150	-	ns
t_{THL}	HIGH to LOW transition time	connector side Figure 18	-	100	-	ns
t_{TLH}	LOW to HIGH transition time	system side Figure 19	-	250	-	ns
t_{THL}	HIGH to LOW transition time	system side Figure 19	-	80	-	ns

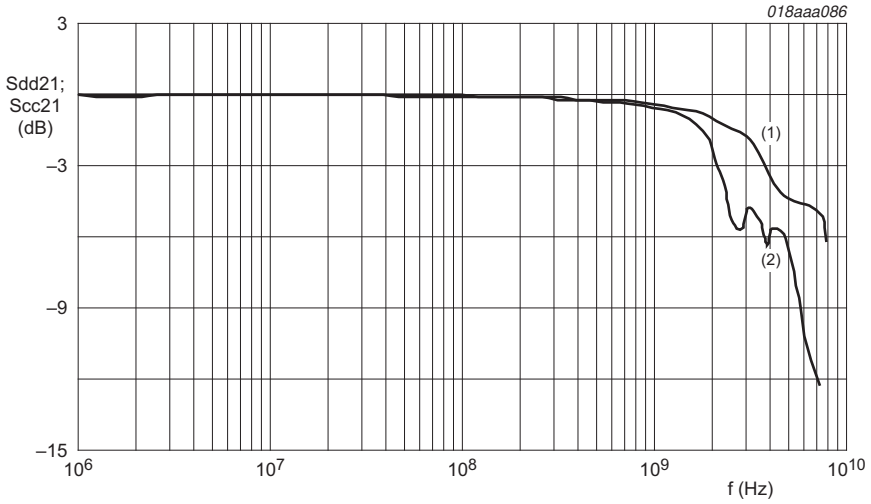
[1] All dynamic measurements are done with a 75 pF load. Rise times are determined by internal pull-up resistors.



t_r = 200 ps; no filter; $V_{CC(5V0)}$ = 5 V

100 Ω differential (CH1 + CH2)

Fig 3. Differential TDR plot

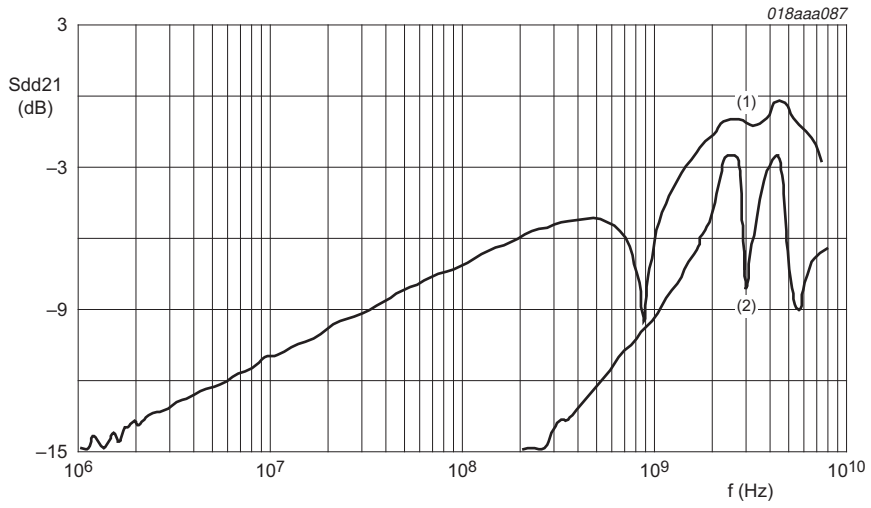


(1) Sdd21

(2) Scc21

Normalized to 100 Ω; differential pairs at signal pins.

Fig 4. Mixed-mode differential and common-mode insertion loss; typical values

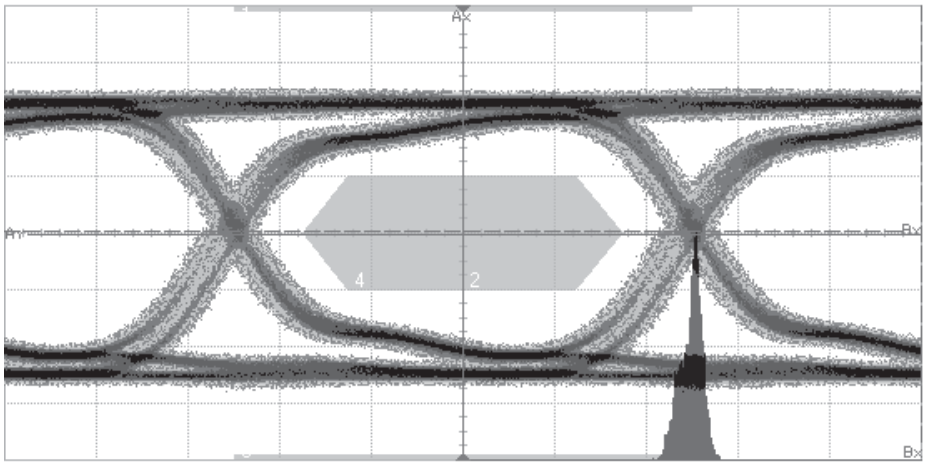


(1) Sdd21; Near End Crosstalk (NEXT)

(2) Sdd21; Far End Crosstalk (FEXT)

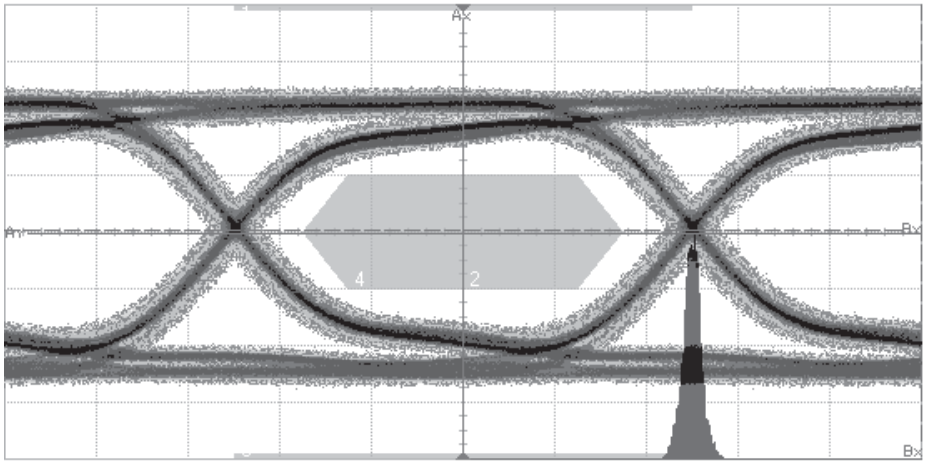
normalized to 100 Ω; differential pairs CH1/CH2 versus CH3/CH4

Fig 5. Mixed-mode differential and common-mode NEXT / FEXT; typical values



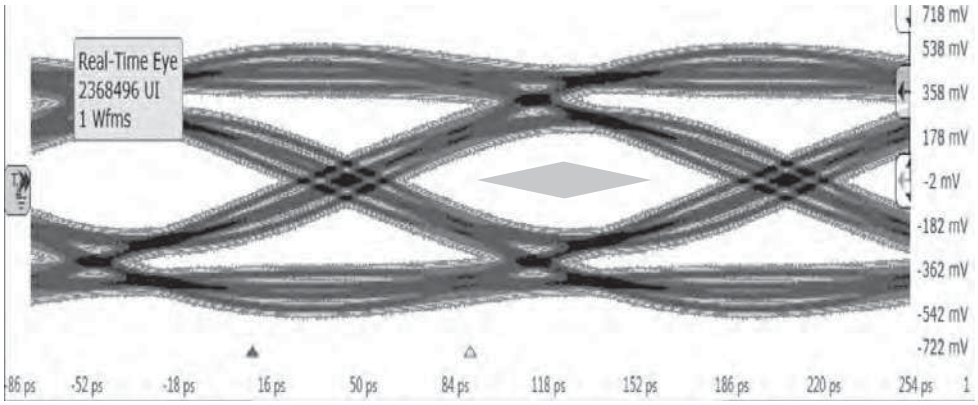
227 MHz pixel clock
Horizontal scale: 90 ps/div
Vertical scale: 200 mV/div
Offset: 42.6 mV

Fig 6. Eye diagram using IP4786CZ32S (1080p, 12 bit)



297 MHz pixel clock
Horizontal scale: 67.5 ps/div
Vertical scale: 200 mV/div
Offset: 42.6 mV

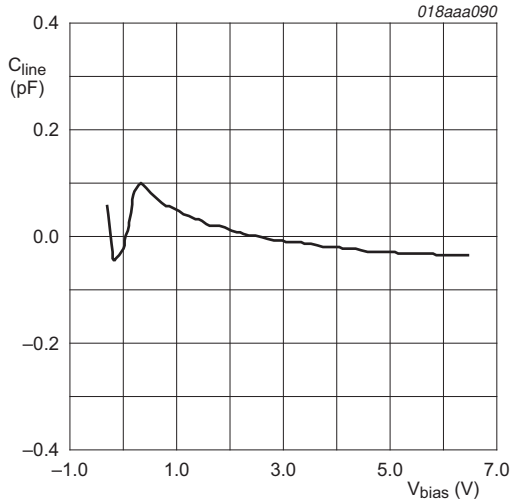
Fig 7. Eye diagram using IP4786CZ32S (1080p, 16 bit)



148.5 MHz test frequency

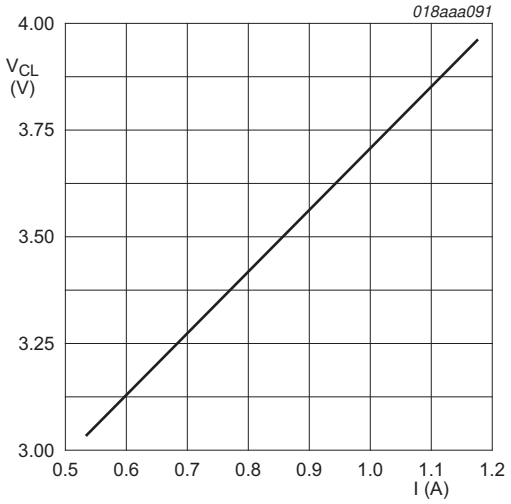
Measured at TP2 with worst cable emulator, reference cable equalizer and worst case negative skew, device powered.

Fig 8. Eye diagram using IP4786CZ32S (2160p, 60 Hz)



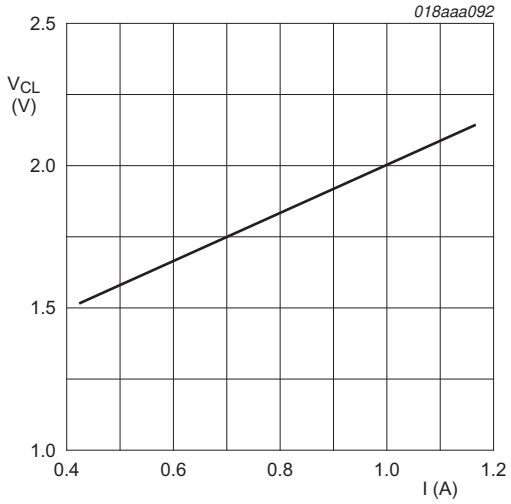
Deviation from typical capacitance normalized at V_{bias} = 2.5 V

Fig 9. Line capacitance as a function of bias voltage; typical values



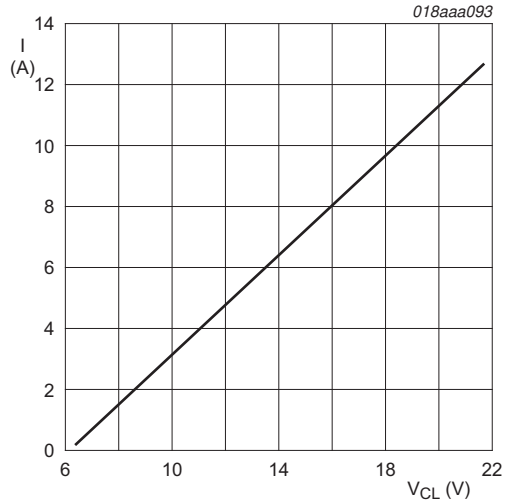
IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 10. Dynamic resistance with positive clamping



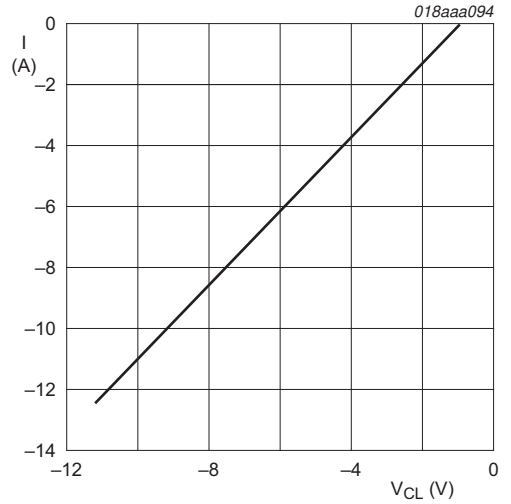
IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 11. Dynamic resistance with negative clamping



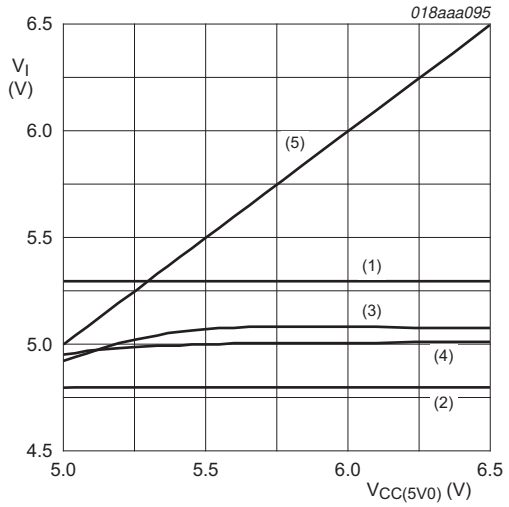
t_p = 100 ns; TLP; signal pins; typical values

Fig 12. Dynamic resistance with positive clamping



t_p = 100 ns; TLP; signal pins; typical values

Fig 13. Dynamic resistance with negative clamping



(1) 5.3 V; maximum values; HDMI CTS TID 7-11

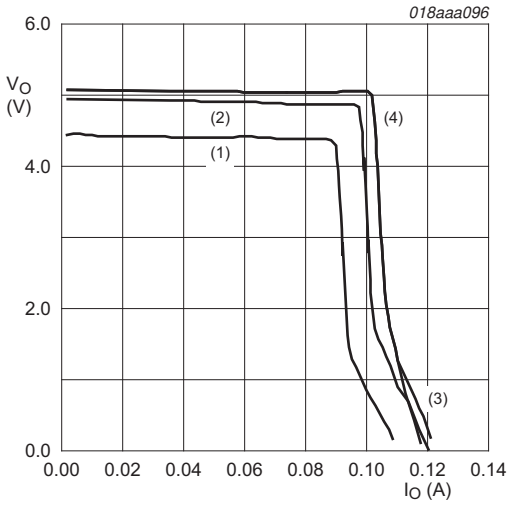
(2) 4.8 V; minimum values; HDMI CTS TID 7-11

(3) I = 0 mA

(4) I = 55 mA

(5) $V_{CC(5V0)}$ supply input; 4.925 V to 6.5 V

Fig 14. Overvoltage limiter function (HDMI_5V0_CON)



(1) $V_{CC(5V0)}$ = 4.5 V

(2) $V_{CC(5V0)}$ = 5.0 V

(3) $V_{CC(5V0)}$ = 5.5 V

(4) $V_{CC(5V0)}$ = 6.5 V

Fig 15. Overcurrent limiter function (HDMI_5V0_CON)

10. AC waveforms

10.1 DDC propagation delay

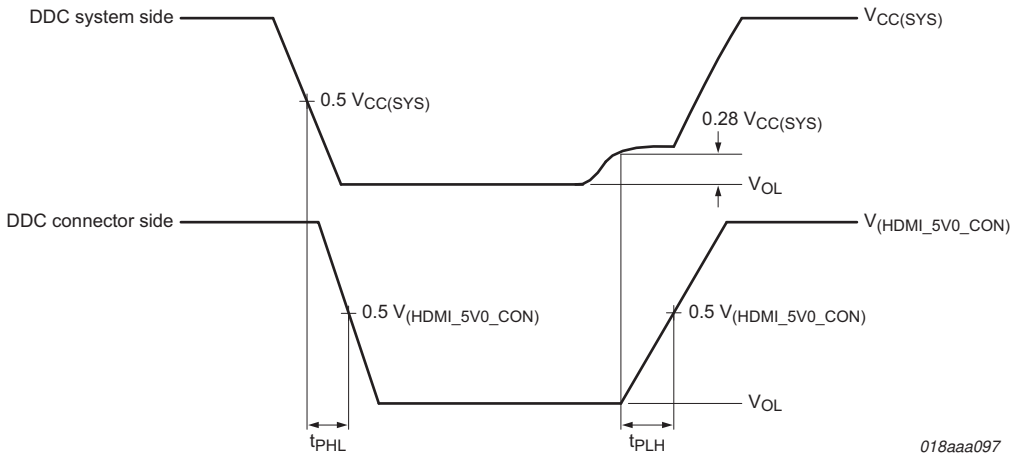


Fig 16. Propagation delay DDC, DDC system side to DDC connector side

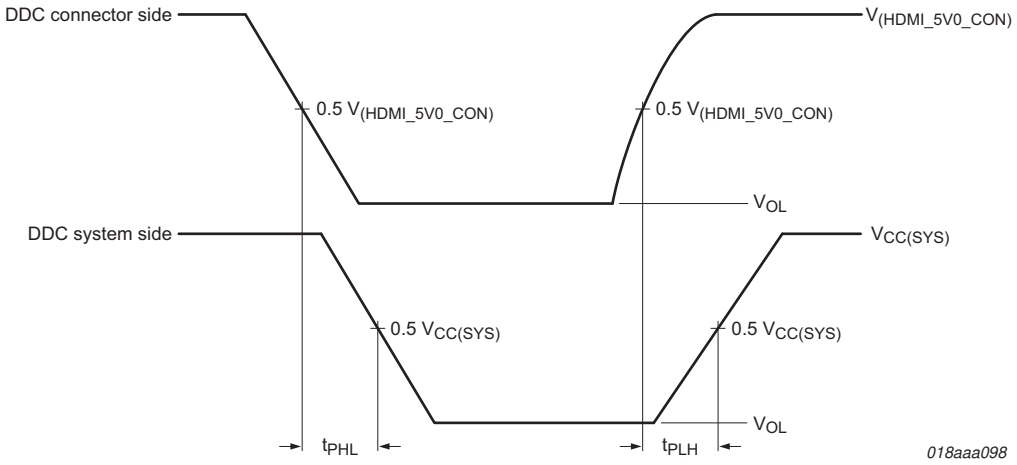


Fig 17. Propagation delay DDC, DDC connector side to DDC system side

10.2 DDC transition time

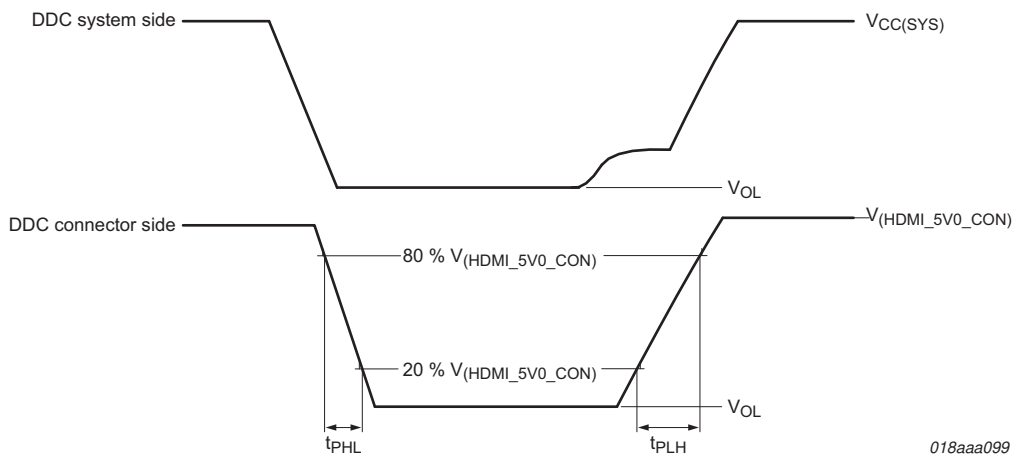


Fig 18. Transition time DDC connector side

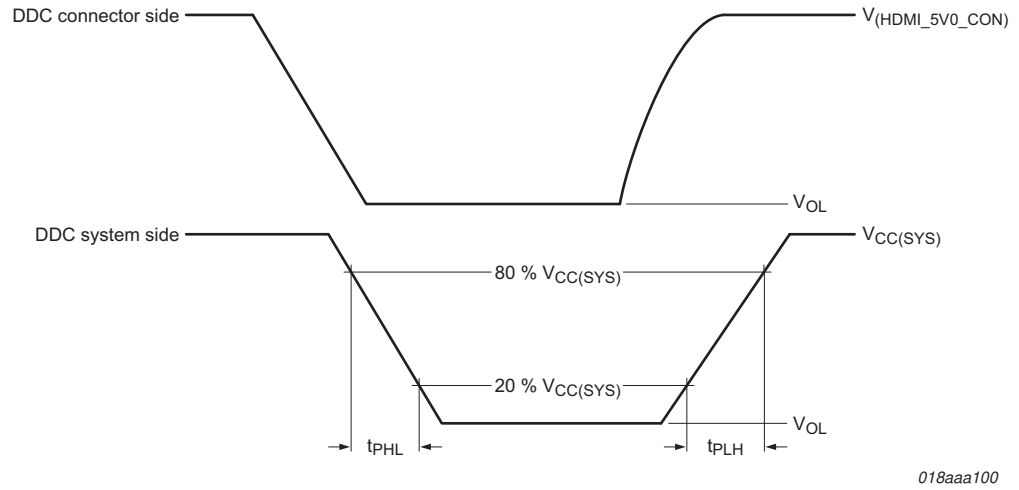


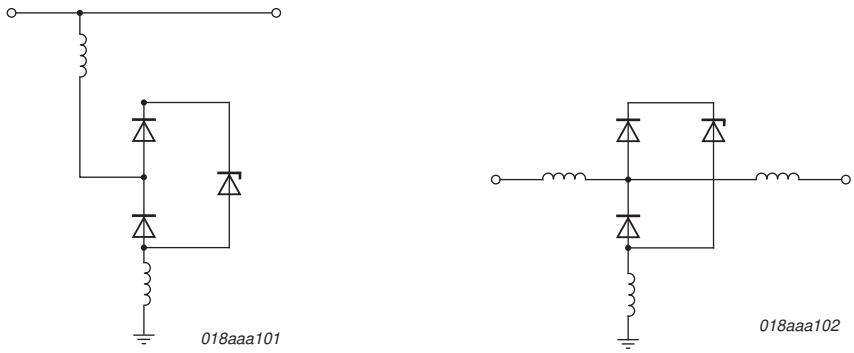
Fig 19. Transition time DDC system side

11. Application information

11.1 TMDS ESD

To protect the TMDS lines and also to comply with the impedance requirements of the HDMI specification, the IP4786CZ32S provides ESD protection with matched TLC ESD structures. Typical Dual Rail Clamp (DRC) or rail-to-rail shunt structures are common for low-capacitance ESD protection (Figure 20; left side) where the dominant factor for the TMDS line impedance dip is determined by the capacitive load to ground. Parasitic lead inductances of the packaging in this case work against the ESD clamping performance by including the $\Delta I/\Delta t$ reactance of the inductance into the path of the ESD shunt.

The IP4786CZ32S utilizes these inherent inductances in series with the transmission line in order to present an effective capacitive load of roughly only 0.7 pF. This TLC structure minimizes the capacitive dip, for ideal signal integrity (Figure 20; right side) without complicated PCB pre-compensation. As a beneficial side effect, this enhances the ESD performance of the device as well, since the reactance of the series inductance attenuates the fast initial peak of the ESD pulse, for a lower residual pulse delivered to the Application Specific Integrated Circuit (ASIC).



a. Classic parallel ESD shunt protection

b. Improved series shunt TLC clamping

Fig 20. TLC ESD protection of TMDS lines

11.2 Operating and standby modes

The operating mode of IP4786CZ32S depends on the availability of the $V_{CC(5V0)}$ and $V_{CC(SYS)}$ supply voltages and on the state of the CEC_STBY input signal. Without availability of both supplies, IP4786CZ32S is in Standby mode. As soon as $V_{CC(5V0)}$ and $V_{CC(SYS)}$ are within the range specified in Section 8, the part is in an operating mode that can be controlled via the CEC_STBY input signal. In case CEC_STBY is LOW, only the CEC buffer is active and enabled to receive or send CEC commands. All other outputs are in a high-ohmic state. A HIGH input signal enables all parts of IP4786CZ32S and puts the device into full operating mode.

Table 11. IP4786CZ32S operating modes

$V_{CC(SYS)}$	$V_{CC(5V0)}$	CEC_STBY[1]	Mode	Description
< 1.1 V	< 4.5 V	X	Standby mode	all outputs high-ohmic
≥ 1.1 V	≥ 4.5 V	L	CEC Standby mode	CEC circuit active; all other outputs high-ohmic
		H	full operating mode	all functional blocks active

[1] X = Don't care (either LOW or HIGH level); L = LOW-level input; H = HIGH-level input

If no CEC Standby mode is required, or if no special Power-down modes are desired, the CEC_STBY pin can be pulled HIGH to $V_{CC(5V0)}$ or $V_{CC(SYS)}$ for continuous HDMI and CEC operation as soon as the supplies are available.

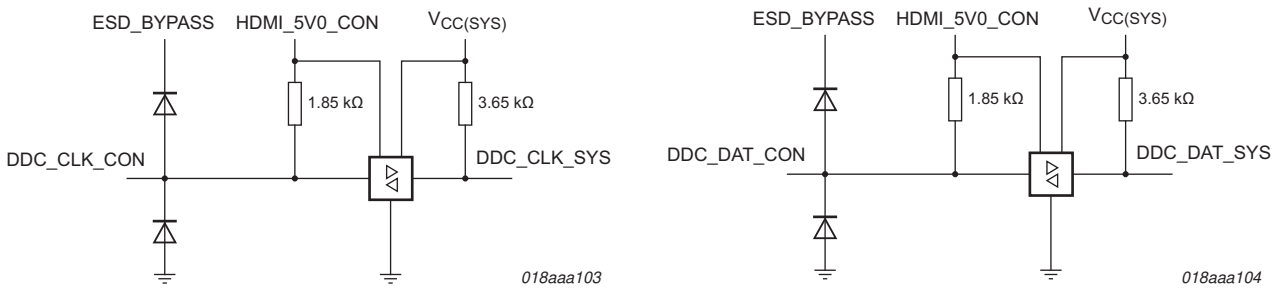
Strapping the CEC_STBY = $V_{CC(SYS)}$ = V_{DD} of the ASIC guarantees that all interface signals ending with the suffix "_SYS" on the system side are disabled when $V_{CC(SYS)}$ goes LOW. This configuration protects the ASIC I/O signals from exceeding its local V_{DD}. In this mode, even if $V_{CC(5V0)}$ is powered, HDMI_5V0_CON goes active and hot plug events can be detected only when the ASIC power supply rail is on.

Strapping CEC_STBY = $V_{CC(5V0)}$ is the most basic configuration where the buffers are enabled whenever the local $V_{CC(5V0)}$ and $V_{CC(SYS)}$ supplies reach minimum operating levels.

11.3 DDC circuit

The DDC bus circuit integrates all required pull-ups, and provides full capacitive decoupling between the HDMI connector and the DDC bus lines on the PCB. The capacitive decoupling ensures that the maximum capacitive load is well within the 50 pF maximum of the HDMI specification. No external pull-ups or pull-downs are required.

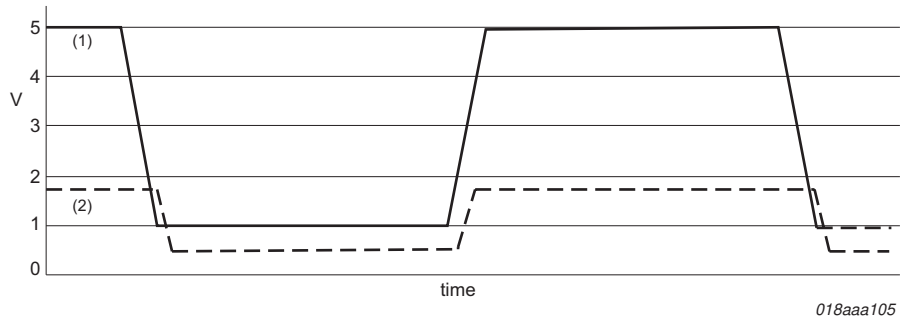
The bidirectional buffers support high-capacitive load on the HDMI cable-side. Various non-compliant but prevalent low-cost cables have been observed with a capacitive load of up to 6 nF on the DDC lines, far exceeding the 700 pF HDMI limit. The IP4786CZ32S can easily decouple this from the weaker ASIC I/O buffers, and drive the rogue cable successfully.



a. DDC clock

b. DDC data

Fig 21. DDC circuit



(1) Valid I^2C signaling example on the cable (connector side) from 5 V (HIGH) to approximately 1 V (LOW).

(2) Valid logic-level signaling example to the ASIC (system side) from 1.8 V (HIGH) to approximately 0.5 V (LOW).

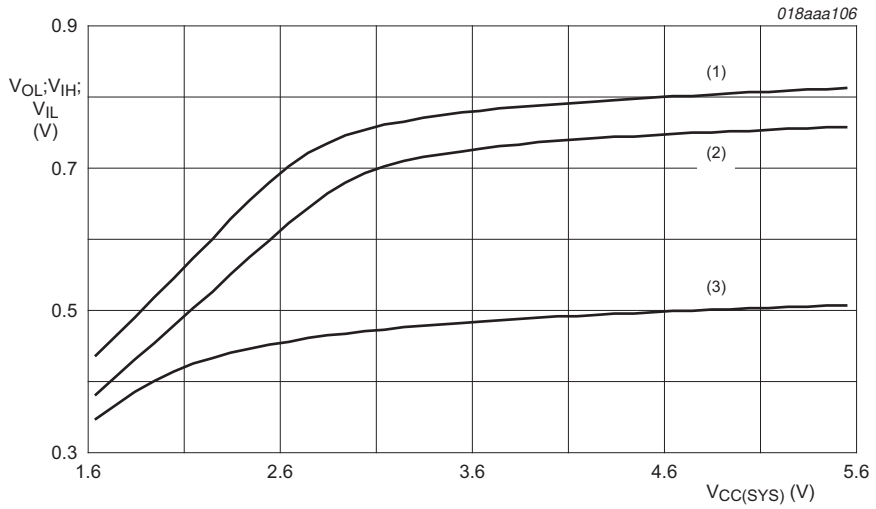
Fig 22. DDC level shifting waveform example

11.4 Logic low I²C voltage shifter

The DDC buffers provide an additional feature commonly required for high-integration HDMI ASICs. In order to be compatible with the 5 V I²C standard used for DDC communication, I/O buffer cells of many HDMI modern transmitter chips require level shifting. As FET-based level shifting just limits the HIGH level of the signal, the LOW level remains unchanged. As a result, the LOW-level voltages on the DDC bus often exceed the 0.3 V_{DD} LOW-level input voltage (V_{IL}) limit of low-voltage I/O buffers.

To enable proper operation that is independent of the system side I/O voltage, the DDC buffers inside IP4786CZ32S shift both the HIGH and the LOW levels by the required amount. This ensures that LOW levels on the system side DDC bus match the LOW-level input voltage requirements down to I/O voltages of 1.8 V.

Besides the DDC buffers, this feature is also included in the CEC buffer, allowing standard I/O buffer cells to be used in HDMI ASICs and microcontrollers.



(1) $V_{OL(max)}$ driven to system (ASIC) side when I²C logic LOW (less than 0.3 × HDMI_5V0_CON)

(2) $V_{IH(min)}$ threshold on system (ASIC) side to drive I²C logic HIGH

(3) $V_{IL(max)}$ threshold on system (ASIC) side to drive I²C logic LOW

Fig 23. Logic voltage thresholds as a function of supply voltage on system side

11.5 Hot plug detect circuit and HEAC support

The IP4786CZ32S includes a hot plug detect circuit that simplifies the hot plug application. The circuit generates a standard logic level from the hot plug signal.

The hot plug detect circuit is pulling down the signal to avoid any floating signal. The comparator guarantees a save detection of the 2 V hot plug signal without any glitches or oscillation at the hot plug output.

The IP4786CZ32S also provides an additional ESD pin to protect the reserved / HEAC pin along with hot plug detect to 12 kV IEC 61000-4-2, level 4.

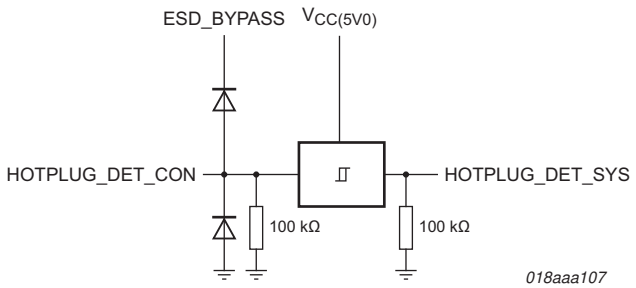


Fig 24. Hot plug detect circuit

11.6 CEC

The logical multidrop topology of the CEC bus can include complex physical stubs, loading cables, and interconnects that may deteriorate signal quality.
The IP4786CZ32S includes a full bidirectional buffer to drive the CEC bus and isolate the CEC microcontroller or ASIC General-Purpose Input/Output (GPIO).

The CEC buffer derives power from an on-board 3.3 V regulator from the $V_{CC(5V0)}$ domain (see Figure 25). This allows extensive system power management configurations and guarantees an HDMI-compliant $V_{(CEC\_CON)}$ on the connector, as well as the backdrive-protected 125 μA nominal CEC pull-up which does not degrade the bus when powered down.

By placing the CEC microcontroller and $V_{CC(5V0)}$ input on a 5 V rail as shown in Figure 28, the CEC microcontroller can communicate over CEC for power commands, and then enable the HDMI port via the CEC_STBY pin, as well as the rest of the system as needed.

The CEC buffer is always active as soon as both supply voltages are present. For details on the operating and Standby modes of IP4786CZ32S, see Section 11.2.

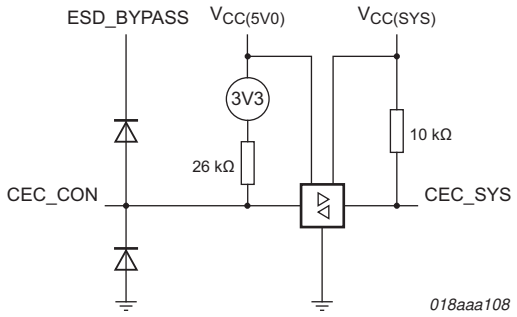


Fig 25. CEC module

11.7 Backdrive protection

The HDMI connector contains various signals which can partly supply current into an HDMI device that is powered down.

Typically, the DDC lines and the CEC signals can force significant current back into the powered-down rails as shown in Figure 26, causing power-on reset problems with the system, and possible damage. The IP4786CZ32S prevents this backdrive condition whenever the I/O voltage is greater than the local supply.

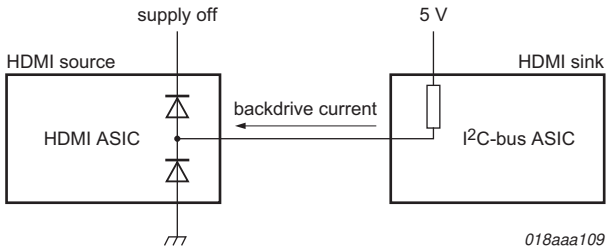


Fig 26. Generalized backdrive protection