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## MOSFET

### 650V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

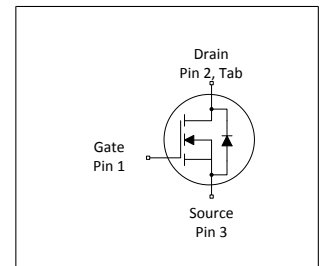
### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} \cdot Q_g$  and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

### Applications

PC Silverbox, Adapters, LCD & PDP TV and indoor Lighting

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	1000	$m\Omega$
$I_{d,typ}$	7.2	A
$Q_{g,typ}$	15.3	nC
$I_{D,pulse}$	12	A
$E_{oss@400V}$	1.5	$\mu J$

Type / Ordering Code	Package	Marking	Related Links
IPA65R1K0CE	PG-TO 220 FullPAK	65S1K0CE	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	7.2 4.6	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	12	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	50	mJ	$I_D=1\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.15	mJ	$I_D=1\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, repetitive	$I_{AR}$	-	-	1.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots480\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation (TO220)	$P_{tot}$	-	-	68	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	-
Continuous diode forward current	$I_S$	-	-	5.1	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	12	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di <sub>f</sub> /dt	-	-	500	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Insulation withstand voltage for TO-220FP	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum duty cycle  $D=0.50$ , TO220 equivalent

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_G$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	3.8	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}, I_D=0.2mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=650, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=650, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.86	1.00	$\Omega$	$V_{GS}=10V, I_D=1.5A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=1.5A, T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	5.5	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	328	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Output capacitance	$C_{oss}$	-	23	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	14	-	pF	$V_{GS}=0V, V_{DS}=0\dots480V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	58.5	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots480V$
Turn-on delay time	$t_{d(on)}$	-	6.6	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=10.2\Omega$ ; see table 9
Rise time	$t_r$	-	5.2	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=10.2\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	41	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=10.2\Omega$ ; see table 9
Fall time	$t_f$	-	13.6	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=10.2\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	1.8	-	nC	$V_{DD}=480V, I_D=2.2A, V_{GS}=0$ to 10V
Gate to drain charge	$Q_{gd}$	-	8	-	nC	$V_{DD}=480V, I_D=2.2A, V_{GS}=0$ to 10V
Gate charge total	$Q_g$	-	15.3	-	nC	$V_{DD}=480V, I_D=2.2A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=480V, I_D=2.2A, V_{GS}=0$ to 10V

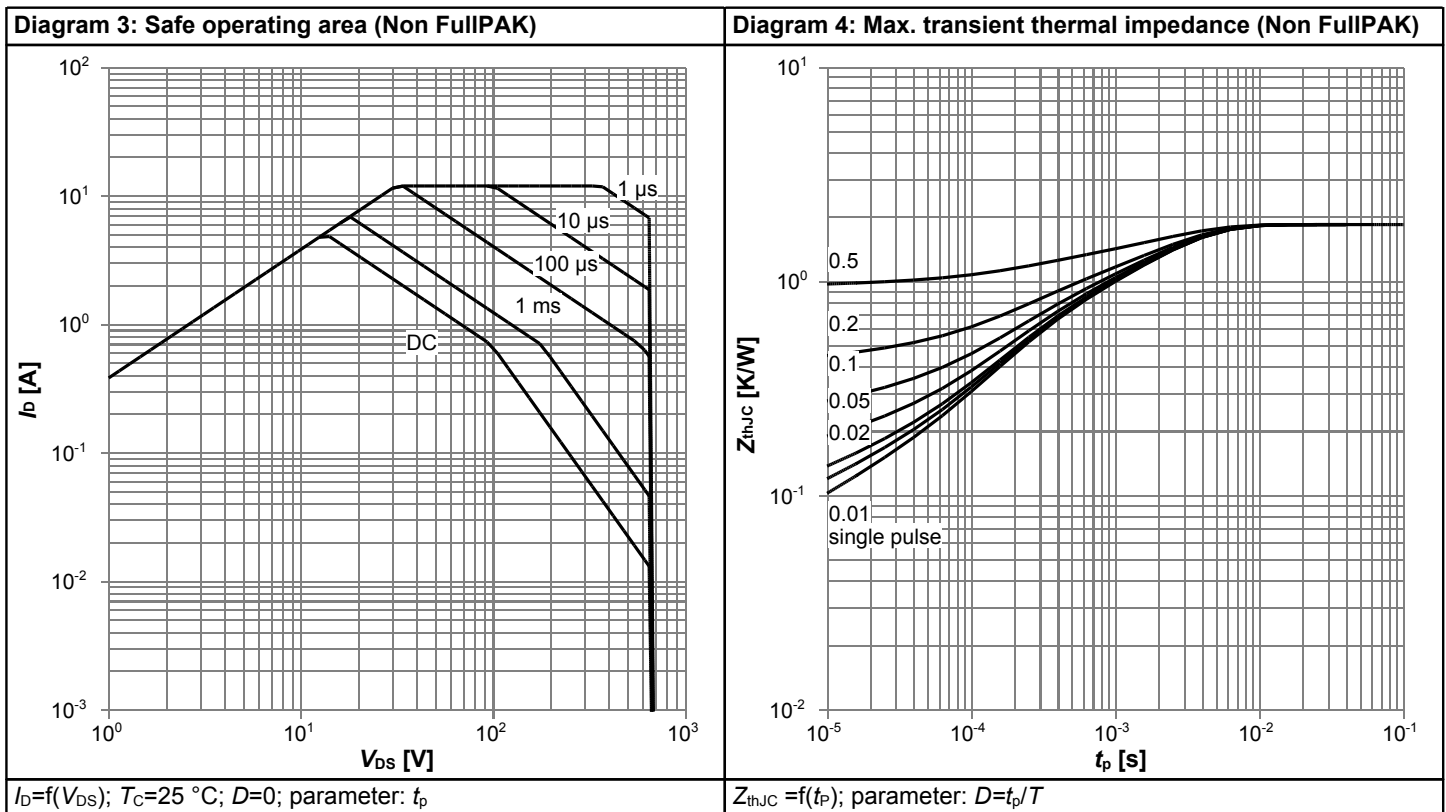
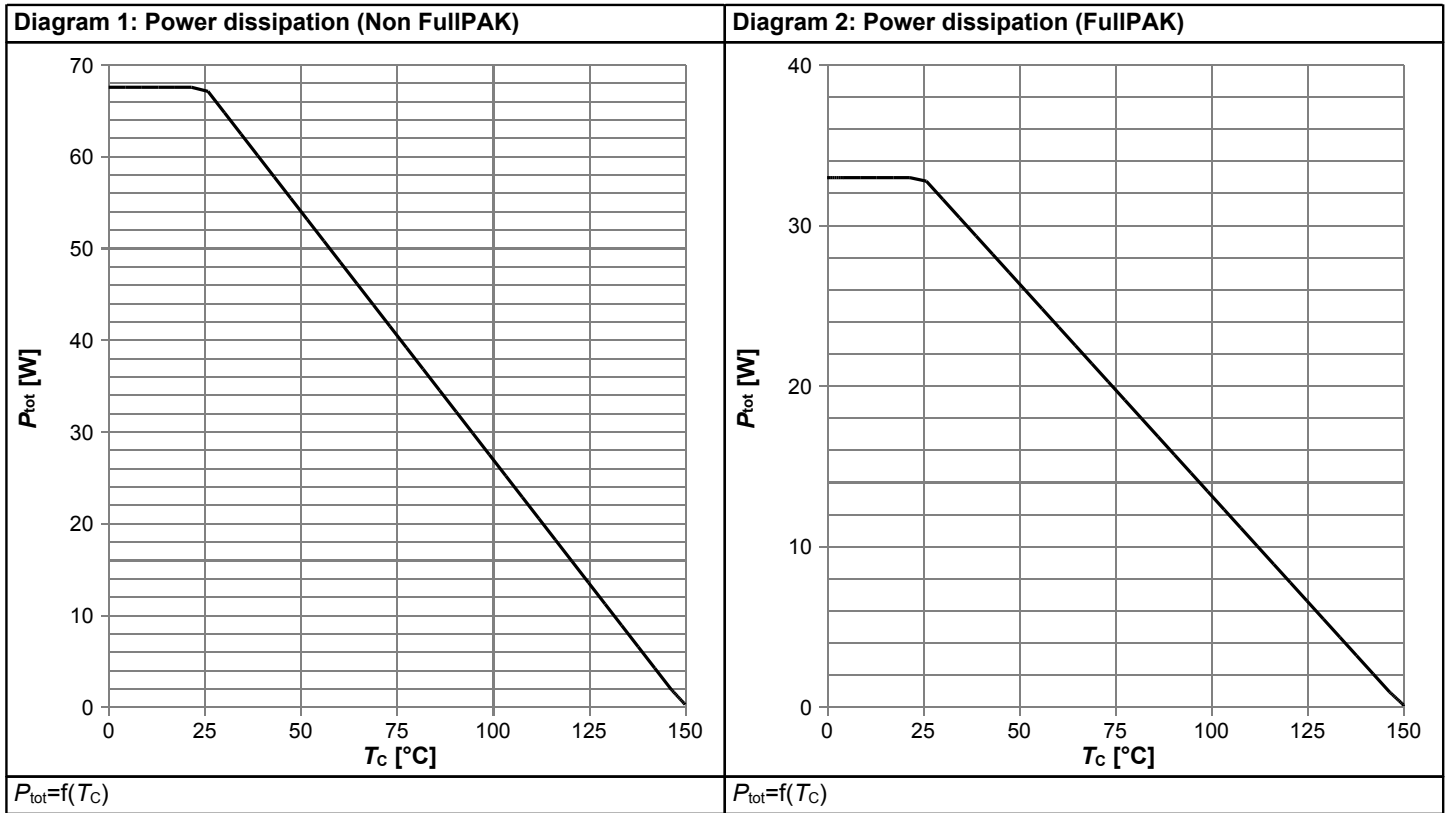
<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{o(BR)DSS}$

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{o(BR)DSS}$

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=2.2A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	226	-	ns	$V_R=400V, I_F=2.2A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	1.3	-	$\mu C$	$V_R=400V, I_F=2.2A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	9.9	-	A	$V_R=400V, I_F=2.2A, di_F/dt=100A/\mu s$ ; see table 8

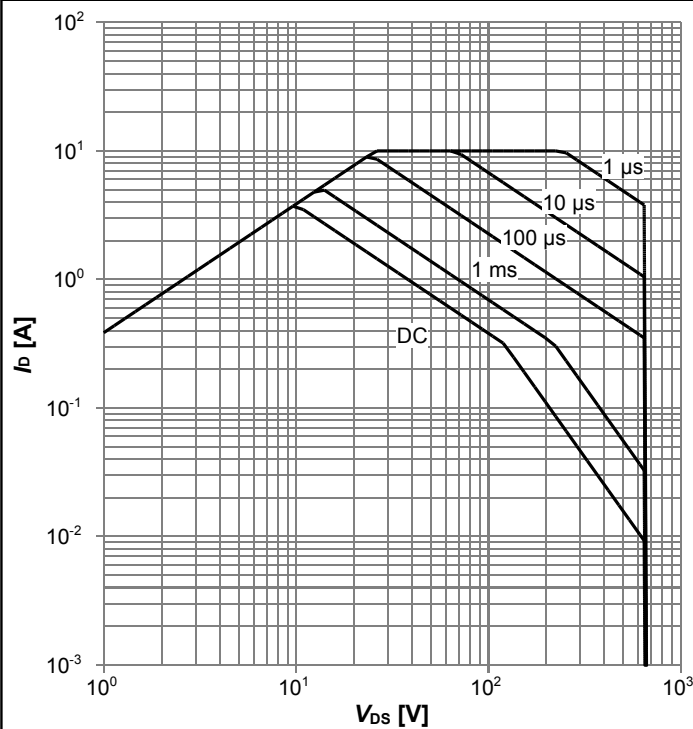
**4 Electrical characteristics diagrams**





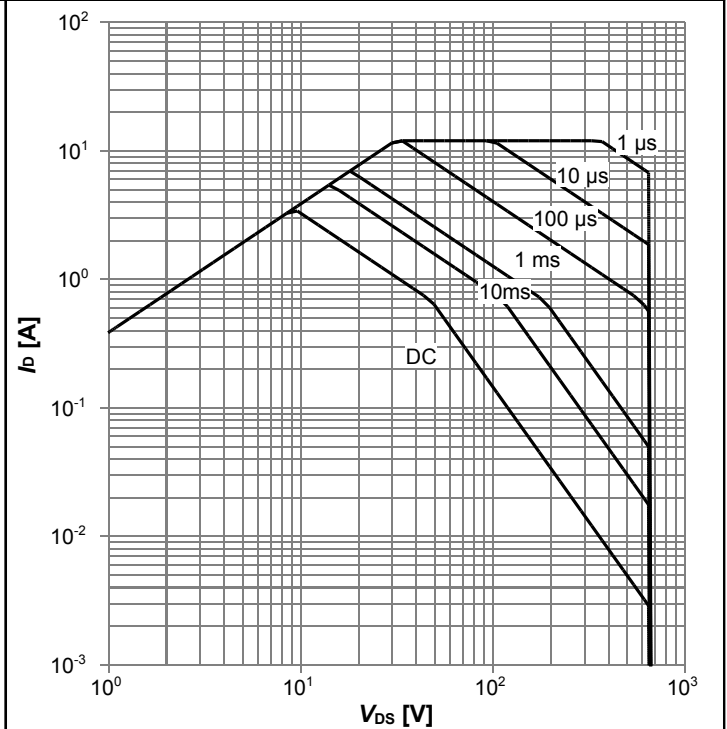
# 650V CoolMOS™ CE Power Transistor IPA65R1K0CE

**Diagram 5: Safe operating area (Non FullPAK)**



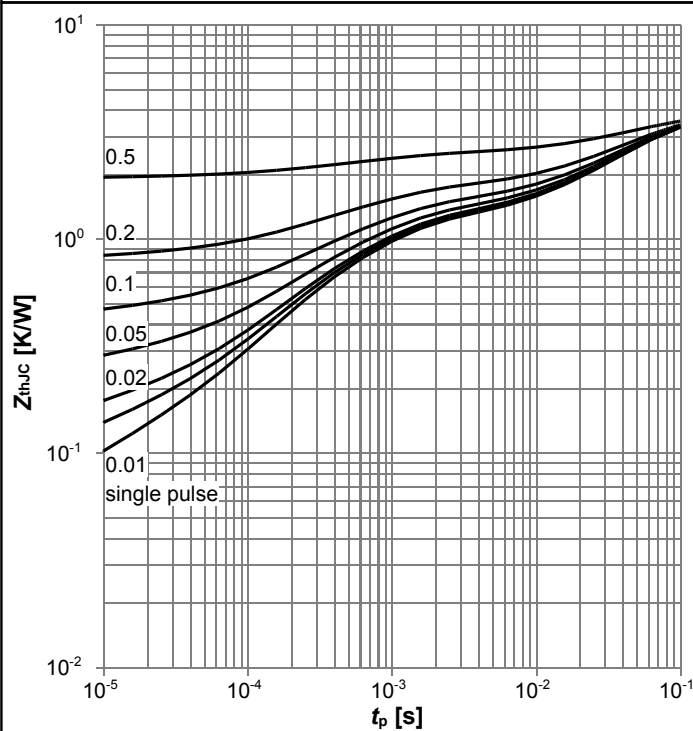
$I_b = f(V_{Ds}); T_C = 80\text{ °C}; D = 0; \text{parameter: } t_p$

**Diagram 6: Safe operating area (FullPAK)**



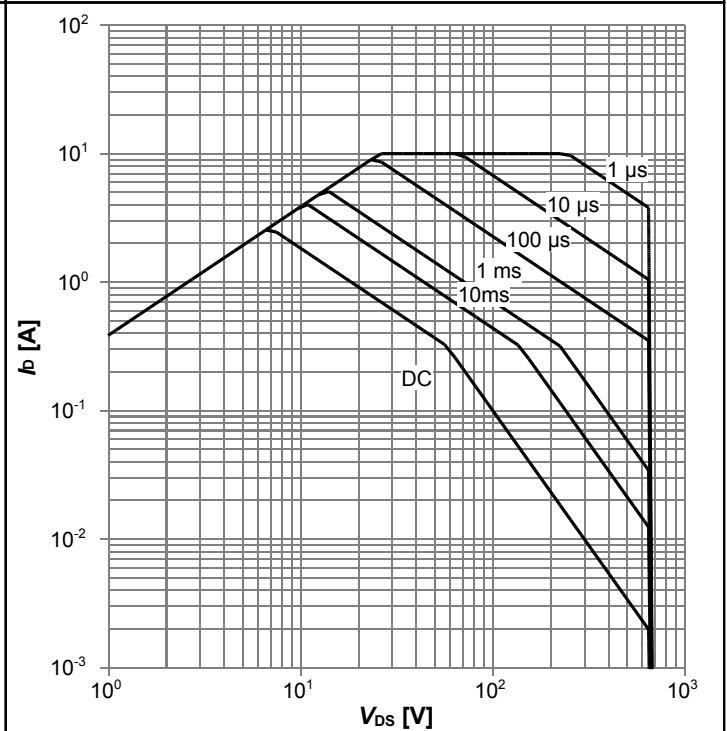
$I_b = f(V_{Ds}); T_C = 25\text{ °C}; D = 0; \text{parameter: } t_p$

**Diagram 7: Max. transient thermal impedance (FullPAK)**



$Z_{thJC} = f(t_p); \text{parameter: } D = t_p/T$

**Diagram 8: Safe operating area (FullPAK)**

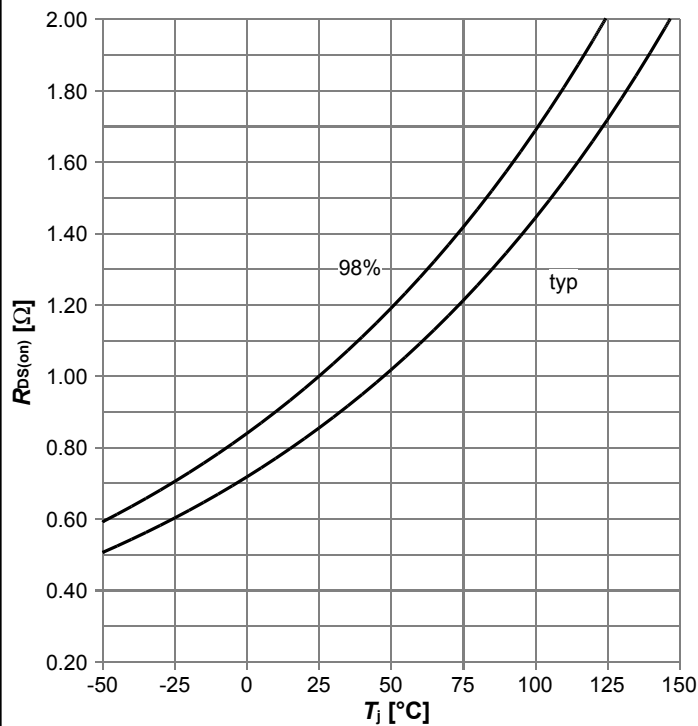


$I_b = f(V_{Ds}); T_C = 80\text{ °C}; D = 0; \text{parameter: } t_p$

# 650V CoolMOS™ CE Power Transistor

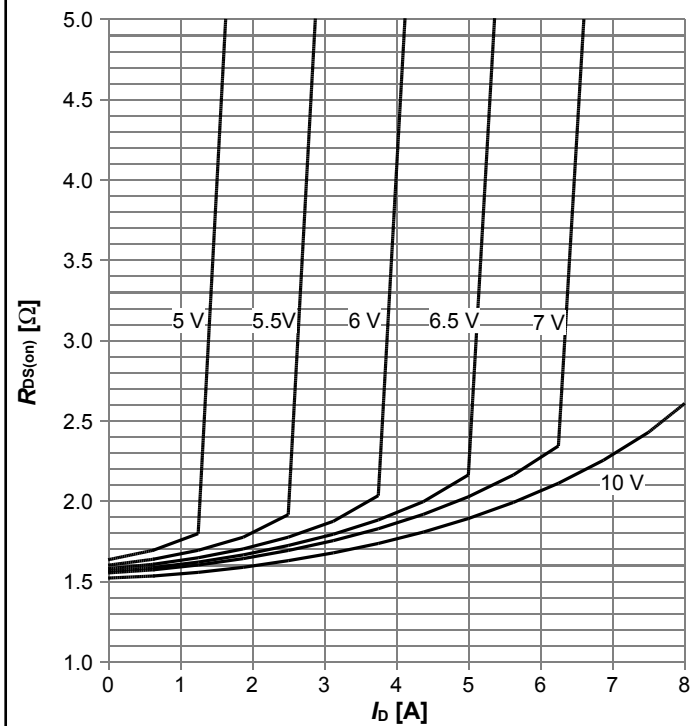
## IPA65R1K0CE

**Diagram 9: Drain-source on-state resistance**



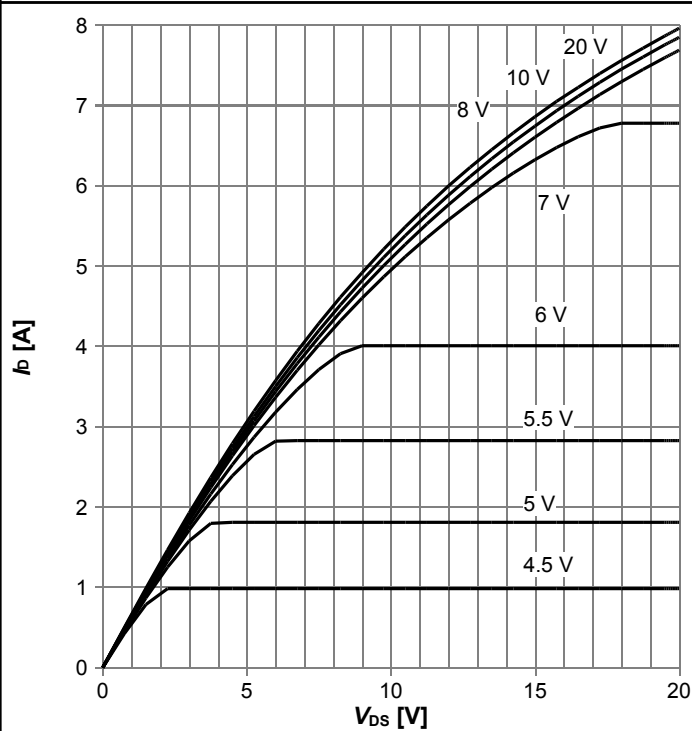
$R_{DS(on)}=f(T_j); I_D=1.5 \text{ A}; V_{GS}=10 \text{ V}$

**Diagram 10: Typ. drain-source on-state resistance**



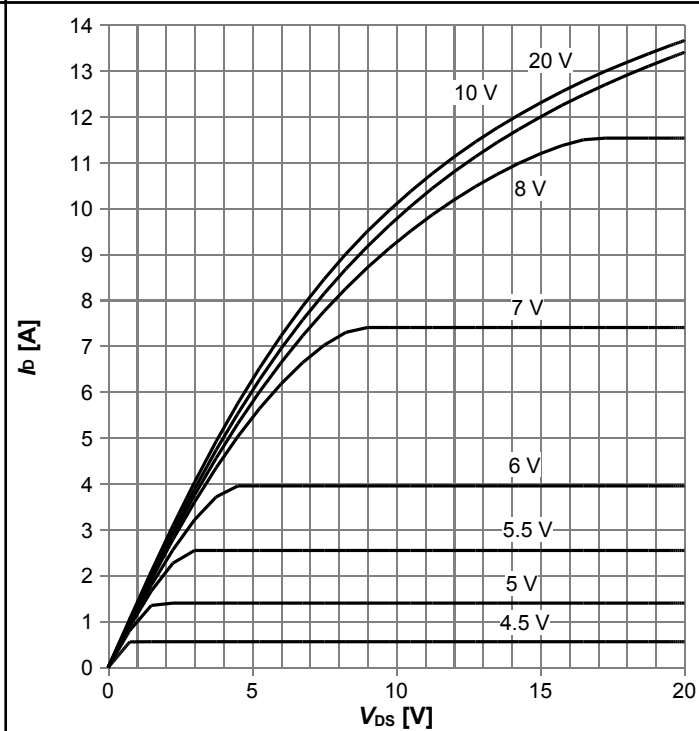
$R_{DS(on)}=f(I_D); T_j=125 \text{ }^{\circ}\text{C}; \text{parameter: } V_{GS}$

**Diagram 11: Typ. output characteristics**



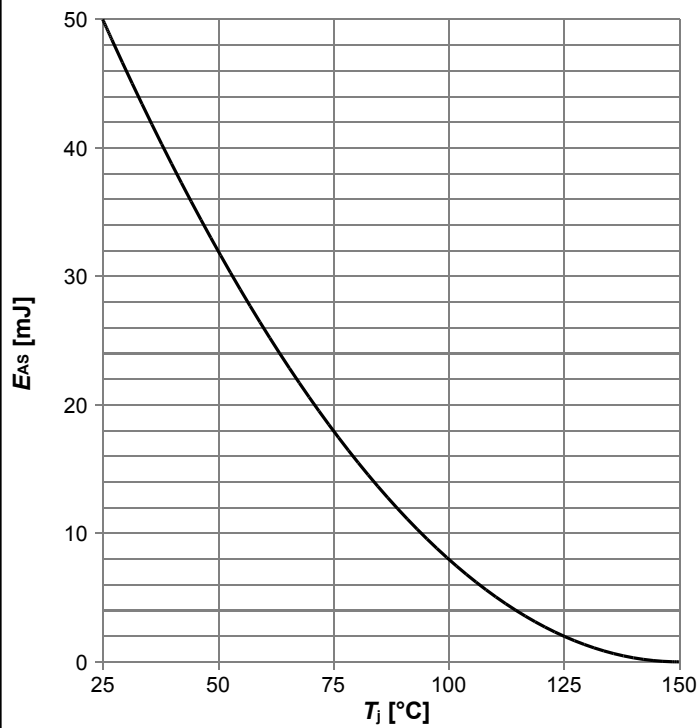
$I_D=f(V_{DS}); T_j=125 \text{ }^{\circ}\text{C}; \text{parameter: } V_{GS}$

**Diagram 12: Typ. output characteristics**



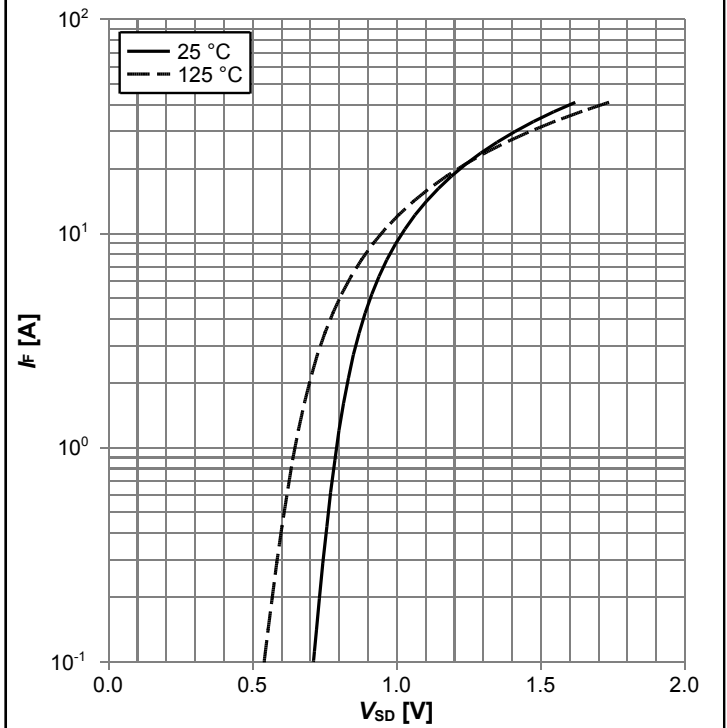
$I_D=f(V_{DS}); T_j=25 \text{ }^{\circ}\text{C}; \text{parameter: } V_{GS}$

**Diagram 13: Avalanche energy**



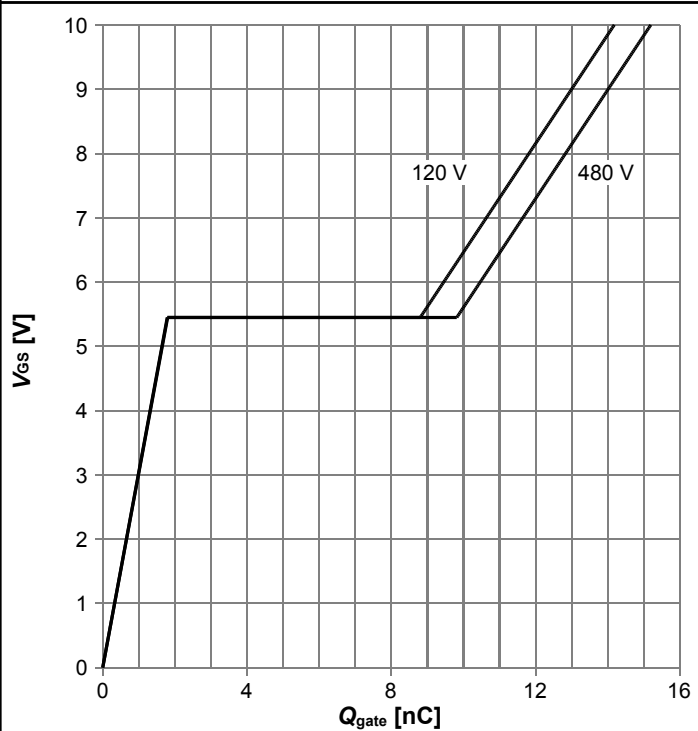
$E_{AS}=f(T_j)$ ;  $I_D=1.0$  A;  $V_{DD}=50$  V

**Diagram 14: Forward characteristics of reverse diode**



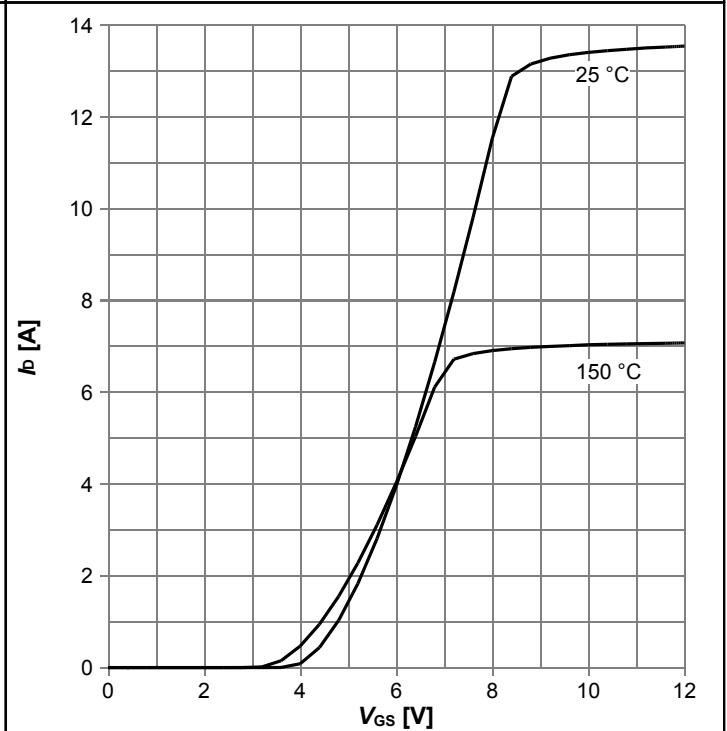
$I_F=f(V_{SD})$ ; parameter:  $T_j$

**Diagram 15: Typ. gate charge**



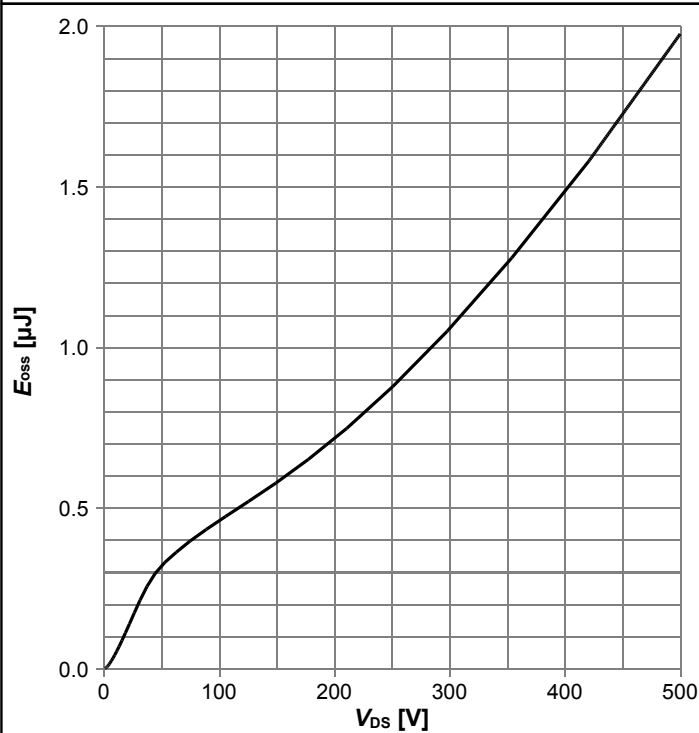
$V_{GS}=f(Q_{gate})$ ;  $I_D=2.2$  A pulsed; parameter:  $V_{DD}$

**Diagram 16: Typ. transfer characteristics**



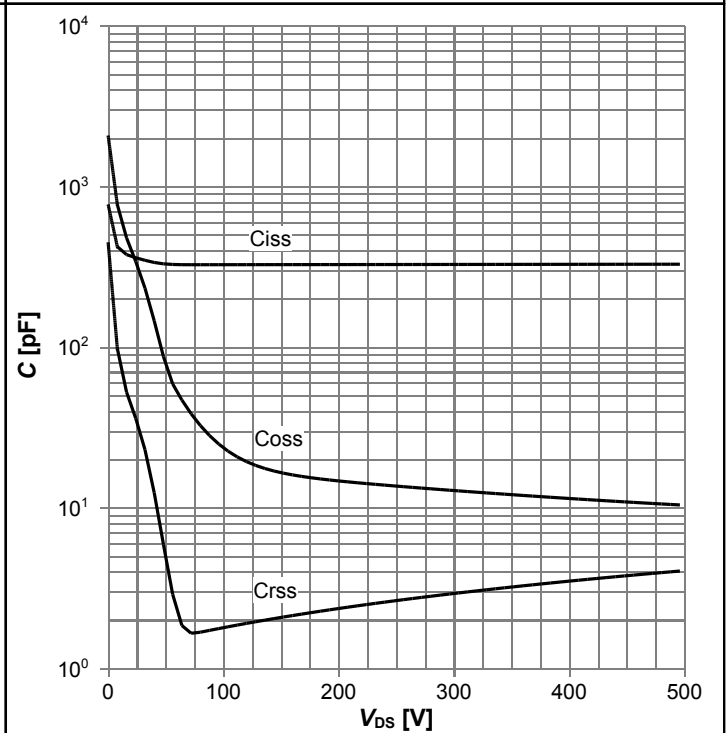
$I_D=f(V_{GS})$ ;  $V_{DS}=20$  V; parameter:  $T_j$

**Diagram 17: Typ. Coss stored energy**



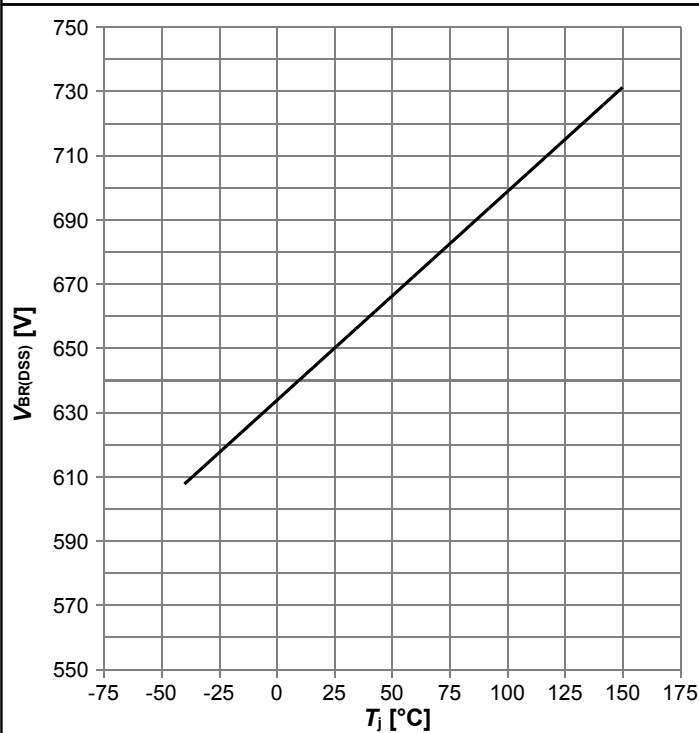
$E_{oss}=f(V_{Ds})$

**Diagram 18: Typ. capacitances**



$C=f(V_{Ds}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

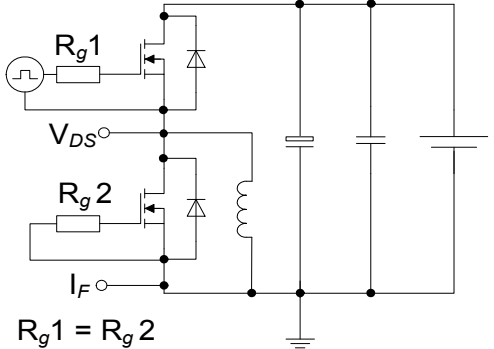
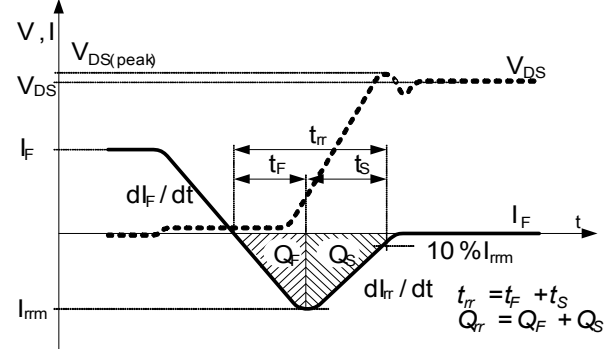
**Diagram 19: Drain-source breakdown voltage**



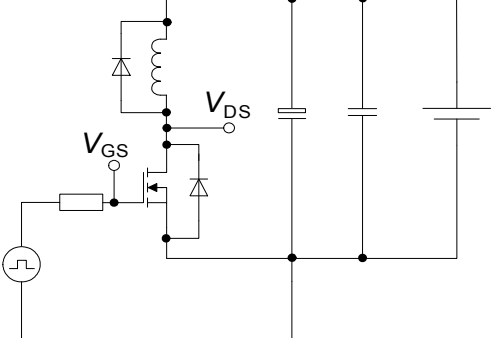
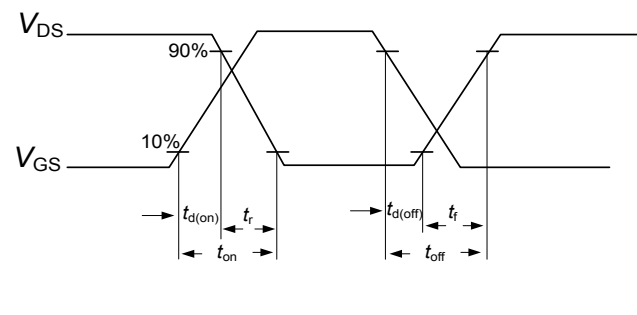
$V_{BR(DSS)}=f(T_j); I_D=1.0\text{ mA}$

## 5 Test Circuits

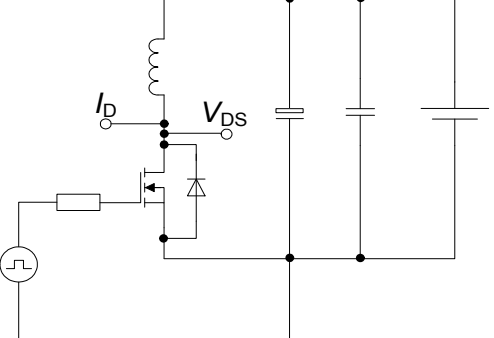
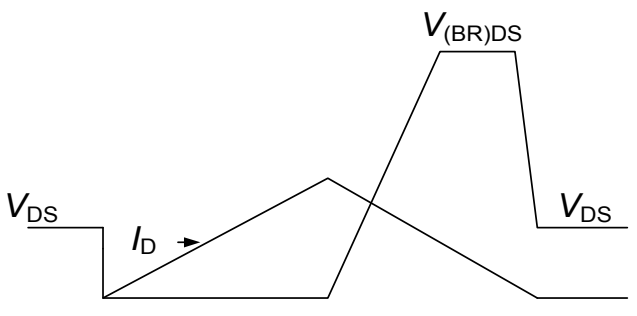
**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
 <p><math>R_{g1} = R_{g2}</math></p>	 <p><math>t_{tr} = t_F + t_S</math>  <math>Q_{tr} = Q_F + Q_S</math></p>

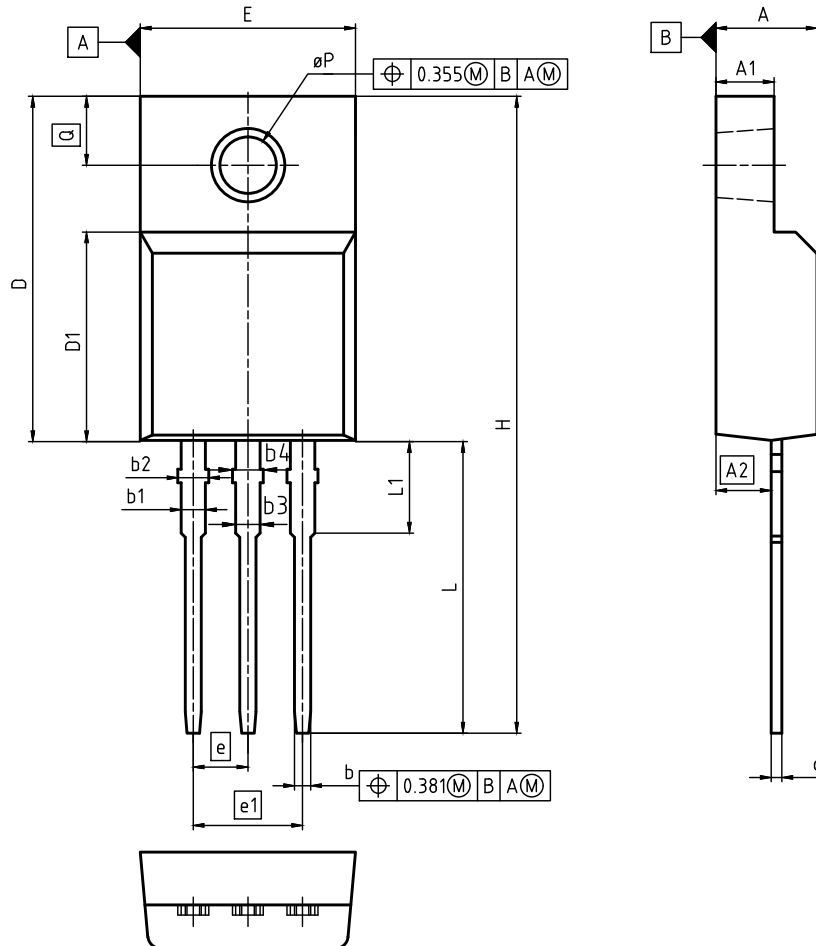
**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform
	

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform
	

## 6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

Dimensions do not include mold flash, protrusions or gate burrs

DOCUMENT NO.  
Z8B00003319

SCALE

EUROPEAN PROJECTION

ISSUE DATE  
05-05-2014

REVISION  
04

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

## 7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ CE application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ CE simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPA65R1K0CE

Revision: 2016-02-19, Rev. 2.0

### Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-02-19	Release of final version

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Trademarks updated August 2015

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