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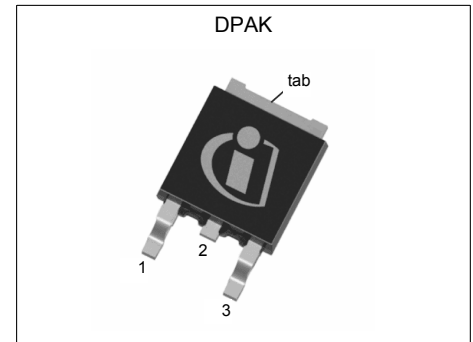
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## MOSFET

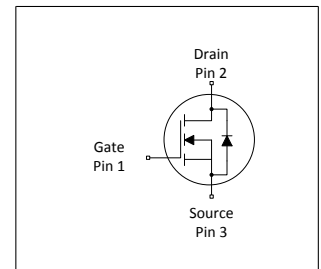
### 650V CoolMOS™ CFDA Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFDA series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter, and cooler.



### Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM  $R_{ds(on)} \cdot Q_g$  and  $E_{oss}$
- Easy to use/drive
- Qualified according to AEC Q101
- Green package (RoHS compliant), Pb-free plating, halogen free for mold compound



### Applications

650V CoolMOS™ CFDA is designed for switching applications.



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	650	V
$R_{DS(on),max}$	0.66	$\Omega$
$Q_g,typ$	20	nC
$I_D,pulse$	17	A
$E_{oss @ 400V}$	1.8	$\mu J$
Body diode $di/dt$	900	$A/\mu s$
$Q_{rr}$	0.2	$\mu C$
$t_{rr}$	65	ns
$I_{rrm}$	4.5	A



Type / Ordering Code	Package	Marking	Related Links
IPD65R660CFDA	PG-TO 252	65F660A	-

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**1 Maximum ratings**  
 at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$			6	A	$T_C = 25^\circ\text{C}$
				3.8		$T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$			17	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$			115	mJ	$I_D = 1.2\text{A}$ , $V_{DD} = 50\text{V}$ (see table 10)
Avalanche energy, repetitive	$E_{AR}$			0.21	mJ	$I_D = 1.2\text{A}$ , $V_{DD} = 50\text{V}$
Avalanche current, repetitive	$I_{AR}$			1.2	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	$V_{GS}$	-20		20	V	static
		-30		30		AC ( $f > 1\text{ Hz}$ )
Power dissipation (SMD) DPAK	$P_{tot}$			62.5	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	$T_j, T_{stg}$	-40		150	$^\circ\text{C}$	
Continuous diode forward current	$I_S$			6	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			17	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_D$ , $T_j = 25^\circ\text{C}$
Maximum diode commutation speed	$di_i/dt$			900	A/ $\mu\text{s}$	(see table 8)

<sup>1)</sup> Limited by  $T_{j,max}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

## 2 Thermal characteristics

**Table 3 Thermal characteristics DPAK**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$			2	K/W	
Thermal resistance, junction - ambient <sup>1)</sup>	$R_{thJA}$			62	K/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm <sup>2</sup> cooling area
Soldering temperature, wave- & reflowsoldering allowed	$T_{sold}$			260	°C	reflow MSL

<sup>1)</sup> Device on 40mm\*40mm\*1.5mm one layer epoxy PCB FR4 with 6cm<sup>2</sup> copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

### 3 Electrical characteristics

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage <sup>1)</sup>	$V_{(BR)DSS}$	650			V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	$V_{DS} = V_{GS}, I_D = 0.2mA$
Zero gate voltage drain current	$I_{DSS}$			1	$\mu A$	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ C$
			100			$V_{DS} = 650V, V_{GS} = 0V, T_j = 150^\circ C$
Gate-source leakage current	$I_{GSS}$			100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		0.594	0.66	$\Omega$	$V_{GS} = 10V, I_D = 3.2A, T_j = 25^\circ C$
			1.54			$V_{GS} = 10V, I_D = 3.2A, T_j = 150^\circ C$
Gate resistance	$R_G$		6.5		$\Omega$	$f = 1MHz, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$		543		pF	$V_{GS} = 0V, V_{DS} = 100V, f = 1MHz$
Output capacitance	$C_{oss}$		32		pF	
Effective output capacitance, energy related <sup>2)</sup>	$C_{o(er)}$		24		pF	$V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Effective output capacitance, time related <sup>3)</sup>	$C_{o(tr)}$		97		pF	$I_D = \text{constant}, V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Turn-on delay time	$t_{d(on)}$		9		ns	$V_{DD} = 400V, V_{GS} = 13V, I_D = 3.2A, R_G = 6.8\Omega$ (see table 9)
Rise time	$t_r$		8		ns	
Turn-off delay time	$t_{d(off)}$		40		ns	
Fall time	$t_f$		10		ns	

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$		3.5		nC	$V_{DD} = 480V, I_D = 3.2A, V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$		11		nC	
Gate charge total	$Q_g$		20		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

<sup>1)</sup> For applications with applied blocking voltage > 65% of the specified blocking voltage, we recommend to evaluate the impact of the cosmic radiation effect in early design phase. For assessment please contact local Infineon sales office.

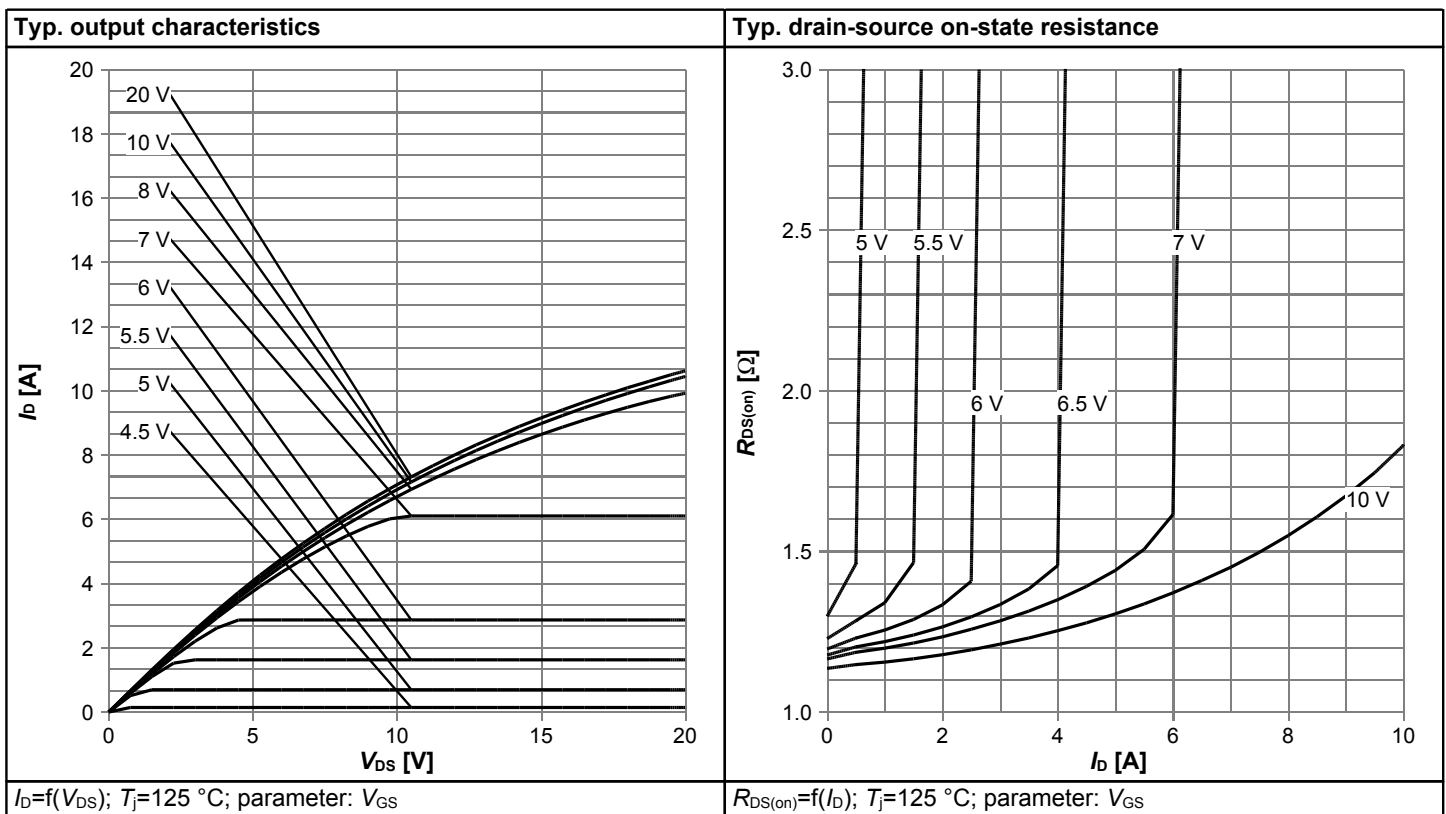
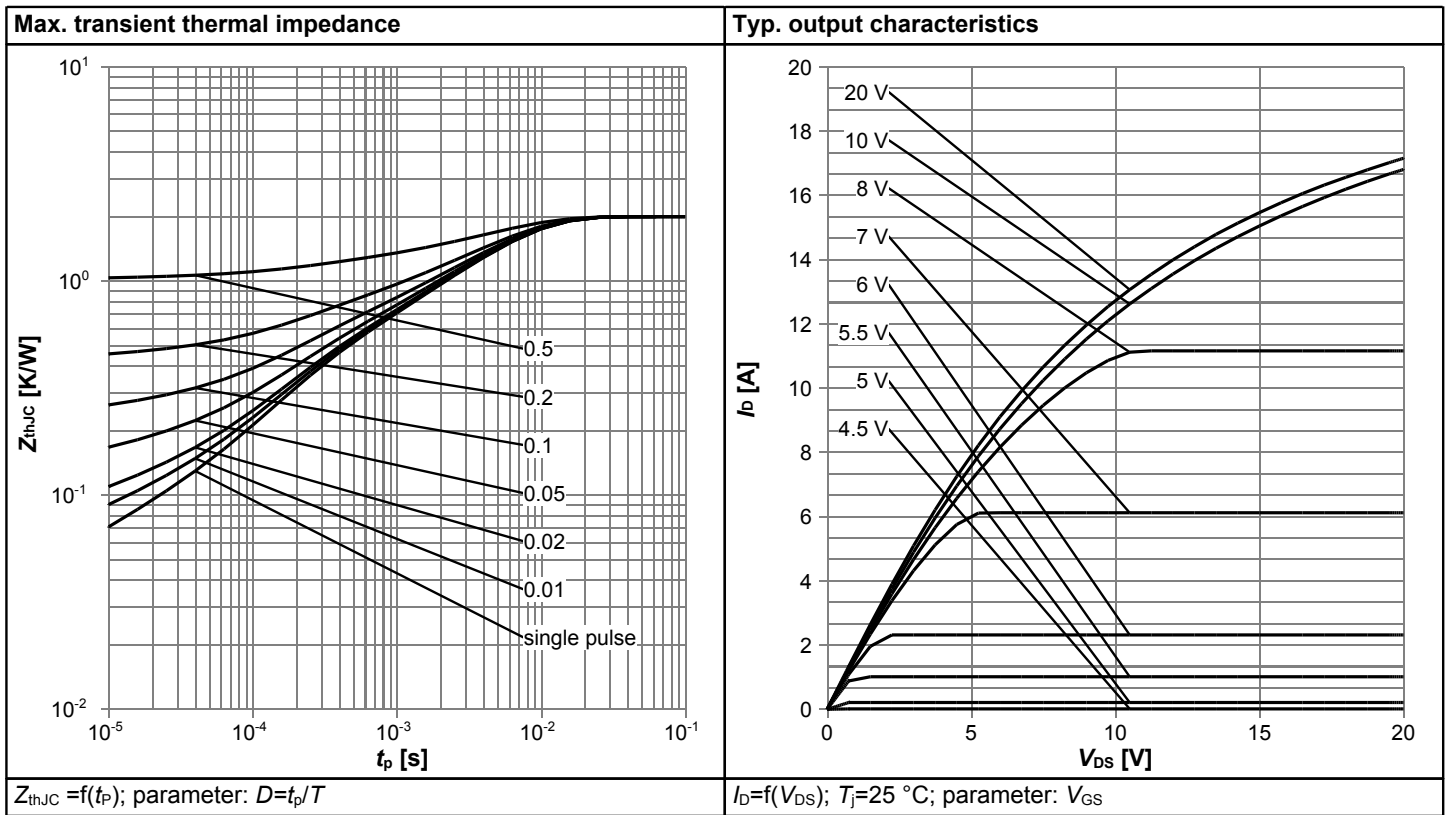
<sup>2)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>3)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$		0.9		V	$V_{GS} = 0V, I_F = 3.2A, T_j = 25^\circ C$
Reverse recovery time	$t_{rr}$		65		ns	$V_R = 400V, I_F = 3.2A,$ $di_F/dt = 100A/\mu s$ (see table 8)
Reverse recovery charge	$Q_{rr}$		0.2		$\mu C$	
Peak reverse recovery current	$I_{rrm}$		4.5		A	

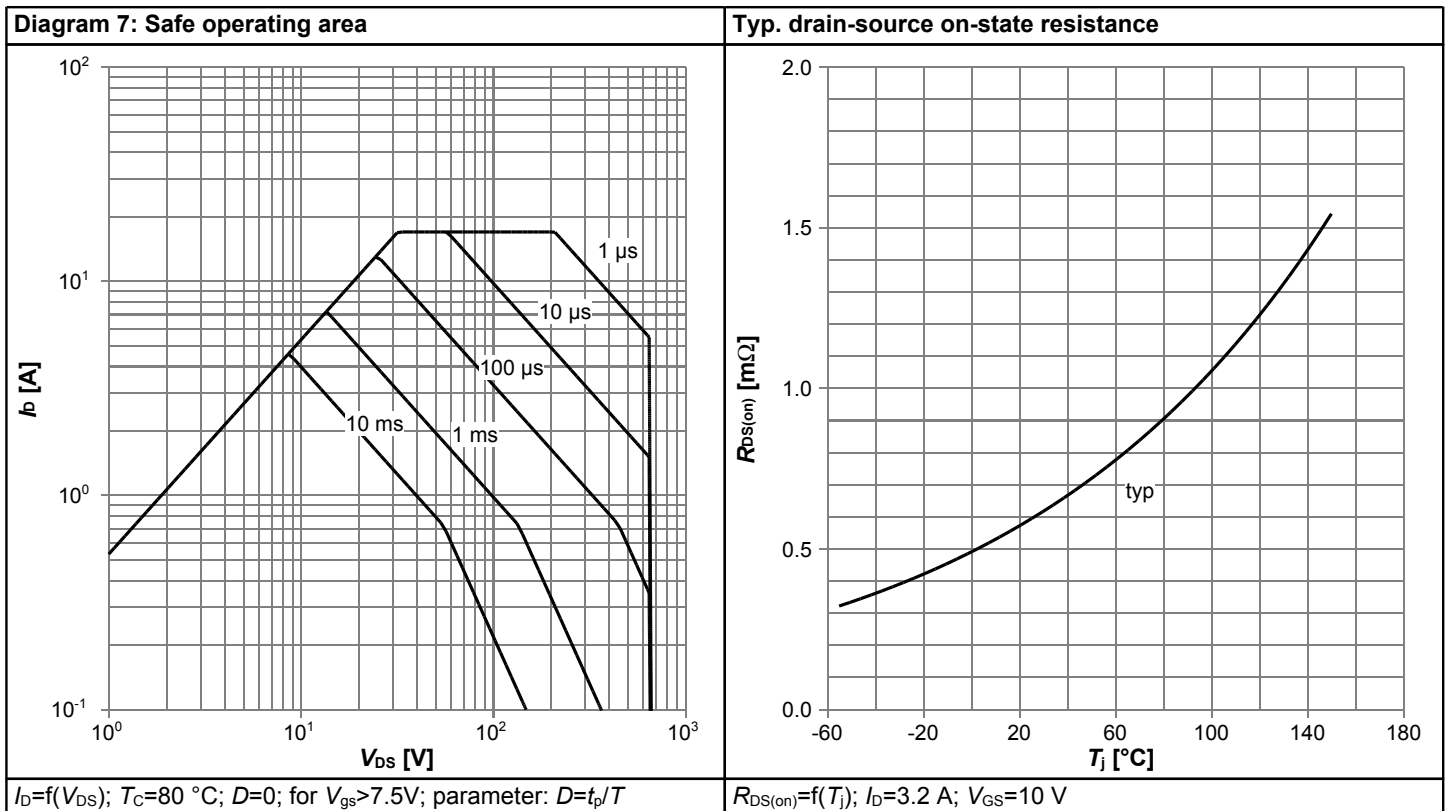
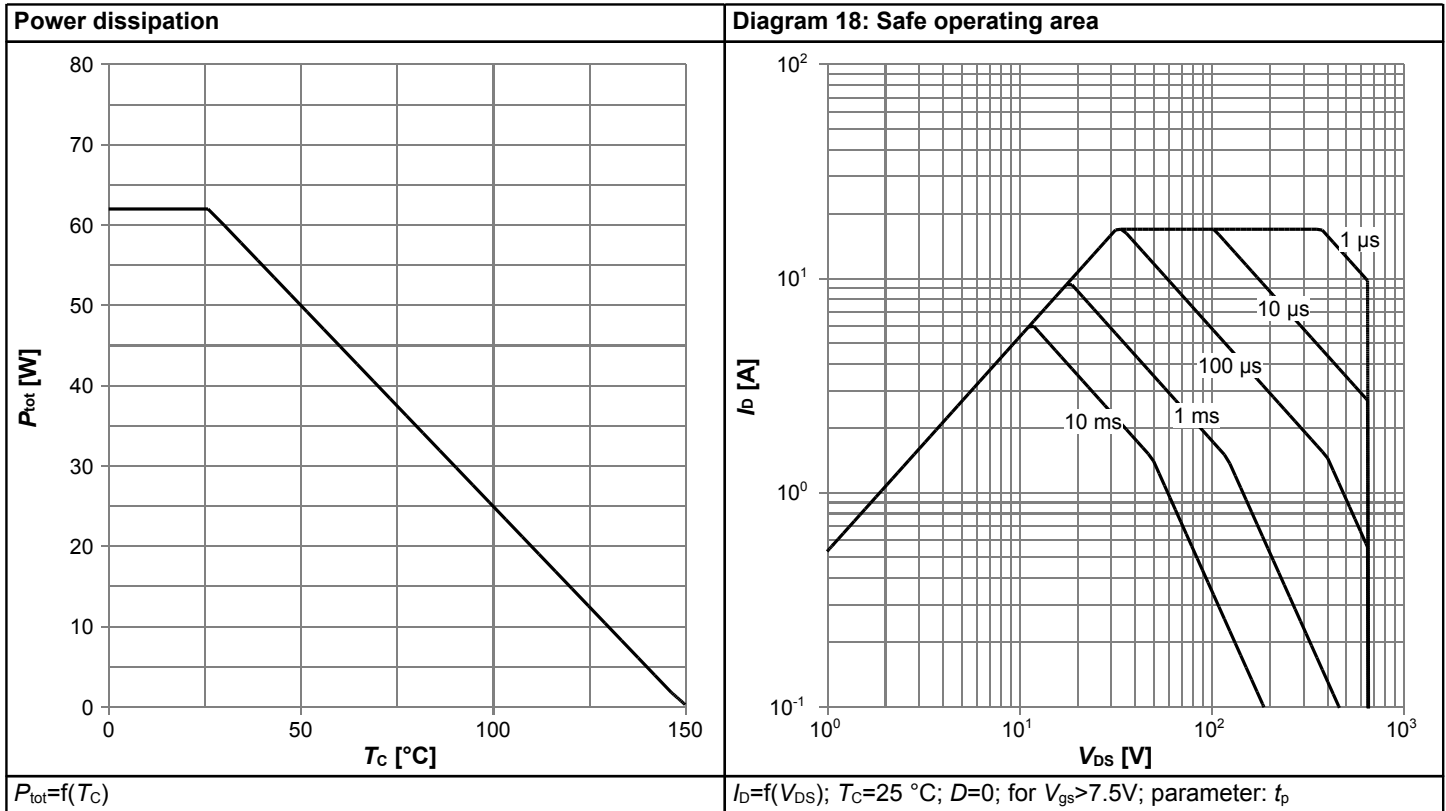
### 4 Electrical characteristics diagrams



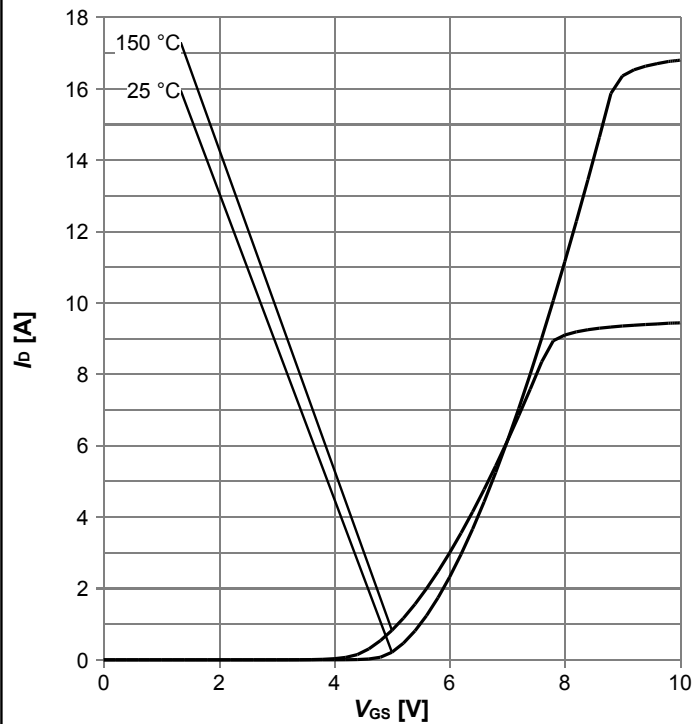


# 650V CoolMOS™ CFDA Power Transistor

## IPD65R660CFDA

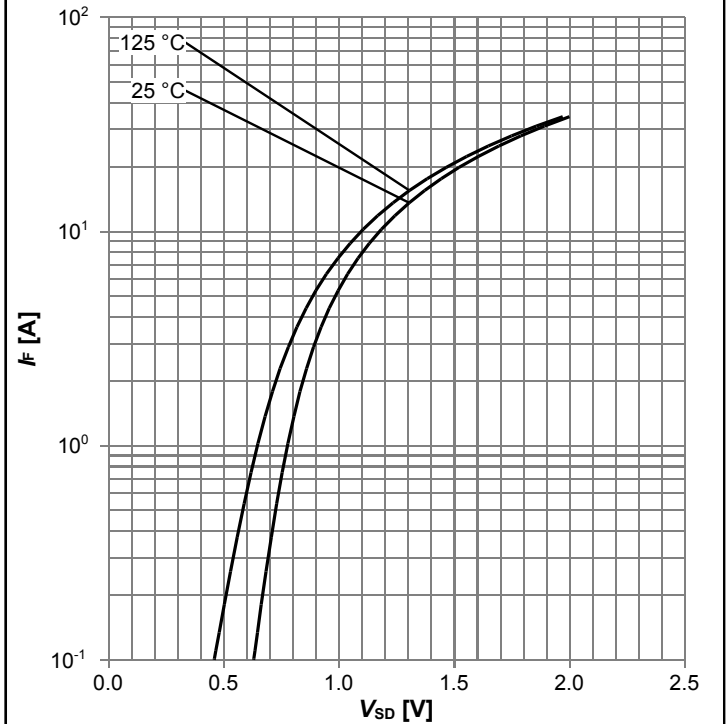


**Typ. transfer characteristics**



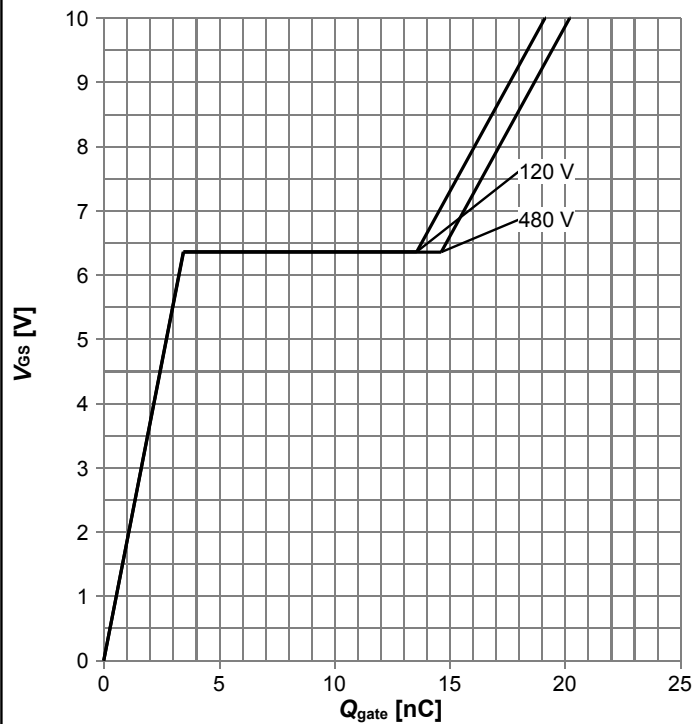
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

**Typ. forward characteristics of reverse diode**



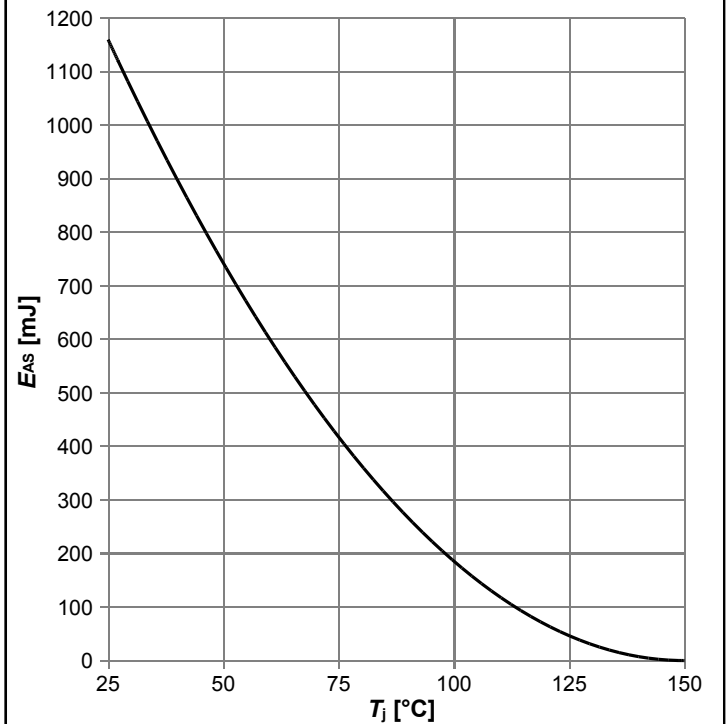
$I_F = f(V_{SD});$  parameter:  $T_j$

**Typ. gate charge**



$V_{GS} = f(Q_{gate}); I_D = 19.2$  A pulsed; parameter:  $V_{DD}$

**Avalanche energy**

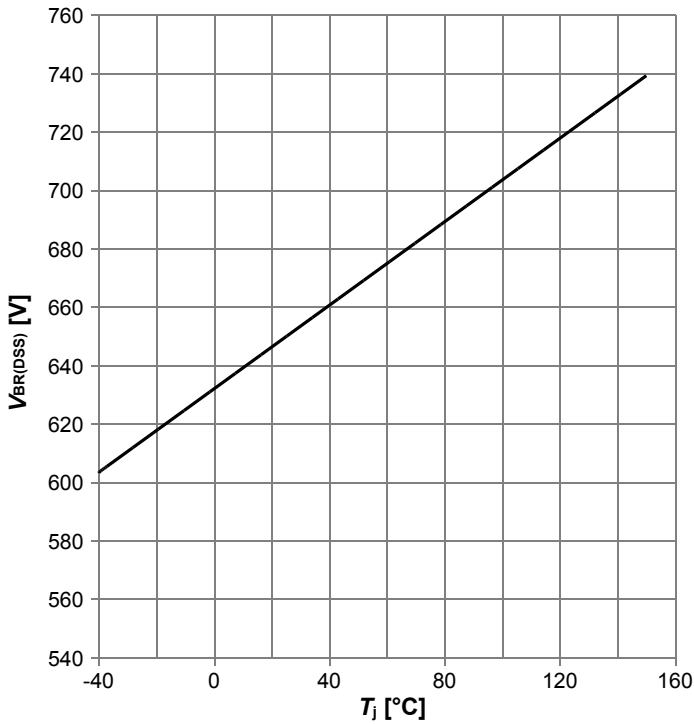


$E_{AS} = f(T_j); I_D = 6.6$  A;  $V_{DD} = 50$  V

# 650V CoolMOS™ CFDA Power Transistor

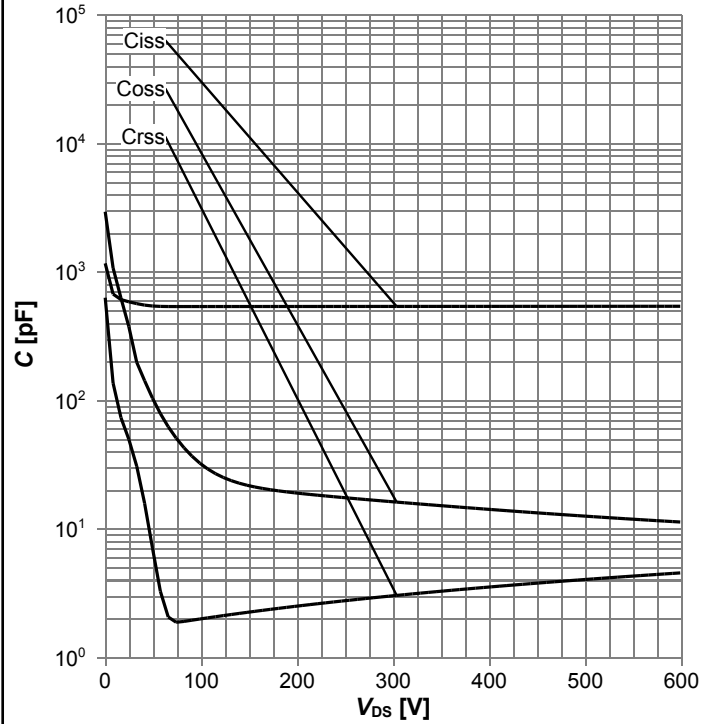
## IPD65R660CFDA

**Drain-source breakdown voltage**



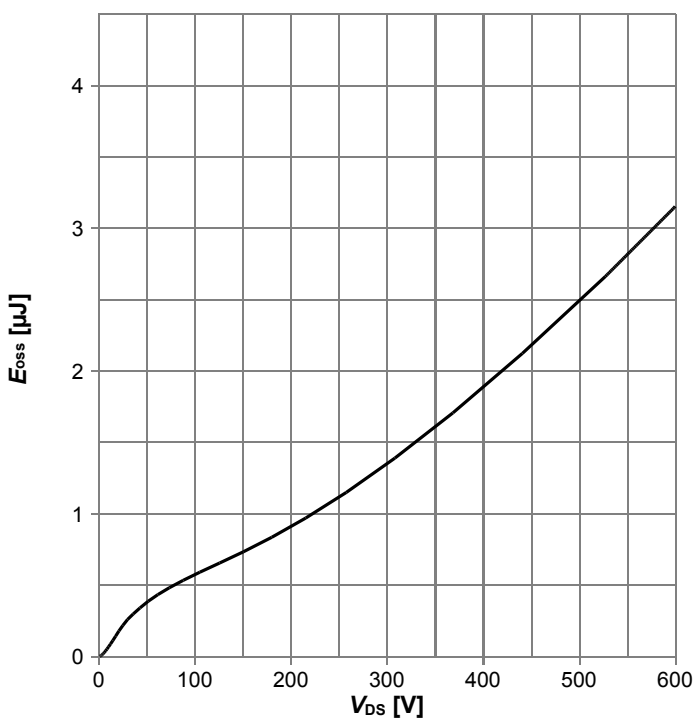
$V_{BR(DSS)} = f(T_j); I_D = 0.25 \text{ mA}$

**Typ. capacitances**



$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Typ. Coss stored energy**



$E_{oss} = f(V_{DS})$

## 5 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
<p><math>R_{g1} = R_{g2}</math></p>	<p><math>t_{rr} = t_F + t_S</math>  <math>Q_{rr} = Q_F + Q_S</math></p>

**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform

6 Package Outlines

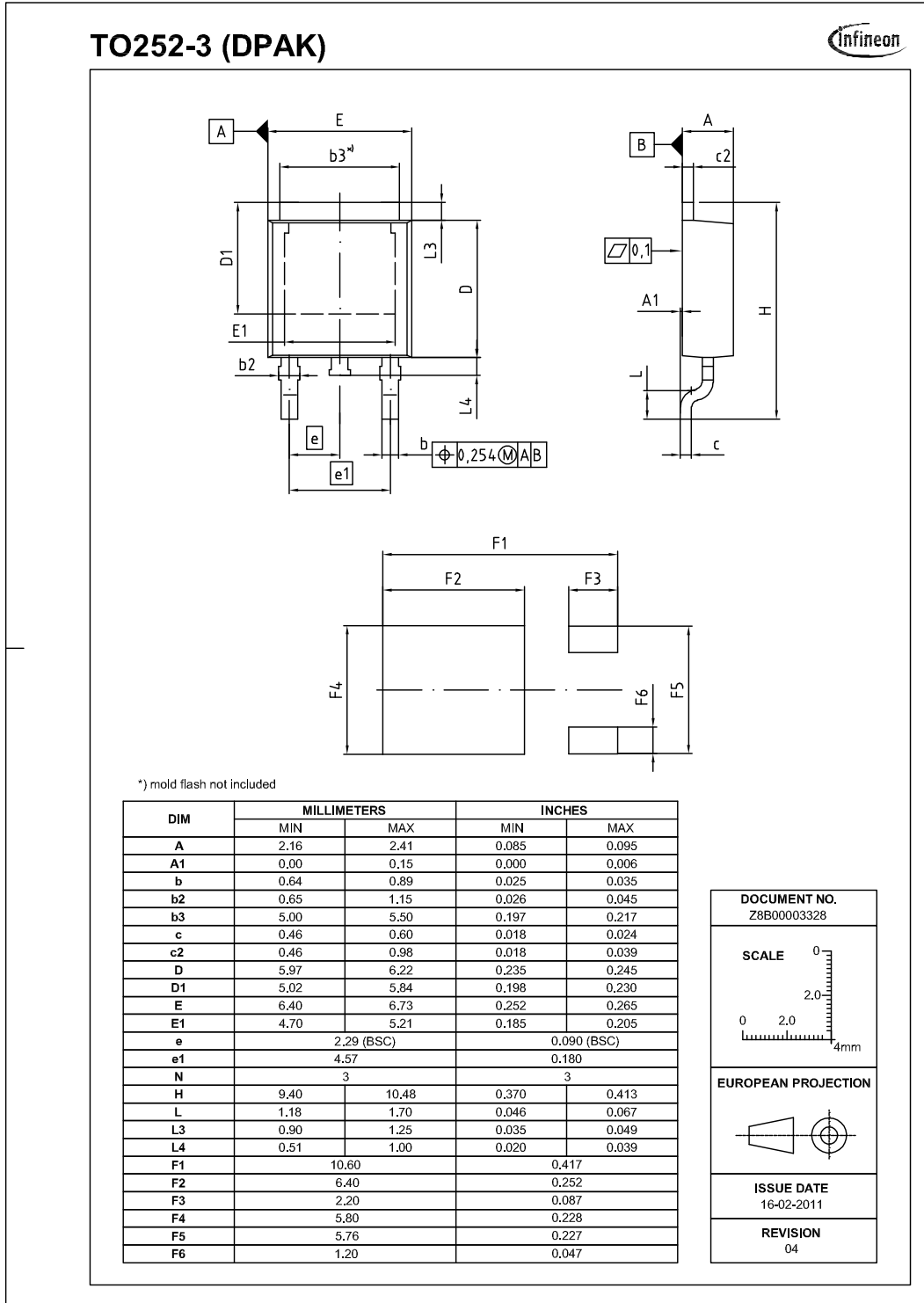


Figure 1 Outline PG-TO 252, dimensions in mm/inches

## Revision History

IPD65R660CFDA

**Revision: 2016-04-18, Rev. 2.2**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2012-07-12	Preliminary
2.1	2014-11-19	Correction of Marking Code
2.2	2016-04-18	Updated: SOA diagrams, Idss at 150C, Rdson vs. Tj.

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