



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



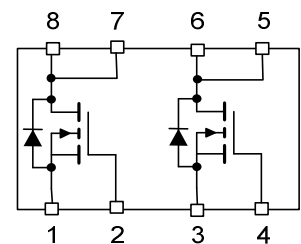
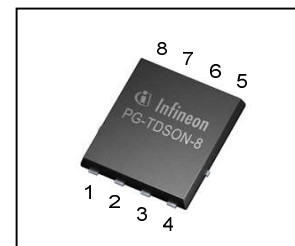
OptiMOS™-T2 Power-Transistor

Features

- Dual N-channel Normal Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	60	V
$R_{DS(on),max}^{4)}$	15.5	mΩ
I_D	20	A

PG-TDSON-8-4


Type	Package	Marking
IPG20N06S4-15	PG-TDSON-8-4	4N0615

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	20	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	20	
Pulsed drain current ²⁾ one channel active	$I_{D,pulse}$	-	80	
Avalanche energy, single pulse ^{2, 4)}	E_{AS}	$I_D=10\text{ A}$	90	mJ
Avalanche current, single pulse ⁴⁾	I_{AS}	-	15	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation one channel active	P_{tot}	$T_C=25\text{ °C}$	50	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	3	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm ² cooling area ³⁾	-	60	-	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=20\text{ }\mu\text{A}$	2.0	3.0	4.0	
Zero gate voltage drain current ⁴⁾	I_{DSS}	$V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	5	100	
Gate-source leakage current ⁴⁾	I_{GSS}	$V_{GS}=16\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance ⁴⁾	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=17\text{ A}$	-	12.9	15.5	m Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance ⁴⁾	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	1740	2260	pF
Output capacitance ⁴⁾	C_{oss}		-	430	560	
Reverse transfer capacitance ⁴⁾	C_{rss}		-	19	38	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=11\ \Omega$	-	12	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	17	-	
Fall time	t_f		-	9	-	

Gate Charge Characteristics^{2, 4)}

Gate to source charge	Q_{gs}	$V_{DD}=48\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	9	12	nC
Gate to drain charge	Q_{gd}		-	2.2	4.4	
Gate charge total	Q_g		-	22	29	
Gate plateau voltage	$V_{plateau}$		-	5.3	-	V

Reverse Diode

Diode continuous forward current ²⁾ one channel active	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	20	A
Diode pulse current ²⁾ one channel active	$I_{S,pulse}$		-	-	80	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=17\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.95	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=30\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	35	-	ns
Reverse recovery charge ^{2, 4)}	Q_{rr}		-	35	-	nC

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 3\text{K/W}$ the chip is able to carry 43A at 25°C.

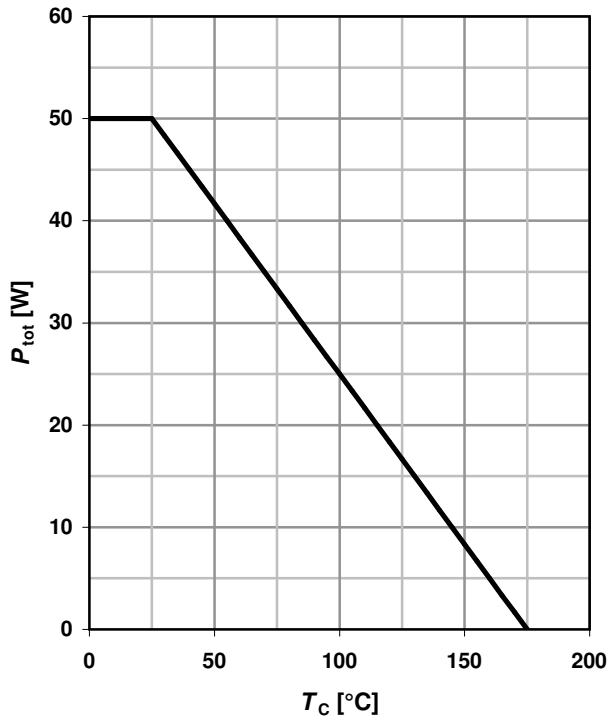
²⁾ Specified by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁴⁾ Per channel

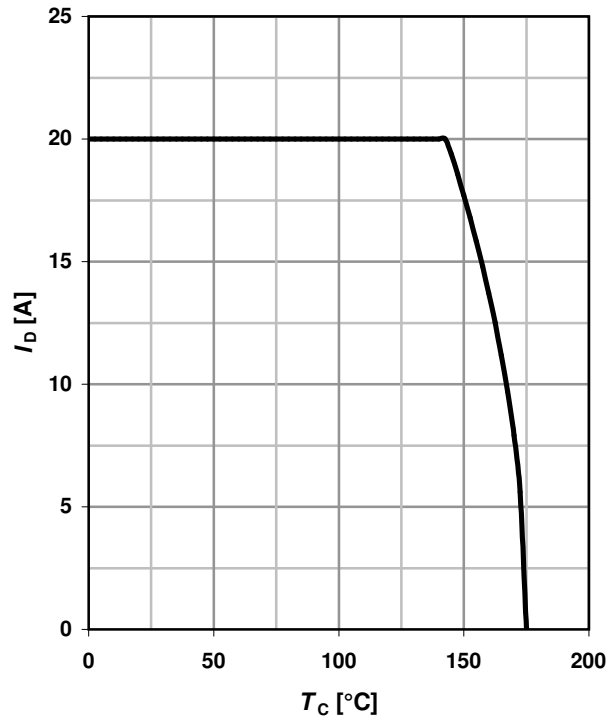
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6\text{ V}$; one channel active



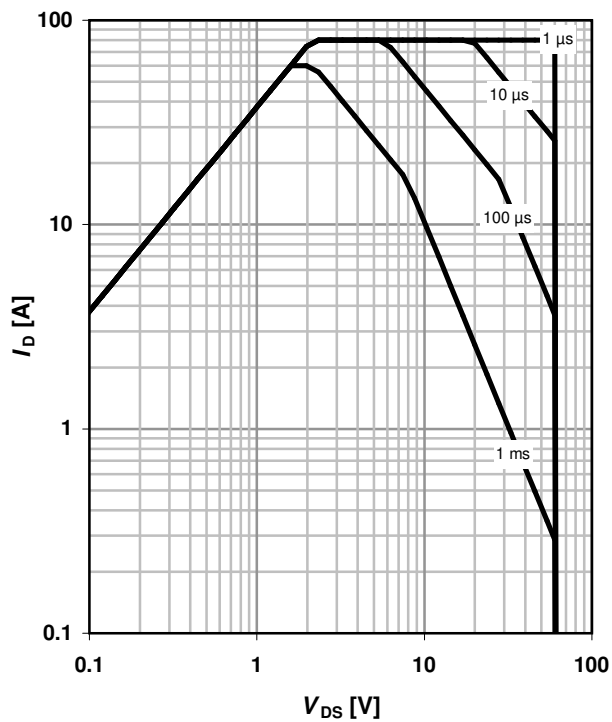
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6\text{ V}$; one channel active



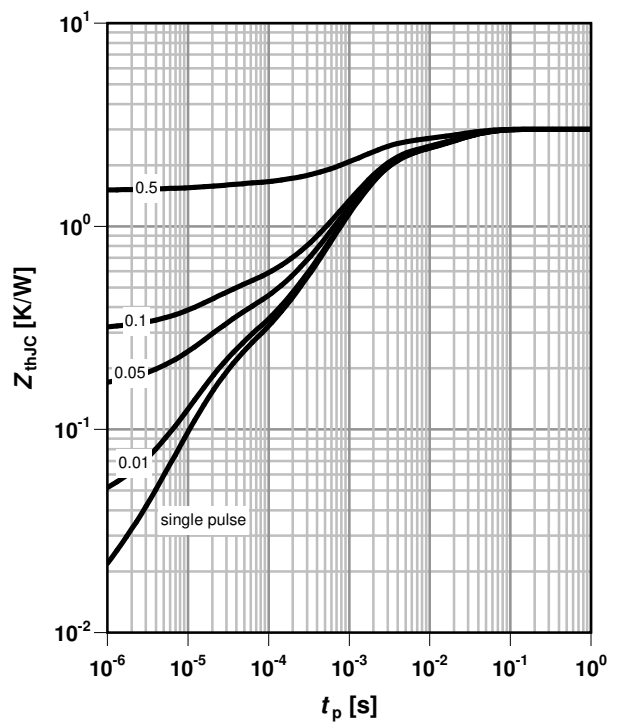
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25^\circ\text{C}$; $D = 0$; one channel active
parameter: t_p



4 Max. transient thermal impedance

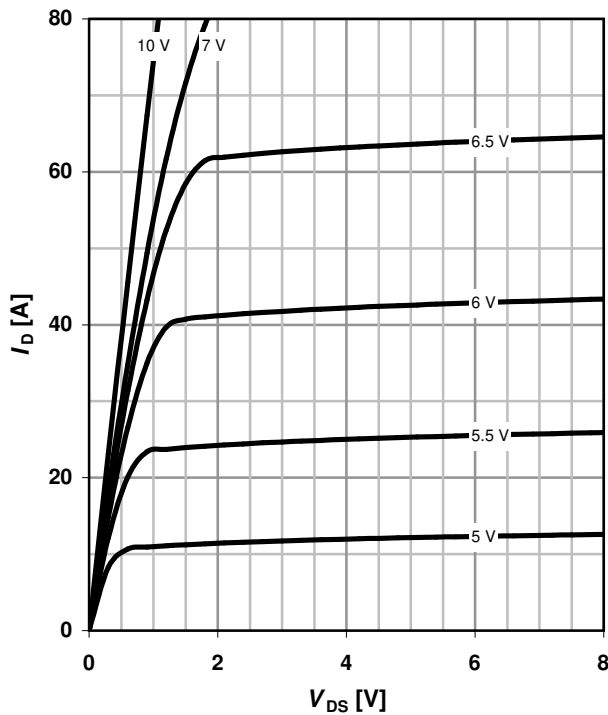
$Z_{thJC} = f(t_p)$
parameter: $D = t_p/T$



5 Typ. output characteristics⁴⁾

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

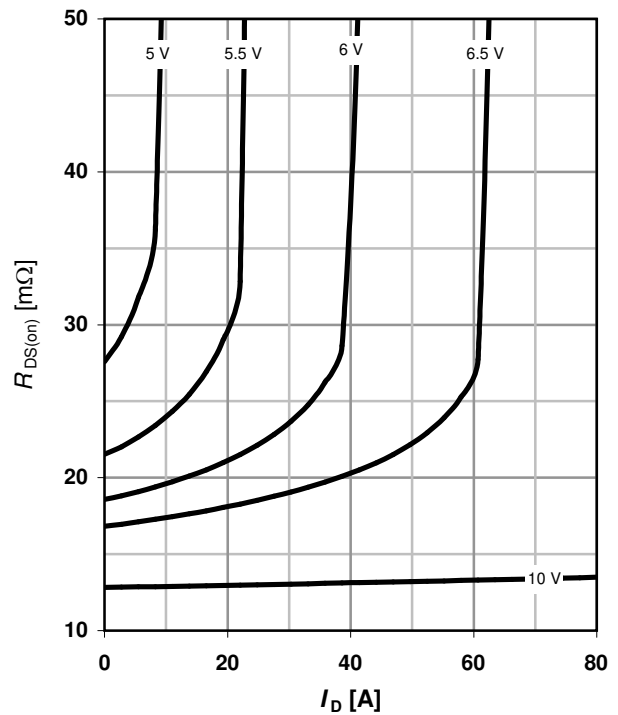
parameter: V_{GS}



6 Typ. drain-source on-state resistance⁴⁾

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

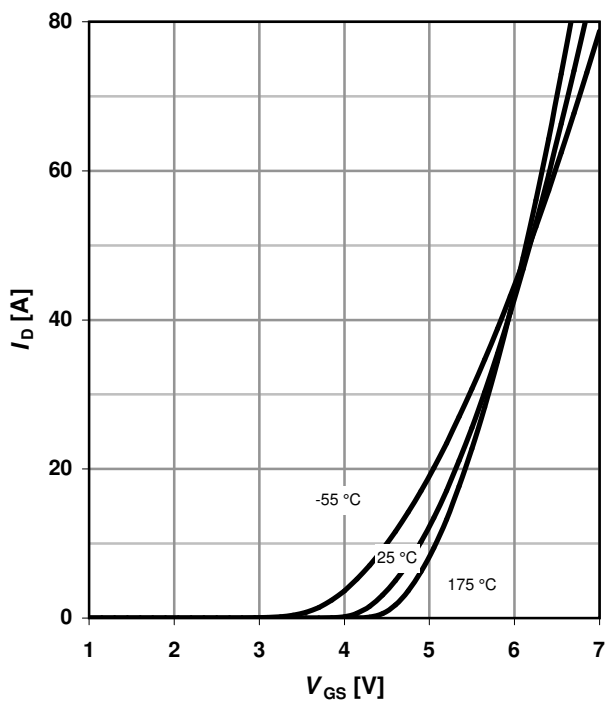
parameter: V_{GS}



7 Typ. transfer characteristics⁴⁾

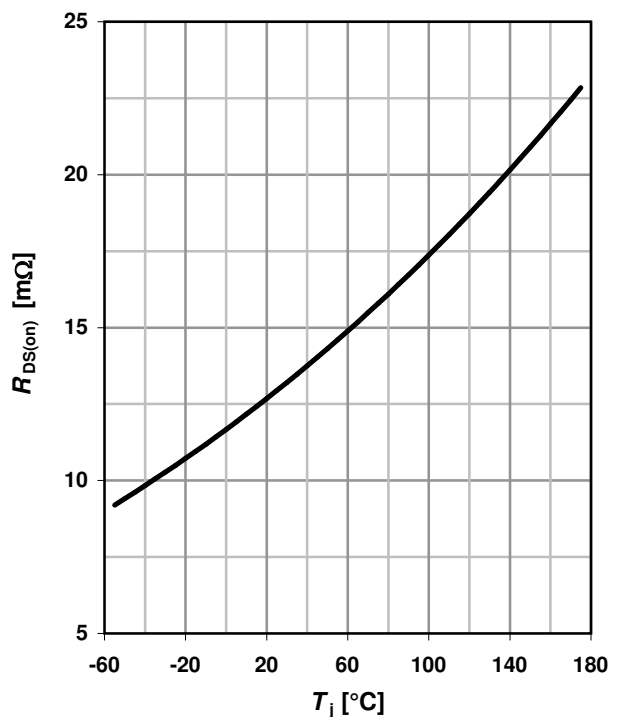
$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j



8 Typ. drain-source on-state resistance⁴⁾

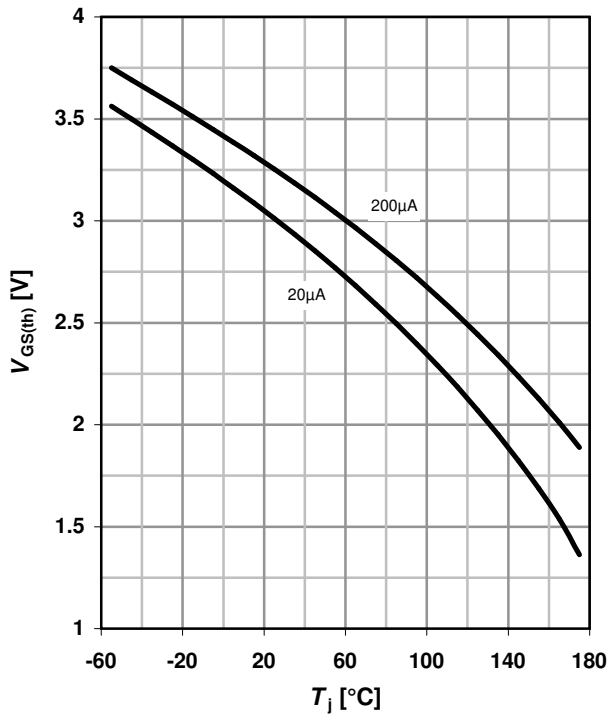
$R_{DS(on)} = f(T_j); I_D = 17\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

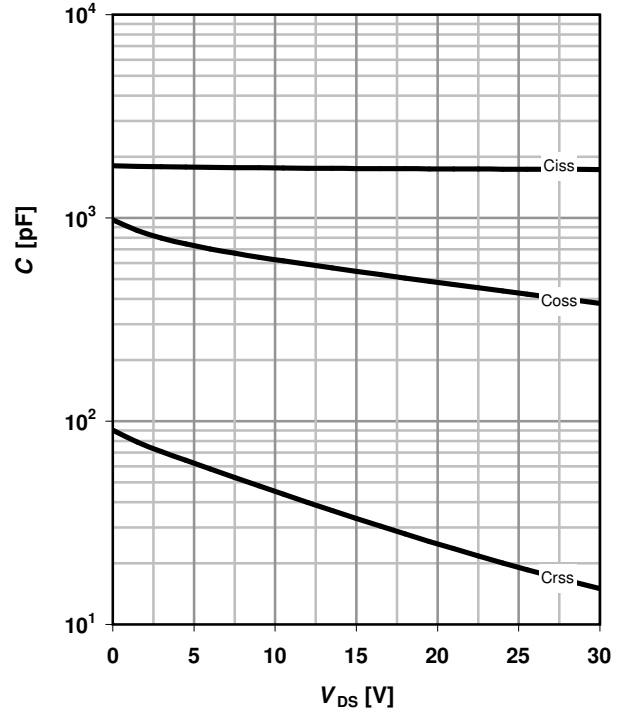
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. Capacitances⁴⁾

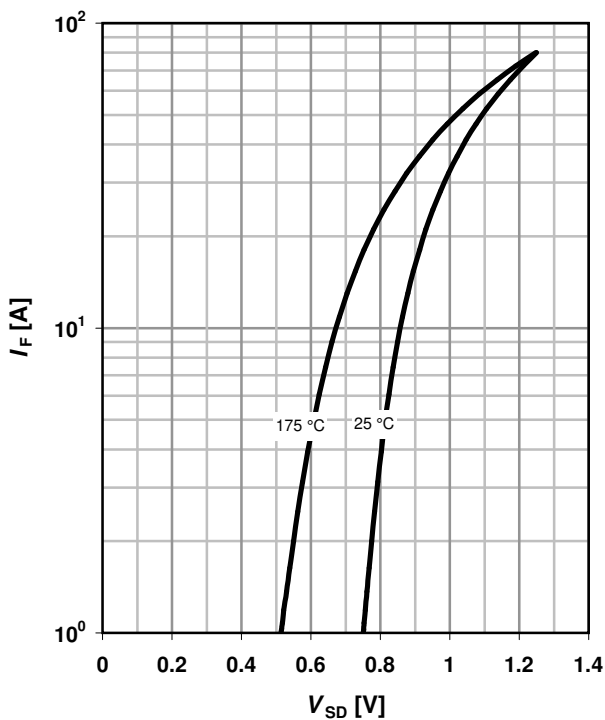
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



11 Typical forward diode characteristics⁴⁾

$I_F = f(V_{SD})$

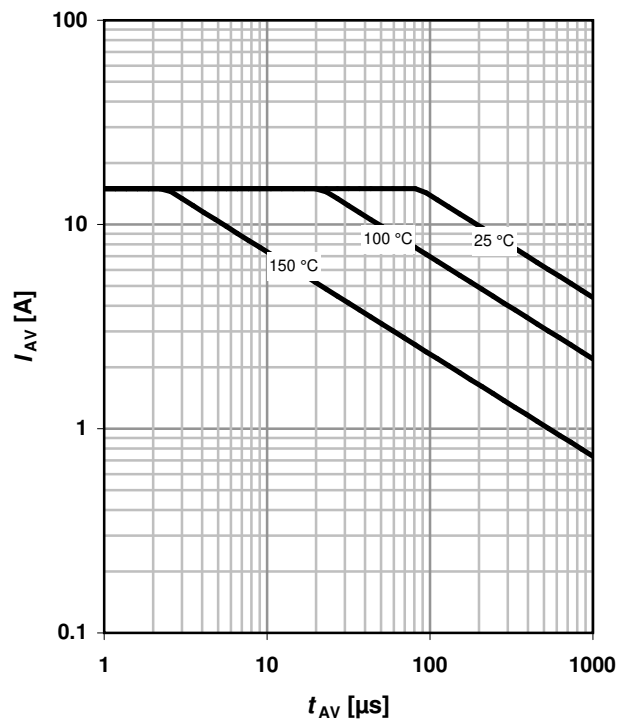
parameter: T_j



12 Avalanche characteristics⁴⁾

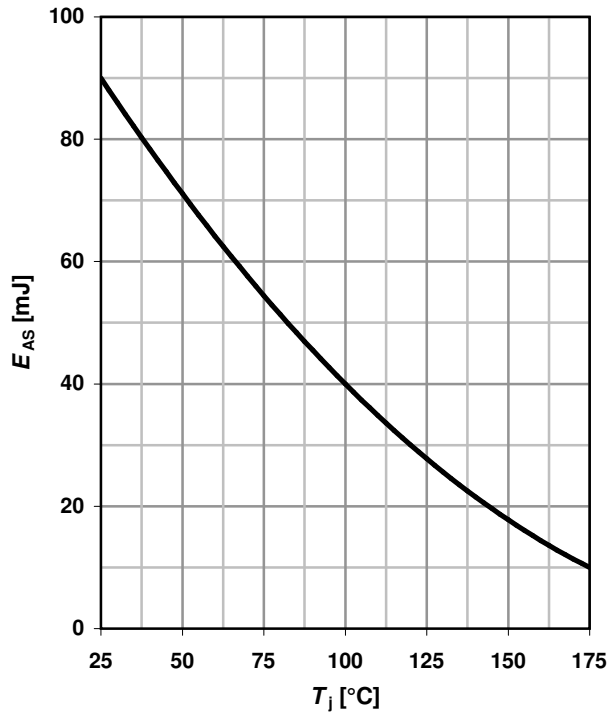
$I_{AS} = f(t_{AV})$

parameter: $T_{j(start)}$



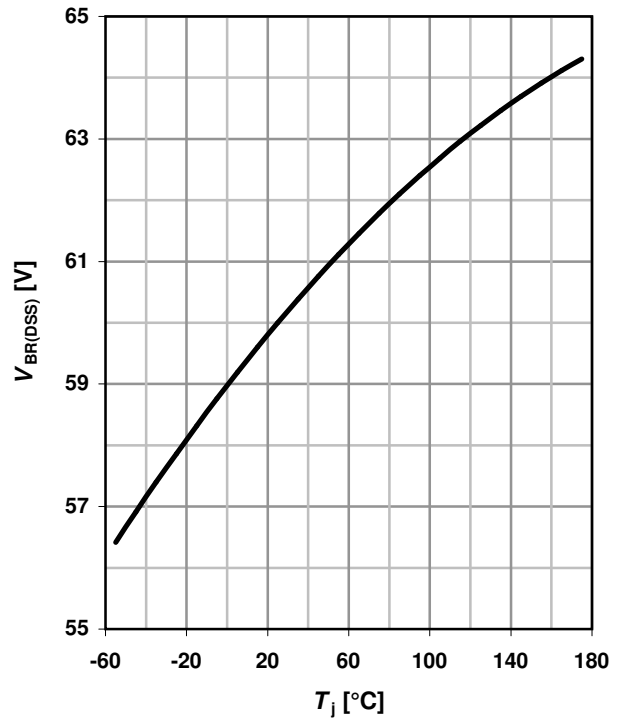
13 Avalanche energy⁴⁾

$E_{AS} = f(T_j), I_D = 10A$



14 Drain-source breakdown voltage

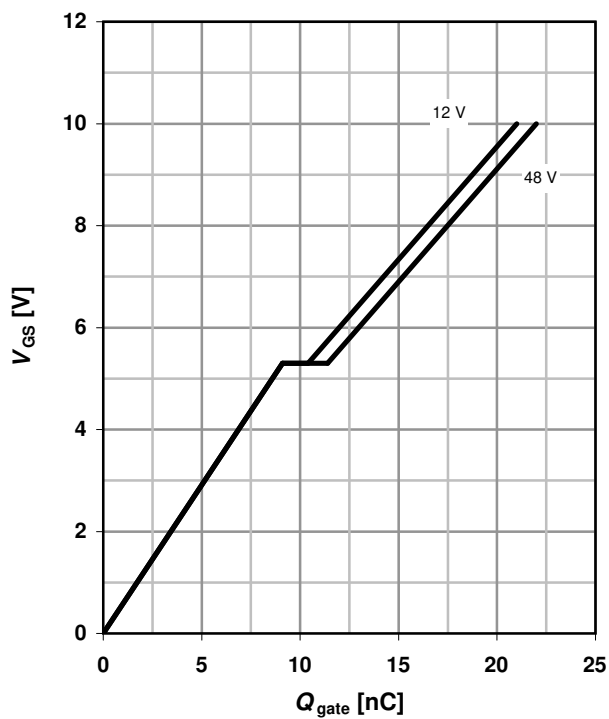
$V_{BR(DSS)} = f(T_j); I_D = 1 mA$



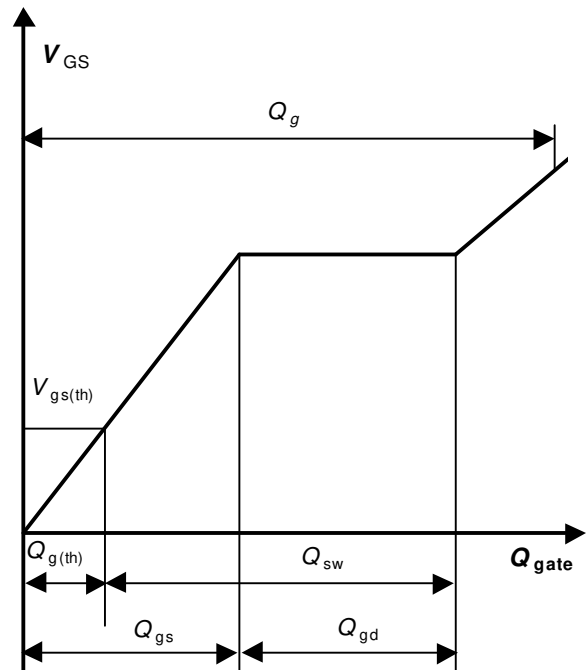
15 Typ. gate charge⁴⁾

$V_{GS} = f(Q_{gate}); I_D = 20 A$ pulsed

parameter: V_{DD}



16 Gate charge waveforms



Published by
Infineon Technologies AG
81726 Munich, Germany

© Infineon Technologies AG 2010
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances.
For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life.
If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	05.10.2010	Data Sheet revision 1.0