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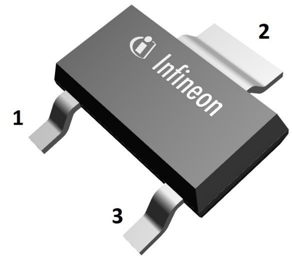
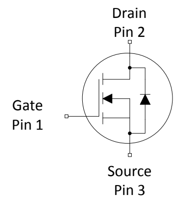
# MOSFET

## 600V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

PG-SOT223




### Features

• Extremely low losses due to very low FOM Rdson*Qg and Eoss
• Very high commutation ruggedness
• Easy to use/drive
• Pb-free plating, Halogen free mold compound
• Qualified for standard grade applications

### Applications

Adapter, Charger and Lighting

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or seperate totem poles is generally recommended.*

### Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ @ $T_{j,max}$ | 650 | V |
| $R_{DS(on),max}$ | 2.1 | Ω |
| $Q_{g,typ}$ | 6.7 | nC |
| $I_{D,pulse}$ | 5.9 | A |
| $E_{oss}$@400V | 0.76 | µJ |
| Body diode di/dt | 500 | A/µs |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| IPN60R2K1CE | PG-SOT223 | 60S2K1 | see Appendix A |

## Table of Contents

# 1 Maximum ratings

at $T_j$ = 25°C, unless otherwise specified

### Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current[1)] | $I_D$ | -<br>- | -<br>- | 3.7<br>2.4 | A | $T_C$ = 25°C<br>$T_C$ = 100°C |
| Pulsed drain current[2)] | $I_{D,pulse}$ | - | - | 5.9 | A | $T_C$ = 25°C |
| Avalanche energy, single pulse | $E_{AS}$ | - | - | 11 | mJ | $I_D$ = 0.4A; $V_{DD}$ = 50V |
| Avalanche energy, repetitive | $E_{AR}$ | - | - | 0.06 | mJ | $I_D$ = 0.4A; $V_{DD}$ = 50V |
| Avalanche current, repetitive | $I_{AR}$ | - | - | 0.4 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 50 | V/ns | $V_{DS}$ = 0...480V |
| Gate source voltage | $V_{GS}$ | -20<br>-30 | -<br>- | 20<br>30 | V | static;<br>AC (f>1 Hz) |
| Power dissipation | $P_{tot}$ | - | - | 5.0 | W | $T_C$ = 25°C |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -40 | - | 150 | °C | - |
| Continuous diode forward current | $I_S$ | - | - | 1.0 | A | $T_C$ = 25°C |
| Diode pulse current[2)] | $I_{S,pulse}$ | - | - | 5.9 | A | $T_C$ = 25°C |
| Reverse diode dv/dt[3)] | dv/dt | - | - | 15 | V/ns | $V_{DS}$ = 0...400V, $I_{SD}$<=$I_S$, $T_j$=25°C |
| Maximum diode commutation speed[3)] | $di_f/dt$ | - | - | 500 | A/µs | $V_{DS}$ = 0...400V, $I_{SD}$<=$I_S$, $T_j$=25°C |

# 2 Thermal characteristics

### Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - solder point | $R_{thJS}$ | - | - | 24.7 | °C/W | - |
| Thermal resistance, junction - ambient for minimal footprint | $R_{thJA}$ | - | - | 160 | °C/W | minimal footprint |
| Thermal resistance, junction - ambient soldered on copper area | $R_{thJA}$ | - | - | 75 | °C/W | Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm$^2$ (one layer 70µm thick) copper area for drain connection and cooling. PCB is vertical without blown air. |
| Soldering temperature, wavesoldering only allowed at leads | $T_{sold}$ | - | - | 260 | °C | reflow MSL3 |

1) DPAK equivalent. Limited by $T_{j\,max}$. Maximum duty cycle D=0.5
2) Pulse width $t_p$ limited by $T_{j,max}$
3) $V_{DClink}$=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical $R_G$

# 3 Electrical characteristics

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 600 | - | - | V | $V_{GS}$=0V, $I_D$=0.25mA |
| Gate threshold voltage | $V_{GS(th)}$ | 2.50 | 3 | 3.50 | V | $V_{DS}$=$V_{GS}$, $I_D$=0.06mA |
| Zero gate voltage drain current | $I_{DSS}$ | -<br>- | -<br>10 | 1<br>- | µA | $V_{DS}$=600V, $V_{GS}$=0V, $T_j$=25°C<br>$V_{DS}$=600V, $V_{GS}$=0V, $T_j$=150°C |
| Gate-source leakage curent | $I_{GSS}$ | - | - | 100 | nA | $V_{GS}$=20V, $V_{DS}$=0V |
| Drain-source on-state resistance | $R_{DS(on)}$ | -<br>- | 1.89<br>4.91 | 2.10<br>- | Ω | $V_{GS}$=10V, $I_D$=0.8A, $T_j$=25°C<br>$V_{GS}$=10V, $I_D$=0.8A, $T_j$=150°C |
| Gate resistance | $R_G$ | - | 12 | - | Ω | $f$=1 MHz, open drain |

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 140 | - | pF | $V_{GS}$=0V, $V_{DS}$=100V, $f$=1MHz |
| Output capacitance | $C_{oss}$ | - | 12 | - | pF | $V_{GS}$=0V, $V_{DS}$=100V, $f$=1MHz |
| Effective output capacitance, energy related[1)] | $C_{o(er)}$ | - | 8.5 | - | pF | $V_{GS}$=0V, $V_{DS}$=0...480V |
| Effective output capacitance, time related[2)] | $C_{o(tr)}$ | - | 29.6 | - | pF | $I_D$=constant, $V_{GS}$=0V, $V_{DS}$=0...480V |
| Turn-on delay time | $t_{d(on)}$ | - | 7 | - | ns | $V_{DD}$=400V, $V_{GS}$=13V, $I_D$=0.9A, $R_G$=12.2Ω |
| Rise time | $t_r$ | - | 7 | - | ns | $V_{DD}$=400V, $V_{GS}$=13V, $I_D$=0.9A, $R_G$=12.2Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 30 | - | ns | $V_{DD}$=400V, $V_{GS}$=13V, $I_D$=0.9A, $R_G$=12.2Ω |
| Fall time | $t_f$ | - | 50 | - | ns | $V_{DD}$=400V, $V_{GS}$=13V, $I_D$=0.9A, $R_G$=12.2Ω |

## Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 0.8 | - | nC | $V_{DD}$=480V, $I_D$=0.9A, $V_{GS}$=0 to 10V |
| Gate to drain charge | $Q_{gd}$ | - | 3.6 | - | nC | $V_{DD}$=480V, $I_D$=0.9A, $V_{GS}$=0 to 10V |
| Gate charge total | $Q_g$ | - | 6.7 | - | nC | $V_{DD}$=480V, $I_D$=0.9A, $V_{GS}$=0 to 10V |
| Gate plateau voltage | $V_{plateau}$ | - | 5.4 | - | V | $V_{DD}$=480V, $I_D$=0.9A, $V_{GS}$=0 to 10V |

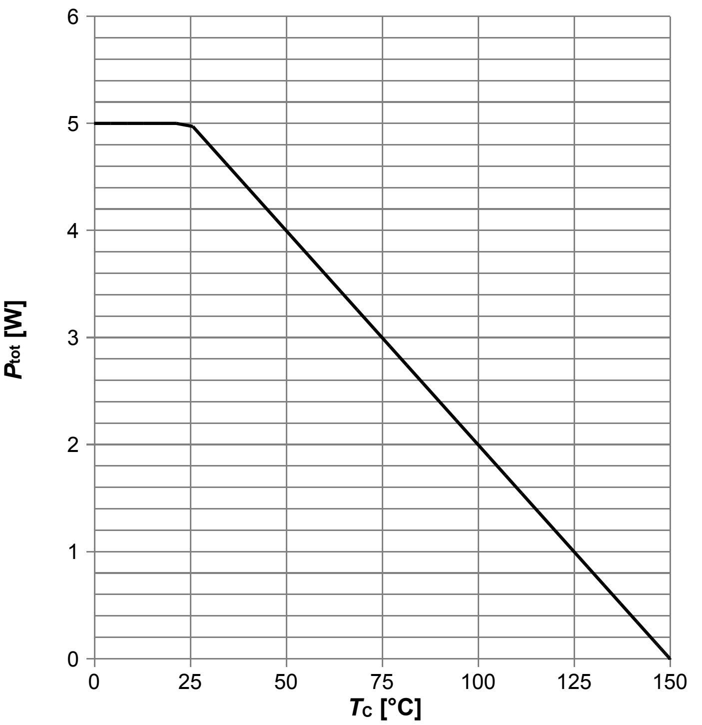
[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 480V
[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 480V

## Table 7 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | $V_{SD}$ | - | 0.9 | - | V | $V_{GS}$=0V, $I_F$=0.9A, $T_f$=25°C |
| Reverse recovery time | $t_{rr}$ | - | 180 | - | ns | $V_R$=400V, $I_F$=0.9A, d$i_F$/d$t$=100A/µs |
| Reverse recovery charge | $Q_{rr}$ | - | 0.67 | - | µC | $V_R$=400V, $I_F$=0.9A, d$i_F$/d$t$=100A/µs |
| Peak reverse recovery current | $I_{rrm}$ | - | 7.1 | - | A | $V_R$=400V, $I_F$=0.9A, d$i_F$/d$t$=100A/µs |

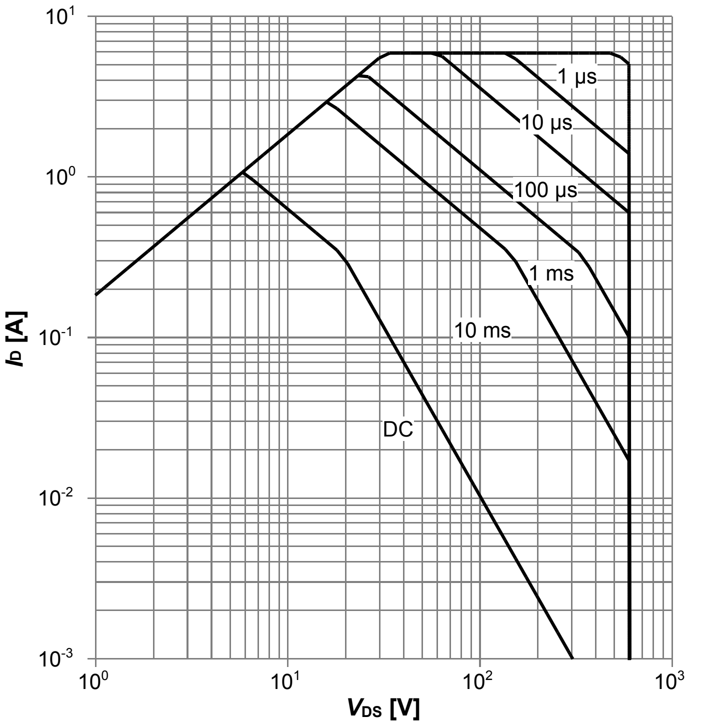
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



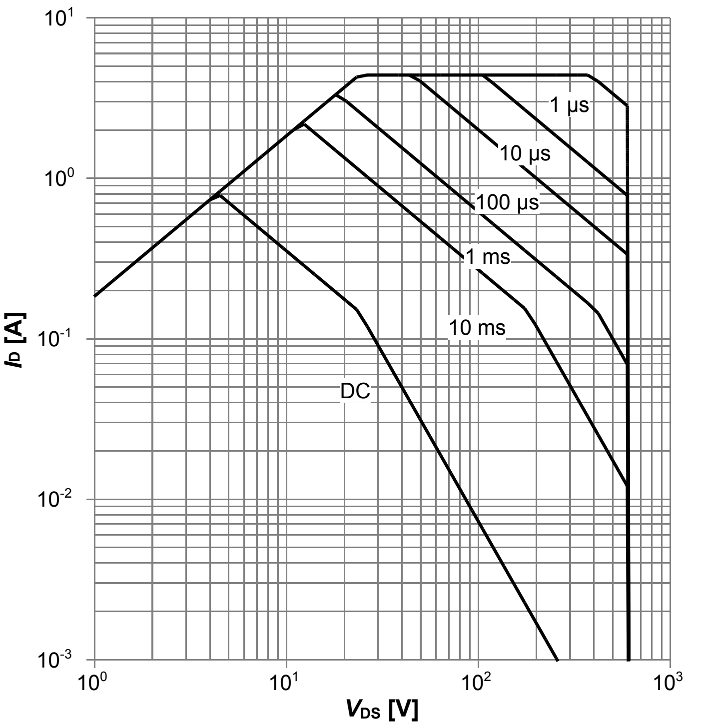

$P_{tot}$=f($T_C$)

**Diagram 2: Safe operating area**



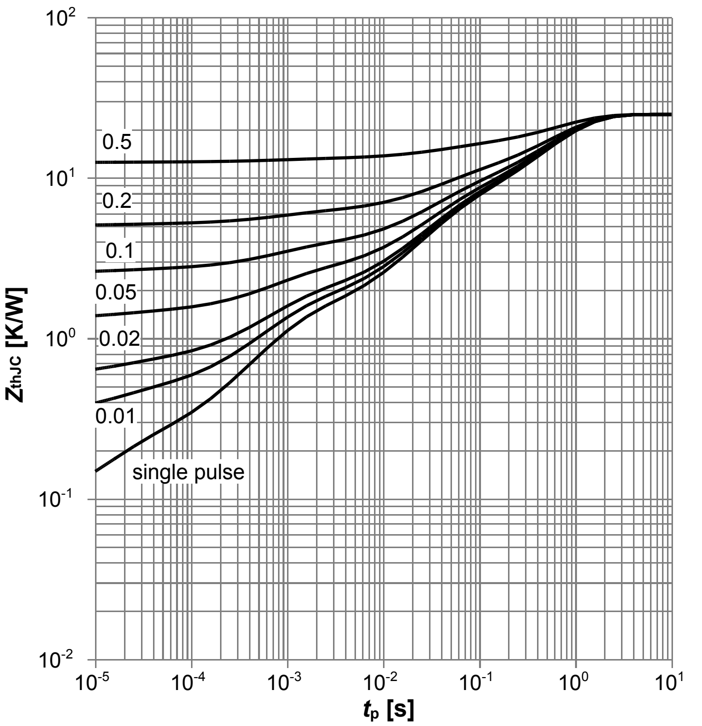

$I_D$=f($V_{DS}$); $T_C$=25 °C; $D$=0; parameter: $t_p$

**Diagram 3: Safe operating area**



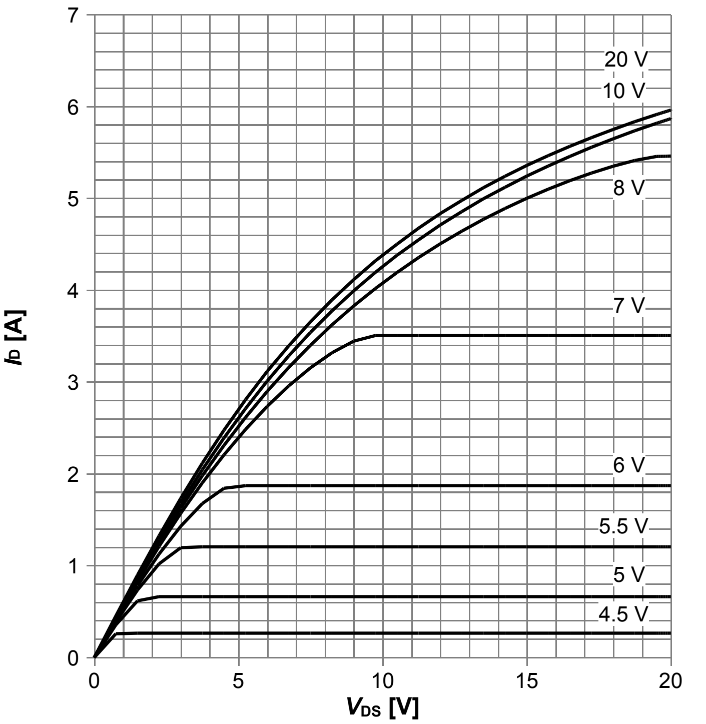

$I_D$=f($V_{DS}$); $T_C$=80 °C; $D$=0; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**



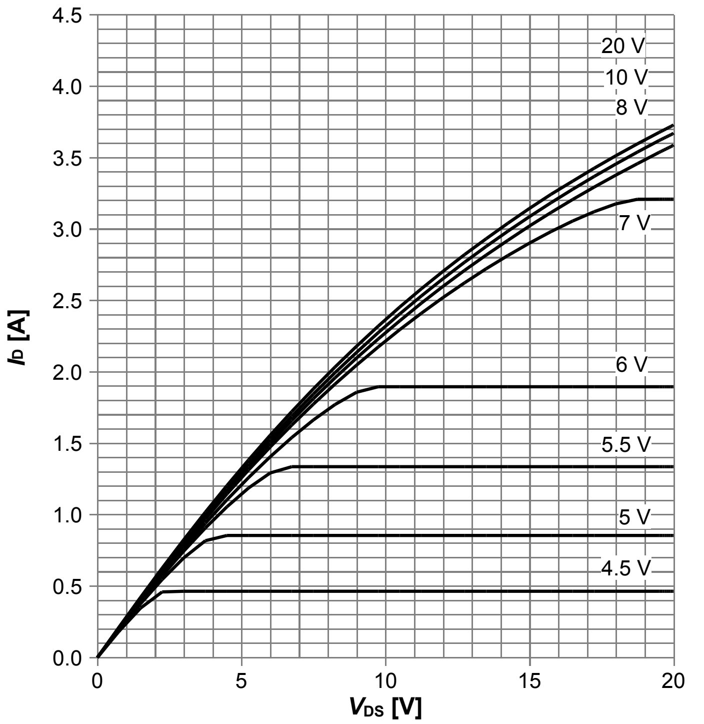

$Z_{thJC}$ =f($t_P$); parameter: $D$=$t_p$/$T$

**Diagram 5: Typ. output characteristics**



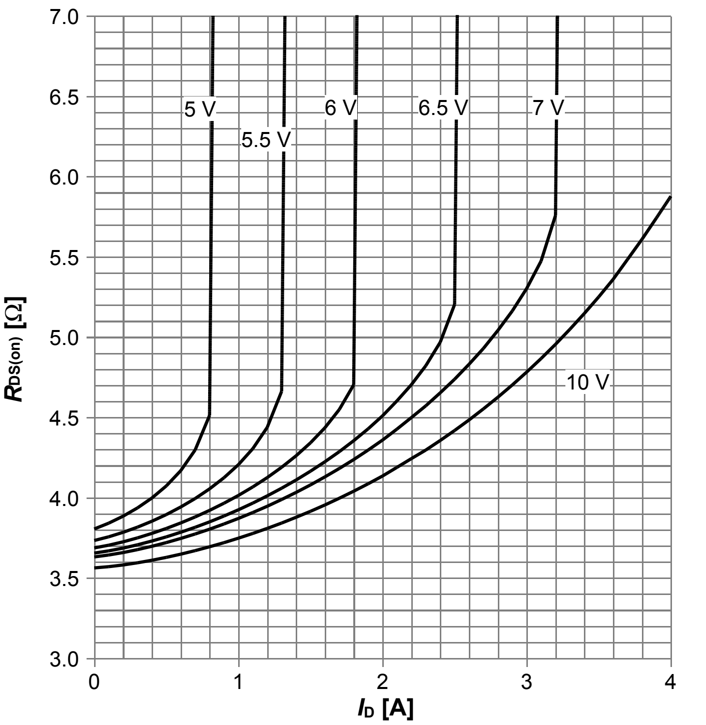

$I_D$=f($V_{DS}$); $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. output characteristics**



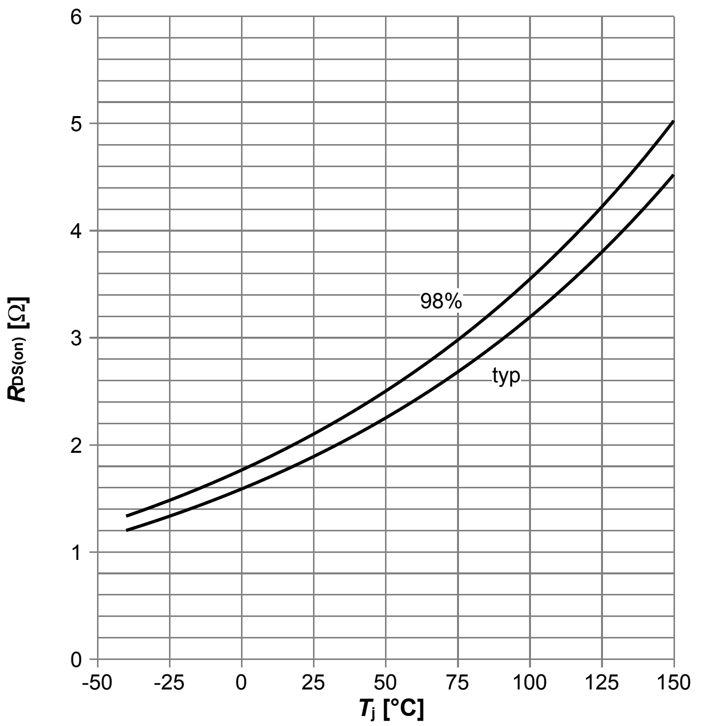

$I_D$=f($V_{DS}$); $T_j$=125 °C; parameter: $V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**



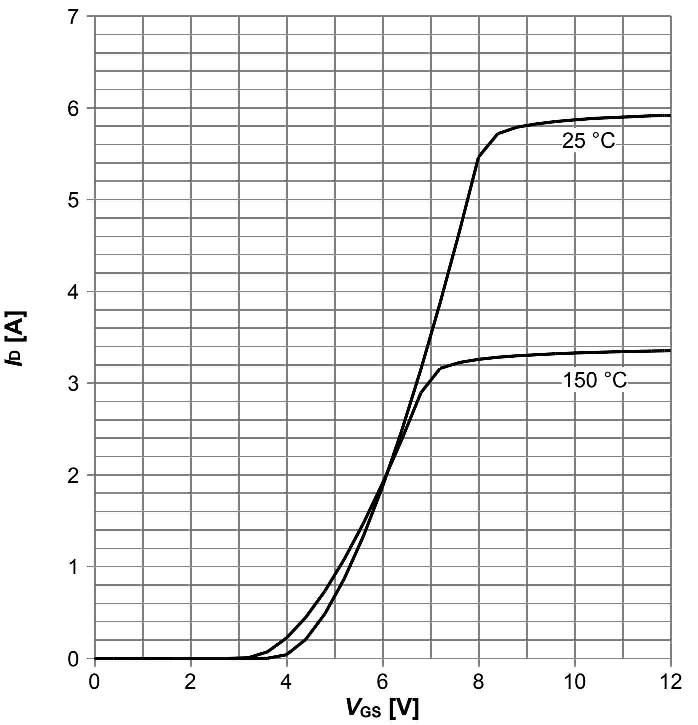

$R_{DS(on)}$=f($I_D$); $T_j$=125 °C; parameter: $V_{GS}$

**Diagram 8: Drain-source on-state resistance**



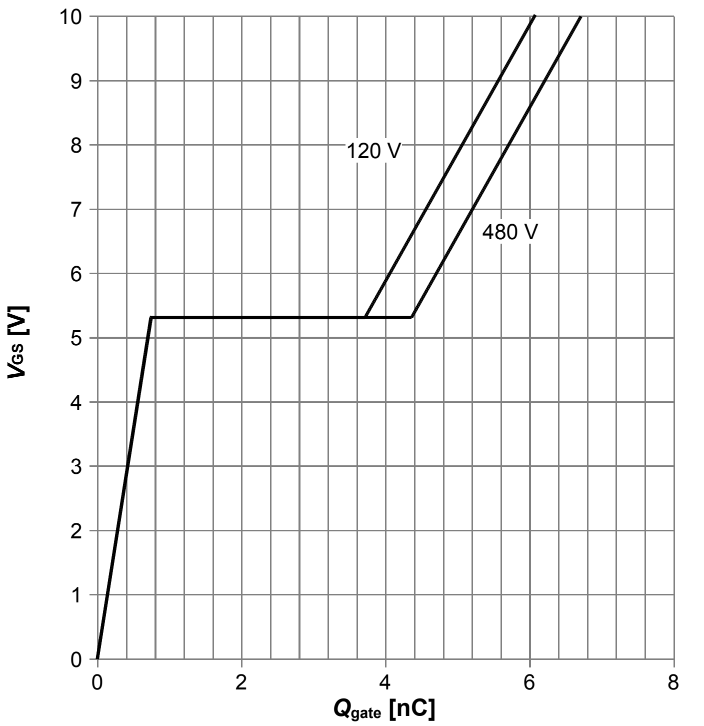

$R_{DS(on)}$=f($T_j$); $I_D$=0.8 A; $V_{GS}$=10 V

**Diagram 9: Typ. transfer characteristics**



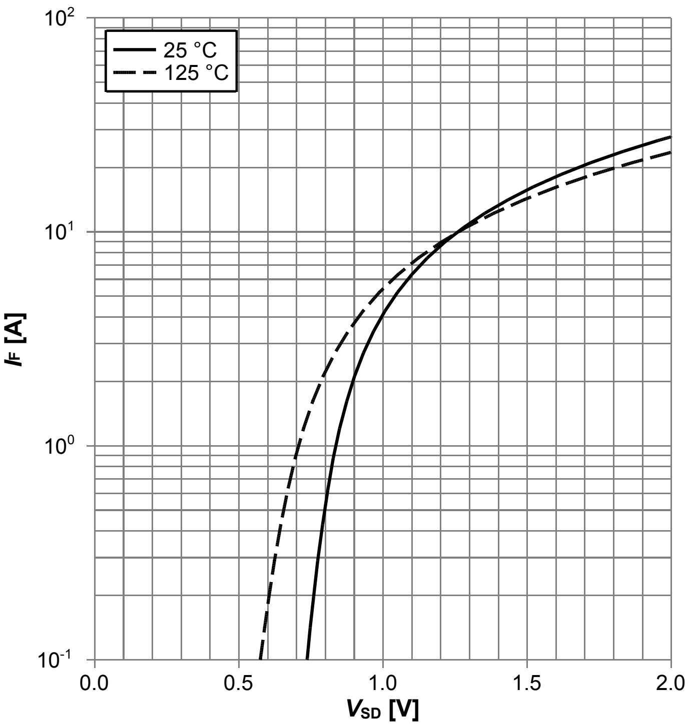

$I_D$=f($V_{GS}$); $V_{DS}$=20V; parameter: $T_j$

**Diagram 10: Typ. gate charge**



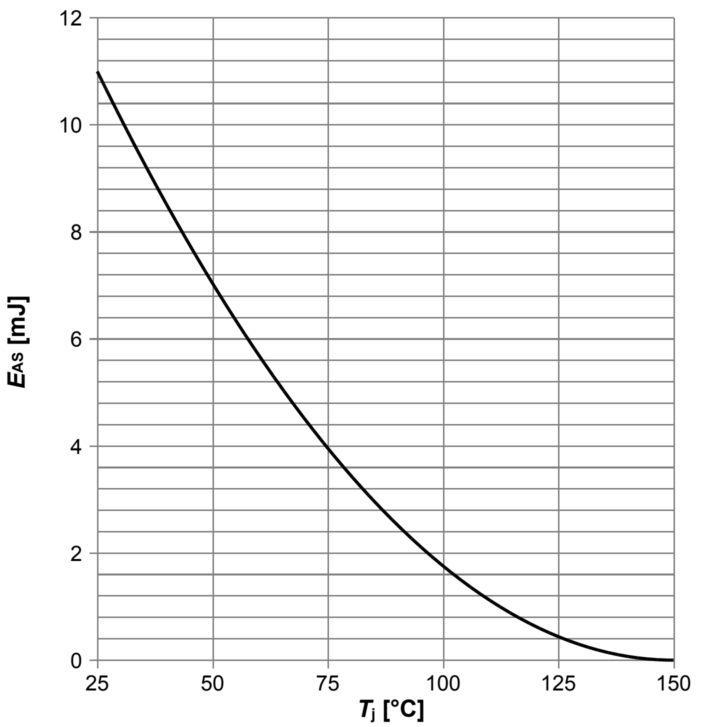

$V_{GS}$=f($Q_{gate}$); $I_D$=0.9 A pulsed; parameter: $V_{DD}$

**Diagram 11: Forward characteristics of reverse diode**



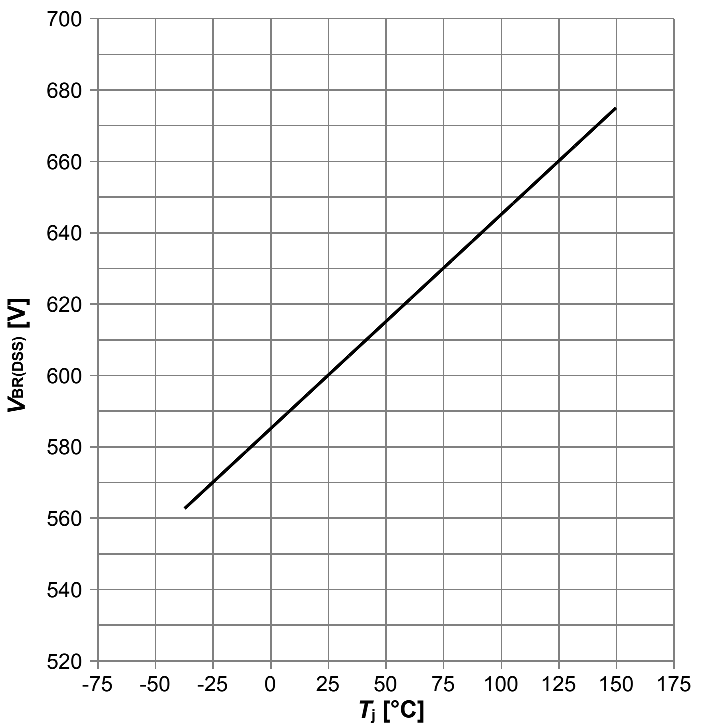

$I_F$=f($V_{SD}$); parameter: $T_j$

**Diagram 12: Avalanche energy**



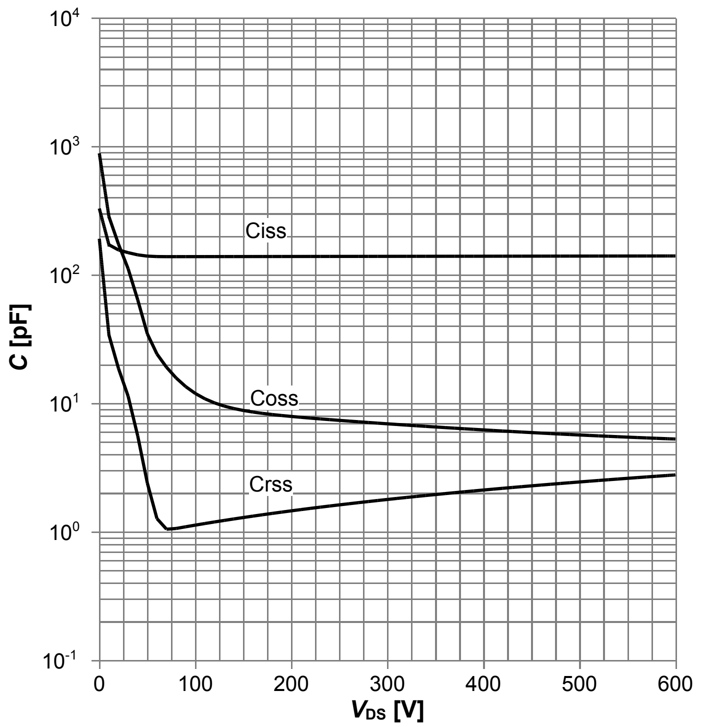

$E_{AS}$=f($T_j$); $I_D$=0.4 A; $V_{DD}$=50 V

**Diagram 13: Drain-source breakdown voltage**



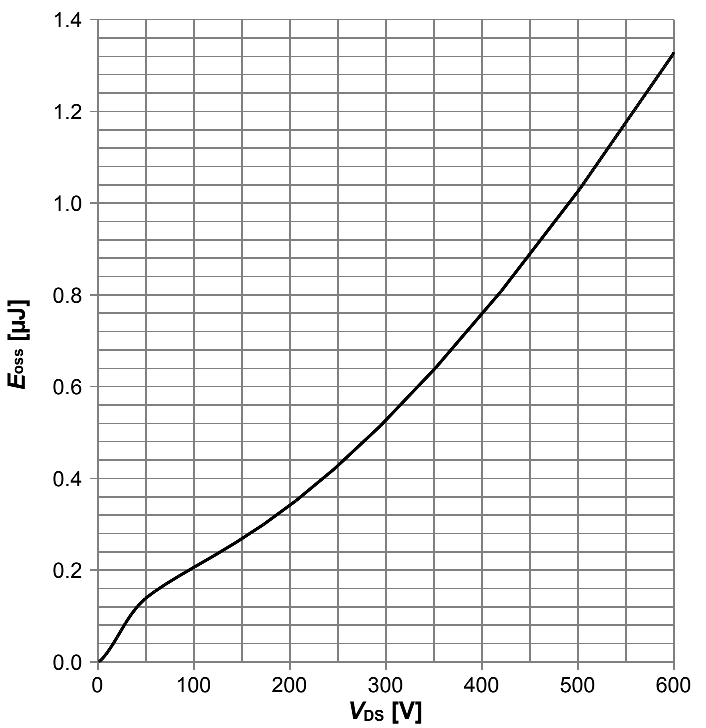

$V_{BR(DSS)}$=f($T_j$); $I_D$=0.25 mA

**Diagram 14: Typ. capacitances**




$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

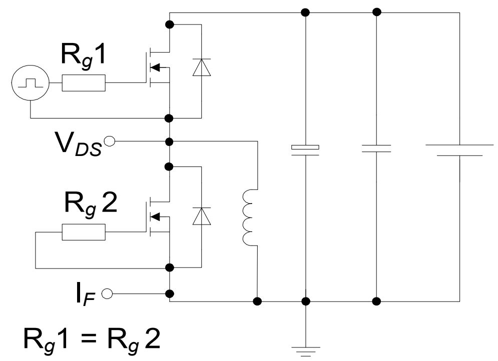
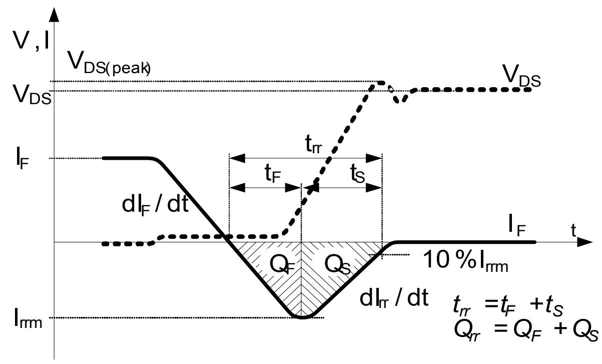
**Diagram 15: Typ. Coss stored energy**




$E_{oss}$=f($V_{DS}$)

# 5 Test Circuits

## Table 8 Diode characteristics

<table>
<tr><th>Test circuit for diode characteristics</th><th>Diode recovery waveform</th></tr>
<tr><td>
</td><td>
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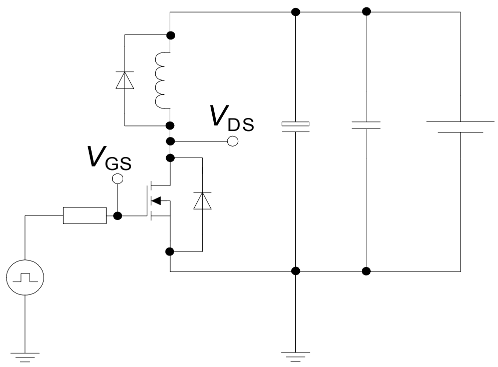
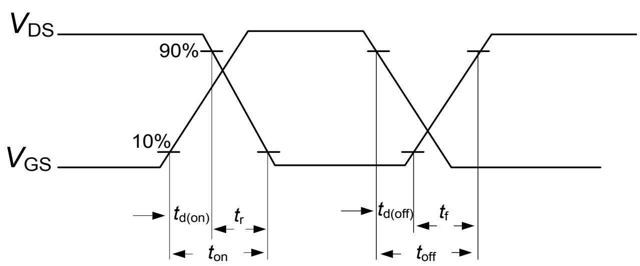
## Table 9 Switching times

<table>
<tr><th>Switching times test circuit for inductive load</th><th>Switching times waveform</th></tr>
<tr><td>
</td><td>
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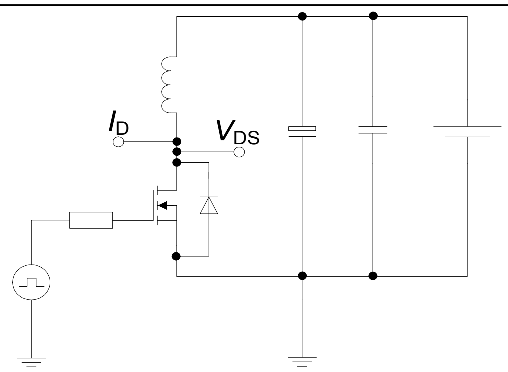
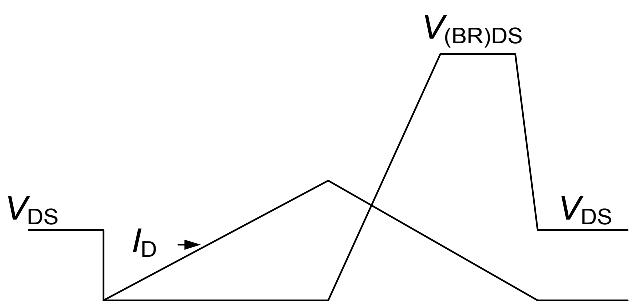
## Table 10 Unclamped inductive load

<table>
<tr><th>Unclamped inductive load test circuit</th><th>Unclamped inductive waveform</th></tr>
<tr><td>
</td><td>
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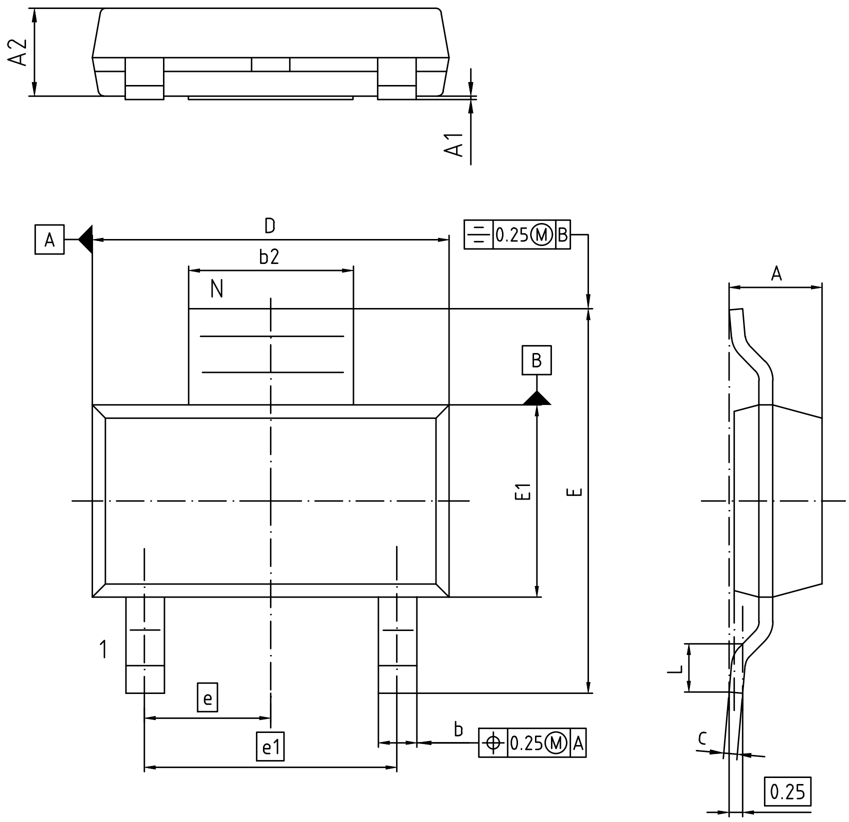
## 6 Package Outlines

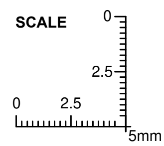



NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

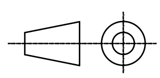
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.52 | 1.80 | 0.060 | 0.071 |
| A1 | - | 0.10 | - | 0.004 |
| A2 | 1,50 | 1.70 | 0.059 | 0.067 |
| b | 0.60 | 0.80 | 0.024 | 0.031 |
| b2 | 2.95 | 3.10 | 0.116 | 0.122 |
| c | 0.24 | 0.32 | 0.009 | 0.013 |
| D | 6.30 | 6.70 | 0.248 | 0.264 |
| E | 6.70 | 7.30 | 0.264 | 0.287 |
| E1 | 3.30 | 3.70 | 0.130 | 0.146 |
| e | 2.3 BASIC | | 0.091 BASIC | |
| e1 | 4.6 BASIC | | 0.181 BASIC | |
| L | 0.75 | 1.10 | 0.030 | 0.043 |
| N | 3 | | 3 | |
| O | 0° | 10° | 0° | 10° |
| | | | | |

**DOCUMENT NO.**
Z8B00180553

**SCALE**




**EUROPEAN PROJECTION**



**ISSUE DATE**
24-02-2016

**REVISION**
01

**Figure 1 Outline PG-SOT223, dimensions in mm/inches**

# 7 Appendix A

## Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

## Revision History

IPN60R2K1CE

**Revision: 2016-04-29, Rev. 2.0**

| Previous Revision | | |
|---|---|---|
| Revision | Date | Subjects (major changes since last revision) |
| 2.0 | 2016-04-29 | Release of final version |

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