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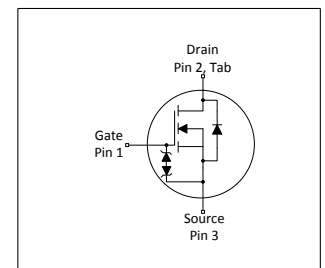
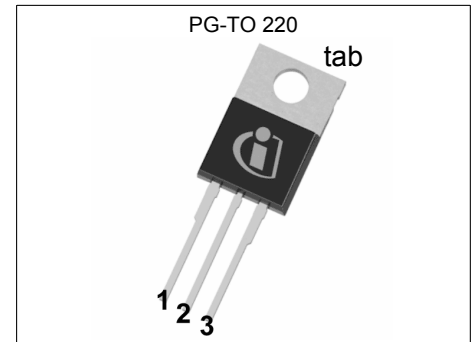
MOSFET

800V CoolMOS™ P7 Power Transistor

The latest 800V CoolMOS™ P7 series sets a new benchmark in 800V super junction technologies and combines best-in-class performance with state of the art ease-of-use, resulting from Infineon's over 18 years pioneering super junction technology innovation.

Features

- Best-in-class FOM $R_{DS(on)} \cdot E_{oss}$; reduced Q_g , C_{iss} , and C_{oss}
- Best-in-class DPAK $R_{DS(on)}$
- Best-in-class $V_{(GS)th}$ of 3V and smallest $V_{(GS)th}$ variation of $\pm 0.5V$
- Integrated Zener Diode ESD protection
- Best-in-class CoolMOS™ quality and reliability; qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- Fully optimized portfolio



Benefits

- Best-in-class performance
- Enabling higher power density designs, BOM savings and lower assembly costs
- Easy to drive and to parallel
- Better production yield by reducing ESD related failures
- Less production issues and reduced field returns
- Easy to select right parts for fine tuning of designs



Applications

Recommended for hard and soft switching flyback topologies for LED Lighting, low power Chargers and Adapters, Audio, AUX power and Industrial power. Also suitable for PFC stage in Consumer applications and Solar.



Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_J=25^{\circ}C$	800	V
$R_{DS(on),max}$	0.28	Ω
$Q_{g,typ}$	36	nC
I_D	17	A
E_{oss} @ 500V	4	μJ
$V_{GS(th),typ}$	3	V
ESD class (HBM)	2	-

Type / Ordering Code	Package	Marking	Related Links
IPP80R280P7	PG-TO 220	80R280P7	see Appendix A

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1 Maximum ratings

at $T_j = 25^{\circ}\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	17 10.6	A	$T_C=25^{\circ}\text{C}$ $T_C=100^{\circ}\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	45	A	$T_C=25^{\circ}\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	43	mJ	$I_D=2.2\text{A}$; $V_{DD}=50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.36	mJ	$I_D=2.2\text{A}$; $V_{DD}=50\text{V}$
Avalanche current, repetitive	I_{AR}	-	-	2.2	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0$ to 400V
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	101	W	$T_C=25^{\circ}\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	$^{\circ}\text{C}$	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	12	A	$T_C=25^{\circ}\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	45	A	$T_C=25^{\circ}\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1	V/ns	$V_{DS}=0$ to 400V, $I_{SD} \leq 3.6\text{A}$, $T_j=25^{\circ}\text{C}$
Maximum diode commutation speed ³⁾	di/dt	-	-	50	A/ μs	$V_{DS}=0$ to 400V, $I_{SD} \leq 3.6\text{A}$, $T_j=25^{\circ}\text{C}$

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.2	$^{\circ}\text{C}/\text{W}$	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	$^{\circ}\text{C}/\text{W}$	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	$^{\circ}\text{C}/\text{W}$	n.a
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	$^{\circ}\text{C}$	1.6mm (0.063 in.) from case for 10s

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.5$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DClink}=400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G ; $t_{cond} < 2\mu\text{s}$

3 Electrical characteristics
at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	$V_{DS}=V_{GS}$, $I_D=0.36\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=800\text{V}$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{DS}=800\text{V}$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$
Gate-source leakage current incl. zener diode	I_{GSS}	-	-	1	μA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.24	0.28	Ω	$V_{GS}=10\text{V}$, $I_D=7.2\text{A}$, $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$, $I_D=7.2\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	1	-	Ω	$f=250\text{kHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1200	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=500\text{V}$, $f=250\text{kHz}$
Output capacitance	C_{oss}	-	20	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=500\text{V}$, $f=250\text{kHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	38	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0$ to 500V
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	490	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0$ to 500V
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=7.2\text{A}$, $R_G=4.7\Omega$
Rise time	t_r	-	6	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=7.2\text{A}$, $R_G=4.7\Omega$
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=7.2\text{A}$, $R_G=4.7\Omega$
Fall time	t_f	-	5	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=7.2\text{A}$, $R_G=4.7\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	5	-	nC	$V_{DD}=640\text{V}$, $I_D=7.2\text{A}$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{GD}	-	15	-	nC	$V_{DD}=640\text{V}$, $I_D=7.2\text{A}$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	36	-	nC	$V_{DD}=640\text{V}$, $I_D=7.2\text{A}$, $V_{GS}=0$ to 10V
Gate plateau voltage	V_{plateau}	-	4.5	-	V	$V_{DD}=640\text{V}$, $I_D=7.2\text{A}$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 500V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 500V

800V CoolMOS™ P7 Power Transistor IPP80R280P7

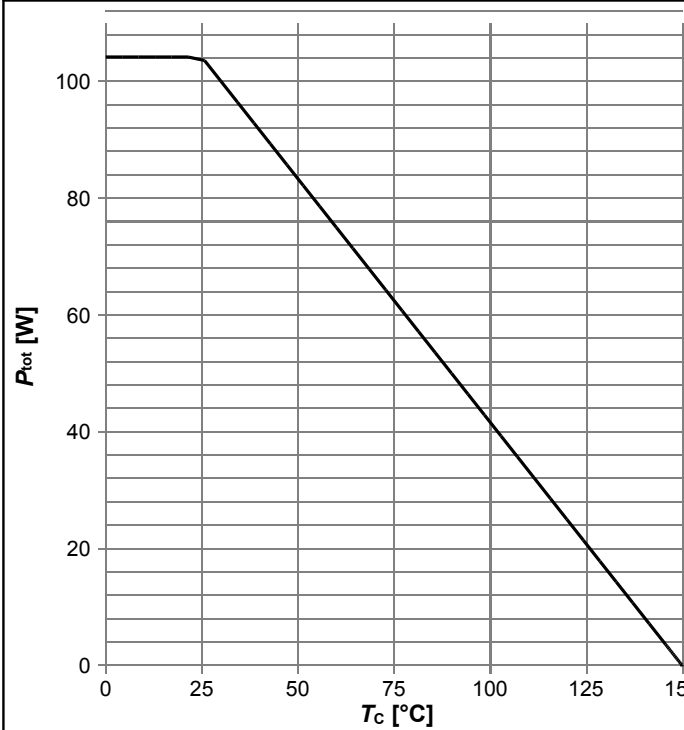
Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=7.2A, T_i=25^\circ C$
Reverse recovery time	t_{rr}	-	1200	-	ns	$V_R=400V, I_F=3.6A, di_F/dt=50A/\mu s$
Reverse recovery charge	Q_{rr}	-	15	-	μC	$V_R=400V, I_F=3.6A, di_F/dt=50A/\mu s$
Peak reverse recovery current	I_{rrm}	-	24	-	A	$V_R=400V, I_F=3.6A, di_F/dt=50A/\mu s$



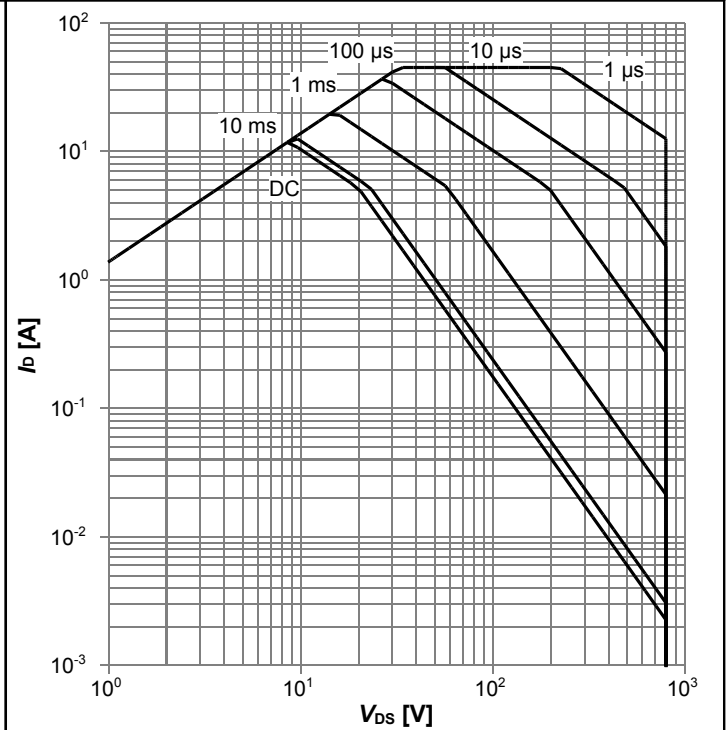
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



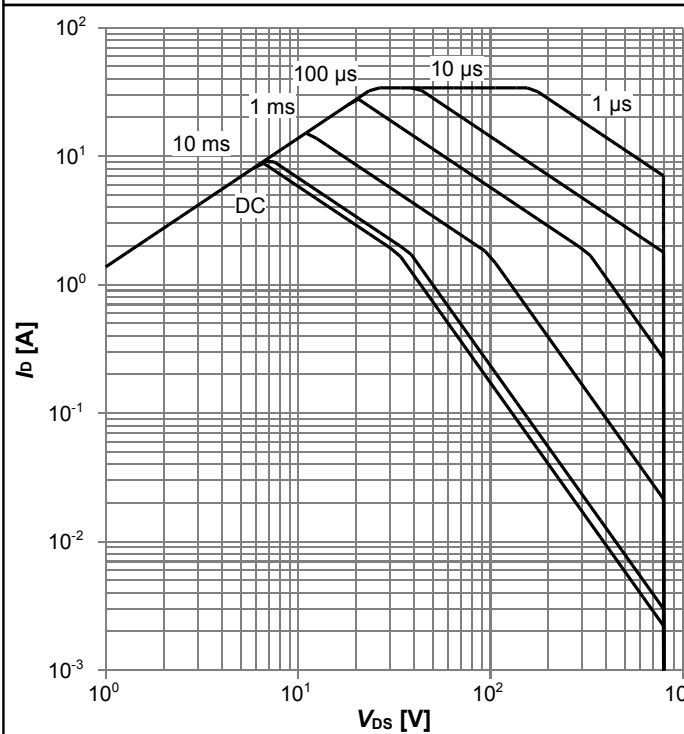
$P_{tot}=f(T_c)$

Diagram 2: Safe operating area



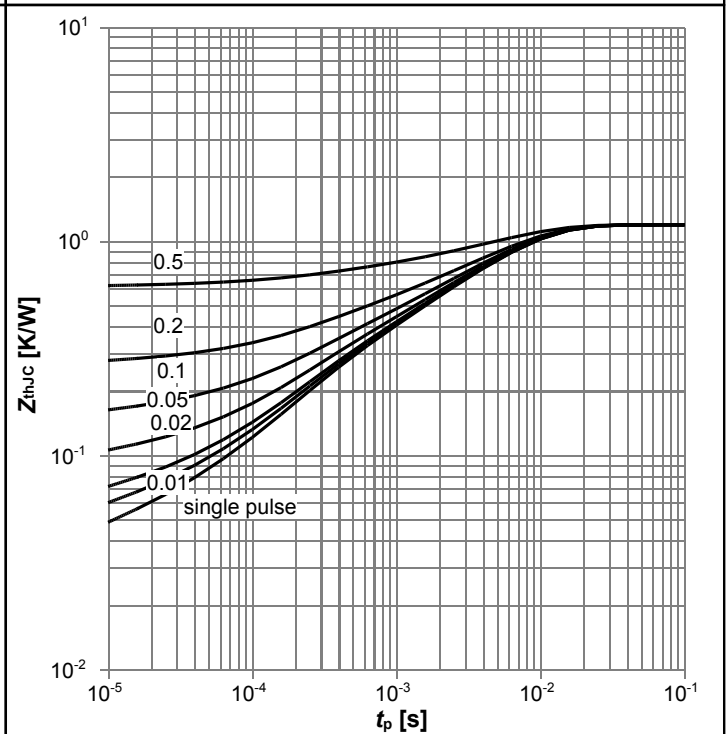
$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0; \text{parameter: } t_p$

Diagram 3: Safe operating area



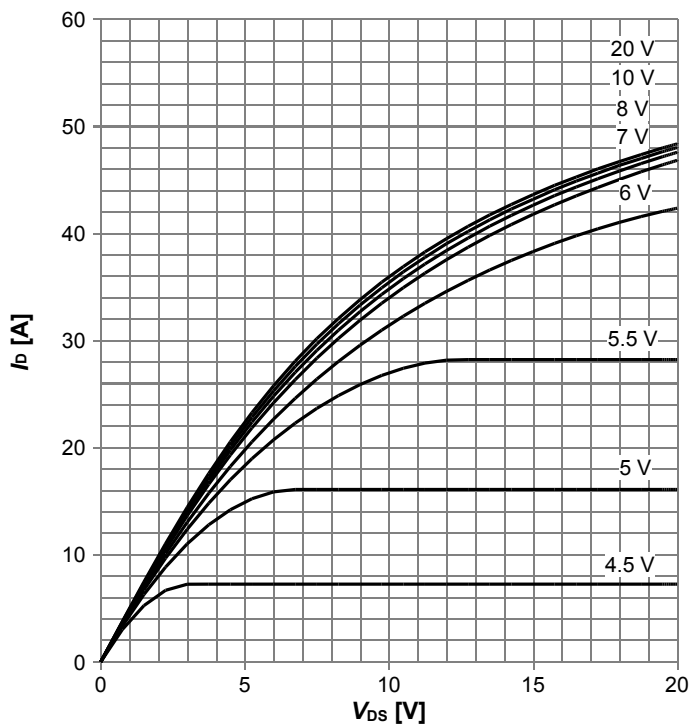
$I_D=f(V_{DS}); T_C=80\text{ °C}; D=0; \text{parameter: } t_p$

Diagram 4: Max. transient thermal impedance



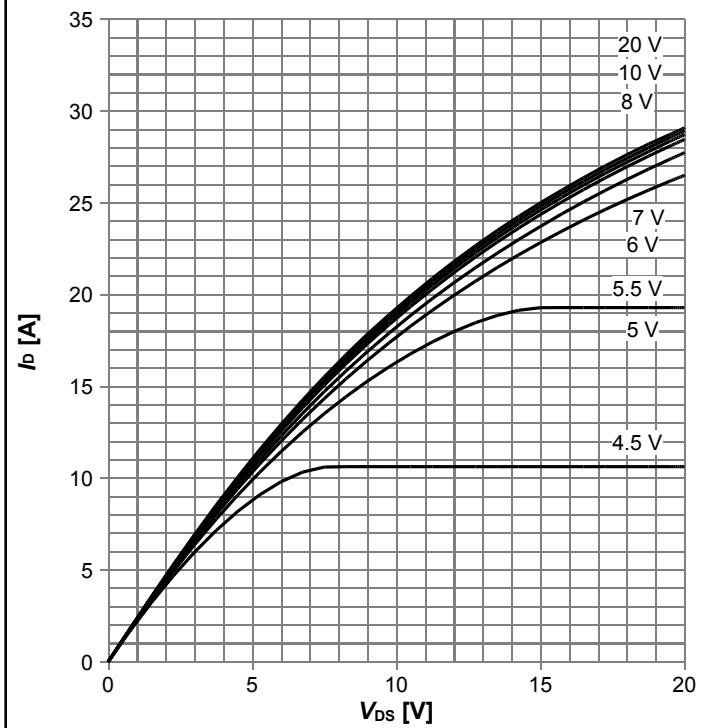
$Z_{thJC}=f(t_p); \text{parameter: } D=t_p/T$

Diagram 5: Typ. output characteristics



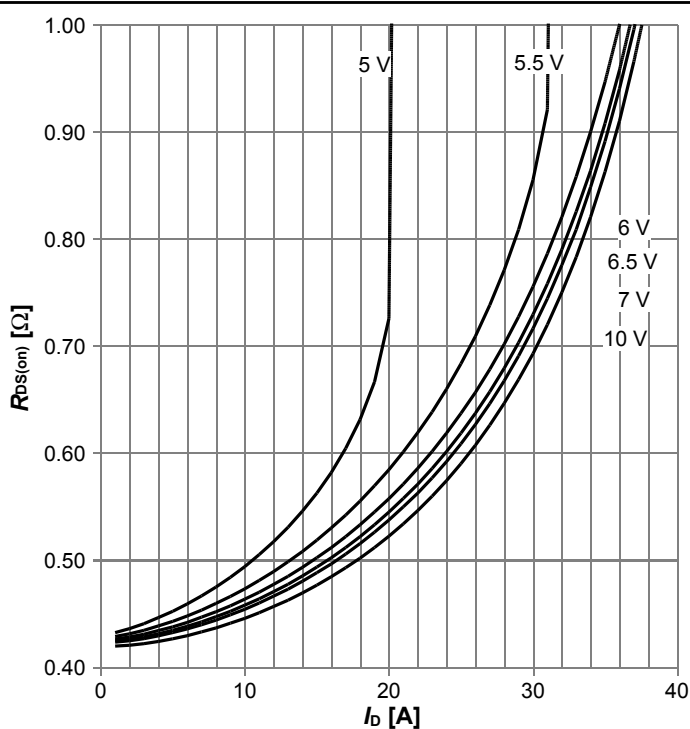
$I_D=f(V_{DS})$; $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



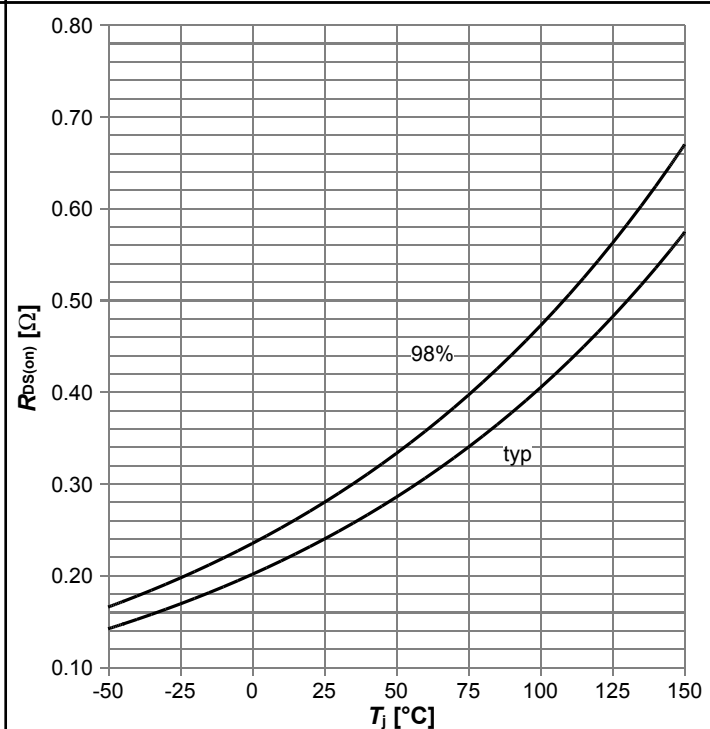
$I_D=f(V_{DS})$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



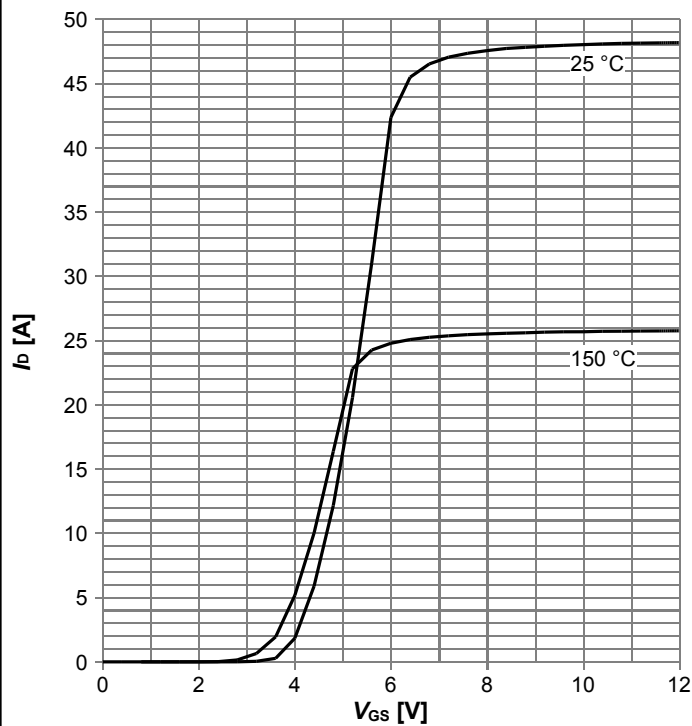
$R_{DS(on)}=f(I_D)$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



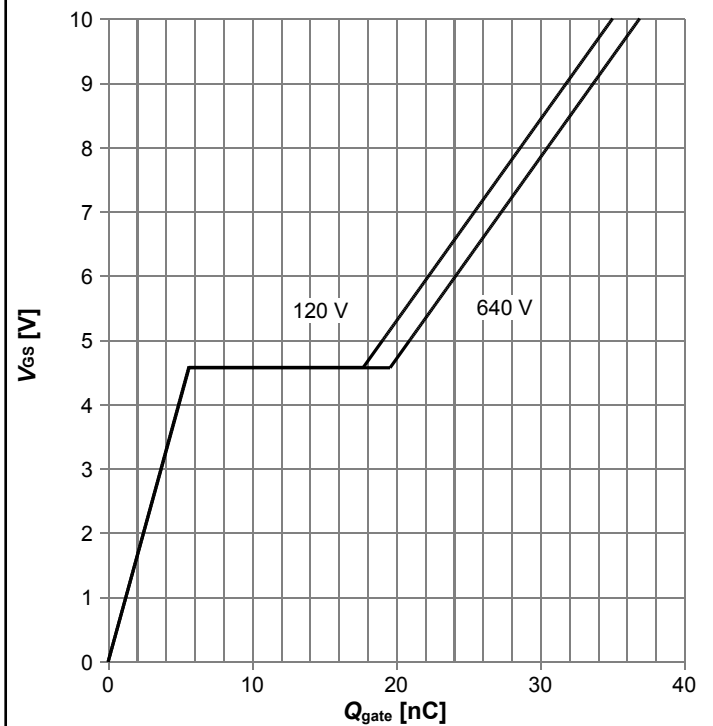
$R_{DS(on)}=f(T_j)$; $I_D=7.2\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



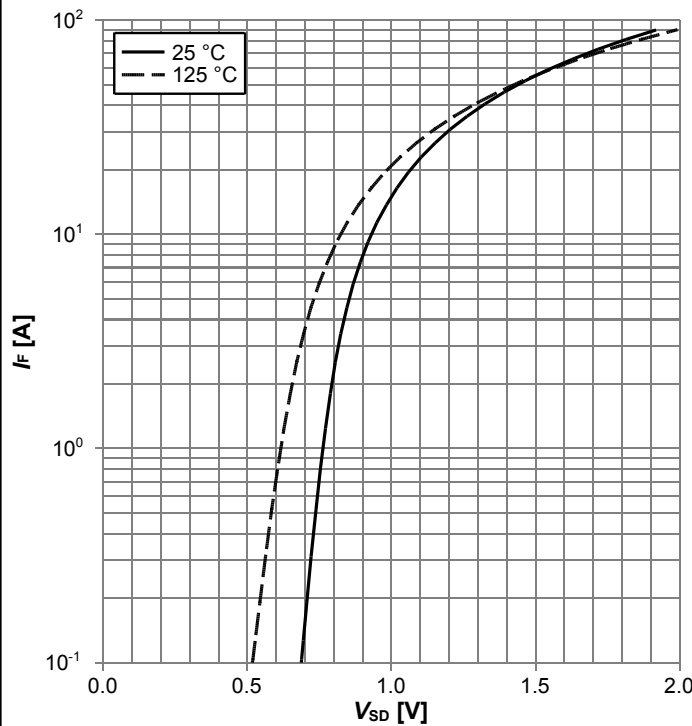
$I_D=f(V_{GS}); V_{DS}=20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



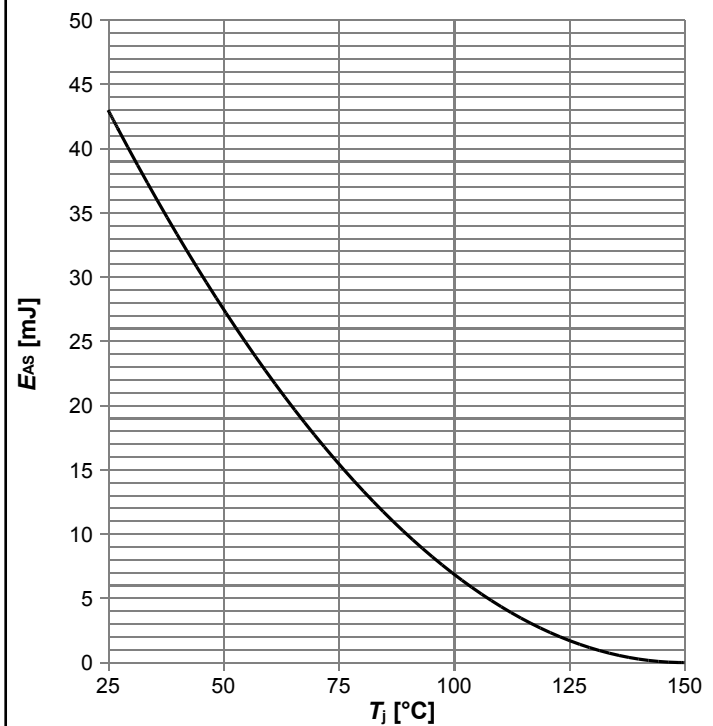
$V_{GS}=f(Q_{gate}); I_D=7.2 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



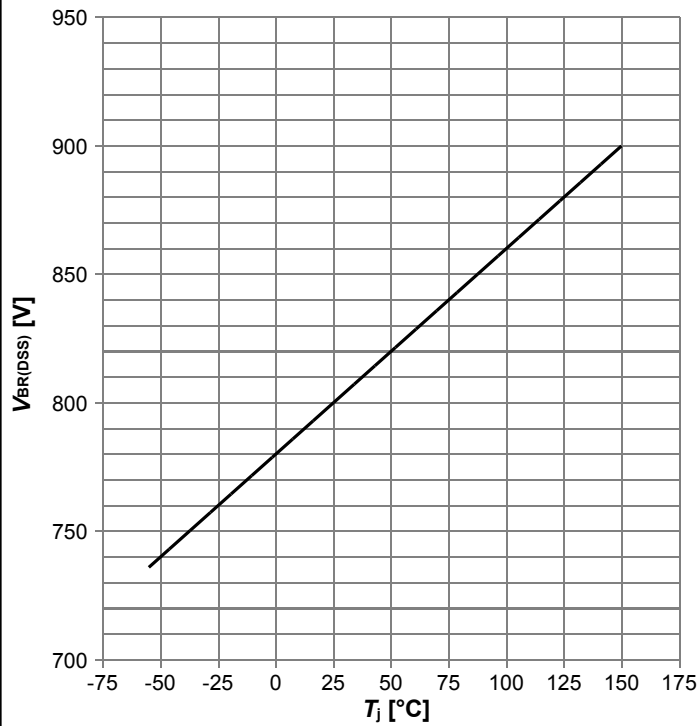
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



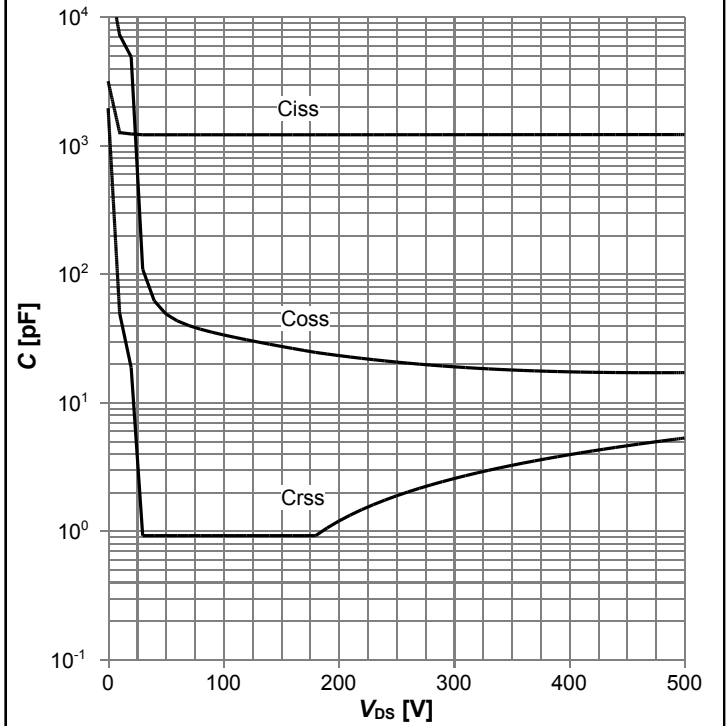
$E_{AS}=f(T_j); I_D=2.2 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



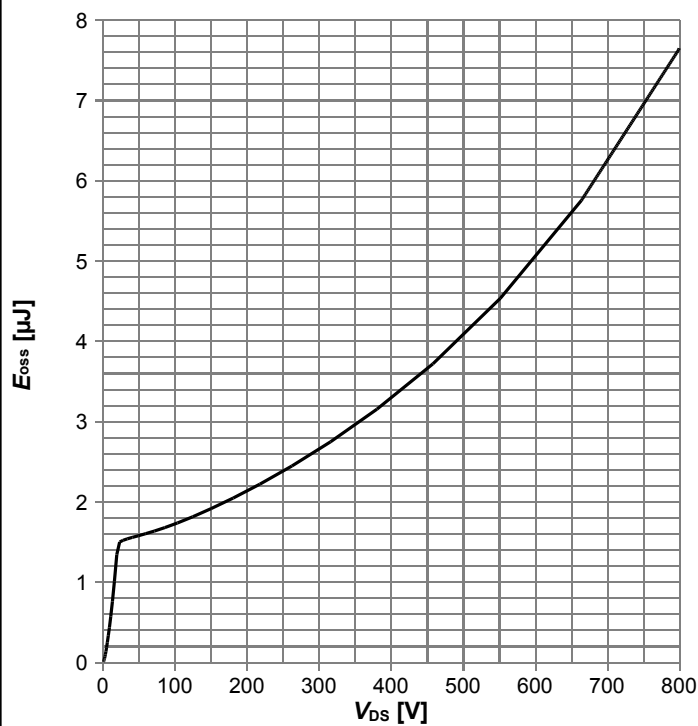
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
<p>$R_{g1} = R_{g2}$</p>	<p>$t_{rr} = t_F + t_S$ $Q_{rr} = Q_F + Q_S$</p>

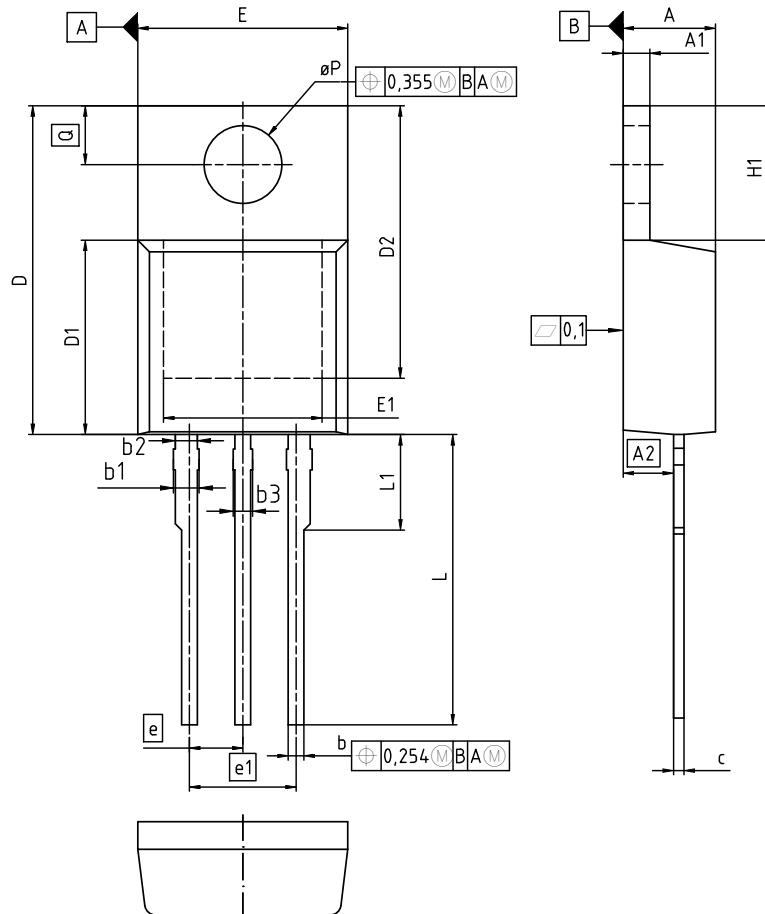
Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	<p>$V_{(BR)DS}$</p>

6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

SCALE

EUROPEAN PROJECTION

ISSUE DATE
30-07-2009

REVISION
06

Figure 1 Outline PG-TO 220, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

800V CoolMOS™ P7 Power Transistor

IPP80R280P7

Revision History

IPP80R280P7

Revision: 2016-07-05, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-07-05	Release of final version

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Published by

Infineon Technologies AG

81726 München, Germany

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