Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Low Latency 100-Gbps Ethernet IP Core User Guide

Subscribe

Send Feedback

Contents

About the LL 100GbE IP Core

2018.01.03

The Intel® Low Latency 100-Gbps Ethernet (LL 100GbE) media access controller (MAC) and PHY MegaCore® functions offer the lowest round-trip latency and smallest size to implement the *IEEE 802.3ba 100G Ethernet Standard* with an option to support the *IEEE 802.3ap-2007 Backplane Ethernet Standard*.

The version of this product that supports Arria® 10 devices is included in the Intel FPGA IP Library and is available from the Quartus® Prime IP Catalog.

Note: The full product name, Low Latency 100-Gbps Ethernet MAC and PHY MegaCore Function, is shortened to Low Latency (LL) 100GbE (LL 100GbE) IP core in this document. In addition, although multiple variations are available from the parameter editor, this document refers to this product as a single IP core, because all variations are configurable from the same parameter editor.

Figure 1-1: LL 100GbE IP Core

Main blocks, internal connections, and external block requirements.

As illustrated, on the MAC client side you can choose a wide, standard Avalon® Streaming (Avalon-ST) interface, or a narrower, custom streaming interface. The MAC client side Avalon Streaming (Avalon-ST) interface data bus is 512 bits wide. The MAC client side custom streaming interface data bus is 256 bits wide. The client-side data maps to ten 10.3125 Gbps transceiver PHY links or to four 25.78125 Gbps transceiver PHY links.

The 100GbE (CAUI) interface has 10x10.3125 Gbps links. For Arria 10 GT devices only, you can configure a 100GbE CAUI-4 option, with 4x25.78125 Gbps links.

The FPGA serial transceivers are compliant with the IEEE 802.3ba standard CAUI and CAUI-4 specifications. The IP core configures the transceivers to implement the relevant specification for your IP core variation. You can connect the transceiver interfaces directly to an external physical medium dependent (PMD) optical module or to another device.

The IP core provides standard MAC and physical coding sublayer (PCS) functions with a variety of configuration and status registers. You can exclude the statistics registers. If you exclude these registers, you can monitor the statistics counter increment vectors that the IP core provides at the client side interface and maintain your own counters.

Related Information

- **LL 100GbE IP Core Functional Description** on page 3-2
  Provides detailed descriptions of LL 100GbE IP core operation and functions.
- **Introduction to Intel FPGA IP Cores**
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- **Creating Version-Independent IP and Qsys Simulation Scripts**
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- **Project Management Best Practices**
  Guidelines for efficient management and portability of your project and IP files.
- **LL 100GbE IP Core User Guide Archives** on page 5-1
- **Low Latency 100G Ethernet Design Example User Guide**

LL 100GbE IP Core Supported Features

All LL 100GbE IP core variations include both a MAC and a PHY, and all variations are in full-duplex mode. These IP core variations offer the following features:

- Designed to the *IEEE 802.3ba-2010 High Speed Ethernet Standard* available on the IEEE website (www.ieee.org).
- Soft PCS logic that interfaces seamlessly to Altera 10.3125 Gbps and 25.78125 Gbps serial transceivers.
- Standard XLAUI or CAUI external interface consisting of FPGA hard serial transceiver lanes operating at 10.3125 Gbps , or the CAUI-4 external interface consisting of four FPGA hard serial transceiver lanes operating at 25.78125 Gbps.
- Supports Synchronous Ethernet (Sync-E) by providing an optional CDR recovered clock output signal to the device fabric.
- Avalon Memory-Mapped (Avalon-MM) management interface to access the IP core control and status registers.
- Avalon-ST data path interface connects to client logic with the start of frame in the most significant byte (MSB) when optional adapters are used. Interface has data width 512 bits.

- Optional custom streaming data path interface with narrower bus width and a start frame possible on 64-bit word boundaries without the optional adapters. Interface has data width 256 bits.
- Support for jumbo packets.
- TX and RX CRC pass-through control.
- Optional TX CRC generation and insertion.
- RX CRC checking and error reporting.
- TX error insertion capability supports test and debug.
- RX and TX preamble pass-through options for applications that require proprietary user management information transfer.
- TX automatic frame padding to meet the 64-byte minimum Ethernet frame length at the LL 100GbE Ethernet connection.
- Hardware and software reset control.
- Pause frame filtering control.
- Received control frame type indication.
- MAC provides cut-through frame processing.
- Optional deficit idle counter (DIC) options to maintain a finely controlled 8-byte or 12-byte inter-packet gap (IPG) minimum average.
- Optional IEEE 802.3 Clause 31 Ethernet flow control operation using the pause registers or pause interface.
- Optional priority-based flow control that complies with the *IEEE Standard 802.1Qbb-2011—Amendment 17: Priority-based Flow Control*, using the pause registers for fine control.
- 1000 bits RX PCS lane skew tolerance, which exceeds the IEEE 802.3-2012 Ethernet standard clause 82.2.12 requirements.
- Optional support for the IEEE Standard 1588-2008 Precision Clock Synchronization Protocol (1588 PTP).
- Optional statistics counters.
- Optional fault signaling: detects and reports local fault and generates remote fault, with *IEEE 802.3ba-2012 Ethernet Standard* Clause 66 support.
- Optional serial PMA loopback (TX to RX) at the serial transceiver for self-diagnostic testing.
- Optional access to Altera Debug Master Endpoint (ADME) for debugging or monitoring PHY signal integrity.

The LL 100GbE IP core can support full wire line speed with a 64-byte frame length and back-to-back or mixed length traffic with no dropped packets.

For a detailed specification of the Ethernet protocol refer to the *IEEE 802.3ba-2010 High Speed Ethernet Standard*.

Related Information
IEEE website
The *IEEE 802.3ba-2010 High Speed Ethernet Standard* and the *IEEE Standard 802.1Qbb-2011—Amendment 17: Priority-based Flow Control* are available on the IEEE website.

IP Core Device Family and Speed Grade Support

The following sections list the device family and device speed grade support offered by the LL 100GbE IP core:

LL 100GbE IP Core Device Family Support on page 1-4

LL 100GbE IP Core Device Speed Grade Support on page 1-5

LL 100GbE IP Core Device Family Support

Table 1-1: Intel FPGA IP Core Device Support Levels

Device Support Level	Definition
Preliminary	The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.
Final	The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Table 1-2: LL 100GbE IP Core Device Family Support

Shows the level of support offered by the LL 100GbE IP core for each Intel FPGA device family.

Device Family	Support
Stratix® V (GX, GT, and GS)	Final
Arria 10 (GX, GT, and SX)	Default support level provided in the Quartus Prime software. Refer to the *Quartus Prime Standard Edition Software and Device Support Release Notes* and the *Quartus Prime Pro Edition Software and Device Support Release Notes.*
Other device families	Not supported

Related Information

- **Timing and Power Models**
  Reports the default device support levels in the current version of the Quartus Prime Standard Edition software.

- **Timing and Power Models**
  Reports the default device support levels in the current version of the Quartus Prime Pro Edition software.
- **LL 100GbE IP Core Device Speed Grade Support** on page 1-5
  Shows which IP core variations support which device family speed grades.

LL 100GbE IP Core Device Speed Grade Support

Table 1-3: Slowest Supported Device Speed Grades

Lists the slowest supported device speed grades for standard variations of the LL 100GbE IP core. IP core variations that include a 1588 PTP module might require Quartus Prime seed sweeping to achieve a comfortable timing margin.

MegaCore Function	Device Family	Supported Speed Grades
LL 100GbE	Stratix V (GX)	I2, C2
	Stratix V (GT)	I2, C2
	Stratix V (GS)	I2, C2
	Arria 10 (GX, GT, SX)	I2, C2
LL 100GbE (CAUI–4 option)	Arria 10 GT	I2, C2

IP Core Verification

To ensure functional correctness of the LL 100GbE IP core, Intel performs extensive validation through both simulation and hardware testing. Before releasing a version of the LL 100GbE IP core, Intel runs comprehensive regression tests in the current or associated version of the Quartus Prime software.

Intel verifies that the current version of theQuartus Prime software compiles the previous version of each IP core. Any exceptions to this verification are reported in the *Intel FPGA IP Release Notes*. Intel does not verify compilation with IP core versions older than the previous release.

Related Information

- **Knowledge Base Errata for Low Latency 40-100GbE IP core**
  Exceptions to functional correctness that first manifest in software releases prior to the 16.1 software release are documented in the Low Latency 40-100GbE IP core errata.
- **Knowledge Base Errata for LL 100GbE IP core**
  Exceptions to functional correctness that first manifest in software releases 16.0 and later are documented in the Low Latency 100GbE IP core errata.
- **Intel FPGA IP Release Notes: Low Latency 100-Gbps Ethernet IP Core Release Notes**
  Changes to the Low Latency 100GbE IP core in software releases 16.0 and earlier are noted in the Intel FPGA IP Release Notes.

Simulation Environment

Intel performs the following tests on the LL 100GbE IP core in the simulation environment using internal and third party standard bus functional models (BFM):

- Constrained random tests that cover randomized frame size and contents
- Randomized error injection tests that inject Frame Check Sequence (FCS) field errors, runt packets, and corrupt control characters, and then check for the proper response from the IP core
- Assertion based tests to confirm proper behavior of the IP core with respect to the specification
- Extensive coverage of our runtime configuration space and proper behavior in all possible modes of operation

Compilation Checking

Intel performs compilation testing on an extensive set of LL 100GbE IP core variations and designs that target different devices, to ensure the Quartus Prime software places and routes the IP core ports correctly.

Hardware Testing

Intel performs hardware testing of the key functions of the LL 100GbE IP core using standard 100Gbps Ethernet network test equipment and optical modules. The Intel hardware tests of the LL 100GbE IP core also ensure reliable solution coverage for hardware related areas such as performance, link synchronization, and reset recovery.

Performance and Resource Utilization

The following sections provide performance and resource utilization data for the LL 100GbE IP core.

Table 1-4: IP Core Variation Encoding for Resource Utilization Tables

"On" indicates the parameter is turned on. The symbol "—" indicates the parameter is turned off or not available.

IP Core Variation / Parameter	A	B	C	D
Data interface	Custom-ST	Avalon-ST	Avalon-ST	Avalon-ST
Flow control mode	No flow control	No flow control	Standard flow control	Standard flow control
Average interpacket gap	12	12	12	12
Enable 1588 PTP	—	—	—	On
Enable link fault generation	—	—	On	On
Enable TX CRC insertion	—	On	On	On
Enable preamble passthrough	—	—	On	On

IP Core Variation	A	B	C	D
Parameter				
Enable alignment EOP on FCS word	—	On	On	On
Enable TX statistics	—	On	On	On
Enable RX statistics	—	On	On	On

Arria 10 Resource Utilization

Resource utilization changes depending on the parameter settings you specify in the LL 100GbE parameter editor. For example, if you turn on pause functionality or statistics counters in the LL 100GbE parameter editor, the IP core requires additional resources to implement the additional functionality.

Table 1-5: IP Core FPGA Resource Utilization in Arria 10 Devices

Lists the resources and expected performance for selected variations of the LL 100GbE IP core in an Arria 10 device.

These results were obtained using the Quartus Prime software v16.1.

- The numbers of ALMs and logic registers are rounded up to the nearest 100.
- The numbers of ALMs, before rounding, are the **ALMs needed** numbers from the Quartus Prime Fitter Report.

LL 100GbE Variation	ALMs	Dedicated Logic Registers	Memory M20K
LL 100GbE variation A	13000	22800	29
LL 100GbE variation B	22500	47100	73
LL 100GbE variation C	22700	47900	73
LL 100GbE variation D	29600	64500	109
CAUI-4 Variation	ALMs	Dedicated Logic Registers	Memory M20K
CAUI-4 variation B	24200	50800	77
CAUI-4 variation B with RS-FEC	54100	113200	143

Related Information

Fitter Resources Reports in the Quartus Prime Help
Information about Quartus Prime resource utilization reporting, including **ALMs needed**.

Stratix V Resource Utilization

Resource utilization changes depending on the parameter settings you specify in the LL 100GbE parameter editor. For example, if you turn on pause functionality or statistics counters in the LL 100GbE parameter editor, the IP core requires additional resources to implement the additional functionality.

Table 1-6: IP Core FPGA Resource Utilization in Stratix V Devices

Lists the resources and expected performance for selected variations of the LL 100GbE IP core in a Stratix V device.

These results were obtained using the Quartus II software v14.1.

Note: Please note that at the time of publication, the LL 100GbE IP core that targets a Stratix V device has not been updated since the version compatible with the Quartus Prime Standard Edition software v16.0.

- The numbers of ALMs and logic registers are rounded up to the nearest 100.
- The numbers of ALMs, before rounding, are the **ALMs needed** numbers from the Quartus Prime Fitter Report.

100GbE Variation	ALMs	Dedicated Logic Registers	Memory M20K
100GbE variation A	9500	23000	29
100GbE variation B	20900	48400	61
100GbE variation C	22100	52500	61
100GbE variation D	26900	63700	65

Related Information

Fitter Resources Reports in the Quartus Prime Help
Information about Quartus Prime resource utilization reporting, including **ALMs needed**.

Release Information

Table 1-7: LL 100GbE IP Core Current Release Information

Item	Description
Version	16.1
Release Date	2016.10.31

Item	Description
Ordering Codes	Low Latency 100G Ethernet MAC and PHY: IP-100GEUMACPHY
	Low Latency 100G Ethernet MAC and PHY with 1588: IP-100GEUMACPHYF
Vendor ID	6AF7

  ⊠ **Subscribe**   💬 **Send Feedback**

The following sections explain how to install, parameterize, simulate, and initialize the LL 100GbE IP core:

Installation and Licensing for LL 100GbE IP Core for Stratix V Devices on page 2-2
The LL 100GbE IP core that targets a Stratix V device is an extended IP core which is not included with the Quartus Prime release. This section provides a general overview of the Intel extended FPGA IP core installation process to help you quickly get started with any Intel extended FPGA IP core.

Installing and Licensing IP Cores on page 2-3
The LL 100GbE IP core that targets an Arria 10 device is a standard Intel FPGA IP core in the Intel FPGA IP Library.

Specifying the IP Core Parameters and Options on page 2-4
The LL 100GbE IP core for Arria 10 devices supports a standard customization and generation process from the Quartus Prime IP Catalog. After you install and integrate the extended IP core in the ACDS release, the LL 100GbE IP core for Stratix V devices also supports the standard customization and generation process. The LL 100GbE IP core is not supported in Qsys.

IP Core Parameters on page 2-5
The LL 100GbE parameter editor provides the parameters you can set to configure the LL 100GbE IP core and simulation and hardware design examples.

Files Generated for Stratix V Variations on page 2-11
The Quartus Prime Standard Edition software generates the following output for your Stratix V LL 100GbE IP core.

Files Generated for Arria 10 Variations on page 2-12
The Quartus Prime software generates the following IP core output file structure when targeting Arria 10 devices.

Integrating Your IP Core in Your Design on page 2-16

IP Core Testbenches on page 2-21
Intel provides a testbench, a hardware design example, and a compilation-only design example with most variations of the LL 100GbE IP core. The testbench is available for simulation of your IP core, and the hardware design example can be run on hardware. You can run the testbench to observe the IP core behavior on the various interfaces in simulation.

Compiling the Full Design and Programming the FPGA on page 2-26

Initializing the IP Core on page 2-26

ALTERA
now part of Intel

Related Information

- **Introduction to Intel FPGA IP Cores**
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- **Creating Version-Independent IP and Qsys Simulation Scripts**
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- **Project Management Best Practices**
  Guidelines for efficient management and portability of your project and IP files.

Installation and Licensing for LL 100GbE IP Core for Stratix V Devices

The LL 100GbE IP core that targets the Stratix V device family is an extended IP core which is not included with the Quartus Prime release. This section provides a general overview of the Intel extended FPGA IP core installation process to help you quickly get started with any Intel extended FPGA IP core.

The Intel extended FPGA IP cores are available from the Self-Service Licensing Center (SSLC). Refer to Related Links below for the correct link for this IP core.

Figure 2-1: IP Core Directory Structure

Directory structure after you install the LL 100GbE IP core.

Note: At the time of publication, the most recent LL 100GbE IP core available from the SSLC is a combined Low Latency 40-100GbE IP core compatible with the Quartus Prime Standard Edition software v16.0.

```
<path>
Installation directory
    ip
    Contains the  Altera IP Library and third-party IP cores
        altera_cloud
        Contains the  Altera extended IP cores that you install
            ethernet
            Contains the Ethernet extended IP cores that you install
                alt_eth_ultra
                Contains the  LL 100-Gbps Ethernet IP core files
```
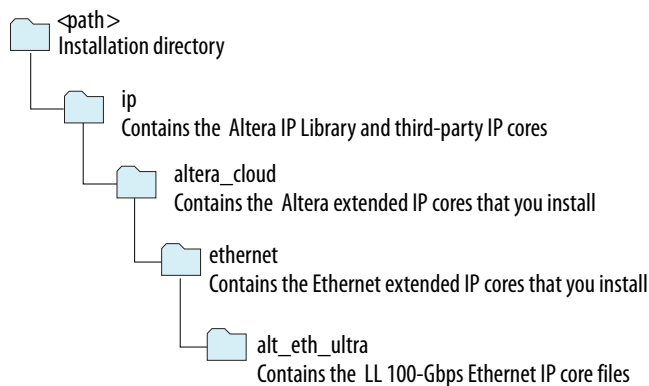
Table 2-1: Default Quartus Prime Standard Edition Installation Locations

Lists the default location of *<path>*. The Stratix V LL 100GbE IP core available in the SSLC at the time of publication is compatible with the Quartus Prime Standard Edition software v16.0.

Default Location in 16.1 Release	Default Location in 16.0 Release	Platform
<drive>:\intelFPGA\quartus\ *<version number>*\	*<drive>*:\altera\quartus*<version number>*\	Windows
<home directory>:/intelFPGA/ quartus/*<version number>*	*<home directory>*:/opt/altera/ quartus/*<version number>*	Linux

You can evaluate an IP core in simulation and in hardware until you are satisfied with its functionality and performance. You must purchase a license for the IP core when you want to take your design to production. After you purchase a license for an Intel FPGA IP core, you can request a license file from the Licensing page of the Altera website and install the license on your computer.

Related Information

- **Intel website**
- **Intel Licensing website**
- **Intel Self-Service Licensing Center**
  After you purchase the LL 100GbE IP core that supports Stratix V devices, the IP core is available for download from the SSLC page in your My Intel account. Intel requires that you create a My Intel account if you do not have one already, and log in to access the SSLC. On the SSLC page, click Run for this IP core. The SSLC provides an installation dialog box to guide your installation of the IP core.

Installing and Licensing IP Cores

The Quartus Prime software installation includes the Intel FPGA IP library. This library provides useful IP core functions for your production use without the need for an additional license. Some MegaCore IP functions in the library require that you purchase a separate license for production use. The OpenCore® feature allows evaluation of any Intel FPGA IP core in simulation and compilation in the Quartus Prime software. Upon satisfaction with functionality and performance, visit the Self Service Licensing Center to obtain a license number for any Intel FPGA product.

The Quartus Prime software installs IP cores in the following locations by default:

Figure 2-2: IP Core Installation Path

📁 **intelFPGA(_pro*)**
└── 📁 **quartus -** Contains the Quartus Prime software
└── 📁 **ip -** Contains the IP library and third-party IP cores
    └── 📁 **altera -** Contains the IP library source code
        └── 📁 *<IP core name>* - Contains the IP core source files
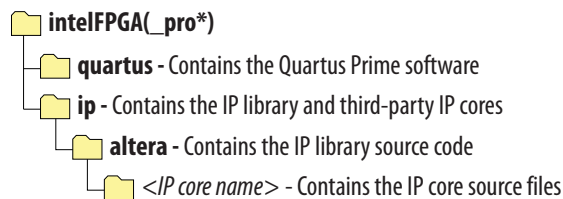
Table 2-2: IP Core Installation Locations

Location	Software	Platform
<drive>:\intelFPGA_pro\quartus\ip\ altera	Quartus Prime Pro Edition	Windows
<drive>:\intelFPGA\quartus\ip\altera	Quartus Prime Standard Edition	Windows
<home directory>:/intelFPGA_pro/ quartus/ip/altera	Quartus Prime Pro Edition	Linux
<home directory>:/intelFPGA/quartus/ ip/altera	Quartus Prime Standard Edition	Linux

Related Information

Release Information on page 1-8
Provides the licensing product codes for the IP core.

OpenCore Plus IP Evaluation

The free OpenCore Plus feature allows you to evaluate licensed MegaCore IP cores in simulation and hardware before purchase. Purchase a license for MegaCore IP cores if you decide to take your design to production. OpenCore Plus supports the following evaluations:

- Simulate the behavior of a licensed IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

OpenCore Plus evaluation supports the following two operation modes:

- Untethered—run the design containing the licensed IP for a limited time.
- Tethered—run the design containing the licensed IP for a longer time or indefinitely. This operation requires a connection between your board and the host computer.

Note: All IP cores that use OpenCore Plus time out simultaneously when any IP core in the design times out.

Related Information

- **Quartus Prime Licensing Site**
- **Quartus Prime Installation and Licensing**

Specifying the IP Core Parameters and Options

The LL 100GbE parameter editor allows you to quickly configure your custom IP variation. Use the following steps to specify IP core options and parameters in the Quartus Prime software.

1. In the IP Catalog (**Tools** > **IP Catalog**), select a target device family. The LL 100GbE IP core is not supported in Qsys.
2. In the IP Catalog, locate and double-click the name of the IP core to customize (**Low Latency 100G Ethernet**). The New IP Variation window appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file with one of the following names:

   - *<your_ip>*.qsys (for Arria 10 variations generated in the Quartus Prime Standard Edition software)
   - *<your_ip>*.ip (for Arria 10 variations generated in the Quartus Prime Pro Edition software)
   - *<your_ip>*.qip (for Stratix V variations)

4. If your IP core targets the Arria 10 device family, you must select a specific device in the **Device** field or maintain the default device the Quartus Prime software lists. If you target a specific Intel development kit, the hardware design example overwrites the selection with the device on the target board.
5. Click **OK**. The parameter editor appears.
6. Specify the parameters and options for your IP variation in the parameter editor, including one or more of the following. Refer to your IP core user guide for information about specific IP core parameters.

- Specify parameters defining the IP core functionality, port configurations, and device-specific features.
- Specify options for processing the IP core files in other EDA tools.
- A functional VHDL IP core is not available. Specify Verilog HDL only, for your IP core variation.

7. For Arria 10 variations, follow these steps:

  a. Optionally, to generate a simulation testbench or example project, follow the instructions in **Generating the LL 100GbE Testbench** on page 2-23.

  b. Click **Generate HDL**. The **Generation** dialog box appears.

  c. Specify output file generation options, and then click **Generate**. The IP variation files generate according to your specifications.

  d. Click **Finish**. The parameter editor adds the top-level `.qsys` file to the current project automatically. If you are prompted to manually add the `.qsys` or `.ip` file to the project, click **Project** > **Add/Remove Files in Project** to add the file.

8. For Stratix V variations, follow these steps:

  a. Click **Finish**.

  b. Optionally, to generate a simulation testbench or example project, follow the instructions in **Generating the LL 100GbE Testbench** on page 2-23.

     After you click Finish and optionally follow the additional step to generate a simulation testbench and example project, if available for your IP core variation, the parameter editor adds the top-level `.qip` file to the current project automatically. If you are prompted to manually add this file to the project, click **Project** > **Add/Remove Files in Project** to add the file.

9. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

IP Core Parameters

The LL 100GbE parameter editor provides the parameters you can set to configure the LL 100GbE IP core and simulation and hardware design examples.

LL 100GbE IP core variations that target an Arria 10 device include an **Example Design** tab. For information about that tab, refer to the *Low Latency 100G Ethernet Design Example User Guide*.

Table 2-3: LL 100GbE Parameters: Main Tab

Describes the parameters for customizing the LL 100GbE IP core on the Main tab of the LL 100GbE parameter editor.

Parameter	Type	Range	Default Setting	Parameter Description
General Options				
Device family	String	• Stratix V • Arria 10	According to the setting in the project or IP Catalog settings.	Selects the device family.

Parameter	Type	Range	Default Setting	Parameter Description
Data interface	String	• Custom–ST • Avalon–ST	Avalon–ST	Selects the Avalon–ST interface or the narrower, custom streaming client interface to the MAC. If you select the custom streaming client interface, the **Flow control mode** and **Enable 1588 PTP** parameters are not available.
PCS/PMA Options				
Enable CAUI4 PCS	Boolean	• True • False	False	If this parameter is turned on, the IP core is a 100GbE CAUI-4 variation, with four 25.78125 Gbps transceiver PHY links. If this parameter is turned off, the IP core is configured with the regular 100 Gbps PHY link option of 10 x 10.3125 Gbps. This parameter is available only in variations that target an Arria 10 device.
Enable RS-FEC for CAUI4	Boolean	• True • False	False	If this parameter is turned on, the IP core implements Reed-Solomon forward error correction (FEC). This parameter is available only in CAUI-4 variations. CAUI-4 variations must target an Arria 10 device.
Enable SyncE	Boolean	• True • False	False	Exposes the RX recovered clock as an output signal. This feature supports the Synchronous Ethernet standard described in the ITU-T G.8261, G.8262, and G.8264 recommendations. This parameter is available only in variations that target an Arria 10 device.
PHY reference frequency	Integer (encoding)	• 322.265625 MHz • 644.53125 MHz	644.53125 MHz	Sets the expected incoming PHY `clk_ref` reference frequency. The input clock frequency must match the frequency you specify for this parameter (± 100ppm).

Parameter	Type	Range	Default Setting	Parameter Description
Use external TX MAC PLL	Boolean	• True • False	False	If you turn this option on, the IP core is configured to expect an input clock to drive the TX MAC. The input clock signal is `clk_txmac_in`.
Flow Control Options				
Flow control mode	String	• No flow control • Standard flow control • Priority-based flow control	No flow control	Configures the flow control mechanism the IP core implements. Standard flow control is Ethernet standard flow control. If you select the custom streaming client interface, the IP core must be configured with no flow control, and this parameter is not available.
Number of PFC queues	Integer	1–8	8	Number of distinct priority queues for priority-based flow control. This parameter is available only if you set **Flow control mode** to **Priority-based flow control**.
Average interpacket gap	String	• Disable deficit idle counter • 8 • 12	12	If you set the value of this parameter to **8** or to **12**, the IP core includes a deficit idle counter (DIC), which maintains an average interpacket gap (IPG) of 8 or 12, as you specify. If you set the value of this parameter to **Disable deficit idle counter**, the IP core is configured without the DIC, and does not maintain the required minimum average IPG. The Ethernet standard requires a minimum average IPG of 12. Turning off the DIC increases bandwidth.
MAC Options				
Enable 1588 PTP	Boolean	• True • False	False	If turned on, the IP core supports the IEEE Standard 1588-2008 Precision Clock Synchronization Protocol, by providing the hooks to implement the Precise Timing Protocol (PTP). If you select the custom streaming client interface, the IP core must be configured without 1588 support, and this parameter is not available.

Parameter	Type	Range	Default Setting	Parameter Description
Enable 96b Time of Day Format	Boolean	• True • False	True	Include the 96-bit interface to the TOD module. If you turn on this parameter, the TOD module that is generated with the IP core has a matching 96-bit timestamp interface. If **Enable 1588 PTP** is turned on, you must turn on at least one of **Enable 96b Time of Day Format** and **Enable 64b Time of Day Format**. You can turn on both **Enable 96b Time of Day Format** and **Enable 64b Time of Day Format** to generate a TOD interface for each format. This parameter is available only in variations with **Enable 1588 PTP** turned on.
Enable 64b Time of Day Format	Boolean	• True • False	False	Include the 64-bit interface to the TOD module. If you turn on this parameter, the TOD module that is generated with the IP core has a matching 64-bit timestamp interface. If **Enable 1588 PTP** is turned on, you must turn on at least one of **Enable 96b Time of Day Format** and **Enable 64b Time of Day Format**. You can turn on both **Enable 96b Time of Day Format** and **Enable 64b Time of Day Format** to generate a TOD interface for each format. This parameter is available only in variations with **Enable 1588 PTP** turned on.
Timestamp fingerprint width	Integer	1–16	1	Specifies the number of bits in the fingerprint that the IP core handles. This parameter is available only in variations with **Enable 1588 PTP** turned on.

Parameter	Type	Range	Default Setting	Parameter Description
Enable link fault generation	Boolean	• True • False	False	If turned on, the IP core includes the link fault signaling modules and relevant signals. If turned off, the IP core is configured without these modules and without these signals. Turning on link fault signaling provides your design a tool to improve reliability, but increases resource utilization.
Enable TX CRC insertion	Boolean	• True • False	True	If turned on, the IP core inserts a 32-bit Frame Check Sequence (FCS), which is a CRC-32 checksum, in outgoing Ethernet frames. If turned off, the IP core does not insert the CRC-32 sequence in outgoing Ethernet communication. Turning on TX CRC insertion improves reliability but increases resource utilization and latency through the IP core. If you turn on flow control, the IP core must be configured with TX CRC insertion, and this parameter is not available.
Enable preamble passthrough	Boolean	• True • False	False	If turned on, the IP core is in RX and TX preamble pass-through mode. In RX preamble pass-through mode, the IP core passes the preamble and SFD to the client instead of stripping them out of the Ethernet packet. In TX preamble pass-through mode, the client specifies the preamble to be sent in the Ethernet frame.

Parameter	Type	Range	Default Setting	Parameter Description
Enable alignment EOP on FCS word	Boolean	• True • False	True	If turned on, the IP core aligns the 32-bit Frame Check Sequence (FCS) error signal with the assertion of the EOP by delaying the RX data bus to match the latency of the FCS computation. If turned off, the IP core does not delay the RX data bus to match the latency of the FCS computation. If the parameter is turned off, the FCS error signal, in the case of an FCS error, is asserted in a later clock cycle than the relevant assertion of the EOP signal. Intel recommends that you turn on this option. Otherwise, the latency between the EOP indication and assertion of the FCS error signal is non-deterministic. You must turn on this parameter if your design relies on the `rx_inc_octetsOK` signal..
Enable TX statistics	Boolean	• True • False	True	If turned on, the IP core includes built–in TX statistics counters. If turned off, the IP core is configured without TX statistics counters. In any case, the IP core is configured with TX statistics counter increment output vectors.
Enable RX statistics	Boolean	• True • False	True	If turned on, the IP core includes built–in RX statistics counters. If turned off, the IP core is configured without RX statistics counters. In any case, the IP core is configured with RX statistics counter increment output vectors.

Configuration, Debug and Extension Options

Parameter	Type	Range	Default Setting	Parameter Description
Enable Altera Debug Master Endpoint (ADME)	Boolean	• True • False	False	If turned on, the IP core turns on the following features in the Arria 10 PHY IP core that is included in the LL 100GbE IP core: • **Enable Altera Debug Master Endpoint (ADME)** • **Enable capability registers** If turned off, the IP core is configured without these features. This parameter is available only in variations that target an Arria 10 device. For information about these Arria 10 features, refer to the **Arria 10 Transceiver PHY User Guide**.

Table 2-4: LL 100GbE PHY Parameter Settings

Lists the PHY parameters that are configured automatically based on parameter values you select in the LL 100GbE parameter editor.

Parameter	LL 100GbE Standard Variations	LL 100GbE CAUI–4 Variations (Arria 10 Devices)
Lanes	10	4
Data rate per lane	10312.5 Mbps	25781.25 Mbps
Available PHY reference clock frequencies	322.265625 MHz 644.53125 MHz	322.265625 MHz 644.53125 MHz

Related Information

- **Clocks** on page 3-57
  The **PHY reference frequency** value is the required frequency of the transceiver reference clock.
- **Arria 10 Transceiver PHY User Guide**
  Information about Arria 10 Native PHY IP core features, including ADME.
- **Low Latency 100G Ethernet Design Example User Guide**
  Information about the **Example Design** tab in the Arria 10 LL 100GbE parameter editor.

Files Generated for Stratix V Variations

The Quartus Prime Standard Edition software generates the following output for your Stratix V LL 100GbE IP core.

Figure 2-3: LL 100GbE IP Core Generated Files for Stratix V Variations

```
📁 <Project Directory>
   📄 <your_ip>.qip - Quartus Prime IP integration file
   📄 <your_ip>.v, .sv, or .vhd - Top-level IP synthesis file
   📁 <your_ip> - IP core synthesis files
      📄 <your_ip>.sv, .v, or .vhd - HDL synthesis files
      📄 <your_ip>.sdc - Timing constraints file
   📄 <your_ip>.bsf - Block symbol schematic file
   📄 <your_ip>.cmp - VHDL component declaration file
   📄 <your_ip>_syn.v or .vhd - Timing & resource estimation netlist[1]
   📄 <your_ip>.sip - Lists files for simulation
   📄 <your_ip>.ppf - XML I/O pin information file
   📄 <your_ip>.spd - Combines individual simulation scripts
   📄 <your_ip>_sim.f - Refers to simulation models and scripts
   📁 <your_ip>_sim - IP core simulation files
      📁 <your_ip>.v
      📁 <simulator_vendor>
         📄 <simulator setup scripts>
   📁 <your_ip>_example_design - Testbench and example project[1]
```

Notes:
1. If generated for your IP variation

Files Generated for Arria 10 Variations

The Quartus Prime software generates the following IP core output file structure when targeting Arria 10 devices.

For information about the file structure of the design example, refer to the *LL 100GbE Design Example User Guide*.

Figure 2-4: LL 100GbE IP Core Generated Files for Arria 10 Variations

<project directory>

    <your_ip>**.qsys** or **.ip** - System or IP integration file

    <your_ip>**.sopcinfo** - Software tool-chain integration file
    (Standard Edition only)

<your_ip>
IP variation files   • • • •   **<your_ip>_<n>**
IP variation files

alt_eth_ultra_100_0_example_design

Example location for your IP core
design example files. The default location is
alt_eth_ultra_100_0_example_design
in your Quartus entry directory.
You are prompted to specify a different path

    <your_ip>**.cmp** - VHDL component declaration file

    <your_ip>**_bb.v** - Verilog HDL black box EDA synthesis file

    <your_ip>**_inst.v** or **.vhd** - Sample instantiation template

    <your_ip>**.ppf** - XML I/O pin information file

    <your_ip>**.qgsimc** - Lists simulation parameters to support incremental regeneration (Pro Edition only)

    <your_ip>**.qgsynthc** - Lists synthesis parameters to support incremental regeneration (Pro Edition only)

    <your_ip>**.qip** - Lists IP synthesis files

    <your_ip>**.sip** - Lists files for simulation

    <your_ip>**_generation.rpt** - IP generation report

    <your_ip>**.debuginfo** - Contains post-generation information (Standard Edition only)

    <your_ip>**.html** - Connection and memory map data

    <your_ip>**.bsf** - Block symbol schematic

    <your_ip>**.spd** - Combines individual simulation scripts

sim
Simulation files

synth
IP synthesis files

<ip subcores_ver>
Subcore libraries

    <your_ip>**.v** or **.vhd**
    Top-level simulation file

    <your_ip>**.v** or **.vhd**
    Top-level IP synthesis file

<EDA tool name>
Simulator scripts

synth
Subcore
synthesis files

sim
Subcore
Simulation files

    <simulator_setup_scripts>

    <HDL files>

    <HDL files>