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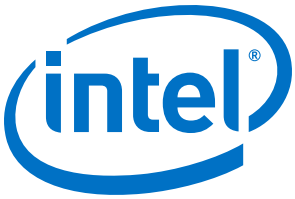

Interlaken (2nd Generation) Intel® Stratix® 10 FPGA IP User Guide

Updated for Intel® Quartus® Prime Design Suite: **18.1**

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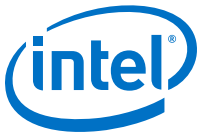
Contents

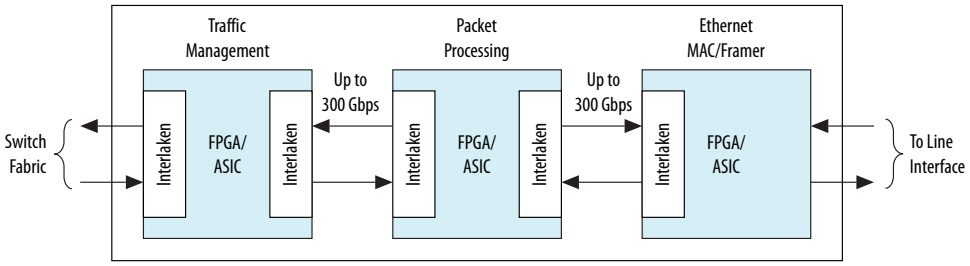


1. About this IP Core

Interlaken is a high-speed serial communication protocol for chip-to-chip packet transfers. The Interlaken (2nd Generation) Intel® FPGA IP implements the *Interlaken Protocol Specification, Revision 1.2*. It supports multiple combinations of number of lanes (4 to 12) and lane rates from 6.25 gigabits per second (Gbps) to 53.125 Gbps, on Intel Stratix® 10 devices, providing raw bandwidth of 25 Gbps to 300 Gbps.

Interlaken provides low I/O count compared to earlier protocols, supporting scalability in both number of lanes and lane speed. Other key features include flow control, low overhead framing, and extensive integrity checking. The Interlaken IP core incorporates a physical coding sublayer (PCS), a physical media attachment (PMA), and a media access control (MAC) block.

Figure 1. Typical Interlaken Application



Related Information

- Interlaken IP Core (2nd Generation) Design Example User Guide
  Describes a simulating testbench and a hardware example design that supports compilation and hardware testing.
- Interlaken Protocol Specifications

1.1. Features

The Interlaken (2nd Generation) Intel Stratix 10 FPGA IP core has the following features:

- Compliant with the Interlaken Protocol Specification, Revision 1.2.
- Supports 4, 6, and 12 serial lanes in configurations that provide up to 318.75 Gbps raw bandwidth.
- Supports per-lane data rates of 6.25, 10.3125, 12.5, 25.3, 25.8 and 53.125 Gbps using Intel FPGA on-chip high-speed transceivers.
- Supports dynamically configurable BurstMax and BurstMin values.
- Supports Packet mode and Interleaved mode for user data transfer.
- Supports up to 256 logical channels in out-of-the-box configuration.

- Supports optional user-controlled in-band flow control with 1, 2, 4, 8, or 16 16-bit calendar pages.
- Supports optional out-of-band flow control blocks.
- Supports memory block ECC.
- Supports per-lane data rate of 53.125 Gbps using pulse amplitude modulation (PAM4) mode in Intel Stratix 10 E-Tile variations
- Supports per lane data rates of 12.5, 25.3, and 25.8 Gbps using non-return-to-zero (NRZ) mode in Intel Stratix 10 E-Tile variations.

Table 1. IP Core Supported Combinations of Number of Lanes and Data Rate

The following combinations are supported in Intel Quartus® Prime Pro Edition 18.1

Device	IP Core Supported Combinations	
	Number of Lanes	Lane Rate (Gbps)
Intel Stratix 10 L-Tile	4	6.25
	12	10.3125
	12	12.5
Intel Stratix 10 H-Tile	4	6.25
	6	25.3
	6	25.8
	12	10.3125
	12	12.5
	12	25.3
	12	25.8
Intel Stratix 10 E-Tile (NRZ)	6	25.3
	6	25.8
	12	12.5
	12	25.3
	12	25.8
Intel Stratix 10 E-Tile (PAM4)	12	26.5625 *Note:* To obtain 6x53.125 Gbps speed in PAM4 mode, you must select 12x26.5625 Gbps combination in Intel Quartus Prime Pro Edition 18.1

Table 2. IP Core Theoretical Raw Aggregate Bandwidth

The following combinations are supported in Intel Quartus Prime Pro Edition 18.1

Number of Lanes	Lane Rate (Gbps)						Number of Words	Data Width (bits)
	6.25	10.3125	12.5	25.3	25.8	26.5625		
4	25	-	-	-	-	-	4	256
6	-	-	-	151.8	154.8	-	8	512
12	-	123.75	150	-	-	-	8	512
12	-	-	-	303.6	309.6	318.75	16	1024

Related Information

Interlaken Protocol Specifications

1.2. Device Family Support

The following lists the device support level definitions for Intel FPGA IP cores:

- **Advance support** — The IP core is available for simulation and compilation for this device family. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
- **Preliminary support** — The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.
- **Final support** — The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Table 3. Device Family Support

Device Family	Support
Intel Stratix 10	Advance

1.3. Performance and Resource Utilization

Lists the resources and expected performance for selected variations of the Interlaken IP core using the Intel Quartus Prime Pro Edition 18.0.1. The numbers of ALMs and logic registers are rounded up to the nearest 100.

Table 4. FPGA Resource Utilization

Device	Parameters		Resource Utilization			
	Number of Lanes	Data/Lane Rate (Gbps)	ALMs needed	Logic Registers		M20K Blocks
				Primary	Secondary	
Intel Stratix 10 L-Tile	4	6.25	8300	16600	4800	28
	12	10.3125	18300	39400	9700	52
	12	12.5	18400	39200	9700	52
Intel Stratix 10 H-Tile	6	25.3	19700	39700	9600	52
	12	25.3	32900	69800	14000	100
Intel Stratix 10 E-Tile (NRZ)	6	25.3	28000	49500	12800	52
	12	12.5	45000	83300	19400	73
	12	25.3	48500	92000	19700	100
Intel Stratix 10 E-Tile (PAM4)	6	53.125	61300	111900	22600	100

1.4. Release Information

Table 5. IP Core Release Information

Item	Value	
Version	Intel Quartus Prime Pro Edition 18.1	
Release Date	2018.09.24	
Ordering Code	**Aggregate Bandwidth**	**Ordering Code**
	20G to <100G	IP-ILKN/50G
	100G to <200G	IP-ILKN/100G
	200G to <400G	IP-ILKN/200G

2. Getting Started

The following sections explain how to install, parameterize, simulate, and initialize the Interlaken IP core.

Related Information

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Generating a Combined Simulator Setup Script
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

2.1. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 2. IP Core Installation Path

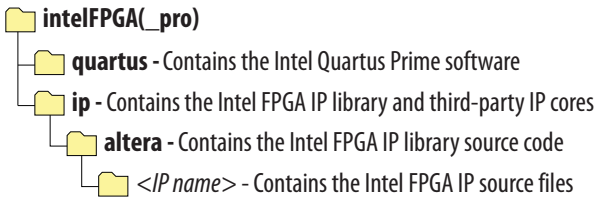


Table 6. IP Core Installation Locations

Location	Software	Platform
<drive>:\intelFPGA_pro\quartus\ip\altera	Intel Quartus Prime Pro Edition	Windows*
<home directory>:/intelFPGA_pro/quartus/ip/altera	Intel Quartus Prime Pro Edition	Linux*

2.1.1. Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

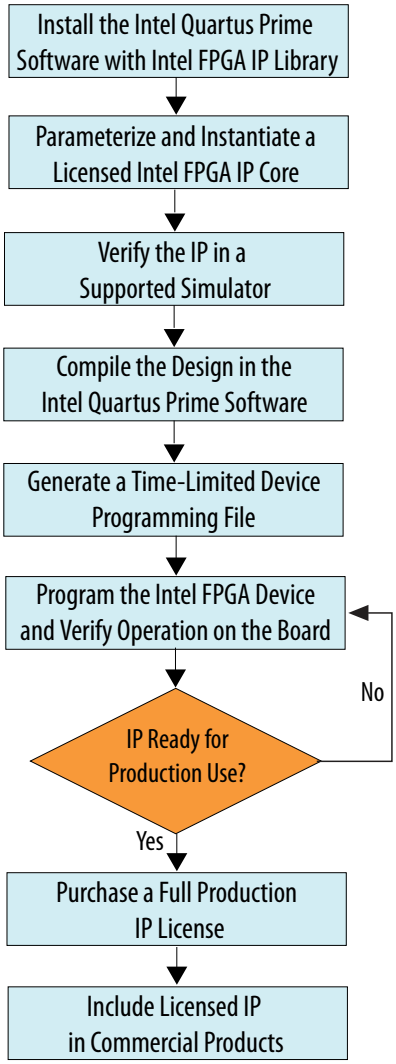
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (*<project name>*`_time_limited.sof`) that expires at the time limit.

Figure 3. Intel FPGA IP Evaluation Mode Flow



Note: Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (*<project name>*`_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the Self-Service Licensing Center or contact your local Intel FPGA representative.

The Intel FPGA Software License Agreements govern the installation and use of licensed IP cores, the Intel Quartus Prime design software, and all unlicensed IP cores.

Related Information

- Intel Quartus Prime Licensing Site
- Intel FPGA Software Installation and Licensing

2.2. Generated File Structure

The Intel Quartus Prime Pro Edition software generates the following IP core output file structure.

For more information about the file structure of the design example, refer to the *Interlaken IP Core (2nd Generation) Design Example User Guide*.

Figure 4. IP Core Generated Files

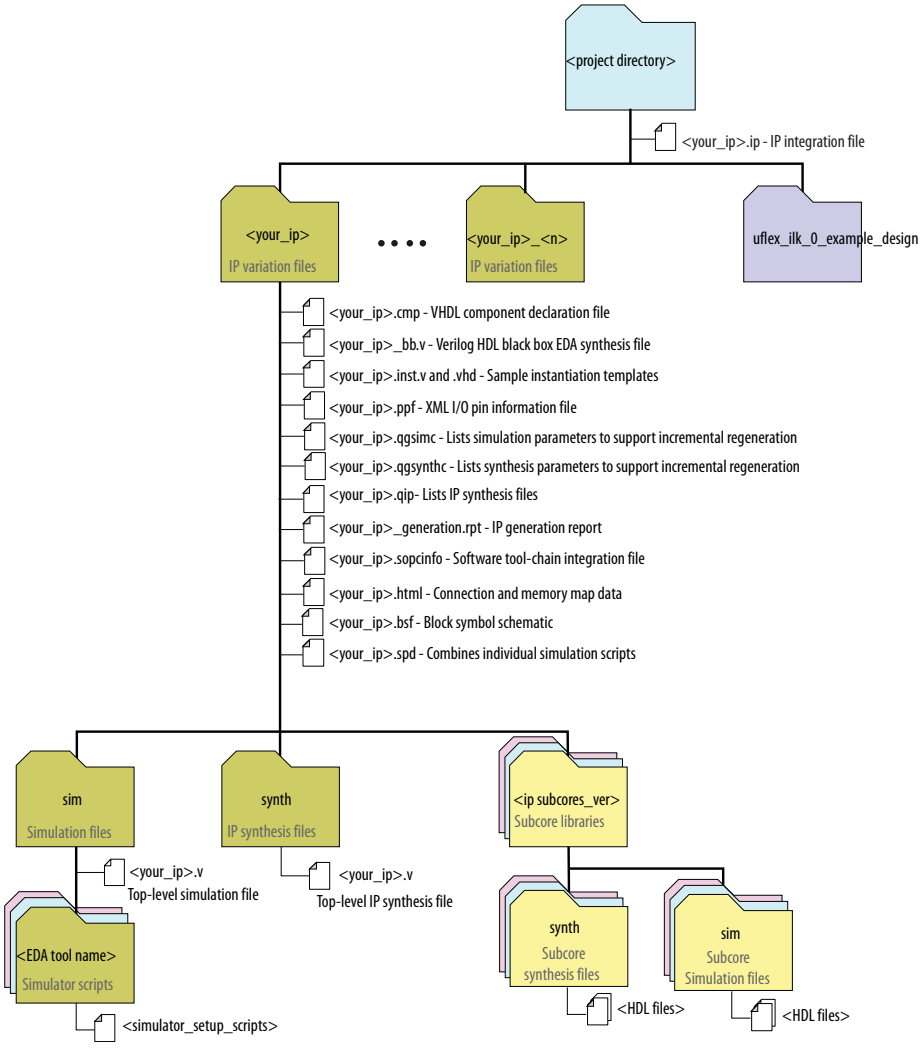


Table 7. IP Core Generated Files

File Name	Description
<*your_ip*>.ip	The top-level IP variation file. <*your_ip*> is the name that you give your IP variation.
<*your_ip*>.cmp	The VHDL Component Declaration (**.cmp**) file is a text file that contains local generic and port definitions that you can use in VHDL design files. This IP core does not support VHDL. However, the Intel Quartus Prime Pro Edition software generates this file.
<*your_ip*>.html	A report that contains connection information, a memory map showing the address of each slave with respect to each master to which it is connected, and parameter assignments.
<*your_ip*>_generation.rpt	IP or Platform Designer generation log file. A summary of the messages during IP generation.
<*your_ip*>.qgsimc	Lists simulation parameters to support incremental regeneration.
<*your_ip*>.qgsynthc	Lists synthesis parameters to support incremental regeneration.
<*your_ip*>.qip	Contains all the required information about the IP component to integrate and compile the IP component in the Intel Quartus Prime software.
<*your_ip*>.sopcinfo	Describes the connections and IP component parameterizations in your Platform Designer system. You can parse its contents to get requirements when you develop software drivers for IP components.
<*your_ip*>.csv	Contains information about the upgrade status of the IP component.
<*your_ip*>.bsf	A Block Symbol File (.**bsf**) representation of the IP variation for use in Intel Quartus Prime Block Diagram Files (**.bdf**).
<*your_ip*>.spd	Required input file for `ip-make-simscript` to generate simulation scripts for supported simulators. The **.spd** file contains a list of files generated for simulation, along with information about memories that you can initialize.
<*your_ip*>.ppf	The Pin Planner File (**.ppf**) stores the port and node assignments for IP components created for use with the Pin Planner.
<*your_ip*>_bb.v	You can use the Verilog black-box (**_bb.v**) file as an empty module declaration for use as a black box.
<*your_ip*>_inst.v or _inst.vhd	HDL example instantiation template. You can copy and paste the contents of this file into your HDL file to instantiate the IP variation. This IP core does not support VHDL. However, the Intel Quartus Prime Pro Edition software generates the _inst.vhd file.
<*your_ip*>.v	HDL files that instantiate each submodule or child IP core for synthesis or simulation.
mentor/	Contains a ModelSim* script msim_setup.tcl to set up and run a simulation.
synopsys/vcs/ synopsys/vcsmx/	Contains a shell script vcs_setup.sh to set up and run a VCS* simulation. Contains a shell script vcsmx_setup.sh and synopsys_ sim.setup file to set up and run a VCS MX* simulation.
cadence/	Contains a shell script ncsim_setup.sh and other setup files to set up and run an NCSim* simulation.
xcelium/	Contains a shell script xcelium_setup.sh to set up and run simulation.
submodules/	Contains HDL files for the IP core submodules.
<*child IP cores*>/	For each generated child IP core directory, Platform Designer generates synth/ and sim/ sub-directories.

Related Information

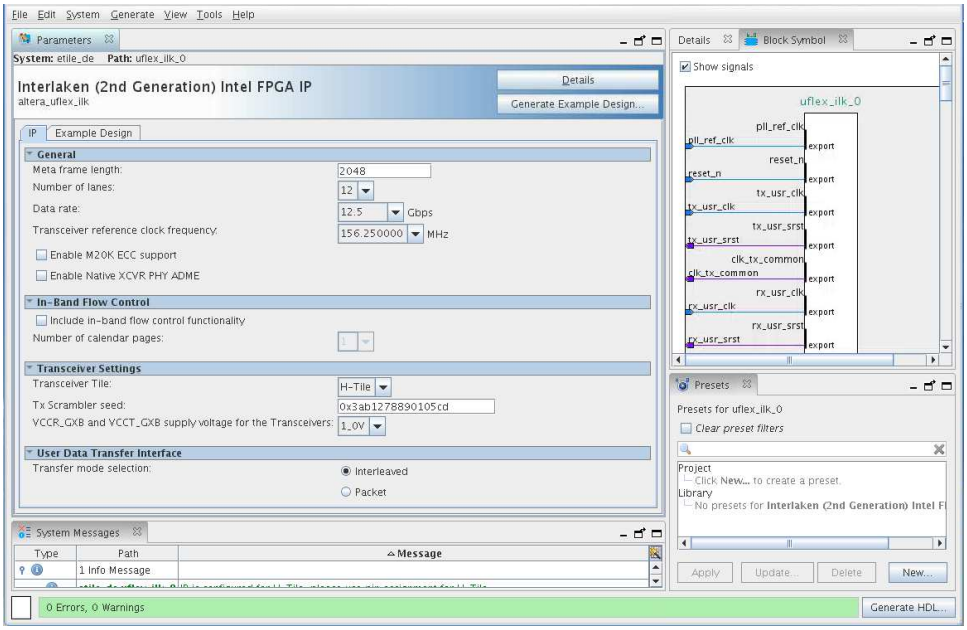
Interlaken IP Core (2nd Generation) Design Example User Guide

2.3. Specifying the IP Core Parameters and Options

The IP parameter editor allows you to quickly configure your custom IP variation. Perform the following steps to specify IP core options and parameters in the Intel Quartus Prime Pro Edition software.

The Interlaken IP core is not supported in Platform Designer. You must use the IP Catalog accessible from the Intel Quartus Prime Pro Edition **Tools** menu. The Interlaken IP core does not support VHDL simulation models. You must specify the Verilog HDL for both synthesis and simulation models.

Figure 5. IP Parameter Editor



1. In the Intel Quartus Prime Pro Edition software, click **File ➤ New Project Wizard** to create a new Intel Quartus Prime project, or **File ➤ Open Project** to open an existing Intel Quartus Prime project. The wizard prompts you to specify a device. Select **Stratix 10 (GX/SX/MX/TX)** as your target device.
2. In the IP Catalog (**Tools ➤ IP Catalog**), locate and double-click **Interlaken (2nd Generation) Intel FPGA IP**. The **New IP Variant** window appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named *<your_ip>*`.ip`.
4. Click **Create**. The parameter editor appears.
5. On the **IP** tab, specify the parameters and options for your IP variation, including one or more of the following. Refer to *Parameter Settings* for information about specific IP core parameters.

- Specify parameters defining the IP core functionality, port configurations, and device-specific features.
- Specify options for processing the IP core files in other EDA tools.

6. Click **Generate HDL**. The **Generation** dialog box appears.
7. Specify output file generation options, and then click **Generate**. The IP variation files generate according to your specifications.
8. Optionally, click **Generate Example Design** tab in the parameter editor to generate a demonstration testbench and example design for your IP core variation.

   Note: To generate the demonstration testbench and example design, you must specify Verilog HDL for both synthesis and simulation models.
9. Click **Finish**. The parameter editor adds the top-level `.ip` file to the project automatically. If you are prompted to manually add the `.ip` file to the project, click **Project ➤ Add/Remove Files in Project** to add the file.
10. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

Related Information

- Interlaken IP Core (2nd Generation) Design Example User Guide
  Describes a simulating testbench and a hardware example design that supports compilation and hardware testing.
- Parameter Settings on page 17

2.4. Simulating the IP Core

You can simulate your Interlaken IP core variation using any of the vendor-specific IEEE encrypted functional simulation models which are generated in the new `<instance name>/sim/<simulator>` subdirectory of your project directory.

The Interlaken IP core supports the Synopsys VCS, Mentor Graphics Modelsim-SE*, and Cadence NCSim and Xcelium Parallel simulators. The Interlaken IP core generates a Verilog HDL and VHDL simulation model and testbench. The IP core parameter editor offers you the option of generating a Verilog HDL or VHDL simulation model for the IP core, but the IP core design example does not support a VHDL simulation model or testbench.

For more information about functional simulation models for Intel FPGA IP cores, refer to the *Simulating Intel FPGA Designs* chapter in *Quartus Prime Pro Edition Handbook Volume 3: Verification*.

Related Information

Simulating Intel FPGA Designs

2.5. Compiling the Full Design and Programming the FPGA

You can use the **Start Compilation** command on the **Processing** menu in the Intel Quartus Prime software to compile your design. After successfully compiling your design, program the targeted Intel device with the Programmer and verify the design in hardware.

Related Information

- Programming Intel FPGA Devices
- Design Compilation

2.6. Integrating Your IP Core in Your Design

2.6.1. Pin Assignment

When you integrate your IP core instance in your design, you must make appropriate pin assignments. You do not need to specify pin assignments for simulation. However, you should make the pin assignments before you compile, to provide direction to the Fitter and to specify the signals that should be assigned to device pins. While compiling the IP core alone, you can create virtual pins to avoid making specific pin assignments for top-level signals. When you are ready to map the design to hardware, you can change to the correct pin assignments.

Related Information

GX and GXT Channel Placement Guidelines

2.6.2. Adding the External PLL

The Interlaken (2nd Generation) IP core variations that target an Intel Stratix 10 L-Tile or H-Tile device require an external TX transceiver PLL to drive the TX transceiver clock, in order to compile and to function correctly in hardware. In many cases, the same PLL can be shared with other transceivers in your design.

You can create an external transceiver PLL from the IP Catalog:

- Select **L-Tile/H-Tile Transceiver ATX PLL Intel Stratix 10 FPGA IP**.
- In the parameter editor, set the following parameter values:
  - Set **PLL output frequency** to one half the per-lane data rate of the IP core variation.
  - Set **PLL auto mode reference clock frequency (integer)** to the value you select for the transceiver reference clock frequency (`pll_ref_clk`) parameter in the Interlaken (2nd Generation) IP parameter editor.
  - Set **VCCR_GXB and VCCT_GXB Supply Voltage for the transceiver** to the same value you specify in the Interlaken (2nd Generation) IP parameter editor.

You must connect `tx_serial_clock` output from the ATX PLL to `tx_serial_clk` input of your Interlaken (2nd Generation) IP core.

The Interlaken (2nd Generation) IP core variations that target an E-Tile device contains transceiver PLLs and do not require an external PLL for the transceivers. These transceiver PLLs require a reference clock (`pll_ref_clk`). Refer to the *Intel Stratix 10 E-Tile Transceiver PHY User Guide* and *Interlaken (2nd Generation) Design Example User Guide* for the reference clock connections.

The E-Tile PAM4 mode variations require an additional `mac_clkin` input clock generated by a PLL. This PLL must use the same reference clock source that drives the `pll_ref_clk`. Refer to *Figure: Interlaken (2nd Generation) Hardware Design*

Example High Level Block Diagram for E-Tile PAM4 Mode Variations in *Interlaken (2nd Generation) Intel FPGA IP Design Example User Guide* for more information on `mac_clkin` connections.

Related Information

- Interlaken IP Core (2nd Generation) Design Example User Guide
- Intel Stratix 10 E-Tile Transceiver PHY User Guide

3. Parameter Settings

You customize the Interlaken IP core by specifying parameters in the IP parameter editor.

Table 8. Interlaken IP Core Parameter Settings: IP Tab

Parameter	Supported Values	Default Setting	Description
General			
Meta frame length (words)	64-8192 words	2048	This parameter specifies the length of the meta frame, in 64-bit (8-byte) words. You must enter this parameter value in power of two. For example, 64, 128, 256 etc. Smaller values for this parameter shorten the time to achieve lock. Larger values reduce overhead while transferring data, after lock is achieved.
Number of lanes	4, 6, 12	12	This parameter specifies the number of lanes available for Interlaken communication. The Interlaken IP core supports various combinations of number of lanes and lane rates. Ensure that your parameter settings specify a supported combination. Refer to *Table: IP Core Supported Combinations of Number of Lanes and Data Rate* in this document.
Data rate	6.25, 10.3125, 12.5, 25.3, 25.8 and 26.5625(1) Gbps	10.3125 Gbps	This parameter specifies the data rate on each lane. All lanes have the same data rate (lane rate). The Interlaken IP core supports various combinations of number of lanes and lane rates. Ensure that your parameter settings specify a supported combination. Refer to *Table: IP Core Supported Combinations of Number of Lanes and Data Rate* in this document.
Transceiver reference clock frequency	Multiple	412.5 MHz	This parameter specifies the expected frequency of the `pll_ref_clk` input clock.

continued...

(1) This data rate is only available when you select PAM4 option for **XCVR Mode** parameter in Intel Stratix 10 E-Tile variations.

<table>
<tr><th>Parameter</th><th>Supported Values</th><th>Default Setting</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Data Rate per Lane (Gbps)</th><th>Valid Frequencies (MHz)</th></tr>
<tr><td>10.3125</td><td>206.25, 257.8125, 322.265625, 412.5, 515.625, 644.53125</td></tr>
<tr><td>12.5, 6.25</td><td>156.25, 195.3125, 250, 312.5, 390.625, 500, 625</td></tr>
<tr><td>25.3</td><td>126.4, 158.0, 197.5, 252.8, 320.0, 395.0, 486.153846(2), 505.6</td></tr>
<tr><td>25.8</td><td>159.135802, 201.40625, 250.291262, 322.25, 402.8125, 495.769231(2) 500.582524</td></tr>
<tr><td>26.5625
Note: To obtain 6x53.125 Gbps speed in PAM4 mode, you must select 12x26.5625 Gbps combination in Intel Quartus Prime Pro Edition 18.0.1</td><td>156.25, 210.813492, 312.5, 390.62, 491.898148</td></tr>
<tr><td colspan="2">If the actual frequency of the <code>pll_ref_clk</code> input clock does not match the value you specify for this parameter, the design fails in both simulation and hardware.</td></tr>
</table>
</td></tr>
<tr><td>Enable M20K ECC support</td><td>On/Off</td><td>Off</td><td>This parameter specifies whether your Interlaken IP core variation supports the ECC feature in the M20K memory blocks that are configured as part of the IP core.
You can turn this parameter on to enable single-error correct, double-adjacent-error correct, and triple-adjacent-error detect ECC functionality in the M20K memory</td></tr>
</table>

continued...

(2) Only available in NRZ mode of Intel Stratix 10 E-Tile device variations

Parameter	Supported Values	Default Setting	Description
			blocks configured in your IP core. This feature enhances data reliability but increases latency and resource utilization.
Enable Native XCVR PHY ADME	On/Off	Off	This parameter specifies whether your Interlaken IP core variation supports the ADME feature. This parameter exposes debugging features of the Intel Stratix 10 Native PHY IP core that specifies the transceiver settings in the Interlaken IP core.
In-Band Flow Control			
Include in-band flow control functionality	On/Off	Off	This parameter specifies whether your Interlaken IP core includes an in-band flow control block.
Number of calender pages	1, 2, 4, 8, and 16	1	This parameter specifies the number of 16-bit pages of in-band flow control data that your Interlaken IP core supports.This parameter is available if you turn on **Include in-band flow control functionality**. Each 16-bit calendar page includes 16 in-band flow control bits. The application determines the interpretation of the in-band flow control bits. The IP core supports a maximum of 256 channels with in-band flow control. If your design requires a different number of pages, select the lowest supported number of pages which is larger than the number required, and ignore any unused pages. For example, if your configuration requires three in-band flow control calendar pages, you can set this parameter to 4 and use pages 3, 2, and 1 while ignoring page 0.
Transceiver Settings			
Transceiver Tile	L-Tile, H-Tile, E-Tile	H-Tile	Specifies the transceiver tile on your target Intel Stratix 10 device. The **Device** setting of the Intel Quartus Prime Pro Edition project in which you generate the IP core determines the transceiver tile type.
XCVR Mode	NRZ, PAM4	NRZ	Specifies the transceiver mode. This parameter is available only in IP core variations that target an Intel Stratix 10 E-Tile device.
Tx Scrambler seed	-	0x3ab1278890105cd	This parameter specifies the initial scrambler state. If a single Interlaken IP Core is configured on your device, you can use the default value of this parameter.

continued...

Parameter	Supported Values	Default Setting	Description
			If multiple Interlaken IP Cores are configured on your device, you must use a different initial scrambler state for each IP core to reduce crosstalk. Try to select random values for each Interlaken IP core, such that they have an approximately even mix of ones and zeros and differ from the other scramblers in multiple spread out bit positions.
VCCR_GXB and VCCT_GXB supply voltage for the Transceivers	1.0V, 1.1V	1.0V	This parameter specifies the VCCR_GXB and VCCT_GXB transceiver supply voltage. Set this parameter value to 1.1V for 25.3 and 25.8 Gbps data rate.
User Data Transfer Interface			
Transfer mode selection	Interleaved and Packet	Interleaved	This parameter specifies whether the Interlaken transmitter expects incoming traffic to the TX user data transfer interface to be interleaved or packet based.

Related Information

- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
- Features on page 4
  For more information on IP core supported combinations of lanes and data rate.
- Intel Stratix 10 E-Tile Transceiver PHY User Guide

4. Functional Description

The Interlaken IP core provides the functionality described in the *Interlaken Protocol Specification, Revision 1.2*.

4.1. Interfaces

The Interlaken IP core supports the following interfaces:

- **User Data Transfer Interface**

  The user data transfer interface, also known as application interface, provides up to 256 logical channels of communication to and from the Interlaken link. This interface is similar to the Avalon-ST interface which supports data bursts or packets, which are carried in the Interlaken MetaFrame Payload.

- **Interlaken Interface**

  The Interlaken interface complies with the *Interlaken Protocol Specification, Revision 1.2*. It is the high-speed transceiver interface to an Interlaken link.

- **Out-of-Band Flow Control Interface**

  The optional out-of-band flow control interface conforms to the out-of-band requirements in *Section 5.3.4.2, Out-of-Band Flow Control, of the Interlaken Protocol Specification, Revision 1.2*.

- **Management Interface**

  The management interface provides access to the Interlaken IP core internal status and control registers. This interface does not provide access to the hard PCS registers on the device. This interface complies with the Avalon Memory-Mapped (Avalon-MM) specification defined in the *Avalon Interface Specifications*.

- **Transceiver Control Interfaces**

  The Interlaken IP core provides several interfaces to control the transceiver. The transceiver control interfaces in your Interlaken IP core variation depend on the device family the variation targets. The Interlaken IP core supports the following transceiver control interfaces:

  — **External PLL Interface**

  The Interlaken IP core variations that target an Intel Stratix 10 L-Tile or H-Tile device require an external transceiver PLL to function correctly in hardware. The Interlaken IP core variations that target an Intel Stratix 10 E-Tile device include transceiver PLLs and do not require an external PLL.

  — **Transceiver Reconfiguration Interface**

  The Intel Stratix 10 transceiver reconfiguration interface provides access to the registers in the embedded Intel Stratix 10 Native PHY IP core. This interface provides direct access to the hard PCS registers on the device. This interface complies with the Avalon Memory-Mapped (Avalon-MM) specification defined in the *Avalon Interface Specifications*.

Related Information

- Interlaken Protocol Specifications
- Avalon Interface Specifications
- Interface Signals on page 44
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
- Intel Stratix 10 E-Tile Transceiver PHY User Guide

4.2. IP Core Clocks

Table 9. Interlaken IP Core Clocks

Clock Name	Device	Direction	Description
pll_ref_clk	Intel Stratix 10 L-, H- and E-Tile	Input	Reference clock for the RX CDR PLL in IP core variations that target an Intel Stratix 10 device.
tx_serial_clk[NUM_LANES-1:0]	Intel Stratix 10 L- and H-Tile	Input	Clocks for the individual transceiver channels in Interlaken IP core variations that target an Intel Stratix 10 device.
rx_usr_clk	Intel Stratix 10 L-, H- and E-Tile	Input	Clock for the receive application interface.
tx_usr_clk	Intel Stratix 10 L-, H- and E-Tile	Input	Clock for the transmit application interface.
mm_clk	Intel Stratix 10 L-, H- and E-Tile	Input	Management clock for Interlaken IP core register access.
reconfig_clk	Intel Stratix 10 L-, H- and E-Tile	Input	Management clock for Intel Stratix 10 hard PCS register access, including access for Intel Stratix 10 transceiver reconfiguration and testing features.
clk_tx_common	Intel Stratix 10 L-, H- and E-Tile	Output	Transmit PCS common lane clock driven by the SERDES transmit PLL.
clk_rx_common	Intel Stratix 10 H-, L- and E-Tile	Output	Receive PCS common lane clock driven by the CDR in transceiver.
mac_clkin	Intel Stratix 10 E-Tile (PAM4 only)	Input	This signal must be driven by a PLL. This PLL must use the same clock source that drives the pll_ref_clk .

Related Information

- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
- Intel Stratix 10 E-Tile Transceiver PHY User Guide

4.3. High Level Data Path Flow

The Interlaken IP core consists of two paths:

- Interlaken TX path
- Interlaken RX path

Each path includes MAC, PCS, and PMA blocks. The PCS blocks are implemented in hard IP.

Figure 6. Interlaken IP Core Block Diagram for H- and L-Tile Device Variations

The figure illustrates the 8-word data transfer scenario.

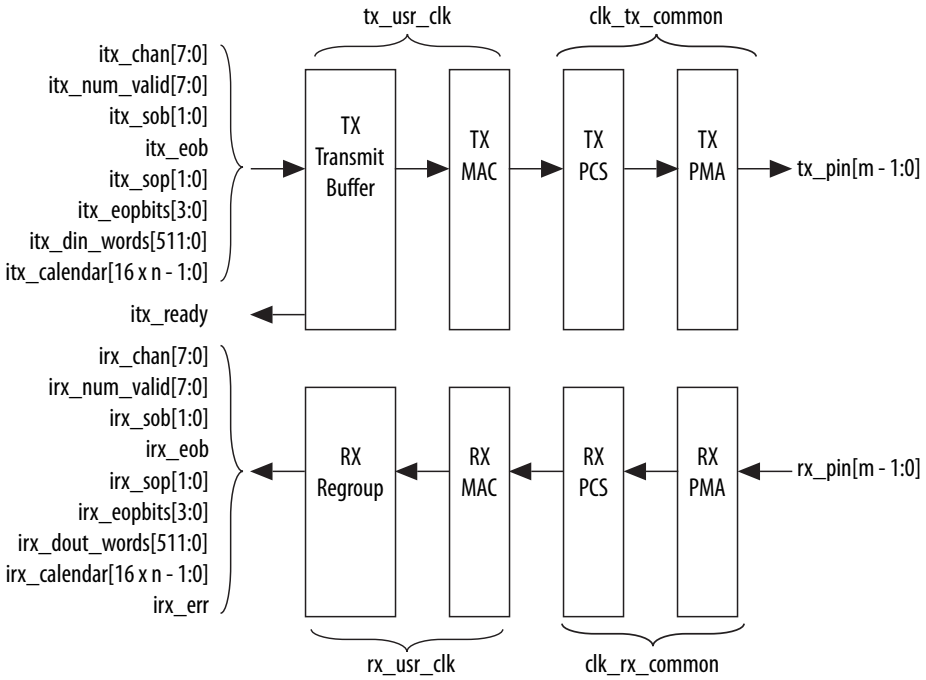
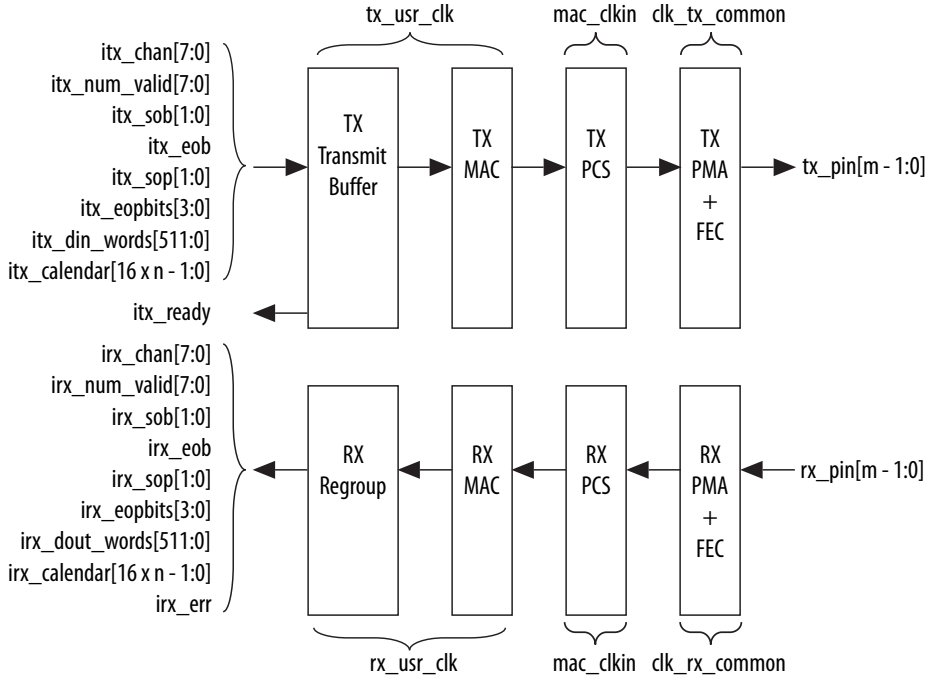


Figure 7. Interlaken IP Core Block Diagram for E-Tile PAM4 Mode Device Variations

The figure illustrates the 8-word data transfer scenario.



Related Information

- Avalon Interface Specifications
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide
- Intel Stratix 10 E-Tile Transceiver PHY User Guide

4.3.1. Interlaken TX Path

The Interlaken IP core accepts application data from up to 256 channels and combines it into a single data stream in which data is labeled with its source channel. The Interlaken TX MAC and PCS blocks format the data into protocol-compliant bursts and insert Idle words where required.

4.3.1.1. Transmit Path Blocks

The Interlaken IP core transmit data path has the following four main functional blocks:

- TX Transmit Buffer
- TX MAC
- TX PCS
- TX PMA

Figure 8. Interlaken IP Core Transmit Path Blocks for L- , H- and E-Tile NRZ Mode Device Variations

The figure illustrates the 8-word data transfer scenario.

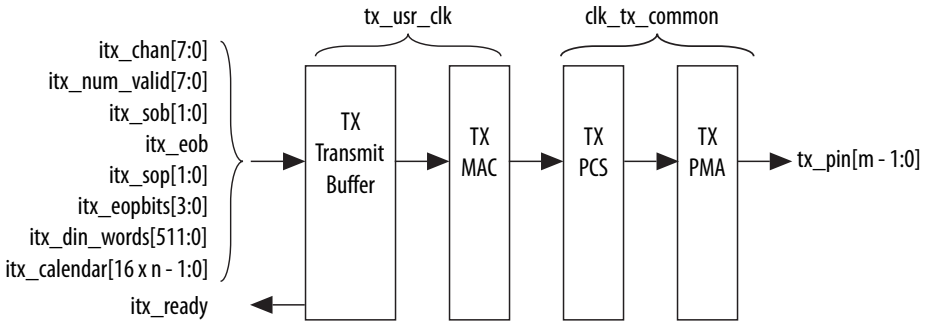
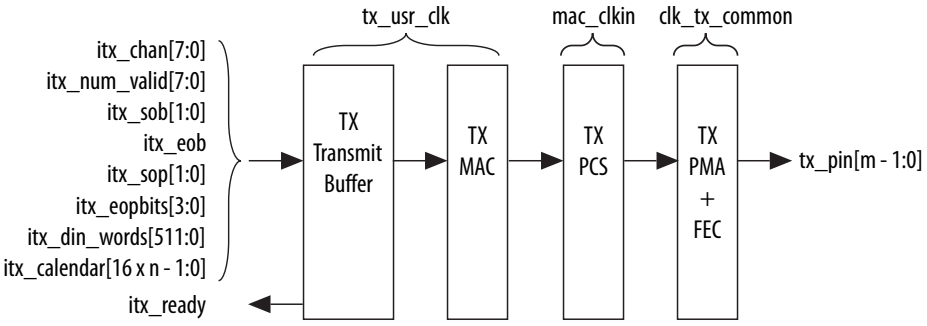


Figure 9. Interlaken IP Core Transmit Path Blocks for E-Tile PAM4 Mode Device Variations

The figure illustrates the 8-word data transfer scenario.



TX Transmit Buffer

The Interlaken IP core TX transmit buffer aligns the incoming user application data, `itx_data` in the IP core internal format.

TX MAC

The Interlaken IP core TX MAC performs the following functions:

- Inserts burst and idle control words in the incoming data stream. Burst delineation allows packet interleaving in the Interlaken protocol.
- Performs flow adaption of the data stream, repacking the data to ensure the maximum number of words is available on each valid clock cycle.
- Calculates and inserts CRC24 bits in all burst and idle words.
- Inserts calendar data in all burst and idle words, if you configure in-band flow control.