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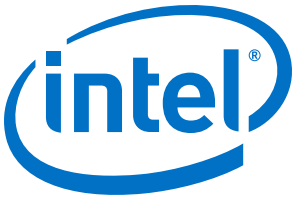

SerialLite III Streaming Intel FPGA IP Core User Guide

Updated for Intel® Quartus® Prime Design Suite: **18.0**

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Contents

1. SerialLite III Streaming Intel FPGA IP Core Quick Reference

The SerialLite III Streaming Intel® FPGA IP core is a lightweight protocol suitable for high bandwidth streaming data in chip-to-chip, board-to-board, and backplane applications.

Table 1. SerialLite III Streaming IP Core

Item		Description
Release Information	Version	18.0 Intel Quartus® Prime Standard Edition (Intel Arria® 10, Stratix® V and Arria V GZ devices) 18.0 Intel Quartus Prime Pro Edition (Intel Stratix 10 and Intel Arria 10 devices)
	Release Date	May 2018
	IP Catalog Name	• SerialLite III Streaming Intel FPGA IP (Intel Stratix 10, Stratix V, and Arria V GZ devices) • SerialLite III Streaming Intel Arria 10 FPGA IP
	Ordering Code	IP-SLITE3/ST
	Product ID	010A
	Vendor ID	6AF7
IP Core Information	Core Features	• Up to 28 Gbps(1) lane data rate for Intel Stratix 10 • Up to 17.4 Gbps lane data rates for Intel Arria 10 devices. • Supports 1–24 serial lanes in configurations that provide nominal bandwidths from 3.125 gigabits per second (Gbps) to over 300 Gbps.
	Protocol Features	• Source (simplex transmitter), sink (simplex receiver), and duplex operations • Support for single or multiple lanes • 64/67B physical layer encoding • Payload and idle scrambling • Error detection • Low overhead framing • Low point-to-point transfer latency
	Typical Application	• High resolution video • Radar processing • Medical imaging • Baseband processing in wireless infrastructure
	Device Family Support	Intel Stratix 10 (Advance support), Intel Arria 10 (Final support) , Arria V GZ (Final support), and Stratix V (Final support) FPGA devices. **Advance support** - The IP core is available for simulation and compilation for this device family. FPGA programming file (.pof) support is not available for Quartus Prime Pro – Stratix 10 Edition Beta software and as such IP timing closure cannot be guaranteed. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon

continued...

(1) Refer to Table 2 on page 8 for maximum lane supported per data rate.

Item		Description
		testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs). **Final support** - The IP core is verified with final timing models for this device family. The IP core meets all the functional and timing requirements for the device family and can be used in production designs.
	Design Tools	• IP parameter editor in the Intel Quartus Prime software for IP design instantiation and compilation • Timing Analyzer in the Intel Quartus Prime software for timing analysis • ModelSim-Intel FPGA Edition, MATLAB, or third-party tool using NativeLink for design simulation or synthesis

Related Information

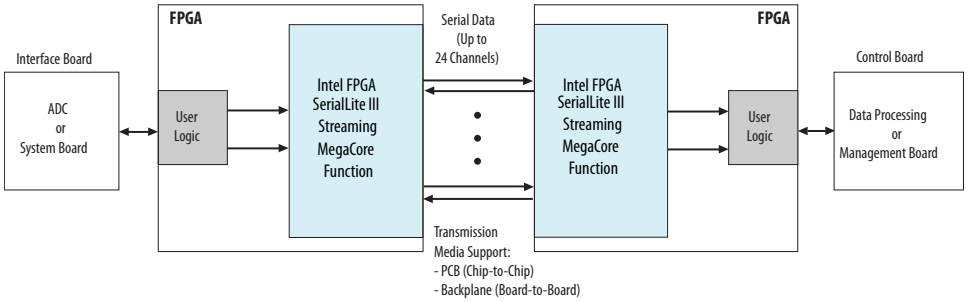
- Intel Software Installation and Licensing
- What's New in Intel IP
- SerialLite III Streaming Intel FPGA IP Core Release Notes
- Errata for Intel FPGA SerialLite III Streaming IP core in the Knowledge Base
- SerialLite III Streaming IP Core User Guide Archives on page 93
  Provides a list of user guides for previous versions of the Intel FPGA SerialLite III Streaming IP core.
- Timing and Power Models
  Reports the default device support levels in the current version of the Quartus Prime Pro Edition software.
- Timing and Power Models
  Reports the default device support levels in the current version of the Quartus Prime Standard Edition software.
- Intel FPGA SerialLite III Streaming IP Core Design Example User Guide for Intel Stratix 10 Devices
- Intel Arria 10 SerialLite III Streaming IP Core Design Example User Guide

2. About the SerialLite III Streaming IP Core

The SerialLite III Streaming IP core is a high-speed serial communication protocol for chip-to-chip, board-to-board, and backplane application data transfers. This protocol offers high bandwidth, low overhead frames, low I/O count, and supports scalability in both number of lanes and lane speed.

The SerialLite III Streaming IP core incorporates a media access control (MAC) block, a physical coding sublayer (PCS), and a physical media attachment (PMA). The IP core transmits and receives streaming data through the Avalon-ST interface on its FPGA fabric interface.

Figure 1. Typical System Application



2.1. SerialLite III Streaming IP Core Protocol

The SerialLite III Streaming IP core implements a protocol that supports the transfer of high bandwidth streaming data over a unidirectional or bidirectional, high-speed serial link.

The SerialLite III Streaming IP core has the following protocol features:

- Source (simplex transmitter), sink (simplex receiver), and duplex (transmitter and receiver) operations
- Support for single or multiple lanes
- 64B/67B physical layer encoding
- Payload and idle scrambling
- Error detection
- Low protocol overhead
- Low point-to-point transfer latency
- Reduces soft logic resource utilization using hardened Transceiver Native PHY Intel Arria 10/Intel Cyclone® 10 GX FPGA IP core and L-Tile/H-Tile Transceiver Intel Stratix 10 FPGA IP Core or Interlaken PHY v18.0 IP core (Stratix V and Arria V GZ devices)

2.2. SerialLite III Streaming IP Core Protocol Operating Modes

The protocol defines two operating modes for different applications: continuous and burst mode.

The IP core that you generate can be in either mode. No parameter option is available to select between continuous and burst modes. The selection depends on how you provide data at the Avalon-ST TX interface.

2.2.1. Continuous Mode

The SerialLite III Streaming link operating in continuous mode accepts and transmits user data over the link, and presents it at the user interface at the receiving link at the same rate and without gaps in the stream, if user logic does not de-assert data valid signal as part of the stream. However, if user logic de-asserts the data valid signal in the middle of data transfer, the streaming interface will no longer operate in continuous mode and there is no guarantee that the end-point sink is able to replicate the exact data pattern of the source. When operating in this mode, a link implementing the protocol looks like a data pipe that can transparently forward all data presented on the user interface to the far end of the link.

Continuous mode is appropriate for applications that require a simple interface to transmit a single, high bandwidth data stream. An example of this application is sensor data links for radar and wireless infrastructure. With this mode, data converters can connect to either end of the link with minimal interface logic.

Important: Continuous mode is applicable only in Standard Clocking Mode in Intel Arria 10, Stratix V, and Arria V devices. It is not possible to operate in this mode with asynchronous clocking implementation because asynchronous clocking requires data valid signal to be de-asserted, to break the data stream to avoid FIFO overflow at the sink due to PPM difference.

2.2.2. Burst Mode

The SerialLite III Streaming IP core link operating in burst mode accepts bursts of data across the user interface and transmits each burst across the link as a discrete data burst.

Burst mode is appropriate for applications where the data stream is divided into bursts of data. An example of this application is uncompressed digital video where the data stream is divided into lines of display raster. This mode provides more flexibility to the clocking and also supports multiplexing of multiple data streams across the link.

Important: The minimum required gap between bursts is 1 user clock cycle on the transmit side. Therefore, you must provide one extra user clock cycle between an end of burst and the start of the next burst. The SerialLite III Streaming IP core allows you to select between 1 or 2 burst gap. To connect the IP core of version 15.1 to IP core of the previous version, you must select a burst gap of 2 for backward compatibility.

Related Information

- Standard Clocking Mode on page 66
- Advanced Clocking Mode on page 71

2.3. Performance and Resource Utilization

These typical resources and expected performance for different SerialLite III Streaming IP core variants are obtained using the Intel Quartus Prime software targeting the Stratix V GX (5SGXMA7H2F35C2), the Arria V GZ (5AGZME7K2F40I3L), the Intel Arria 10 (10AX115S1F45I1SGES), and the Intel Stratix 10 (1SG280HN1F43E1VG) FPGA devices.

Note: The numbers of ALMs and logic registers in the following table are rounded up to the nearest 100.

Table 2. SerialLite III Streaming IP Core Performance and Resource Utilization

Device	Direction	Clocking Mode	Maximum Supported Data Lanes	Per-Lane Data Rate (Mbps)	ECC	ALMs	Primary	Secondary	M20K
Intel Stratix 10	Source	Standard	16	17400	Disabled	2427	3840	653	26
		Standard	16	17400	Enabled	7161	8304	339	33
		Standard	2	25000(2)	Disabled	1255	1456	118	5
		Standard	2	25000(2)	Enabled	1245	1476	130	5
		Standard	4	28000(3)	Disabled	2248	2566	133	9
		Standard	4	28000(3)	Enabled	2204	2543	152	9
		Advanced	16	17400	Disabled	2424	3892	599	26
		Advanced	16	17400	Enabled	7155	8326	318	33
		Advanced	2	25000(2)	Disabled	1265	1503	123	5
		Advanced	2	25000(2)	Enabled	1259	1471	143	5
		Advanced	4	28000(3)	Disabled	2227	2538	167	9
		Advanced	4	28000(3)	Enabled	2263	2605	199	9
	Sink	Standard	16	17400	Disabled	3651	5211	1112	26
		Standard	16	17400	Enabled	3948	5166	1135	33
		Standard	2	25000(2)	Disabled	680	888	220	5
		Standard	2	25000(2)	Enabled	683	906	208	5
		Standard	4	28000(3)	Disabled	1046	1414	343	9
		Standard	4	28000(3)	Enabled	1071	1475	309	9
		Advanced	16	17400	Disabled	3076	4673	1466	0
		Advanced	16	17400	Enabled	3076	4673	1466	0
		Advanced	2	25000(2)	Disabled	573	781	230	0
		Advanced	2	25000(2)	Enabled	573	781	230	0
		Advanced	4	28000(3)	Disabled	895	1305	372	0

continued...

(2) Available only with - L and H-Tile transceivers speed grade 2.

(3) Available only with - H-Tile transceiver speed grade 1.

Device	Direction	Clocking Mode	Maximum Supported Data Lanes	Per-Lane Data Rate (Mbps)	ECC	ALMs	Primary	Secondary	M20K
		Advanced	4	28000(3)	Enabled	895	1305	372	0
	Duplex	Standard	16	17400	Disabled	5290	7980	1743	52
		Standard	16	17400	Enabled	9986	12388	1473	66
		Standard	2	25000(2)	Disabled	1818	2479	316	10
		Standard	2	25000(2)	Enabled	1782	2290	278	10
		Standard	4	28000(3)	Disabled	3021	3423	474	18
		Standard	4	28000(3)	Enabled	3061	3308	414	18
		Advanced	16	17400	Disabled	4725	7578	1967	26
		Advanced	16	17400	Enabled	9375	11910	1793	33
		Advanced	2	25000(2)	Disabled	1656	2116	334	5
		Advanced	2	25000(2)	Enabled	1642	2066	348	5
		Advanced	4	28000(3)	Disabled	2887	3506	438	9
		Advanced	4	28000(3)	Enabled	2935	3661	394	9
Intel Arria 10	Source	Standard	24	17400 (4)	Disabled	2613	5049	780	39
		Standard	24	17400 (4)	Enabled	5961	9680	525	72
		Advanced	24	17400 (4)	Disabled	3009	5240	570	39
		Advanced	24	17400 (4)	Enabled	6065	9659	552	72
	Sink	Standard	24	17400 (4)	Disabled	3974	7550	1750	49
		Standard	24	17400 (4)	Enabled	4065	7570	1632	50
		Advanced	24	17400 (4)	Disabled	3297	5815	1580	0
		Advanced	24	17400 (4)	Enabled	3275	5524	1870	0
	Duplex	Standard	24	17400 (4)	Disabled	6152	12511	2000	88
		Standard	24	17400 (4)	Enabled	9313	16606	2193	122
		Advanced	24	17400 (4)	Disabled	5833	10462	2146	39
		Advanced	24	17400 (4)	Enabled	8868	14853	2112	72
Stratix V GX and Arria V GZ	Source	Standard	24	10312.50	Disabled	5684	6114	46	39
		Standard	24	10312.50	Enabled	11122	13422	271	72
		Advanced	24	10312.50	Disabled	5680	6104	43	39
		Advanced	24	10312.50	Enabled	11015	13418	239	72
	Sink	Standard	24	10312.50	Disabled	5499	9601	93	49
		Standard	24	10312.50	Enabled	5517	9510	91	50
		Advanced	24	10312.50	Disabled	4356	7757	43	0

continued...

(4) Available only with transceiver speed grade 1.

Device	Direction	Clocking Mode	Maximum Supported Data Lanes	Per-Lane Data Rate (Mbps)	ECC	ALMs	Primary	Secondary	M20K
		Advanced	24	10312.50	Enabled	4356	7757	43	0
	Duplex	Standard	24	10312.50	Disabled	8742	15024	165	88
		Standard	24	10312.50	Enabled	14045	22279	337	122
		Advanced	24	10312.50	Disabled	7550	13211	74	39
		Advanced	24	10312.50	Enabled	12606	20534	293	72

3. Getting Started

Related Information

- Introduction to Intel IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

3.1. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 2. IP Core Installation Path

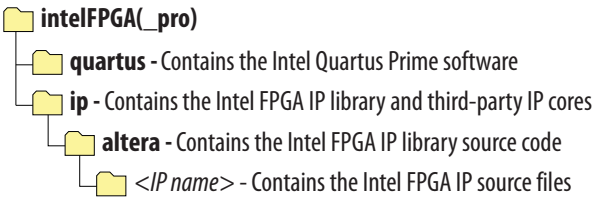


Table 3. IP Core Installation Locations

Location	Software	Platform
<drive>:\intelFPGA_pro\quartus\ip\altera	Intel Quartus Prime Pro Edition	Windows*
<drive>:\intelFPGA\quartus\ip\altera	Intel Quartus Prime Standard Edition	Windows
<home directory>:/intelFPGA_pro/quartus/ip/altera	Intel Quartus Prime Pro Edition	Linux*
<home directory>:/intelFPGA/quartus/ip/altera	Intel Quartus Prime Standard Edition	Linux

3.2. Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

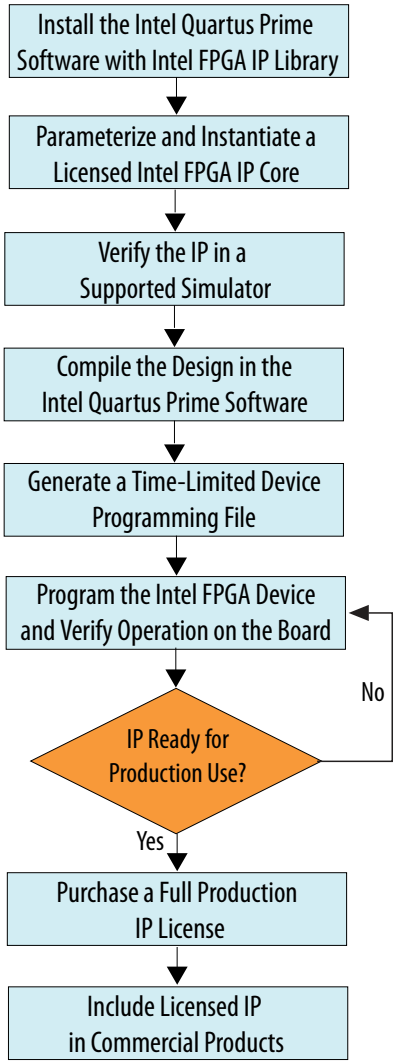
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (*<project name>*`_time_limited.sof`) that expires at the time limit.

Figure 3. Intel FPGA IP Evaluation Mode Flow



Note: Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (*<project name>*`_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the Self-Service Licensing Center or contact your local Intel FPGA representative.

The Intel FPGA Software License Agreements govern the installation and use of licensed IP cores, the Intel Quartus Prime design software, and all unlicensed IP cores.

Related Information

- Intel Quartus Prime Licensing Site
- Intel FPGA Software Installation and Licensing

3.2.1. Intel FPGA IP Evaluation Mode Timeout Behavior

All IP cores in a device time out simultaneously when the most restrictive evaluation time is reached. If there is more than one IP core in a design, the time-out behavior of the other IP cores may mask the time-out behavior of a specific IP core .

For IP cores, the untethered time-out is one hour; the tethered time-out value is indefinite. Your design stops working after the hardware evaluation time expires. The Intel Quartus Prime software uses Intel FPGA IP Evaluation Mode Files (`.ocp`) in your project directory to identify your use of the Intel FPGA IP Evaluation Mode evaluation program. After you activate the feature, do not delete these files.

When the evaluation time expires, the `link_up` signal goes low.

Related Information

AN 320: Using Intel FPGA IP Evaluation Mode

3.3. Specifying IP Core Parameters and Options

Follow these steps to specify IP core parameters and options.

1. In the Platform Designer IP Catalog (**Tools ➤ IP Catalog**), locate and double-click the name of the IP core to customize. The parameter editor appears.
2. Specify a top-level name for your custom IP variation. This name identifies the IP core variation files in your project. If prompted, also specify the target FPGA device family and output file HDL preference. Click **OK**.
3. Specify parameters and options for your IP variation:
   - Optionally select preset parameter values. Presets specify all initial parameter values for specific applications (where provided).
   - Specify parameters defining the IP core functionality, port configurations, and device-specific features.
   - Specify options for generation of a timing netlist, simulation model, testbench, or example design (where applicable).
   - Specify options for processing the IP core files in other EDA tools.
4. Click **Finish** to generate synthesis and other optional files matching your IP variation specifications. The parameter editor generates the top-level `.qsys` IP variation file and HDL files for synthesis and simulation. Some IP cores also simultaneously generate a testbench or example design for hardware testing.

The top-level IP variation is added to the current Intel Quartus Prime project. Click **Project ➤ Add/Remove Files in Project** to manually add a `.qsys` (Intel Quartus Prime Standard Edition) or `.ip` (Intel Quartus Prime Pro Edition) file to a project. Make appropriate pin assignments to connect ports.

3.3.1. SerialLite III Streaming IP Core Parameter Editor

Based on the values you set, the SerialLite III Streaming IP core parameter editor automatically calculates the rest of the parameters, and provides you with the following values or information:

- Input data rate per lane
- Transceiver data rate per lane
- A list of feasible transceiver reference clock frequencies, one of which you select to provide to the core

Important: If your design targets Stratix V or Arria V GZ devices, you cannot migrate your design to Intel Arria 10 and Intel Stratix 10 devices automatically. For Intel Arria 10 devices, the transceiver reconfiguration functionality is embedded inside the transceivers. Therefore, you must re-instantiate the IP core to target Intel Arria 10 devices. For Intel Stratix 10 devices, you must re-instantiate the IP core to target Intel Stratix 10 devices due to the transceiver architecture differences.

Related Information

Parameter Settings for Intel Stratix 10 Devices on page 16

3.3.2. Intel Arria 10 Designs

If your design targets the Intel Arria 10 devices:

- The parameter editor displays a message about the required output clock frequency of the external TX PLL IP clock. For source or duplex modes, connect the Transceiver PHY Reset Controller to the TX PLL to ensure the appropriate HSSI power-up sequence.
- For source only Intel Arria 10 implementations, the parameter editor does not provide the transceiver reference clock frequency because the user is expected to provide the transmit serial clock. If you use an on-chip PLL to generate the transmit serial clock, you can use the same PLL reference clock frequency that you provide to the core in the sink direction, operating at the same user clock frequency (or equivalent transceiver lane data rate).
- The SerialLite III Streaming Intel Arria 10 FPGA IP core expects the user to provide the transmitter's serial clock. If you compile the IP without the proper serial clock, the Intel Quartus Prime Compiler issues a compilation error.
- When generating the example testbench, the SerialLite III Streaming Intel Arria 10 FPGA IP core instantiates an external transceiver ATX PLL for the transmit serial clock based on the required user clock only when configured in sink or duplex mode. The transceiver ATX PLL core is configured with the transceiver reference clock specified in the parameter editor and transmit serial clock.
- To generate the SerialLite III Streaming Intel Arria 10 FPGA IP Core example testbench using the parameter editor, select **Generate Example Designs > *<directory_name>***. Intel recommends that you generate the Intel Arria 10 simulation testbench for the sink or duplex direction.

Related Information

- Parameter Settings for Intel Stratix 10 Devices on page 16
- Intel Arria 10 versus Stratix V and Arria V GZ Variations

- Intel FPGA SerialLite III Streaming IP Core Design Example User Guide for Intel Stratix 10 Devices
- Intel Arria 10 SerialLite III Streaming IP Core Design Example User Guide

3.4. SerialLite III Streaming IP Core Parameters

3.4.1. Parameter Settings for Intel Stratix 10 Devices

Table 4. IP

Parameter	Value	Default	Description
General Design Options			
Direction	**Source**, **Sink**, **Duplex**	**Duplex**	Select the variation of the IP core. Supports source, sink, or full duplex transmissions.
Number of lanes	1–24	6	Specifies the number of lanes (equal to physical transceiver links) that are used to transfer the streaming data.
Meta frame length in words	200–8191	200	Specifies the metaframe length.
Transceiver reference clock frequency	*<Range supported by the transceiver PLLs>*	312.5 MHz	Supports multiple transceiver reference clock frequencies for flexibility in the oscillator and PLL choices. This transceiver reference clock frequency must match the external PLL reference clock frequency.
VCCR_GXB and VCCT_GXB supply voltage for the Transceiver	**1_1V**, **1_0V**	**1_0V**	Select `VCCR_GXB` and `VCCT_GXB` supply voltages. Refer to *Intel Stratix 10 GX, MX, and SX Device Family Pin Connection Guidelines* for more information related to these pins.
Transceiver channel type	**GX**, **GXT**	**GX**	Select the transceiver channel variant. Select **GXT** as the transceiver variant to implement data rate more than 17.4 Gbps.
Enable M20K ECC support	Yes/No	No	Select to use error correcting code (ECC) protection to strengthen the FIFO buffers from single-event upset (SEU) changes. Enables built-in error correcting code (ECC) support on the M20K embedded block memory for single-error correction, double-adjacent-error correction, and triple-adjacent-error detection.
Transceiver Tile	**L-Tile**, **H-Tile**	**L-Tile**	Reports the actual transceiver crete tile. The value changes according to the transceiver crete tile chosen in the device.
User Interface			
Streaming Mode	**Basic**, **Full**	**Full**	Specifies the streaming mode. • Basic: This is a pure streaming mode where data is sent without burst, sync, empty cycle, and frame delimiter to increase bandwidth. • Full: This mode sends a burst and sync cycle at the start of frame and a burst and empty cycle at the end of frame. Provide a gap of one empty cycle between two data frames.
Required idle cycles between bursts	1, 2	2	Supports two values to optimize for bandwidth efficiency or maintain backward compatibility with existing SerialLite III Streaming IP cores (legacy).

continued...

Parameter	Value	Default	Description
			• 1: Recommended for high bandwidth streaming. The same Burst Gap setting must be set for both source and sink IP core. • 2: For backward compatibility with Quartus II version 15.1 and older sink IP core.
Adaptation FIFO partial full threshold	8 - 18	15	Specifies the partial full threshold of the transmit FIFO. `ready_tx` signal will de-assert when data reaches this level in the FIFO.
Clocking mode	**Standard clocking mode**, **Advanced clocking mode**	**Standard clocking mode**	Specifies the clocking mode. Refer to SerialLite III Streaming IP Core Clocking Guidelines on page 66 for more information.
User input	**User clock frequency**, **Transceiver data rate**	**User clock frequency**	Select **User clock frequency** to specify the user clock input and allow the IP core to determine the transceiver data rate. Select **Transceiver data rate** to specify the desired data rate and allow the IP core to determine the user clock frequency.
User clock frequency required	Minimum: 50 MHz Maximum: Limited by the supported transceiver data rates	177.556818 MHz	Specifies the desired frequency for the user clock input for the transmit (Standard Clocking Mode and Advanced Clocking Mode) and receive user interface (Standard Clocking Mode). This frequency in turn determines the required transceiver data rate to support the calculated transmit and receive bandwidths.
Transceiver data rate	required user clock frequency * overheads * 64	12.5 Gbps	The effective data rate at the output of the transceivers, incorporating transmission and other overheads. The parameter editor automatically calculates this value by adding the input data rate with transmission overheads to provide you with a selection of user clock frequency.
Aggregate user bandwidth	number of lanes * required user clock frequency * 64	68.18 Gbps	This value is derived by multiplying the number of lanes and user interface data rate.

Table 5. IP Debug and Phy Dynamic Reconfiguration

Parameter	Value	Default	Description
Dynamic Reconfiguration			
Enable dynamic reconfiguration	On/Off	On	Enables the dynamic reconfiguration interface.
Enable Altera Debug Master Endpoint	On/Off	Off	Enables ADME and Optional Reconfiguration Logic parameters of the L-Tile/H-Tile Transceiver Native PHY Intel Stratix 10 FPGA IP Core.
Optional Reconfiguration Logic			
Enable capability registers	On/Off	Off	Enables capability registers that provide high level information about the configuration f the transceiver channel.
Set user-defined IP identifier	User-defined	0	Sets a user-defined numeric identifier that can be read from the

continued...

Parameter	Value	Default	Description
			`user_identifier` offset when the capability registers are enabled.
Enable control and status registers	On/Off	Off	Enables soft registers to read status signals and write control signals on the PHY interface through the embedded debug.
Enable PRBS (Pseudo Random Binary Sequence) soft accumulators	On/Off	Off	Enables soft logic for performing PRBS bit and error accumulation when the hard PRBS generator and checker are used.

Related Information

- SerialLite III Streaming IP Core Parameter Editor on page 15
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide - Dynamic Reconfiguration Parameters

3.4.2. Parameter Settings for Intel Arria 10 Devices

Table 6. IP

Parameter	Value	Default	Description
General Design Options			
Direction	Source, Sink, Duplex	Duplex	Supports source, sink, or full duplex transmissions.
Number of lanes	1–24	2	Specifies the number of lanes (equal to physical transceiver links) that are used to transfer the streaming data.
Transceiver reference clock frequency	*<Range supported by the transceiver PLLs>*	644.53125 MHz	Supports multiple transceiver reference clock frequencies for flexibility in the oscillator and PLL choices. This transceiver reference clock frequency must match the external PLL reference clock frequency.
Meta frame length in words	200–8191	200	Specifies the metaframe length.
Enable Transceiver Native PHY ADME	On/Off	Off	Turn on to enable ADME and Optional Reconfiguration Logic parameters of the Transceiver Native PHY Intel Arria 10/Intel Cyclone 10 GX FPGA IP core.
Enable M20K ECC support	On/Off	Off	Turn on to use error correcting code (ECC) protection to strengthen the FIFO buffers from single-event upset (SEU) changes. Enables built-in error correcting code (ECC) support on the M20K embedded block memory for single-error correction, double-adjacent-error correction, and triple-adjacent-error detection.
User Interface			
Required idle cycles between bursts	1, 2	2	Supports two values to optimize for bandwidth efficiency or maintain backward compatibility with existing SerialLite III Streaming IP cores (legacy). • 1: Recommended for high bandwidth streaming. The same Burst Gap setting must be set for both source and sink IP core. • 2: For backward compatibility with Quartus II version 15.1 and older sink IP core.

continued...

Parameter	Value	Default	Description
Clocking mode	Standard clocking mode, Advanced clocking mode	Standard clocking mode	Specifies the clocking mode. Refer to SerialLite III Streaming IP Core Clocking Guidelines on page 66 for more information.
User input	User clock frequency, Transceiver data rate	User clock frequency	Select **User clock frequency** to specify the user clock input and allow the IP core to determine the transceiver data rate. Select **Transceiver data rate** to specify the desired data rate and allow the IP core to determine the user clock frequency.
User clock frequency required	Minimum: 50 MHz Maximum: Limited by the supported transceiver data rates	150 MHz	Specifies the desired frequency for the user clock input for the transmit (Standard Clocking Mode and Advanced Clocking Mode) and receive user interface (Standard Clocking Mode). This frequency in turn determines the required transceiver data rate to support the calculated transmit and receive bandwidths.
User clock frequency output	Minimum: 50 MHz Maximum: Limited by the supported transceiver data rates	150 MHz	Specifies the actual user clock frequency as produced by the fPLL or I/O PLL and is ideally the same as the required clock frequency. In certain very high precision situations where the desired user clock is provided up to higher decimal places, this value can vary slightly due to the fPLL or I/O PLL constraints. Change the required clock frequency to correct the issue if the minute variation is intolerable.
Transceiver data rate	required user clock frequency * overheads * 64	10.312499 Gbps	The effective data rate at the output of the transceivers, incorporating transmission and other overheads. The parameter editor automatically calculates this value by adding the input data rate with transmission overheads to provide you with a selection of user clock frequency.
Aggregate user bandwidth	number of lanes * required user clock frequency * 64	18.75 Gbps	This value is derived by multiplying the number of lanes and user interface data rate.

3.4.3. Parameter Settings for Stratix V and Arria V GZ Devices

Table 7. IP

Parameter	Value	Default	Description
General Design Options			
Direction	Source, Sink, Duplex	Duplex	Supports source, sink, or full duplex transmissions.
Number of lanes	1–24	2	Specifies the number of lanes (equal to physical transceiver links) that are used to transfer the streaming data.
Device speed grade	1–4	2	Specifies the device speed grade.
PLL type	ATX, CMU	CMU	Selects the transceiver PLL type.
Transceiver reference clock frequency	*<Range supported by the transceiver PLLs>*	644.53125 MHz	Supports multiple transceiver reference clock frequencies for flexibility in the oscillator and PLL choices. This transceiver reference clock frequency must match the external PLL reference clock frequency.
Meta frame length in words	200–8191	200	Specifies the metaframe length.

continued...

Parameter	Value	Default	Description
Enable M20K ECC support	On/Off	Off	Turn on to use error correcting code (ECC) protection to strengthen the FIFO buffers from single-event upset (SEU) changes. Enables built-in error correcting code (ECC) support on the M20K embedded block memory for single-error correction, double-adjacent-error correction, and triple-adjacent-error detection.
User Interface			
Required idle cycles between bursts	1, 2	2	Supports two values to optimize for bandwidth efficiency or maintain backward compatibility with existing SerialLite III Streaming IP cores (legacy). • 1: Recommended for high bandwidth streaming. The same Burst Gap setting must be set for both source and sink IP core. • 2: For backward compatibility with Quartus II version 15.1 and older sink IP core.
Clocking mode	Standard clocking mode, Advanced clocking mode	Standard clocking mode	Specifies the clocking mode. Refer to SerialLite III Streaming IP Core Clocking Guidelines on page 66 for more information.
User input	User clock frequency, Transceiver data rate	User clock frequency	Select **User clock frequency** to specify the user clock input and allow the IP core to determine the transceiver data rate. Select **Transceiver data rate** to specify the desired data rate and allow the IP core to determine the user clock frequency.
User clock frequency required	Minimum: 50 MHz Maximum: Limited by the supported transceiver data rates	146.484375 MHz	Specifies the desired frequency for the user clock input for the transmit (Standard Clocking Mode and Advanced Clocking Mode) and receive user interface (Standard Clocking Mode). This frequency in turn determines the required transceiver data rate to support the calculated transmit and receive bandwidths.
User clock frequency output	Minimum: 50 MHz Maximum: Limited by the supported transceiver data rates	146.484375 MHz	Specifies the actual user clock frequency as produced by the fPLL or I/O PLL and is ideally the same as the required clock frequency. In certain very high precision situations where the desired user clock is provided up to higher decimal places, this value can vary slightly due to the fPLL or I/O PLL constraints. Change the required clock frequency to correct the issue if the minute variation is intolerable.
Transceiver data rate	Required user clock frequency * overheads * 64	10.3125 Gbps	The effective data rate at the output of the transceivers, incorporating transmission and other overheads. The parameter editor automatically calculates this value by adding the input data rate with transmission overheads to provide you with a selection of user clock frequency.
Aggregate user bandwidth	Number of lanes * required user clock frequency * 64	18.3125 Gbps	This value is derived by multiplying the number of lanes and user interface data rate.

3.5. Transceiver Reconfiguration Controller for Stratix V and Arria V GZ Designs

If your design targets Stratix V or Arria V GZ devices, the transceiver reconfiguration controller is not included in the generated IP core. To create a complete system, refer to the design example block diagram on how to connect the transceiver reconfiguration controller.

Note: If your design targets Intel Arria 10 and Intel Stratix 10 devices, the transceiver reconfiguration functionality is embedded inside the transceivers. The `phy_mgmt` bus interface connects directly to the Avalon Memory-Mapped (Avalon-MM) dynamic reconfiguration interface of the embedded Intel Arria 10 and Intel Stratix 10 Native PHY IP core. This interface is provided at the top level. For Quartus compilation design, create clock constraints for the `phy_mgmt_clk` and `reconfig_to_xcvr[0]` (for Stratix V and Arria V GZ) signals to avoid unconstrained clock warnings.

3.6. Files Generated for Intel FPGA IP Cores and Platform Designer Systems

The Intel Quartus Prime Pro Edition software generates the following output file structure for IP cores and Platform Designer systems. The Intel Quartus Prime Pro Edition Platform Designer software automatically adds the generated `.ip` and `.qsys` files to your Intel Quartus Prime project.

Figure 4. Files generated for IP cores and Platform Designer Systems

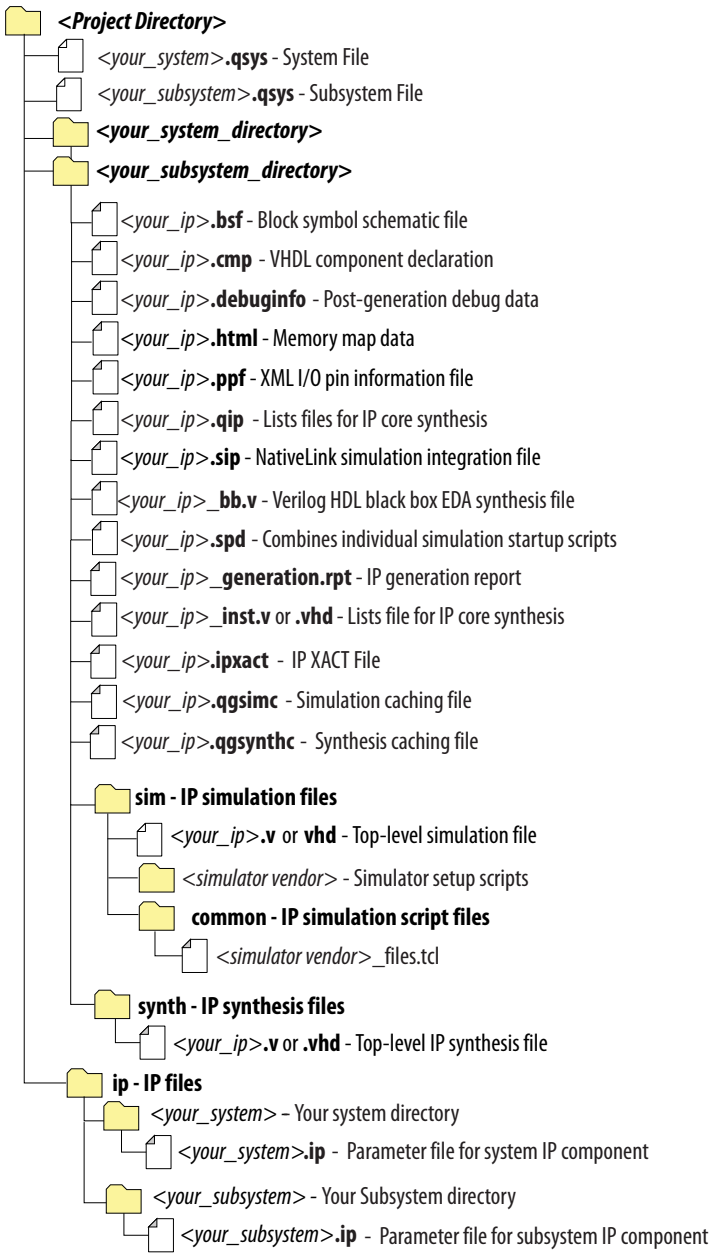


Table 8. IP Core and Platform Designer (Standard) Simulation Files

File Name	Description
<*my_system*>.qsys	The Platform Designer system.
<*my_subsystem*>.qsys	The Platform Designer subsystem.
ip/	Contains the parameter files for the IP components in the system and subsystems.

continued...

File Name	Description
<*my_ip*>.cmp	The VHDL Component Declaration (**.cmp**) file is a text file that contains local generic and port definitions that you can use in VHDL design files.
<*my_ip*>_generation.rpt	IP or Platform Designer (Standard) generation log file. A summary of the messages during IP generation.
<*my_ip*>.qgsimc	Simulation caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.
<*my_ip*>.qgsynth	Synthesis caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.
<*my_ip*>.qip	Contains all the required information about the IP component to integrate and compile the IP component in the Intel Quartus Prime software.
<*my_ip*>.csv	Contains information about the upgrade status of the IP component.
<*my_ip*>.bsf	A Block Symbol File (.**bsf**) representation of the IP variation for use in Block Diagram Files (**.bdf**).
<*my_ip*<>.spd	Required input file for ip-make-simscript to generate simulation scripts for supported simulators. The **.spd** file contains a list of files generated for simulation, along with information about memories that you can initialize.
<*my_ip*>.ppf	The Pin Planner File (**.ppf**) stores the port and node assignments for IP components created for use with the Pin Planner.
<*my_ip*>_bb.v	Use the Verilog black box (**_bb.v**) file as an empty module declaration for use as a black box.
<*my_ip*>.sip	Contains information required for NativeLink simulation of IP components. Add the **.sip** file to your Intel Quartus Prime Standard Edition project to enable NativeLink for supported devices. The Intel Quartus Prime Pro Edition software does not support NativeLink simulation.
<*my_ip*>_inst.v or _inst.vhd	HDL example instantiation template. Copy and paste the contents of this file into your HDL file to instantiate the IP variation.
<*my_ip*>.regmap	If the IP contains register information, the Intel Quartus Prime software generates the **.regmap** file. The **.regmap** file describes the register map information of master and slave interfaces. This file complements the .**sopcinfo** file by providing more detailed register information about the system. This file enables register display views and user customizable statistics in System Console.
<*my_ip*>.svd	Allows HPS System Debug tools to view the register maps of peripherals connected to HPS within a Platform Designer (Standard) system. During synthesis, the Intel Quartus Prime software stores the .svd files for slave interface visible to the System Console masters in the .sof file in the debug session. System Console reads this section, which Platform Designer (Standard) can query for register map information. For system slaves, Platform Designer (Standard) can access the registers by name.
<*my_ip*>.v <*my_ip*>.vhd	HDL files that instantiate each submodule or child IP core for synthesis or simulation.
mentor/	Contains a ModelSim® script msim_setup.tcl to set up and run a simulation.
aldec/	Contains a Riviera-PRO script rivierapro_setup.tcl to setup and run a simulation.
/synopsys/vcs /synopsys/vcsmx	Contains a shell script vcs_setup.sh to set up and run a VCS® simulation. Contains a shell script vcsmx_setup.sh and synopsys_ sim.setup file to set up and run a VCS MX® simulation.

continued...

File Name	Description
/cadence	Contains a shell script ncsim_setup.sh and other setup files to set up and run an NCSIM simulation.
/xcelium	Contains a shell script xcelium_setup.sh and other setup files to set up and run a Xcelium simulation.
/common	Contains a set of Tcl files, <simulator>_files.tcl, which provide all design related simulation information required by a corresponding simulation script. The Tcl file contains designs from current system-level hierarchy, and references to sub-systems and IP components.
/submodules	Contains HDL files for the IP core submodule.
<*IP submodule*>/	For each generated IP submodule directory, Platform Designer (Standard) generates /synth and /sim sub-directories.

3.7. Simulating

3.7.1. Simulating Intel FPGA IP Cores

The Intel Quartus Prime software supports IP core RTL simulation in specific EDA simulators. IP generation creates simulation files, including the functional simulation model, any testbench (or example design), and vendor-specific simulator setup scripts for each IP core. Use the functional simulation model and any testbench or example design for simulation. IP generation output may also include scripts to compile and run any testbench. The scripts list all models or libraries you require to simulate your IP core.

The Intel Quartus Prime software provides integration with many simulators and supports multiple simulation flows, including your own scripted and custom simulation flows. Whichever flow you choose, IP core simulation involves the following steps:

1. Generate simulation model, testbench (or example design), and simulator setup script files.
2. Set up your simulator environment and any simulation scripts.
3. Compile simulation model libraries.
4. Run your simulator.

3.7.2. Simulation Parameters

After design generation, simulation files are available for you to simulate your design. To simulate your design, ensure that the SerialLite III Streaming IP core source and sink cores are both generated with the same parameters or are duplex cores.

- Stratix V and Arria V GZ files are located in the <*variation name*>**_sim** directory
- Intel Arria 10 and Intel Stratix 10 files are located in the <*variation name*> directory

The example testbench simulates the core using the user-specified configuration.

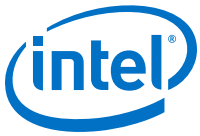


Table 9. Stratix V and Arria V GZ Testbench Default Simulation Parameters

Parameter	Default Value	Comments
user clock frequency output (`user_clock_frequency`)	Standard clocking: 145.98375 MHz Advanced clocking: 146.484375 MHz	—
Number of lanes (`lanes`)	2	—
Transceiver reference clock frequency (`pll_ref_freq`)	644.53125 MHz	—
Transceiver data rate (`data_rate`)	10312.5 Mbps	—
Meta frame length in words (`meta_frame_length`)	200	—
Simulation-specific parameters		
Total samples to transfer (`total_samples_to_transfer`)	2000	Total samples to transfer during simulation.
Mode (`mode`)	Continuous/burst	The testbench environment may automatically choose one of the modes depending on the random seed with which it is provided.
Skew insertion enable (`skew_insertion_enable`)	Yes	Skew testing is enabled. The testbench environment randomly inserts skew in the lanes within the range 0 - 107 UI.
Enable M20K ECC support (`ecc_enable`)	0	When set, the core is simulated with the ECC-enabled variant. Use the ECC-enabled variant in the test environment. When ECC mode is disabled, the two most significant bits of the error buses in the source or sink direction are *Don't Care*.

Table 10. Intel Arria 10 Testbench Default Simulation Parameters

Parameter	Default Value	Comments
user clock frequency output (`user_clock_frequency`)	Standard clocking: 146.484375 MHz	—
Number of lanes (`lanes`)	2	—
Transceiver reference clock frequency (`pll_ref_freq`)	644.531187 MHz	—
Transceiver data rate (`data_rate`)	10.312499 Gbps	—
Meta frame length in words (`meta_frame_length`)	200	—
Simulation-specific parameters		
Total samples to transfer (`total_samples_to_transfer`)	2000	Total samples to transfer during simulation.
Mode (`mode`)	Continuous/burst	The testbench environment may automatically choose one of the modes depending on the random seed with which it is provided.
Skew insertion enable (`skew_insertion_enable`)	Yes	Skew testing is enabled.

continued...