Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

International
IOR Rectifier

Data Sheet No.PD 60148-K

IPS021(S)

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

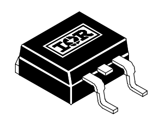
Description

The IPS021/IPS021S are fully protected three terminal SMART POWER MOSFETs that feature over-current, over-temperature, ESD protection and drain to source active clamp.These devices combine a HEXFET® POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 5A. These devices restart once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

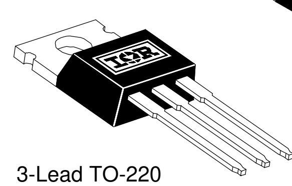
Product Summary

$R_{ds(on)}$	150mΩ (max)
V_{clamp}	50V
$I_{shutdown}$	5A
T_{on}/T_{off}	1.5µs

Packages

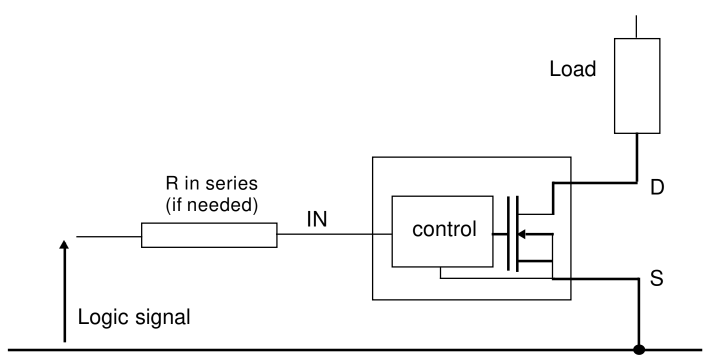


3-Lead D^2Pak
IPS021S



3-Lead TO-220
IPS021

Typical Connection



(Refer to lead assignment for correct pin configuration)

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard foot-print with 70 µm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7	V	
$I_{in, max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continous current (1)			A	
	(rth=62°C/W) IPS021	—	2.8		
	(rth=10°C/W) IPS021	—	8		
	(rth=80°C/W) IPS021S	—	2.2		
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	10A		
P_d	Maximum power dissipation(1)			W	
	(rth=62°C/W) IPS021	—	2		
	(rth=80°C/W) IPS021S	—	1.56		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5	kV	C=200pF, R=0Ω, L=10µH
$T_{stor.}$	Max. storage temperature	-55	150	°C	
T_j max.	Max. junction temperature.	-40	150	°C	
T_{lead}	Lead temperature (soldering, 10 seconds)	—	300	°C	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance free air	—	60	—	°C/W	TO-220
R_{th} 2	Thermal resistance junction to case	—	5	—	°C/W	TO-220
R_{th} 1	Thermal resistance with standard footprint	—	80	—	°C/W	D2PAK (SMD220)
R_{th} 2	Thermal resistance with 1" square footprint	—	50	—	°C/W	D2PAK (SMD220)
R_{th} 3	Thermal resistance junction to case	—	5	—	°C/W	D2PAK (SMD220)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V_{ds} (max)	Continuous drain to source voltage	—	35	V
V_{IH}	High level input voltage	4	6	V
V_{IL}	Low level input voltage	0	0.5	V
I_{ds} Tamb=85°C	Continuous drain current (TAmbient = 85°C, IN = 5V, rth = 60°C/W, Tj = 125°C)	—	1.8	A
R_{in}	Recommended resistor in series with IN pin	0.5	5	kΩ
$T_{r\text{-}in}$ (max)	Max recommended rise time for IN signal (see fig. 2)	—	1	µS
$F_{r\text{-}Isc}$ (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operations at higher switching frequencies is possible. See Appl. Notes.

Static Electrical Characteristics

Standard footprint 70 µm copper thickness. $T_j = 25^oC$ (unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance $T_j = 25^oC$	100	130	150	mΩ	V_{in} = 5V, I_{ds} = 1A
	$T_j = 150^oC$	—	220	280		
$I_{dss\ 1}$	Drain to source leakage current	0	0.01	25	µA	V_{cc} = 14V, $T_j = 25^oC$
$I_{dss\ 2}$	Drain to source leakage current	0	0.1	50		V_{cc} = 40V, $T_j = 25^oC$
V clamp 1	Drain to source clamp voltage 1	48	54	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	50	56	60		$I_d = I_{shutdown}$ (see Fig.3 & 4)
$V_{in\ clamp}$	IN to source clamp voltage	7	8	9.5		I_{in} = 1 mA
V_{th}	IN threshold voltage	1	1.5	2		I_d = 50mA, V_{ds} = 14V
$I_{in,\ -on}$	ON state IN positive current	25	90	200	µA	V_{in} = 5V
$I_{in,\ -off}$	ON state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 10Ω, Rinput = 50Ω, 100µs pulse, $T_j = 25^oC$, (unless otherwise specified).

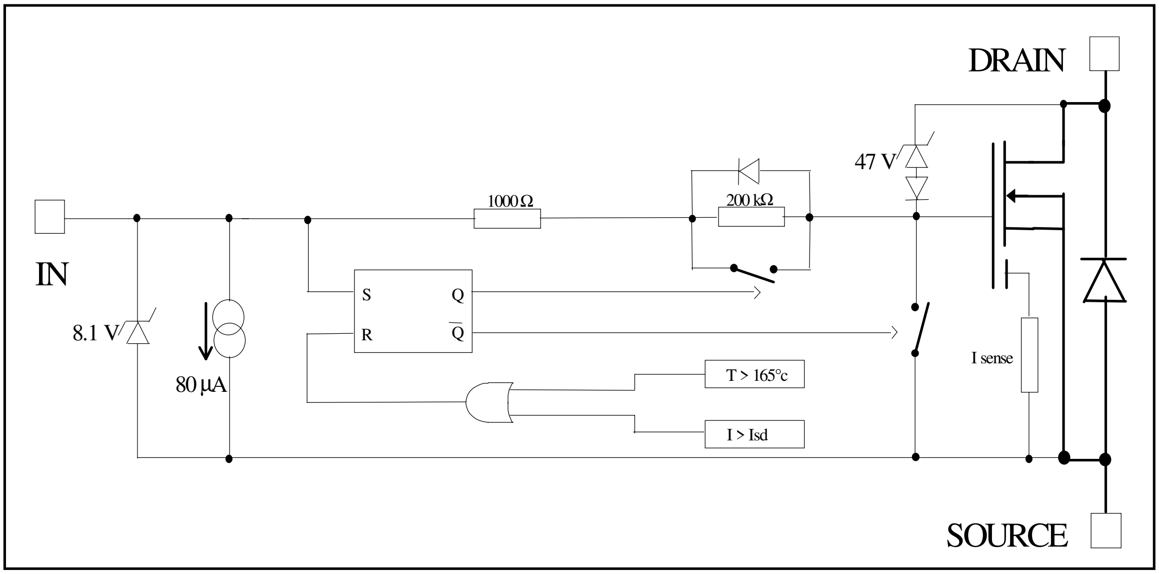
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.15	0.5	1	µs	See figure 2
T_r	Rise time	0.4	0.9	2		
T_{rf}	Time to (final $R_{ds(on)}$ 1.3)	2	6	12		
T_{off}	Turn-off delay time	0.8	2	3.5		See figure 2
T_f	Fall time	0.5	1.3	2.5		
Q_{in}	Total gate charge	—	3.3	—	nC	V_{in} = 5V

Protection Characteristics

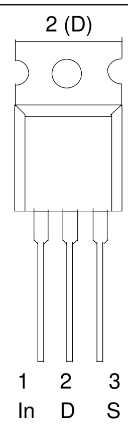
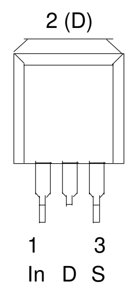
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	^oC	See fig. 1
I_{sd}	Over current threshold	4	5.5	7	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, Tj = 25^oC
EOI_OT	Short circuit energy (see application note)	—	400	—	µJ	V_{cc} = 14V

Functional Block Diagram

All values are typical



Lead Assignments

 TO-220	 D^2PAK (SMD220)
IPS021	**IPS021S**
Part Number	

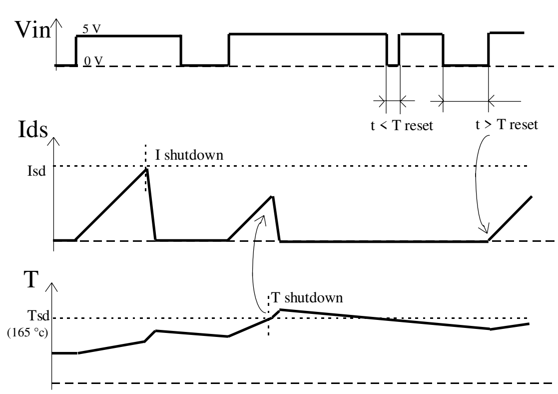


Figure 1 - Timing diagram

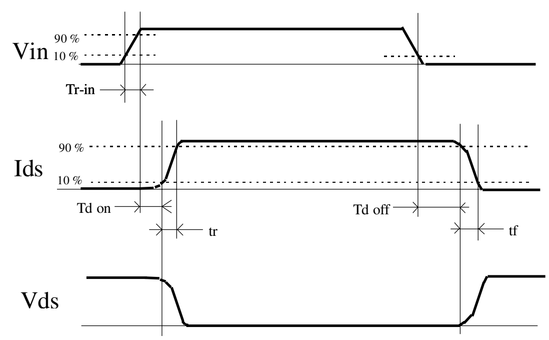


Figure 2 - IN rise time & switching time definitions

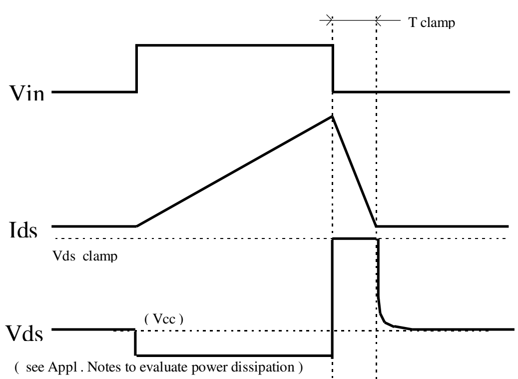


Figure 3 - Active clamp waveforms

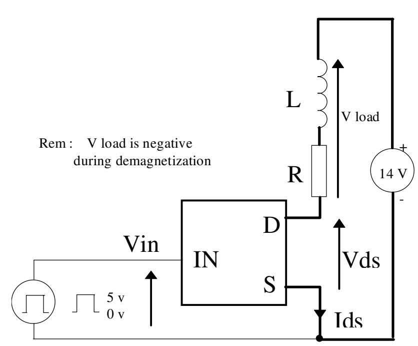


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

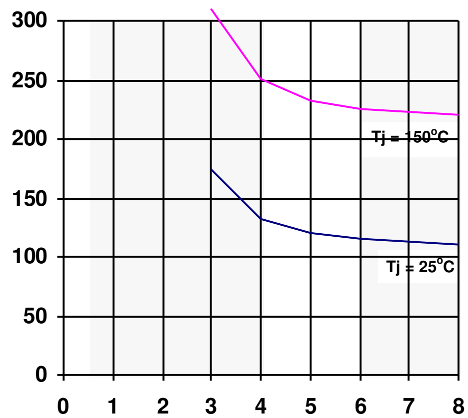


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

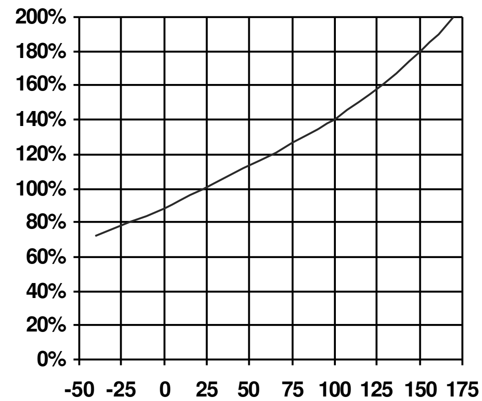


Figure 6 - Normalized Rds(on) (%) Vs Tj (°C)

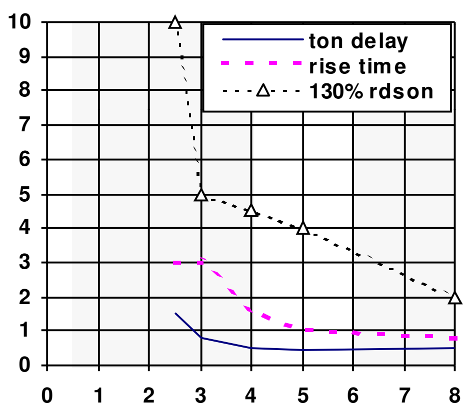


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final $Rds_{(on)}$ (us) Vs Input Voltage (V)

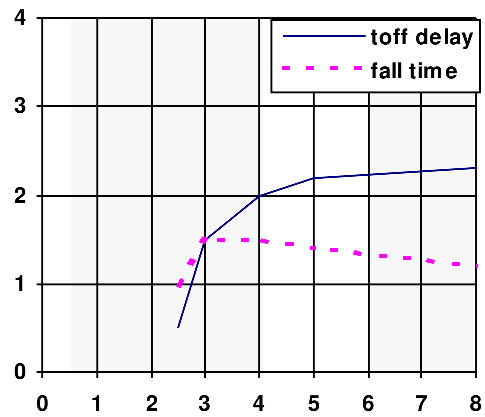


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

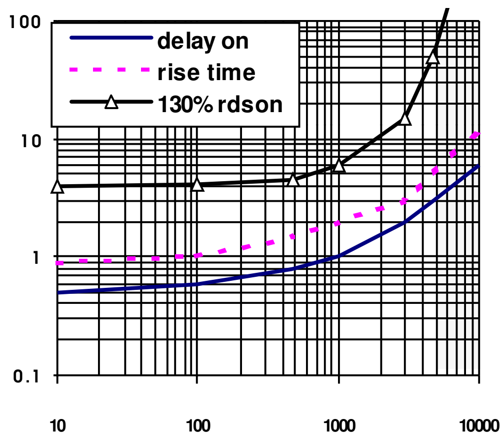


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs IN Resistor (Ω)

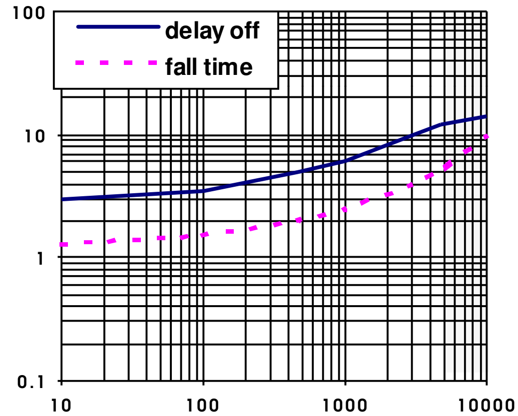


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

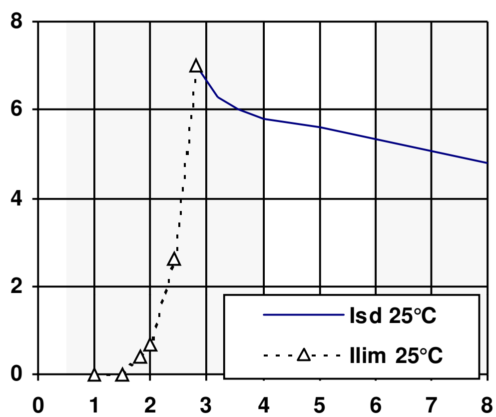


Figure 11 - Current lim. & I shutdown (A) Vs Vin (V)

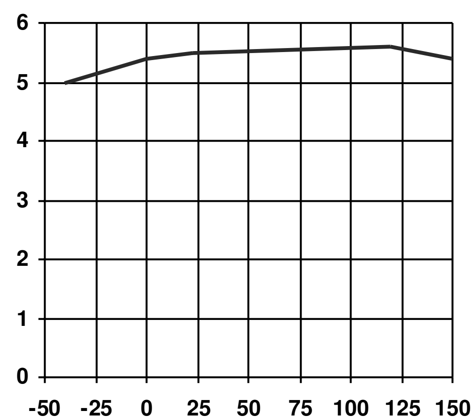


Figure 12 - I shutdown (A) Vs Temperature (ºC)

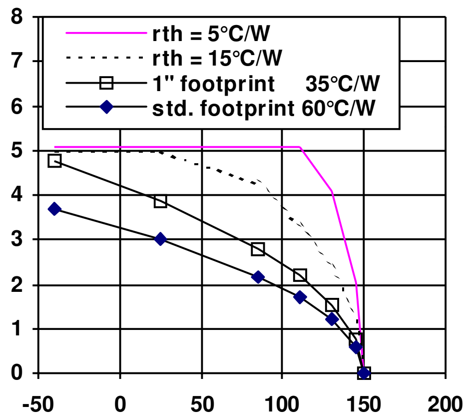


Figure 13 - Max.Cont. Ids (A)
Vs Amb. Temperature (ºC) IPS021/IPS021S

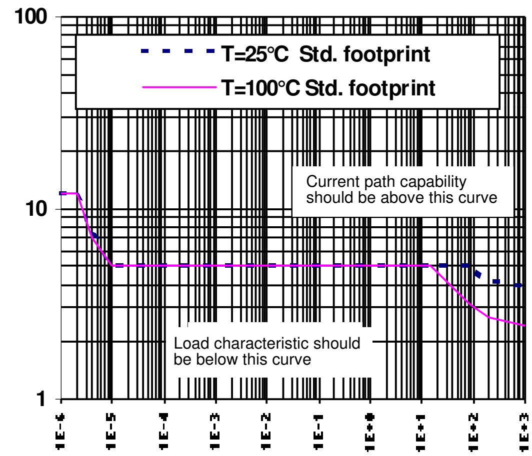


Figure 14 - Ids (A) Vs Protection Resp. Time (s)
IPS021 & IPS021S

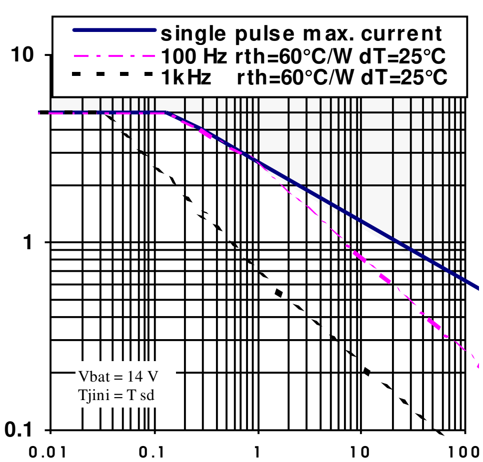


Figure 15a - Iclamp (A) Vs Inductive Load (mH)
IPS021

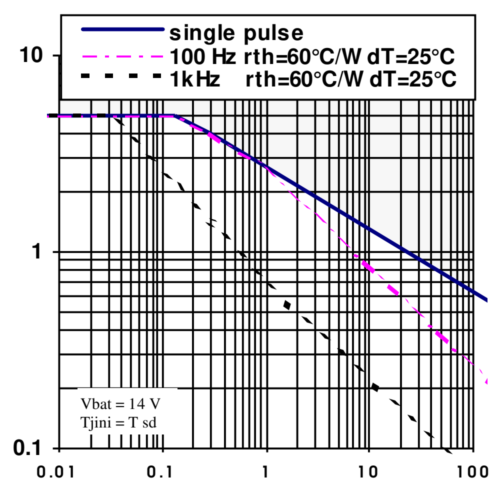


Figure 15b - Max. Iclamp (A) Vs Inductive Load
(mH) IPS021S

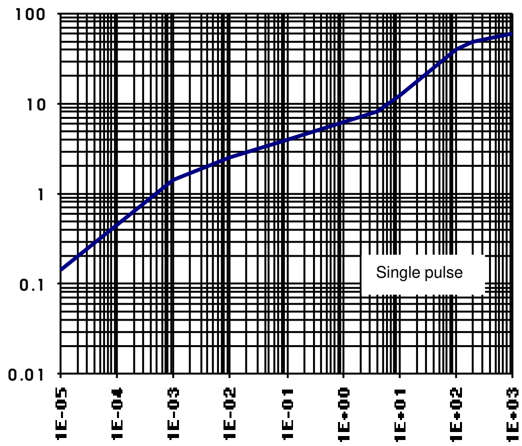


Figure 16 - Transient Thermal Imped. (°C/W)
Vs Time (s)

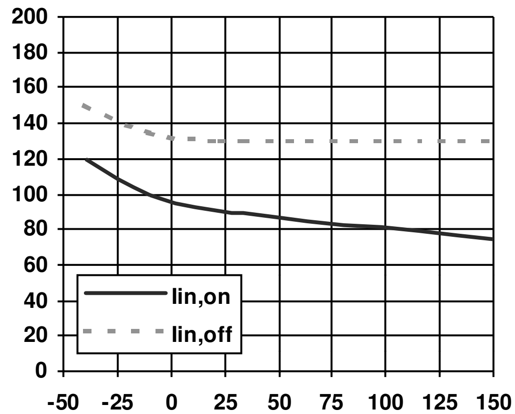


Figure 17 - Input Current (uA) Vs
Junction Temperature (°C)

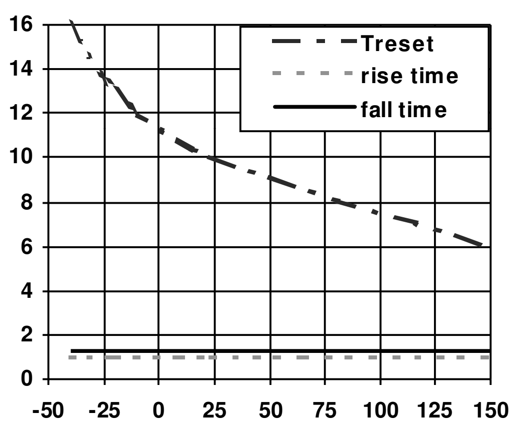


Figure 18 - Rise Time, Fall Time and Treset (µs)
Vs Tj (°C)

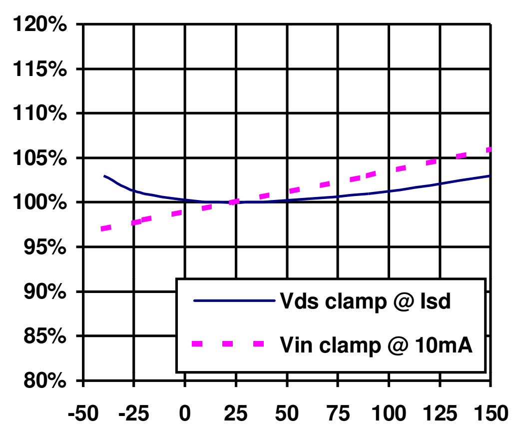
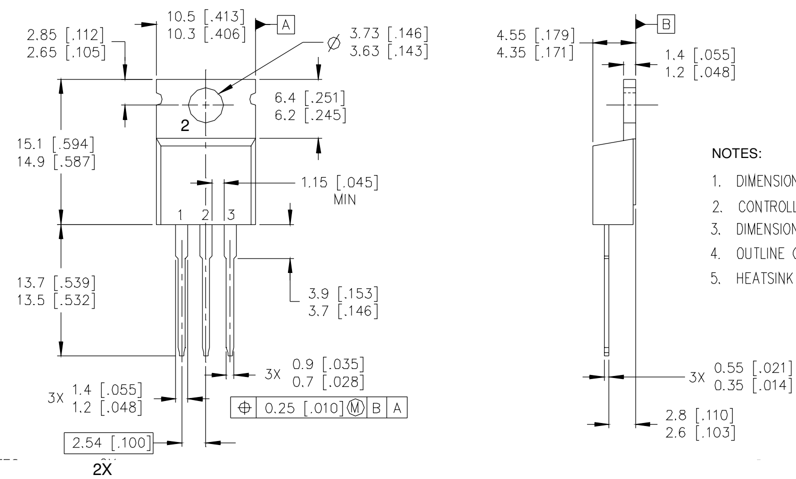


Figure 19 -Vin clamp and Vds clamp (%) Vs
Tj (°C)

Case Outline

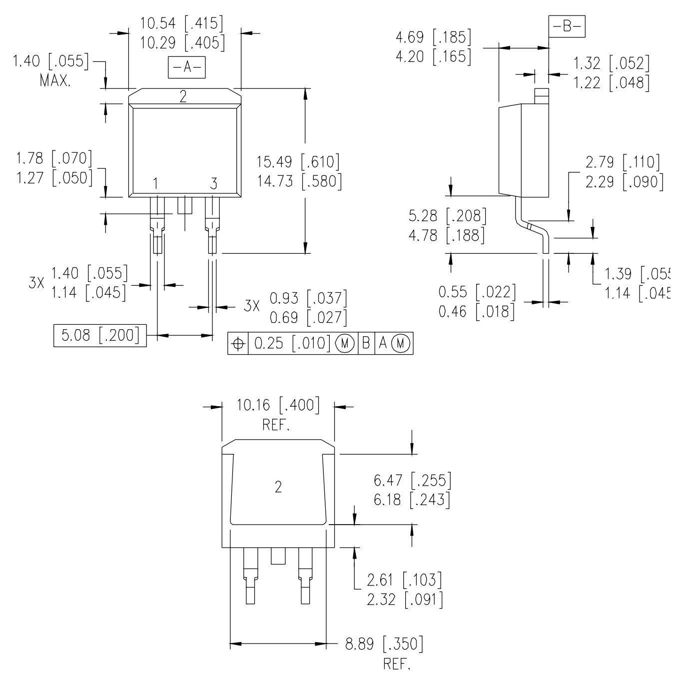


NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
5. HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

3-Lead TO-220AB

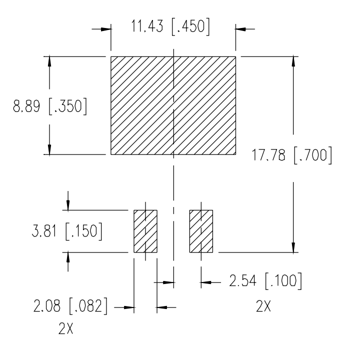
01-6024 00
IRGB 01-3026 01 (TO-220AB)



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSIONS AFTER SOLDER DIP.
5. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

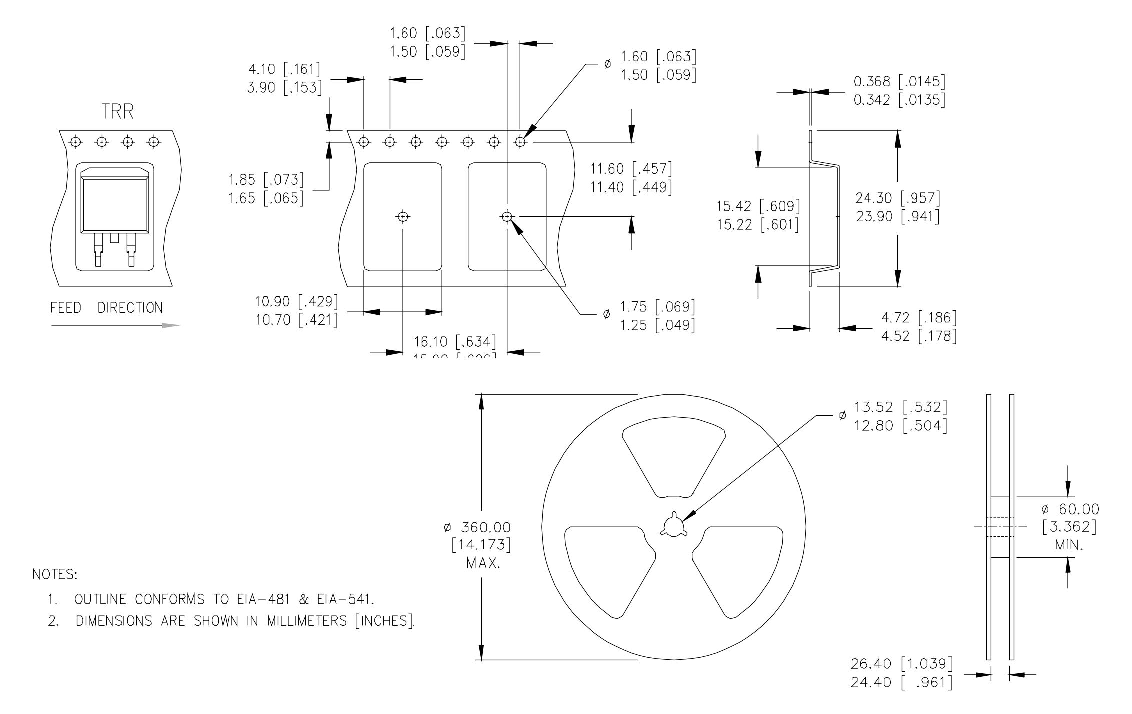
MINIMUM RECOMMENDED FOOTPRINT



3-Lead D²PAK

01-6022 00
01-0016 05 (TO-263AB)

Tape & Reel - D^{2}PAK (SMD220)



01-3072 00

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

Data and specifications subject to change without notice. 6/11/2001

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/