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Data Sheet No.PD60156-J

International
IOR Rectifier

IPS511G/IPS512G/IPS514G

FULLY PROTECTED HIGH SIDE POWER MOSFET SWITCH

Features

- Over temperature protection (with auto-restart)
- Short-circuit protection (current limit)
- Active clamp
- E.S.D protection
- Status feedback
- Open load detection
- Logic gound isolated from power ground

Product Summary

$R_{ds(on)}$	150mΩ (max)
V_{clamp}	50V
I_{Limit}	5A
$V_{open\ load}$	3V

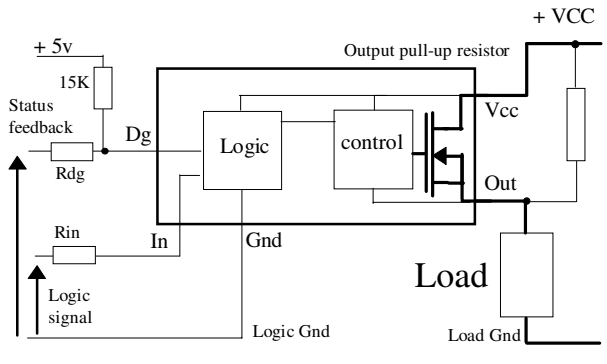
Description

The IPS511G/IPS512G/IPS514G are fully protected five terminal high side switches with built in short-circuit, over-temperature, ESD protection, inductive load capability and diagnostic feedback. The output current is controlled when it reaches I_{lim} value. The current limitation is activated until the thermal protection acts. The over-temperature protection turns off the high side switch if the junction temperature exceeds Tshutdown. It will automatically restart after the junction has cooled 7ºC below Tshutdown. A diagnostic pin is provided for status feedback of short-circuit, over-temperature and open load detection. The double level shifter circuitry allows large offsets between the logic ground and the load ground.

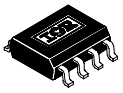
Truth Table

Op. Conditions	In	Out	Dg
Normal	H	H	H
Normal	L	L	L
Open load	H	H	H
Open load	L	H	H
Over current	H	L (limiting)	L
Over current	L	L	L
Over-temperature	H	L (cycling)	L
Over-temperature	L	L	L

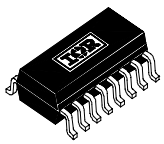
Typical Connection



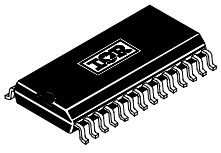
Available Package



8 Lead SOIC
(Single)
IPS511G



16 Lead SOIC
(Dual)
IPS512G



28 Lead SOIC WB
(Quad)
IPS514G

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to GROUND lead. (T_j = 25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{out}	Maximum output voltage	V_{CC}-50	V_{CC}+0.3	V	
V_{offset}	Maximum logic ground to load ground offset	V_{CC}-50	V_{CC}+0.3		
V_{in}	Maximum Input voltage	-0.3	5.5		
$I_{in, max}$	Maximum IN current	-5	10	mA	
V_{dg}	Maximum diagnostic output voltage	-0.3	5.5	V	
$I_{dg, max}$	Maximum diagnostic output current	-1	10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1) (IPS511G)	—	1.4	A	
	(per leg/both legs ON - IPS512G)	—	0.8		
	(per leg/all legs ON - IPS514G)	—	0.7		
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	10		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10μH
P_d	Maximum power dissipation (rth=125°C/W) IPS511G	—	1	W	
	(rth=85°C/W, both legs on) IPS512G	—	1.5		
	(rth=50°C/W, all legs on) IPS514G	—	2.5		
T_j max.	Max. storage & operating junction temp.	-40	+150	°C	
Vcc max.	Maximum Vcc voltage	—	50	V	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th1}	Thermal resistance with standard footprint	—	100	—	°C/W	8 Lead SOIC
R_{th2}	Thermal resistance with 1" square footprint	—	80	—		
R_{th1} (2 mos on)	Thermal resistance with standard footprint (2 mosfets on)	—	85	—		16 Lead SOIC
R_{th2} (1) (1 mos on)	Thermal resistance with standard footprint (1 mosfet on)	—	100	—		
R_{th2} (2 mos on)	Thermal resistance with 1" square footprint (2 mosfets on)	—	50	—		
R_{th1}	Thermal resistance with standard footprint	—	60	—		28 Lead SOIC
R_{th2} (2 mos on)	Thermal resistance with standard footprint (2 mosfets on)	—	55	—		
R_{th3} (4 mos on)	Thermal resistance with standard footprint (4 mosfets on)	—	50	—		
R_{th1}	Thermal resistance with 1" square footprint	—	45	—		
R_{th2} (2 mos on)	Thermal resistance with 1" square footprint (2 mosfets on)	—	40	—		
R_{th3} 4 mos on)	Thermal resistance with 1" square footprint (4 mosfets on)	—	35	—		

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
V_{cc}	Continuous V_{cc} voltage	5.5	35	V
V_{IH}	High level input voltage	4	5.5	
V_{IL}	Low level input voltage	-0.3	0.9	
I_{out} Tamb=85°C	Continuous output current (TAmbient = 85°C, Tj = 125°C, rth = 100°C/W) IPS511G	—	1.4	A
I_{out} Tamb=85°C	Continuous output current per leg (TAmbient = 85°C, Tj = 125°C R_{th} = 85°C/W both legs on) IPS512G	—	1.0	
I_{out} Tamb=85°C	Continuous output current per leg (TAmbient = 85°C, Tj = 125°C R_{th} = 60°C/W all legs on) IPS514G	—	0.85	
Rin	Recommended resistor in series with IN pin	4	6	kΩ
Rdg	Recommended resistor in series with DG pin	10	20	

Static Electrical Characteristics

(T_j = 25°C, V_{cc} = 14V unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$ @Tj=25°C	ON state resistance T_j = 25°C	—	130	150	mΩ	V_{in} = 5V, I_{out} = 2.5A
$R_{ds(on)}$ (V_{cc}=6V)	ON state resistance @ V_{cc} = 6V	—	130	150		V_{in} = 5V, I_{out} = 1A
$R_{ds(on)}$ @Tj=150°C	ON state resistance Tj = 150°C	—	220	—		V_{in} = 5V, I_{out} = 2.5A
V_{cc} oper.	Operating voltage range	5.5	—	35	V	
V clamp 1	V_{cc} to OUT clamp voltage 1	50	56	—		I_d = 10mA (see Fig.1 & 2)
V clamp 2	V_{cc} to OUT clamp voltage 2	—	58	65		I_d = I_{sd} (see Fig.1 & 2)
V_f	Body diode forward voltage	—	0.9	1.2		I_d = 2.5A, V_{in} = 0V
I_{cc} off	Supply current when OFF	—	16	50	µA	V_{in} = 0V, V_{out} = 0V
I_{cc} on	Supply current when ON	—	0.7	2	mA	V_{in} = 5V
I_{cc} ac	Ripple current when ON (AC RMS)	—	20	—	µA	V_{in} = 5V
Vdgl	Low level diagnostic output voltage	—	0.15	0.4	V	I_{dg} = 1.6 mA
I_{oh}	Output leakage current	—	60	120	µA	V_{out} = 6V
I_{ol}	Output leakage current	0	—	25		V_{out} = 0V
I_{dg} leakage	Diagnostic output leakage current	—	—	10		V_{dg} = 5.5V
V_{ih}	IN high threshold voltage	—	2.3	3	V	
V_{il}	IN low threshold voltage	1	2	—		
I_{in}, on	On state IN positive current	—	70	200	µA	V_{in} = 5V
In, hyst.	Input hysteresis	0.1	0.25	0.5	V	

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 5.6Ω, T_j = 25°C, (unless otherwise specified).

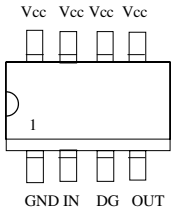
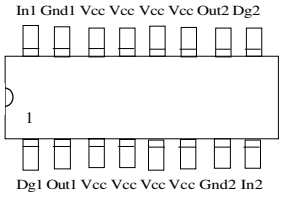
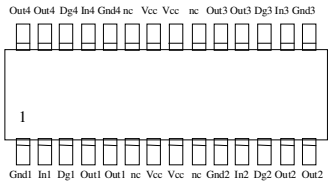
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{don}	Turn-on delay time	—	7	50	µs	See figure 3
T_{r1}	Rise time to V_{out} = V_{cc} - 5V	—	10	50		
T_{r2}	Rise time from the end of Tr1 to V_{out} = 90% of V_{cc}	—	45	95		
dV/dt (on)	Turn ON dV/dt	—	1.3	4	V/µs	
E_{on}	Turn ON energy	—	400	—	µs	See figure 4
T_{doff}	Turn-off delay time	—	15	50		
T_f	Fall time to V_{out} = 10% of V_{cc}	—	10	50		
dV/dt (off)	Turn OFF dV/dt	—	2	6	V/µs	
E_{off}	Turn OFF energy	—	80	—	µJ	
T_{diag}	V_{out} to Vdiag propagation delay	—	5	15	µs	See figure 6

Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{lim}	Internal current limit	3	5	7	A	V_{out} = 0V
T_{sd+}	Over-temp. positive going threshold	—	165	—	°C	See fig. 2
T_{sd-}	Over-temp. negative going threshold	—	158	—	°C	See fig. 2
V_{sc}	Short-circuit detection voltage (3)	2	3	4	V	See fig. 2
$V_{open\ load}$	Open load detection threshold	2	3	4	V	

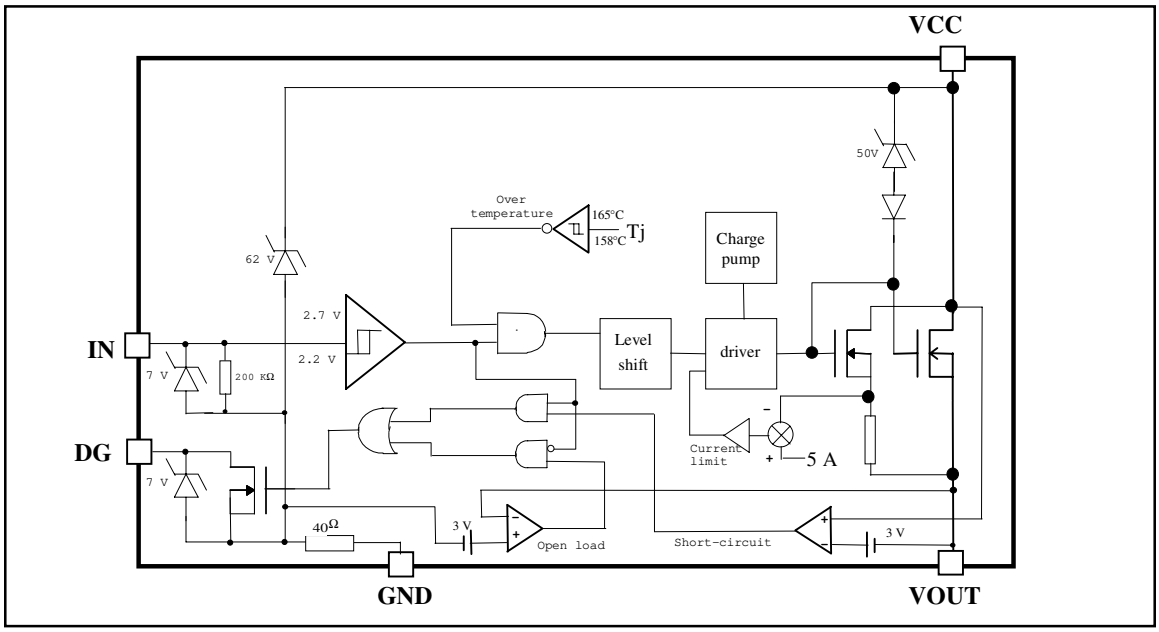
(3) Referenced to V_{cc}

Lead Assignments

		
8 Lead SOIC	16 Lead SOIC	28 Lead SOIC WB
IPS511G	**IPS512G**	**IPS514G**
Part Number		

Functional Block Diagram

All values are typical



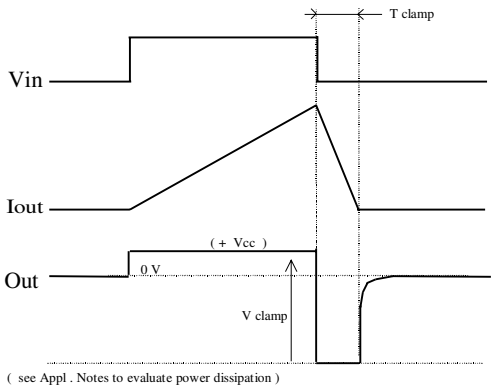


Figure 1 - Active clamp waveforms

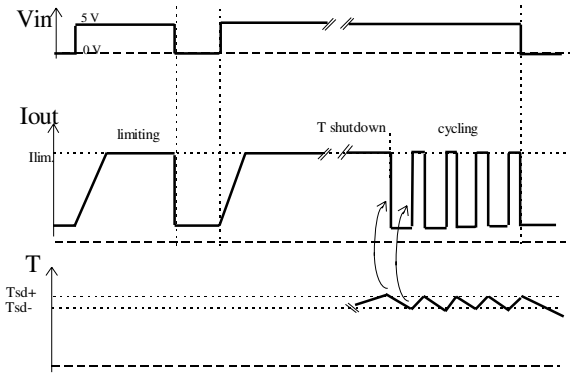


Figure 2 - Protection timing diagram

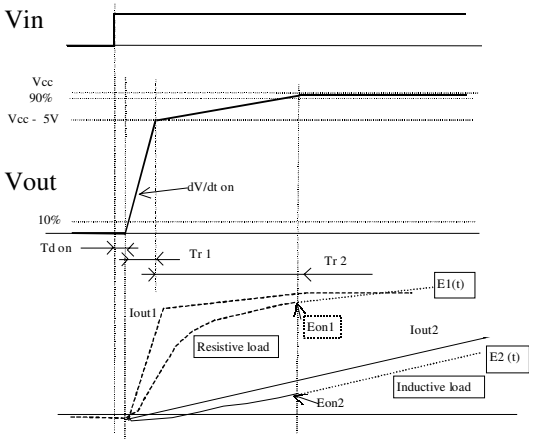


Figure 3 - Switching times definition (turn-on)
Turn on energy with a resistive or an inductive load

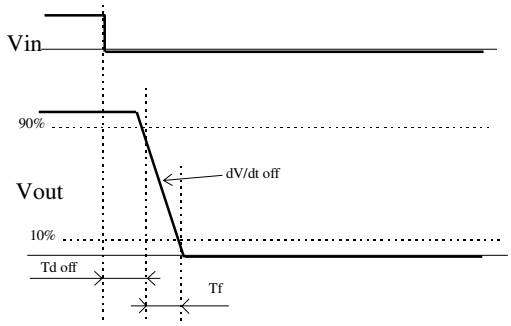


Figure 4 - Switching times definition (turn-off)

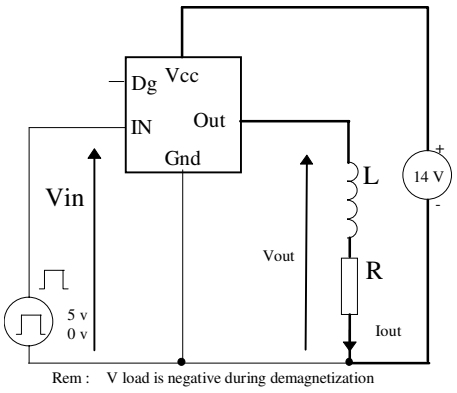


Figure 5 - Active clamp test circuit

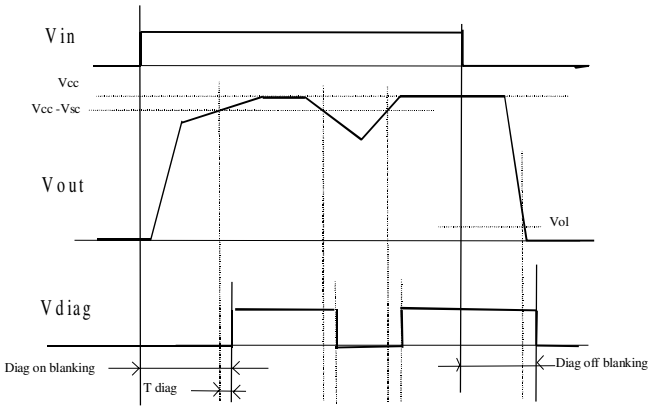


Figure 6 - Diagnostic delay definitions

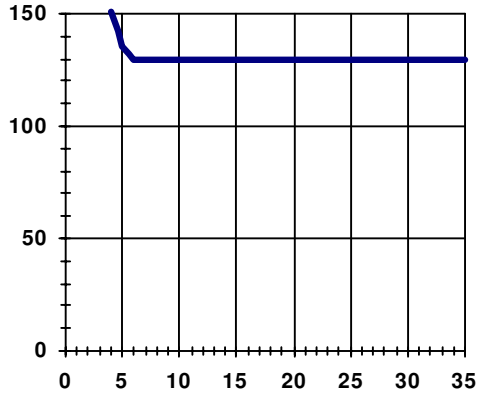


Figure 7 - $R_{ds(on)}$ (mΩ) Vs V_{cc} (V)

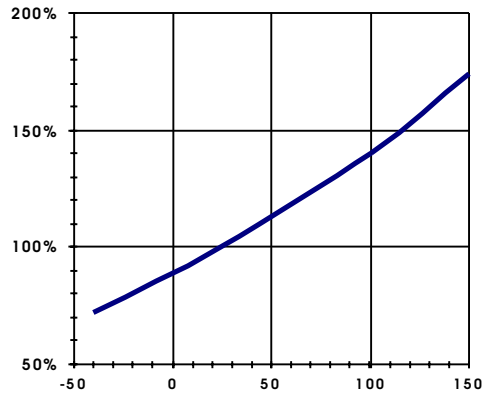


Figure 8 - Normalized $R_{ds(on)}$ (%) Vs T_j (°C)

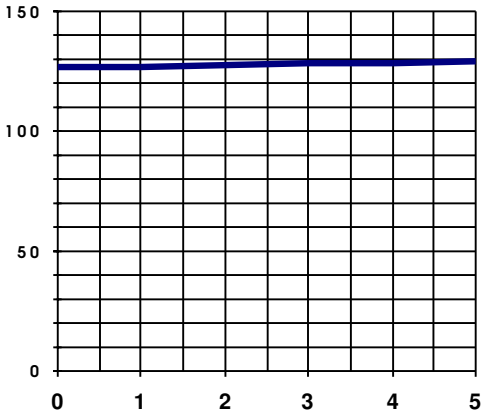


Figure 9 - Rds(on) (mΩ) Vs I_{out} (A)

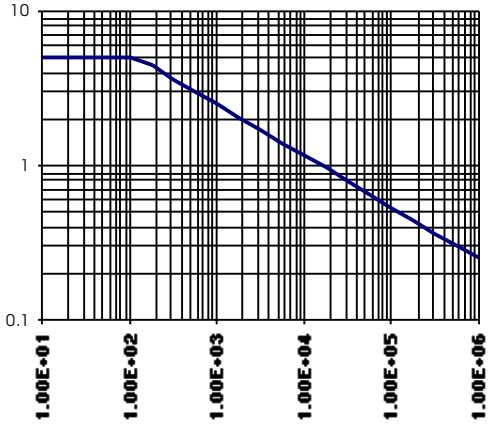


Figure 10 - Max. I_{out} (A) Vs Load Inductance (uH)

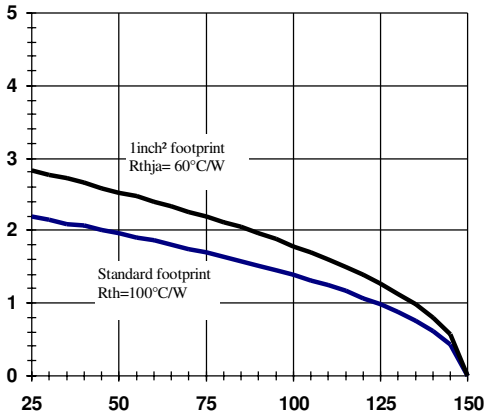


Figure 11a - Max load current (A) Vs Tamb (ºC)
IPS511G

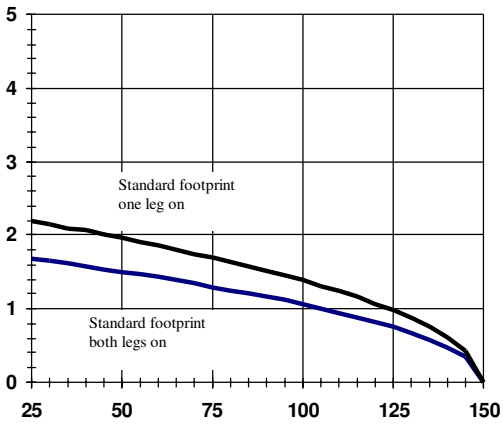


Figure 11b - Max load current (A) Vs Tamb (ºC)
IPS512G

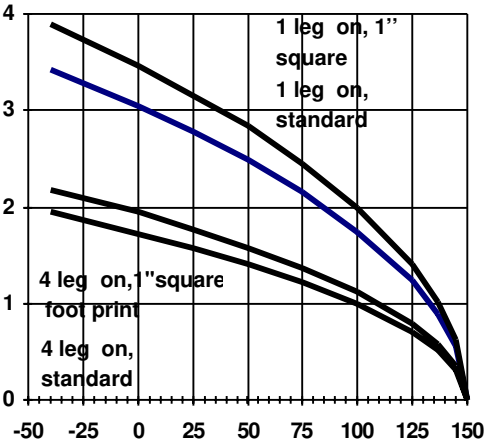


Figure 11c - Max load current (A) Vs Tamb (ºC)
IPS514G

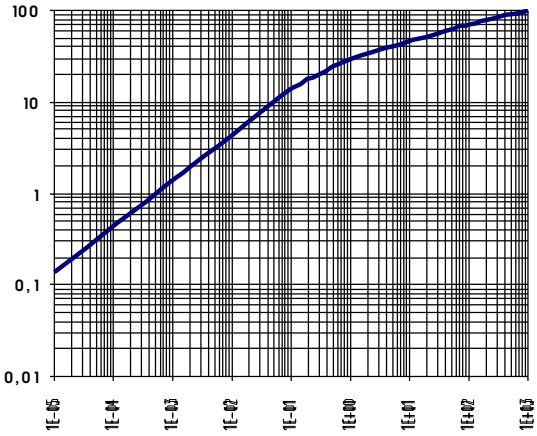


Figure 12a - Transient Thermal Impedance (ºC/W)
Vs Time (S) - IPS511G/IPS512G

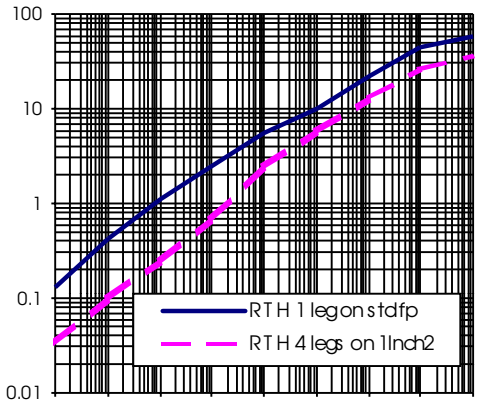


Figure 12b - Transient Thermal Impedance (ºC/W) Vs Time (S) - IPS514G

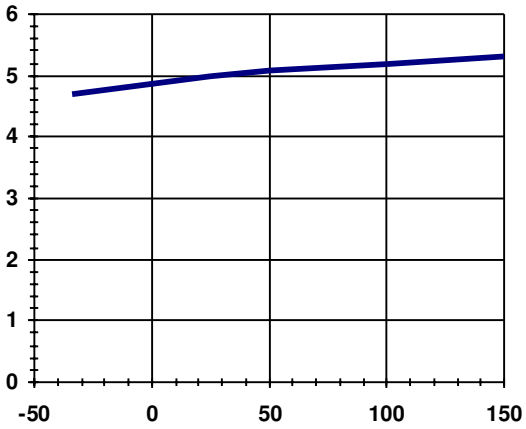


Figure 13 - I_{lim} (A) Vs T_j (ºC)

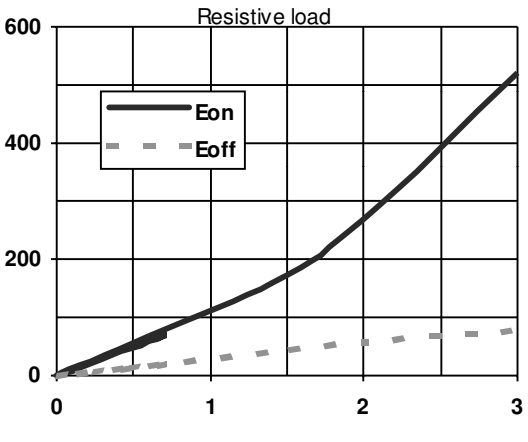


Figure 14 - Eon, Eoff (µJ) vs I (A)

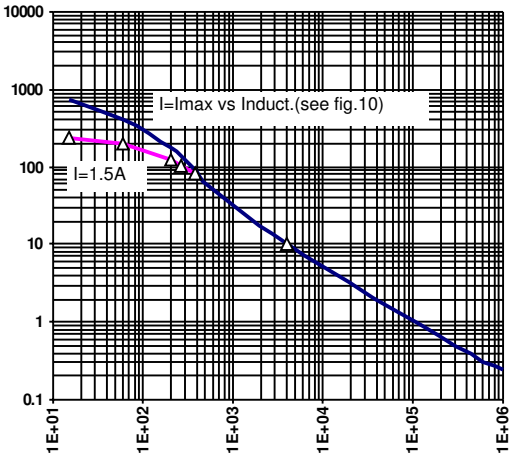


Figure 15 - E_{on} (µJ) Vs Load Inductance (µH) (see Fig. 3)

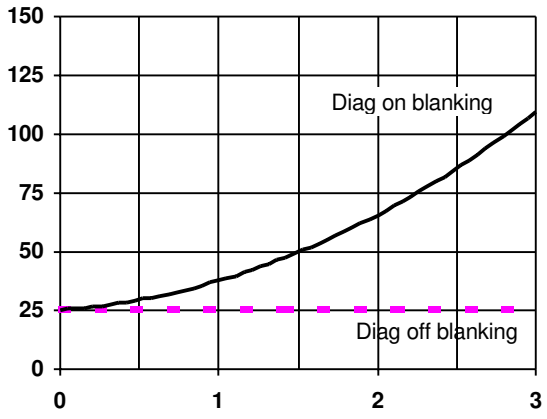


Figure 16 - Diag Blanking time (µS) Vs I_{out} (A)
(resistive load - see Fig. 6)

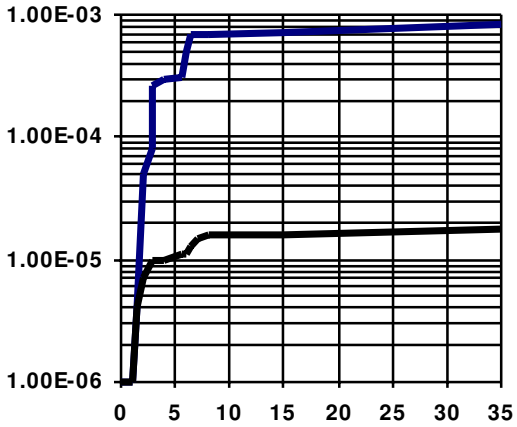
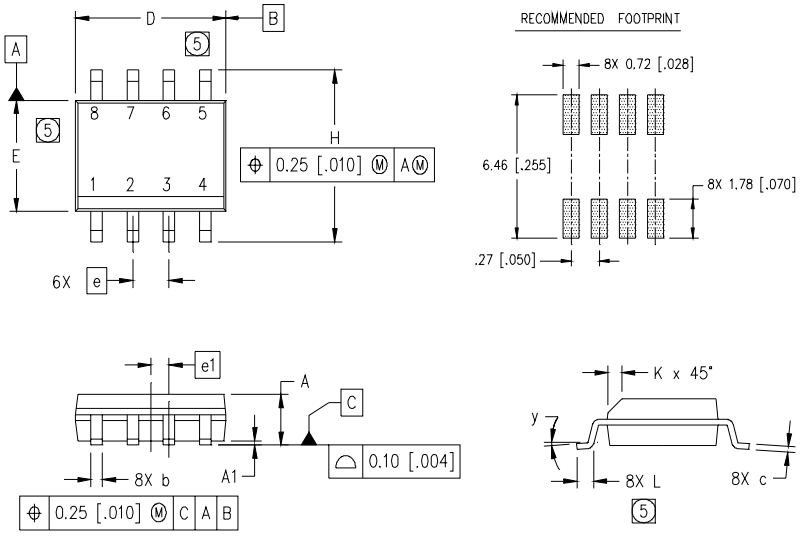


Figure 17 - I_{cc} (mA) Vs V_{cc} (V)

Case Outline - IPS511G



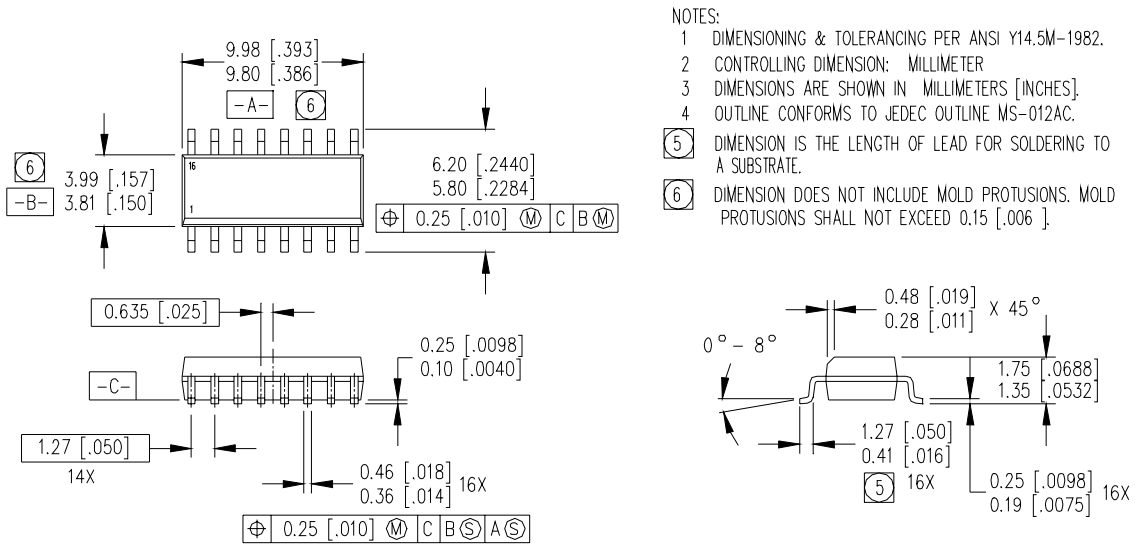
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

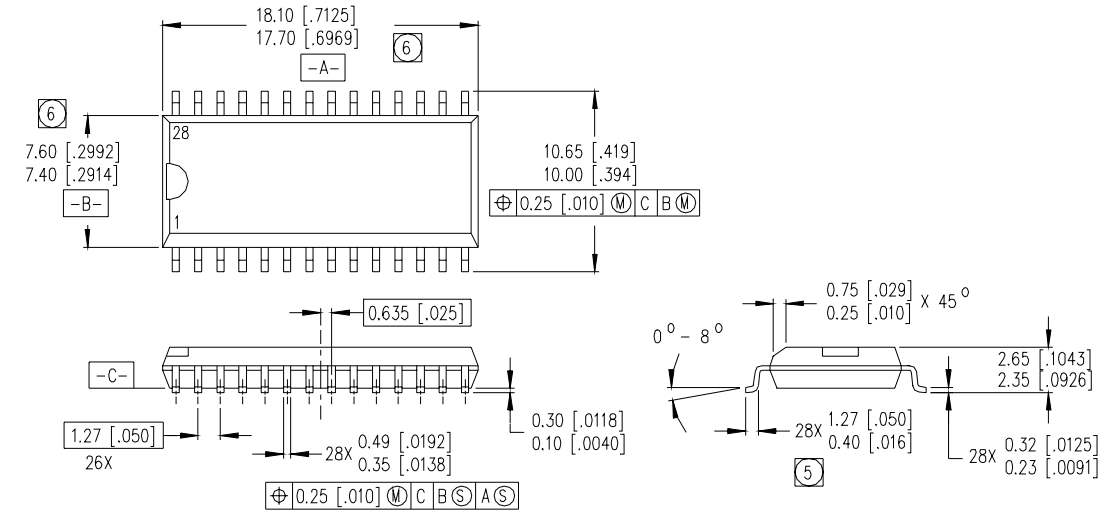
(MS-012AA) 01-0021 09

Case Outline - IPS512G



16 Lead SOIC (narrow body) 01-3064 00

Case Outline - IPS514G



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28 Lead SOIC

01-3040 02

International
IOR Rectifier

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