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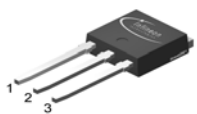



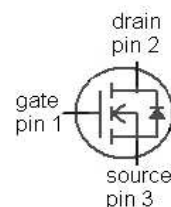
**OptiMOS®2 Power-Transistor**
**Package**
**Marking**

- Qualified according to JEDEC<sup>1)</sup> for target applications
- N-channel - Logic level
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Superior thermal resistance
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant

**Product Summary**

$V_{DS}$	30	V
$R_{DS(on),max}$	6.3	mΩ
$I_D$	50	A

Type	IPUH6N03LB	IPSH6N03LB
		
<b>Package</b>	PG-TO251-3	PG-TO251-3-11
<b>Marking</b>	H6N03LB	H6N03LB


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ °C}^{2)}$	50	A
		$T_C=100\text{ °C}$	50	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}^{3)}$	200	
Avalanche energy, single pulse	$E_{AS}$	$I_D=50\text{ A}, R_{GS}=25\text{ Ω}$	160	mJ
Reverse diode $dv/dt$	$dv/dt$	$I_D=50\text{ A}, V_{DS}=20\text{ V},$ $di/dt=200\text{ A/μs},$ $T_{j,max}=175\text{ °C}$	6	kV/μs
Gate source voltage <sup>4)</sup>	$V_{GS}$		±20	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	83	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

<sup>1)</sup> J-STD20 and JESD22

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{thJC}$		-	-	1.8	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>5)</sup>	-	-	40	

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=40\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=30\text{ A}$	-	7.4	9.3	m $\Omega$
		$V_{GS}=10\text{ V}, I_D=50\text{ A}$	-	5.2	6.3	
Gate resistance	$R_G$		-	1.2	-	$\Omega$
Transconductance	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=50\text{ A}$	39	78	-	S

<sup>2)</sup> Current is limited by bondwire; with an  $R_{thJC}=1.8\text{ K/W}$  the chip is able to carry 86 A.

<sup>3)</sup> See figure 3

<sup>4)</sup>  $T_{j,max}=150\text{ °C}$  and duty cycle  $D<0.25$  for  $V_{GS}<-5\text{ V}$

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	2100	2800	pF
Output capacitance	$C_{oss}$		-	750	1000	
Reverse transfer capacitance	$C_{rss}$		-	97	150	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=25\text{ A}, R_G=2.7\ \Omega$	-	7	10	ns
Rise time	$t_r$		-	6	8	
Turn-off delay time	$t_{d(off)}$		-	25	37	
Fall time	$t_f$		-	4.0	6.0	

**Gate Charge Characteristics<sup>6)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=15\text{ V}, I_D=25\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	6.5	8.7	nC
Gate charge at threshold	$Q_{g(th)}$		-	3.3	4.5	
Gate to drain charge	$Q_{gd}$		-	4.2	6.4	
Switching charge	$Q_{sw}$		-	7.4	11	
Gate charge total	$Q_g$		-	16	22	
Gate plateau voltage	$V_{plateau}$		-	3.1	-	
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$	-	14	19	nC
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	17	22	

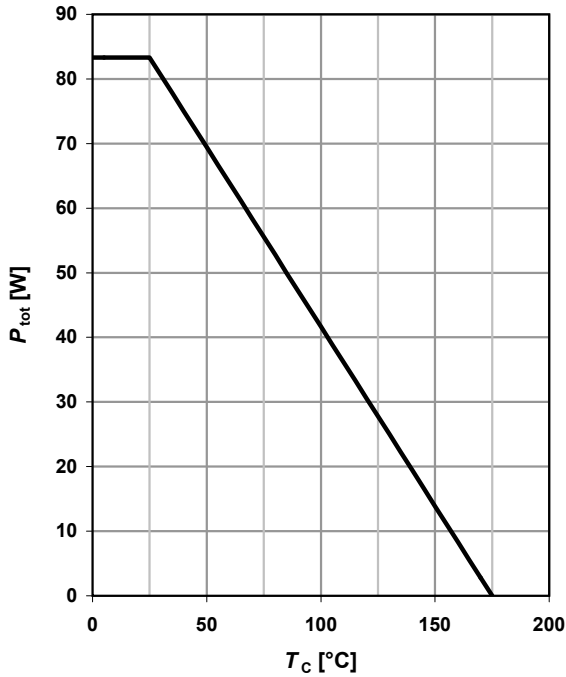
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	200	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.93	1.2	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

<sup>6)</sup> See figure 16 for gate charge parameter definition

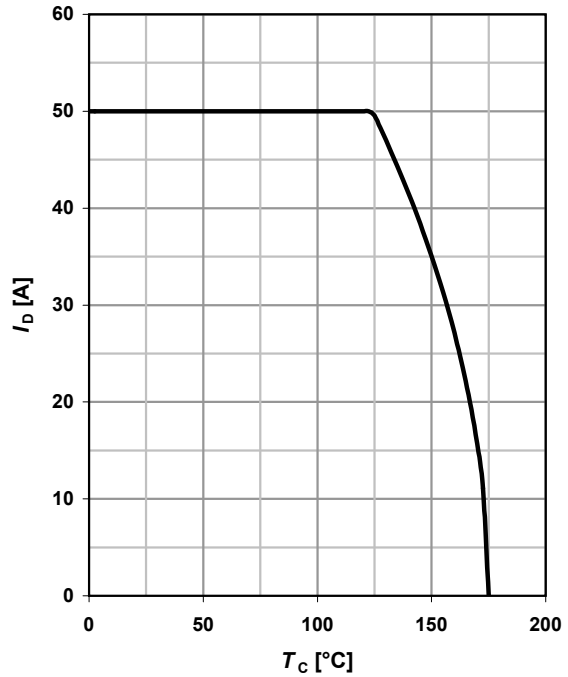
**1 Power dissipation**

$$P_{tot} = f(T_C)$$



**2 Drain current**

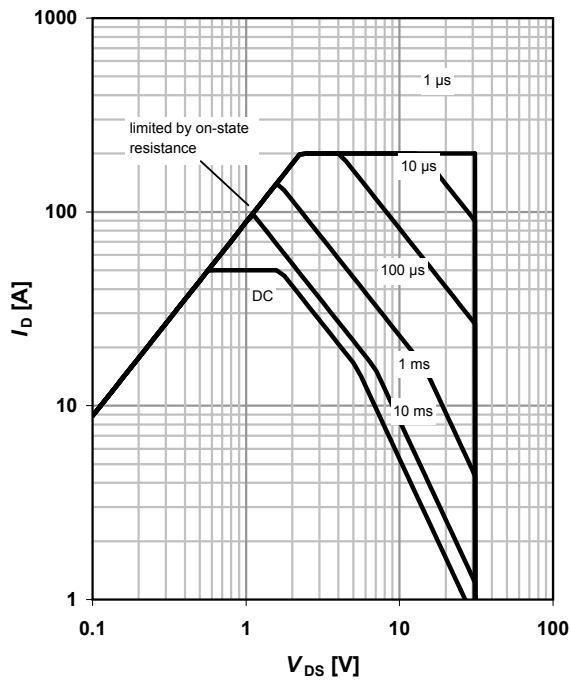
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



**3 Safe operating area**

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

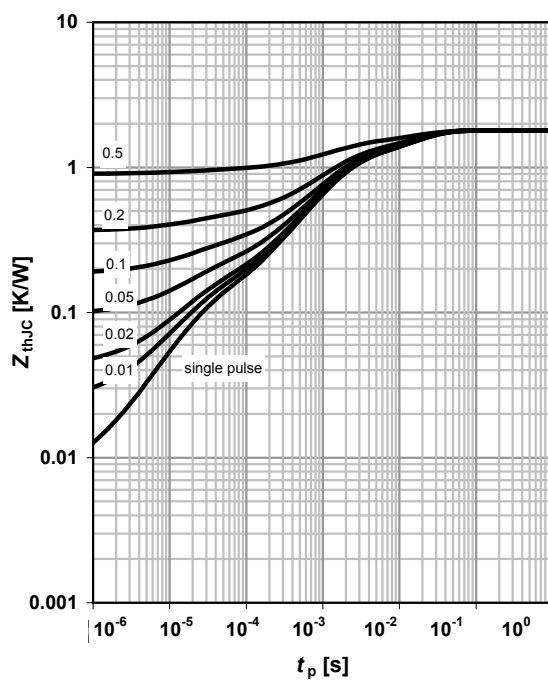
parameter:  $t_p$



**4 Max. transient thermal impedance**

$$Z_{thJC} = f(t_p)$$

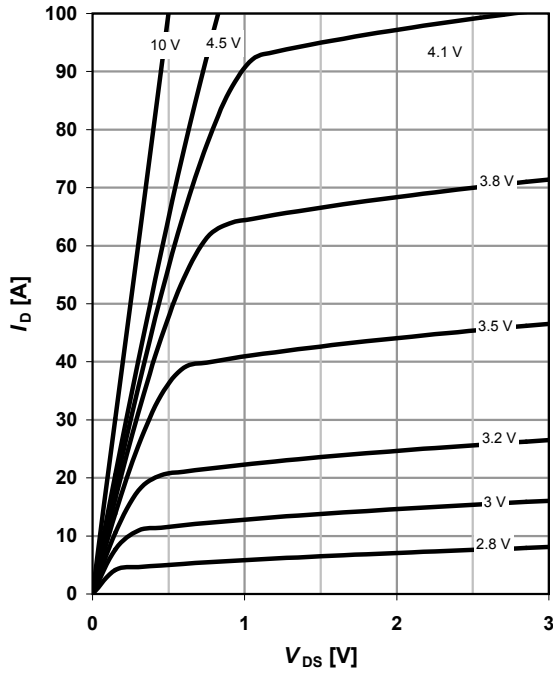
parameter:  $D = t_p / T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

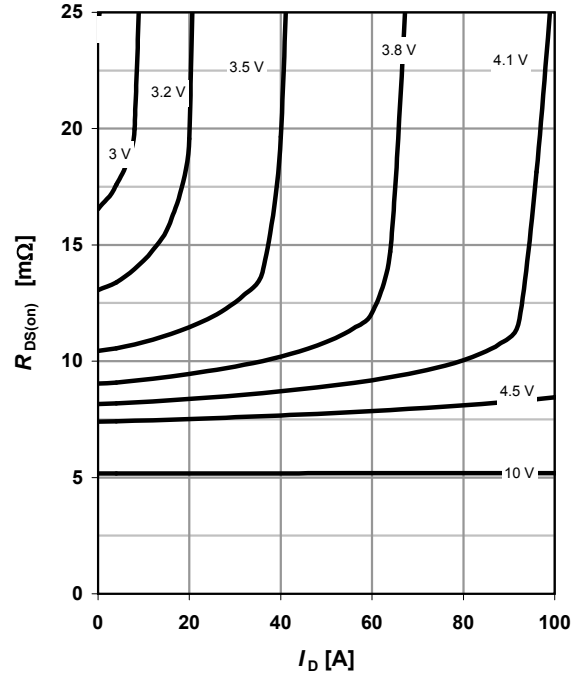
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

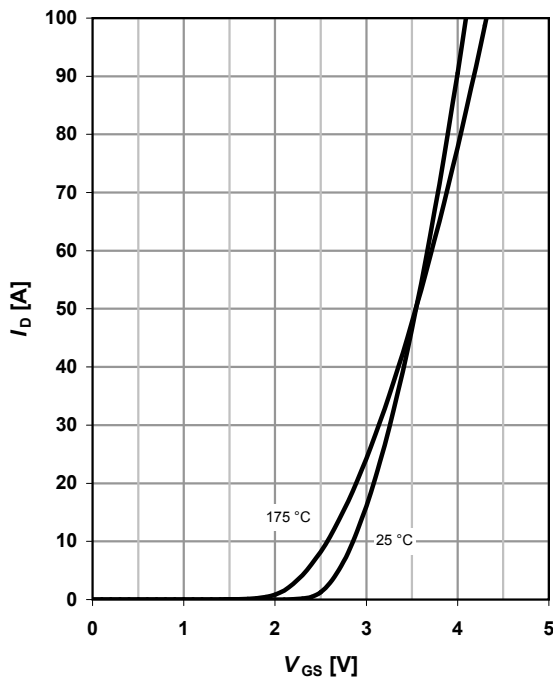
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

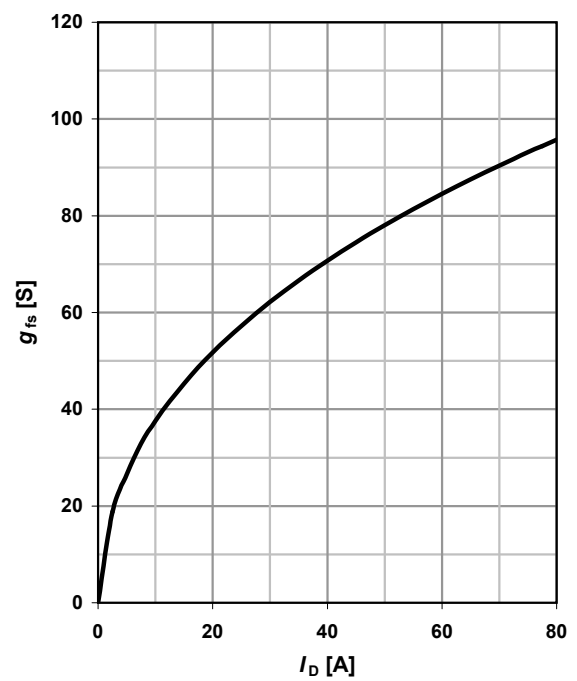
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



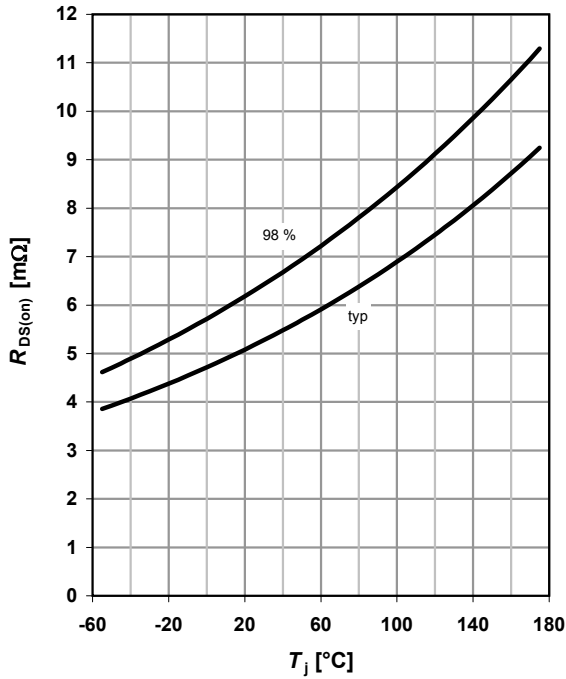
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



**9 Drain-source on-state resistance**

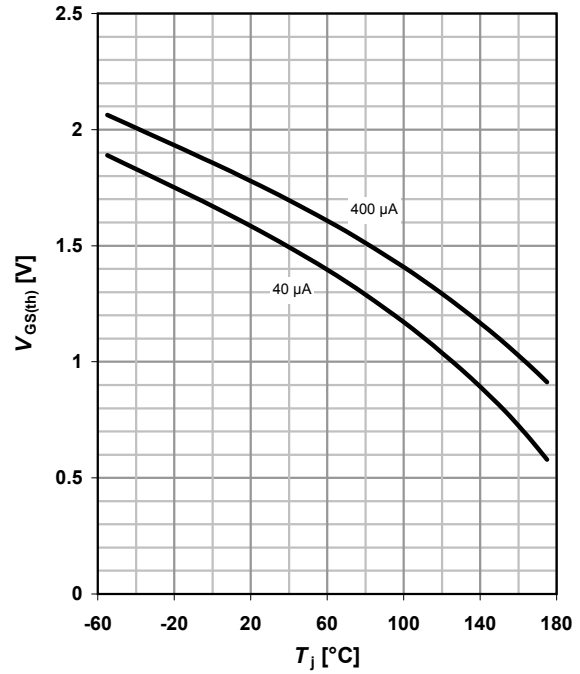
$R_{DS(on)} = f(T_j); I_D = 50 \text{ A}; V_{GS} = 10 \text{ V}$



**10 Typ. gate threshold voltage**

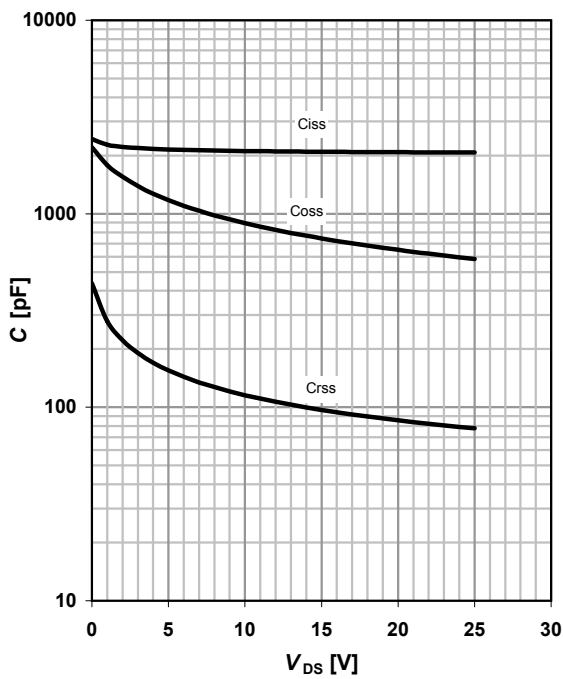
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**11 Typ. Capacitances**

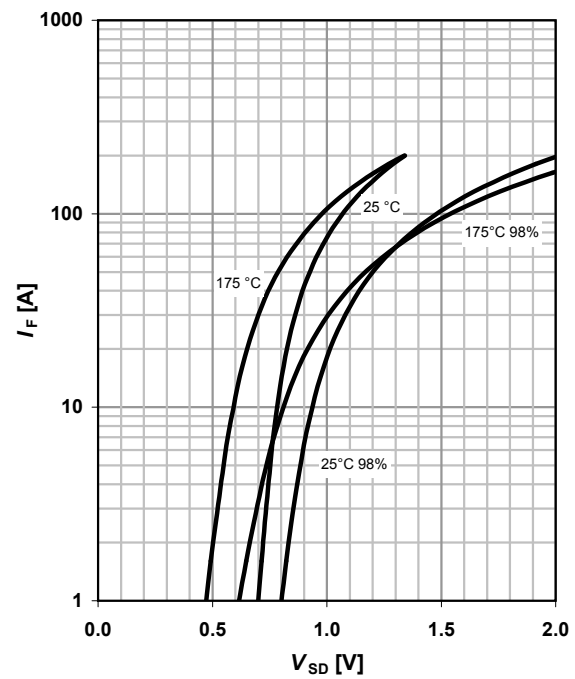
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F = f(V_{SD})$

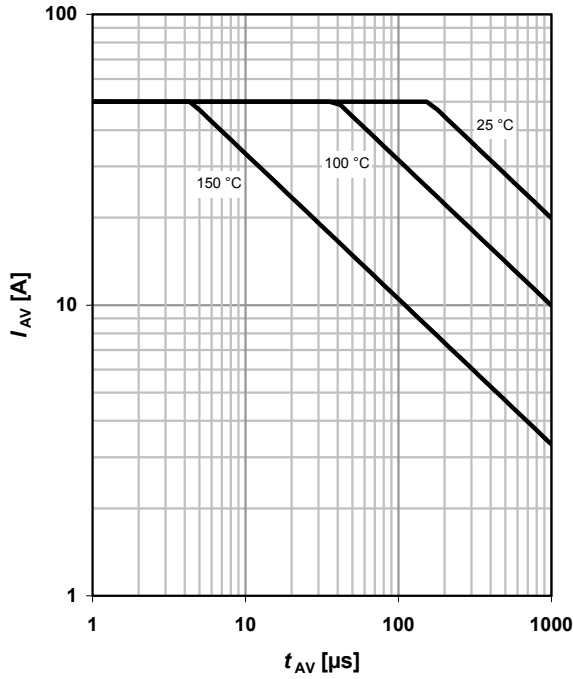
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

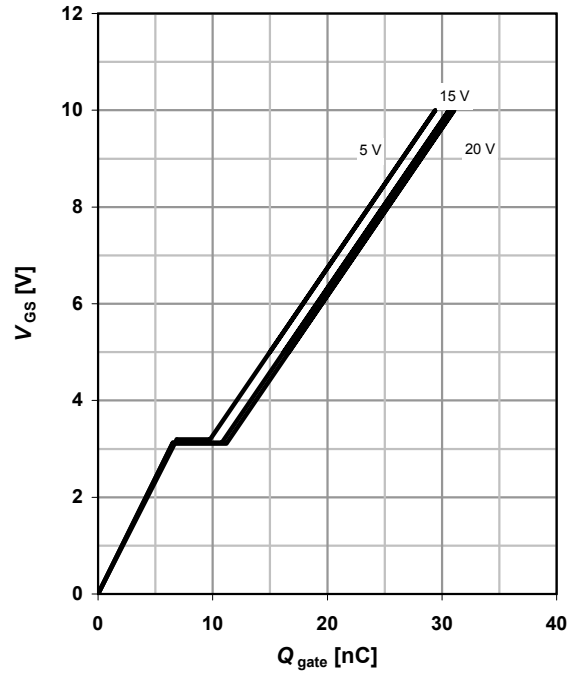
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

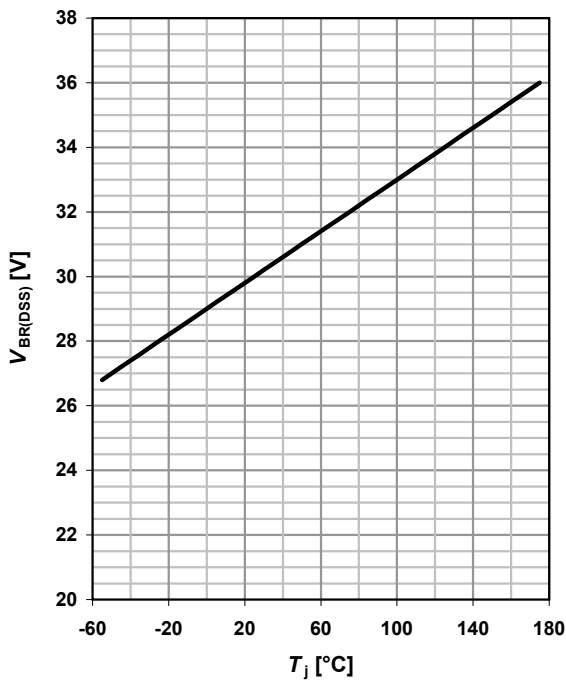
$V_{GS}=f(Q_{gate}); I_D=25 \text{ A pulsed}$

parameter:  $V_{DD}$

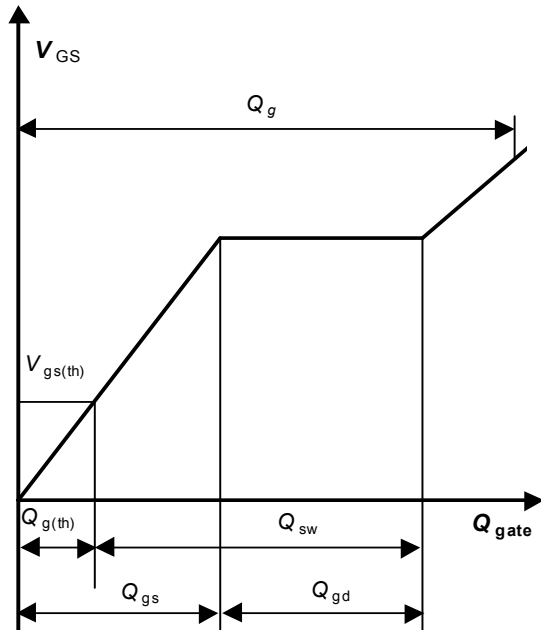


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

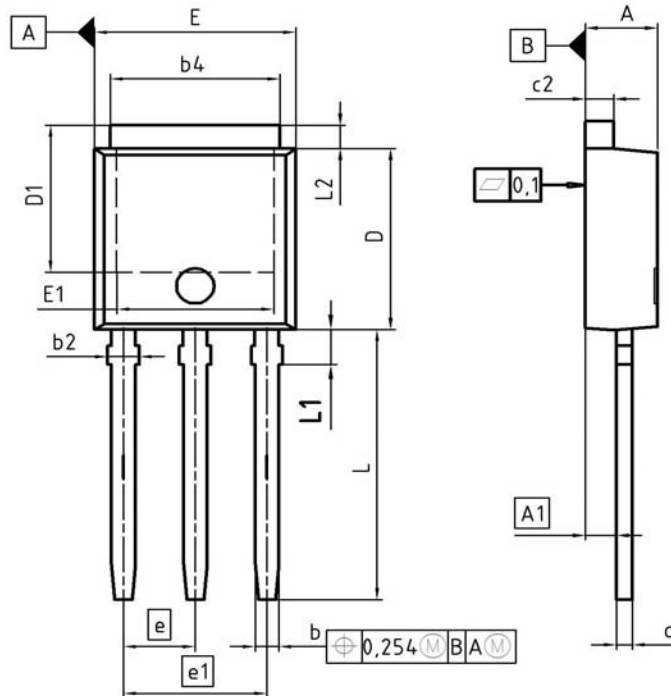


**16 Gate charge waveforms**





PG-T0251-3: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.90	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.77	0.198	0.227
E	6.35	6.73	0.250	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	8.89	9.65	0.350	0.380
L1	1.90	2.29	0.075	0.090
L2	0.89	1.37	0.035	0.054

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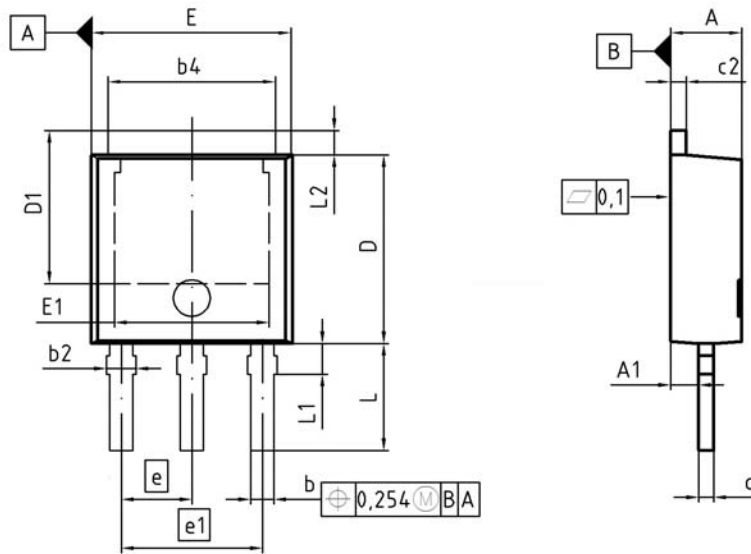
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PG-TO251-3-11: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.39	0.086	0.094
A1	0.80	1.14	0.031	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.58	0.018	0.023
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.44	0.198	0.214
E	6.35	6.73	0.250	0.265
E1	4.90	5.10	0.193	0.201
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	3.40	3.60	0.134	0.142
L1	0.90	1.10	0.035	0.043
L2	0.90	1.10	0.035	0.043

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