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DSP Builder Handbook

Volume 2: DSP Builder Standard Blockset

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Feedback

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Section I. DSP Builder Standard Blockset User Guide

1. About DSP Builder Standard Blockset

Note: DSP Builder standard blockset is a legacy product and Altera recommends you do not use it for new designs, except as a wrapper for advanced blockset designs.

Device Family Support

DSP Builder supports the following Altera® device families:

- Arria V
- Arria V GZ
- Arria 10
- Cyclone IV GX
- Cyclone IV E
- Cyclone V
- Stratix® IV
- Stratix V

Features

DSP Builder standard blockset supports the following features:

- Altera DSP MegaCore® functions in a DSP Builder design model.
- Fixed-point arithmetic and logical operators for use with the Simulink software.
- Avalon® Memory-Mapped (Avalon-MM) interfaces including user configurable blocks, which you can use to build custom logic that works with the Nios® II processor and other Qsys designs.
- Avalon Streaming (Avalon-ST) interfaces including an Packet Format Converter block and configurable Avalon-ST sink and Avalon-ST source blocks.
- VHDL testbench.
- Rapid prototyping using Altera development boards.
- The SignalTap® II logic analyzer—an embedded signal analyzer that probes signals from the Altera device on the DSP board and imports the data into the MATLAB workspace to ease visual analysis.
- HDL import of VHDL or Verilog HDL design entities and HDL defined in a Quartus Prime project file.
- Hardware-in-the loop (HIL) to enable FPGA hardware accelerated cosimulation with Simulink.
- Tabular and graphical state machine editing.

For information about new features and errata in this release, refer to the *DSP Builder Release Notes*.

General Description

Digital signal processing (DSP) system design in Altera FPGAs requires both high-level algorithm and hardware description language (HDL) development tools.

Altera's DSP Builder integrates these tools by combining the algorithm development, simulation, and verification capabilities of The MathWorks MATLAB and Simulink system-level design tools with VHDL and Verilog HDL design flows, including the Altera Quartus Prime software.

DSP Builder shortens DSP design cycles by helping you create the hardware representation of a DSP design in an algorithm-friendly development environment.

You can combine existing MATLAB functions and Simulink blocks with Altera DSP Builder blocks and Altera intellectual property (IP) MegaCore functions to link system-level design and implementation with DSP algorithm development. In this way, DSP Builder allows system, algorithm, and hardware designers to share a common development platform.

The DSP Builder `Signal Compiler` block reads Simulink Model Files (**.mdl**) that contain other DSP Builder blocks and MegaCore functions. `Signal Compiler` then generates the VHDL files and Tcl scripts for synthesis, hardware implementation, and simulation.

You can use blocks from the standard blockset to create a hardware implementation of a system modeled in Simulink. DSP Builder contains bit- and cycle-accurate Simulink blocks—which cover basic operations such as arithmetic or storage functions—and takes advantage of key device features such as built-in PLLs, DSP blocks, and embedded memory.

You can integrate complex functions by including IP cores in your DSP Builder model. You can also use the faster performance and richer instrumentation of hardware cosimulation by implementing parts of your design in an FPGA.

The standard blockset supports imported HDL subsystems including HDL defined in a Quartus Prime project file.

High-Speed DSP with FPGAs

FPGAs give compelling performance advantage over dedicated DSP devices. You can configure FPGA's element arrays as complex processor routine.

You can link these routines together in serial (the same way that a DSP processor executes them), or connect them in parallel. When connected in parallel, they give many times better performance than standard DSP devices by executing hundreds of instructions at the same time.

Algorithms that benefit from this improved performance include forward-error correction (FEC), modulation and demodulation, and encryption.

Interoperability with the Advanced Blockset

Any standard blockset design can include an advanced blockset design as a single hierarchical entity.

For more information about the advanced blockset, refer to *Volume 3: DSP Builder Advanced Blockset* in the *DSP Builder Handbook*.

For more information about the differences between the standard and advanced blocksets and about design flows that combine both blocksets, refer to *Volume 1: Introduction to DSP Builder* in the *DSP Builder Handbook*.

2. Getting Started

This chapter describes the design flow and a getting started tutorial.

Creating a Design in DSP Builder

1. Create a Simulink design model in the MATLAB software.
2. Compile directly in the Quartus Prime software.
3. Output VHDL files for synthesis and Quartus II compilation or generate files for VHDL simulation.

☞ DSP Builder generates VHDL and does not generate Verilog HDL.

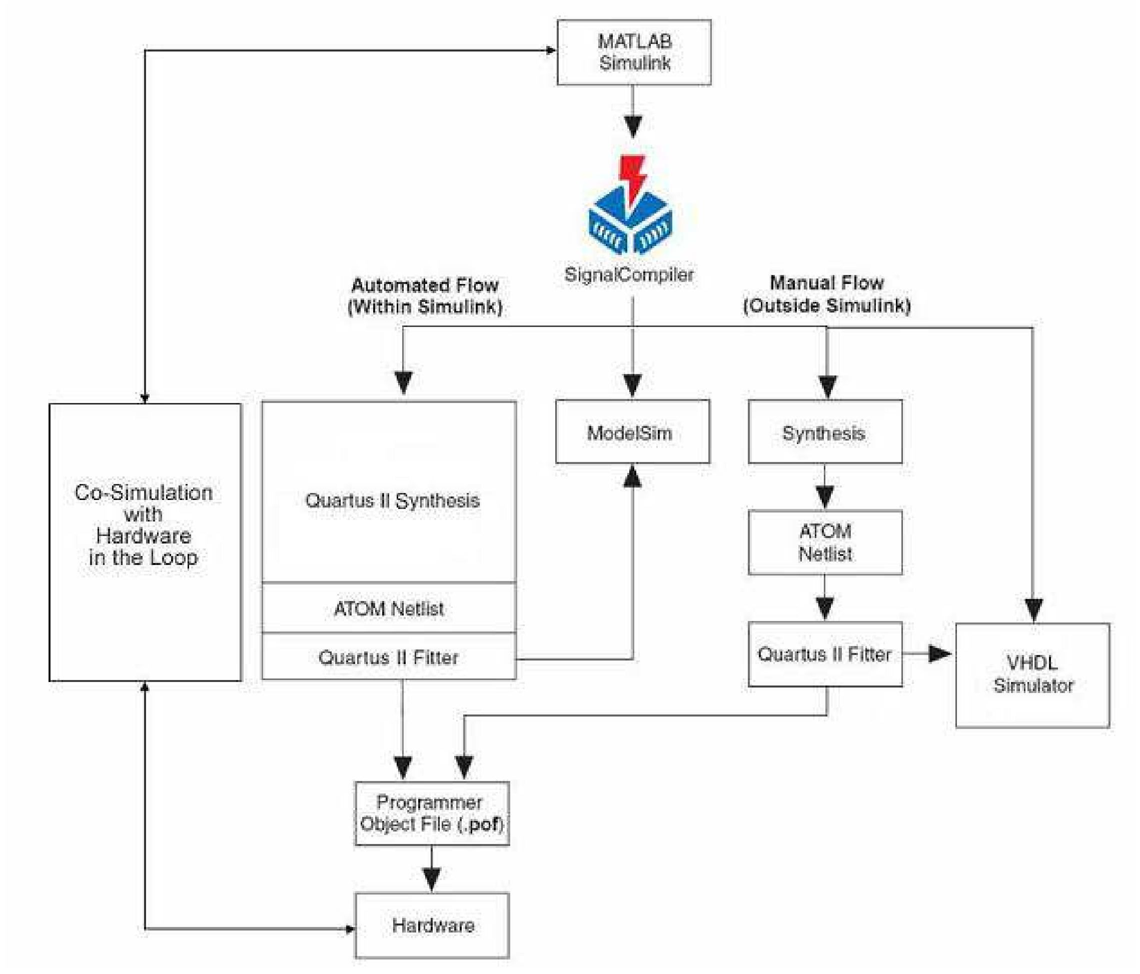
4. Use the `quartus_map` command in the Quartus Prime software to run a simulation netlist flow that generates files for Verilog HDL simulation.

For information about this flow, refer to the Quartus Prime help.

Design Flow

Figure 2–1 shows the system-level design flow using DSP Builder.

Figure 2–1. System-Level Design Flow



The design flow involves the following steps:

1. Use the MathWorks software to create a model with a combination of Simulink and DSP Builder blocks.

   ☞ Separate The DSP Builder blocks in your design from the Simulink blocks by `Input` and `Output` blocks from the DSP Builder IO and Bus library.

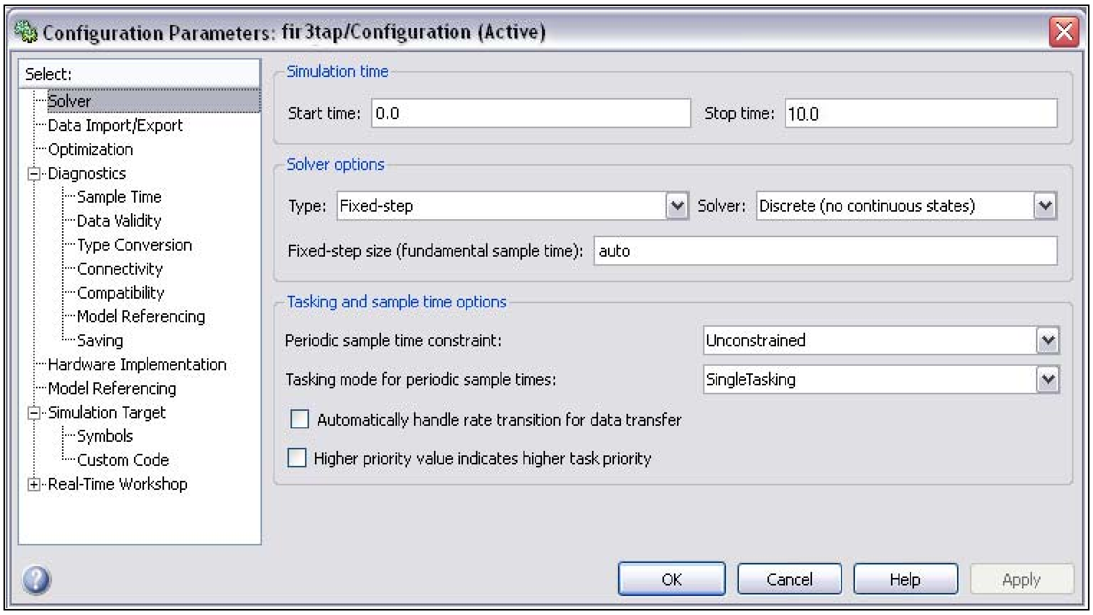
2. Include a `Clock` block from the DSP Builder AltLab library to specify the base clock for your design, which must have a period greater than 1ps but less than 2.1 ms.

   ☞ If no base clock exists in your design, DSP Builder creates a default clock with a 20ns real-world period and a Simulink sample time of 1. You can derive additional clocks from the base clock by adding `Clock_Derived` blocks.

3. Set a discrete (no continuous states) solver in Simulink. Choose a **Fixed-step** solver type if you are using a single clock domain or a **Variable-step** type if you use multiple clock domains.

   To set the solver options, click **Configuration Parameters** on the Simulation menu to open the **Configuration Parameters** dialog box and select the **Solver** page (Figure 2–2).

Figure 2–2. Configuration Parameters for Simulation



Start time: 0.0
Stop time: 10.0
Type: Fixed-step
Solver: Discrete (no continuous states)
Fixed-step size (fundamental sample time): auto
Periodic sample time constraint: Unconstrained
Tasking mode for periodic sample times: SingleTasking
☐ Automatically handle rate transition for data transfer
☐ Higher priority value indicates higher task priority

For detailed information about solver options, refer to the description of the “Solver Pane” in the Simulink Help.

4. Simulate your model in Simulink using a `Scope` block to monitor the results.
5. Run `Signal Compiler` to setup RTL simulation and synthesis.
6. Perform RTL simulation. DSP Builder supports an automated flow for the ModelSim software (using the `TestBench` block). You can also use the generated VHDL for manual simulation in other simulation tools.
7. Use the output files generated by the DSP Builder `Signal Compiler` block to perform RTL synthesis. Alternatively, you can synthesize the VHDL files manually using other synthesis tools.
8. Compile your design in the Quartus II software.
9. Download to a hardware development board and test.

For an automated design flow, the `Signal Compiler` block generates VHDL and Tcl scripts for synthesis in the Quartus II software. The Tcl scripts let you perform synthesis and compilation automatically in the MATLAB and Simulink environment. You can synthesize and simulate the output files in other software tools without the Tcl scripts. In addition, the `Testbench` block generates a testbench and supporting files for VHDL simulation.

For information about controlling the DSP Builder design flow using `Signal Compiler`, refer to "Design Flows for Synthesis, Compilation and Simulation" on page 3–19.

For more information about the blocks in the DSP Builder blockset, refer to the *DSP Builder Standard Blockset Libraries* section in volume 2 of the *DSP Builder Handbook*.

Creating an Amplitude Modulation Design Example

The amplitude modulation design example, **singen.mdl**, demonstrates the DSP Builder design flow.

The amplitude modulation design example is a modulator that has a sine wave generator, a quadrature multiplier, and a delay element. Each block in the model is parameterizable. When you double-click a block in the model, a dialog box displays where you can enter the parameters for the block. Click the **Help** button in these dialog boxes to view help for a specific block.

This tutorial assumes the following points:

- You are using a PC running Windows.
- You are familiar with the MATLAB, Simulink, Quartus II, and ModelSim® software and the software is installed on your PC in the default locations.
- You have basic knowledge of the Simulink software.

  For information about using the Simulink software, refer to the Simulink Help.

You can use the **singen.mdl** model file in <*DSP Builder install path*>**\DesignExamples\Tutorials\GettingStartedSinMdl** or you can create your own amplitude modulation model.

Creating a New Model

To create a new model:

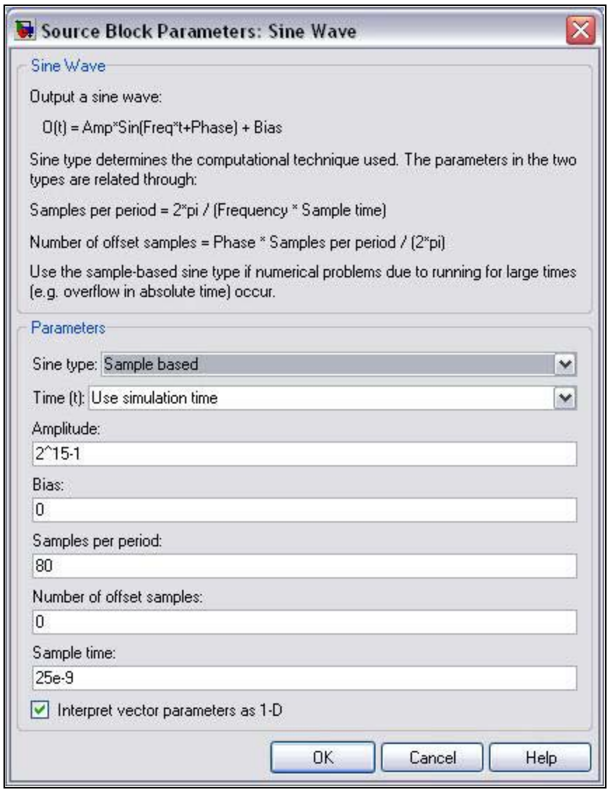
1. Start the MATLAB software.
2. On the File menu, point to **New,** and click **Model** to create a new model window.
3. In the new model window, on the File menu click **Save**.
4. Browse to a directory, your working directory, to save the file. This tutorial uses the working directory <*DSP Builder install path*>**\DesignExamples\Tutorials\GettingStartedSinMdl\my_SinMdl**.
5. Type the file name into the **File name** box. This tutorial uses the name **singen.mdl**.
6. Click **Save**.
7. Click the MATLAB **Start** button. Point to **Simulink** and click **Library Browser**.

Adding the Sine Wave Block

To add the `Sine Wave` block:

1. In the Simulink Library Browser, click **Simulink** and **Sources** to view the blocks in the Sources library.
2. Drag and drop a `Sine Wave` block into your model.
3. Double-click the `Sine Wave` block in your model to display the **Block Parameters** dialog box (Figure 2–3).

Figure 2–3. 500-kHz, 16-Bit Sine Wave Specified in the Sine Wave Dialog Box



Source Block Parameters: Sine Wave

Sine Wave

Output a sine wave:

O(t) = Amp*Sin(Freq*t+Phase) + Bias

Sine type determines the computational technique used. The parameters in the two types are related through:

Samples per period = 2*pi / (Frequency * Sample time)

Number of offset samples = Phase * Samples per period / (2*pi)

Use the sample-based sine type if numerical problems due to running for large times (e.g. overflow in absolute time) occur.

Parameters

Sine type: Sample based

Time (t): Use simulation time

Amplitude: 2^15-1

Bias: 0

Samples per period: 80

Number of offset samples: 0

Sample time: 25e-9

☑ Interpret vector parameters as 1-D

4. Set the `Sine Wave` block parameters (Table 2–1).

Table 2–1. Parameters for the Sine Wave Block

Parameter	Value
Sine type	Sample based
Time	simulation time
Amplitude	2^15–1
Bias	0
Samples per period	80
Number of offset examples	0
Sample time	25e-9
Interpret vector parameters a 1-D	On

5. Click **OK**.

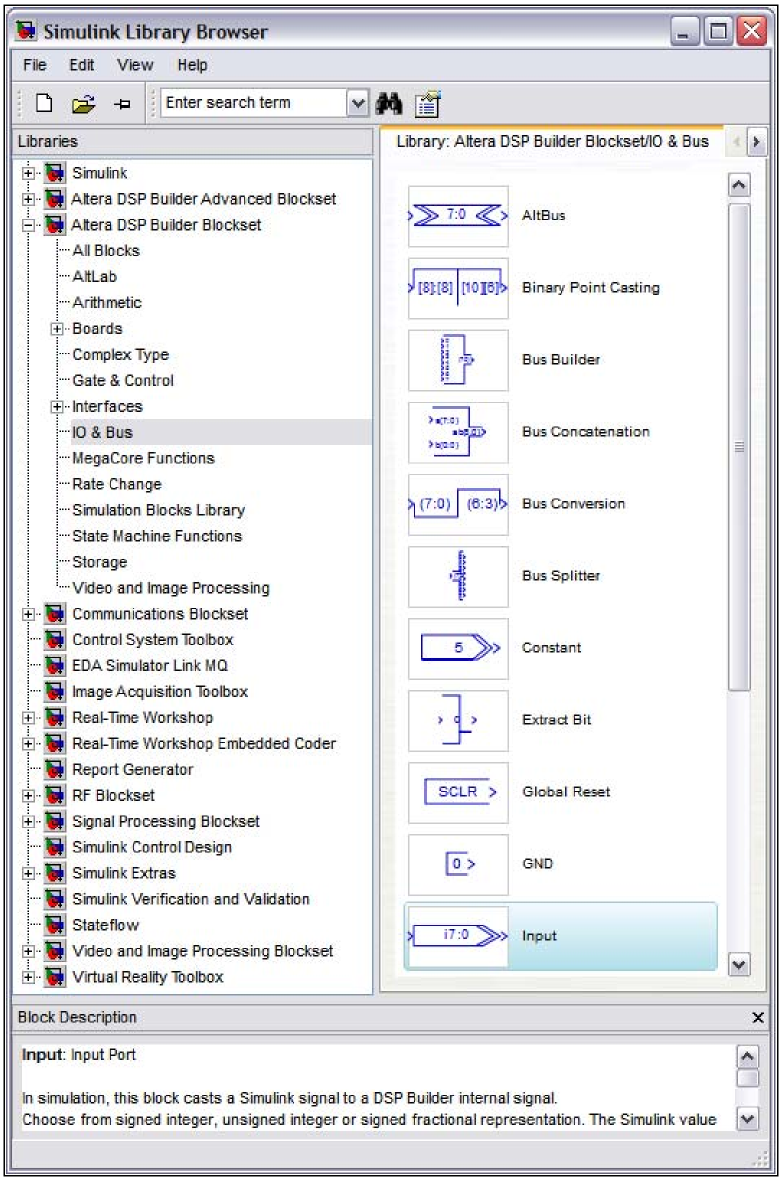
For information about how you can calculate the frequency., refer to the equation in "Frequency Design Rules" on page 3–8.

Adding the SinIn Block

To add the `SinIn` block:

1. In the Simulink Library Browser, expand the **Altera DSP Builder Blockset** folder to display the DSP Builder libraries (Figure 2–4).

Figure 2–4. Altera DSP Builder Folder in the Simulink Library Browser



Input: Input Port

In simulation, this block casts a Simulink signal to a DSP Builder internal signal.
Choose from signed integer, unsigned integer or signed fractional representation. The Simulink value

2. Select the **IO & Bus** library.

3. Drag and drop the `Input` block from the Simulink Library Browser into your model. Position the block to the right of the `Sine Wave` block.

   If you are unsure how to position the blocks or draw connection lines, refer to the completed design (Figure 2–7 on page 2–14).

   ☞ You can use the Up, Down, Right, and Left arrow keys to adjust the position of a block.

4. Click the text under the block icon in your model. Delete the text `Input` and type the text `SinIn` to change the name of the block instance.
5. Double-click the `SinIn` block in your model to display the **Block Parameters** dialog box.
6. Set the `SinIn` block parameters (Table 2–2).

Table 2–2. Parameters for the SinIn Block

Parameter	Value
Bus Type	Signed Integer
[number of bits].[]	16
Specify Clock	Off

7. Click **OK**.
8. Draw a connection line from the right side of the `Sine Wave` block to the left side of the `SinIn` block by holding down the left mouse button and dragging the cursor between the blocks.

   ☞ Alternatively, you can select a block, hold down the Ctrl key and click the destination block to automatically make a connection between the two blocks.

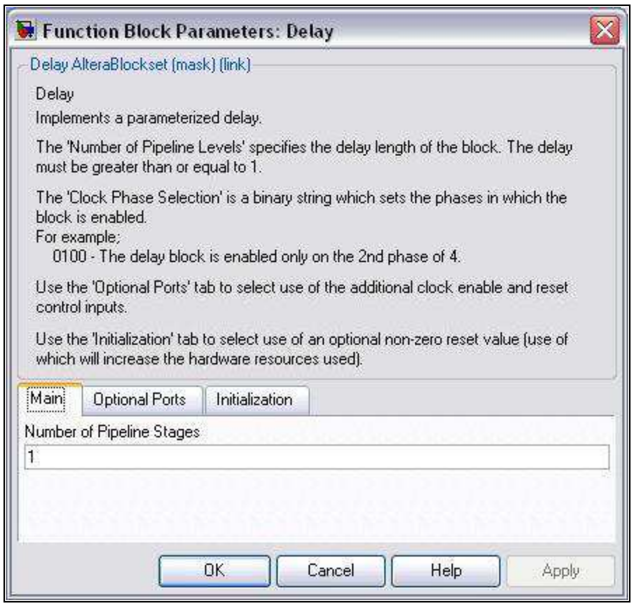
Adding the Delay Block

To add the `Delay` block:

1. Select the **Storage** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop the `Delay` block into your model and position it to the right of the `SinIn` block.
3. Double-click the `Delay` block in your model to display the **Block Parameters** dialog box (Figure 2–5).

4. Type `1` as the **Number of Pipeline Stages** for the `Delay` block.

Figure 2–5. Setting the Downsampling Delay



Function Block Parameters: Delay

Delay AlteraBlockset (mask) (link)

Delay

Implements a parameterized delay.

The 'Number of Pipeline Levels' specifies the delay length of the block. The delay must be greater than or equal to 1.

The 'Clock Phase Selection' is a binary string which sets the phases in which the block is enabled.
For example;
0100 - The delay block is enabled only on the 2nd phase of 4.

Use the 'Optional Ports' tab to select use of the additional clock enable and reset control inputs.

Use the 'Initialization' tab to select use of an optional non-zero reset value (use of which will increase the hardware resources used).

Number of Pipeline Stages: 1

5. Click the **Optional Ports** tab and set the parameters (Table 2–3).

Table 2–3. Parameters for the Delay Block.

Parameter	Value
Clock Phase Selection	01
Use Enable Port	Off
Use Synchronous Clear port	Off

6. Click **OK**.
7. Draw a connection line from the right side of the `SinIn` block to the left side of the `Delay` block.

Adding the SinDelay and SinIn2 Blocks

To add the `SinDelay` and `SinIn2` blocks:

1. Select the **IO & Bus** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop two `Output` blocks into your model, positioning them to the right of the `Delay` block.
3. Click the text under the block symbols in your model. Change the block instance names from `Output` and `Output1` to `SinDelay` and `SinIn2`.
4. Double-click the `SinDelay` block in your model to display the **Block Parameters** dialog box.

5. Set the `SinDelay` block parameters (Table 2–4).

Table 2–4. Parameters for the SinDelay Block

Parameter	Value
Bus Type	Signed Integer
[number of bits].[]	16
External Type	Inferred

6. Click **OK**.
7. Repeat steps 4 to 6 for the `SinIn2` block setting the parameters (Table 2–5).

Table 2–5. Parameters for the SinIn2 Block

Parameter	Value
Bus Type	Signed Integer
[number of bits].[]	16
External Type	Inferred

8. Draw a connection line from the right side of the `Delay` block to the left side of the `SinDelay` block.

Adding the Mux Block

To add the `Mux` block, follow these steps:

1. Select the Simulink **Signal Routing** library in the Simulink Library Browser.
2. Drag and drop a `Mux` block into your design, positioning it to the right of the `SinDelay` block.
3. Double-click the `Mux` block in your model to display the **Block Parameters** dialog box.
4. Set the `Mux` block parameters (Table 2–6).

Table 2–6. Parameters for the Mux Block

Parameter	Value
Number of Inputs	2
Display Options	bar

5. Click **OK**.
6. Draw a connection line from the bottom left of the `Mux` block to the right side of the `SinDelay` block.
7. Draw a connection line from the top left of the `Mux` block to the line between the `SinIn2` block.
8. Draw a connection line from the `SinIn2` block to the line between the `SinIn` and `Delay` blocks.

Adding the Random Bitstream Block

To add the `Random Bitstream` block, follow these steps:

1. Select the Simulink **Sources** library in the Simulink Library Browser.
2. Drag and drop a `Random Number` block into your model, positioning it underneath the `Sine Wave` block.
3. Double-click the `Random Number` block in your model to display the **Block Parameters** dialog box.
4. Set the `Random Number` block parameters (Table 2–7).

Table 2–7. Parameters for the Random number Block

Parameter	Value
Mean	0
Variance	1
Initial seed	0
Sample time	25e–9
Interpret vector parameters as 1-D	On

5. Click **OK**.
6. Rename the `Random Noise` block `Random Bitstream`.

Adding the Noise Block

To add the `Noise` block, follow these steps:

1. Select the **IO & Bus** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop an `Input` block into your model, positioning it to the right of the `Random Bitstream` block.
3. Click the text under the block icon in your model. Rename the block `Noise`.
4. Double-click the `Noise` block to display the **Block Parameters** dialog box.
5. Set the `Noise` block parameters (Table 2–8).

Table 2–8. Parameters for the Noise Block

Parameter	Value
Bus Type	Single Bit
Specify Clock	Off

☞ The dialog box options change to display only the relevant options when you select a new bus type.

6. Click **OK**.
7. Draw a connection line from the right side of the `Random Bitstream` block to the left side of the `Noise` block.

Adding the Bus Builder Block

The `Bus Builder` block converts a bit to a signed bus. To add the `Bus Builder` block, follow these steps:

1. Select the **IO & Bus** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop a `Bus Builder` block into your model, positioning it to the right of the `Noise` block.
3. Double-click the `Bus Builder` block in your model to display the **Block Parameters** dialog box.
4. Set the `Bus Builder` block parameters (Table 2–9).

Table 2–9. Parameters for the Bus Builder Block

Parameter	Value
Bus Type	Signer Integer
[number of bits].[]	2

5. Click **OK**.
6. Draw a connection line from the right side of the `Noise` block to the top left side of the `Bus Builder` block.

Adding the GND Block

To add the `GND` block, follow these steps:

1. Select the **IO & Bus** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop a `GND` block into your model, positioning it underneath the `Noise` block.
3. Draw a connection line from the right side of the `GND` block to the bottom left side of the `Bus Builder` block.

Adding the Product Block

To add the `Product` block, follow these steps:

1. Select the **Arithmetic** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop a `Product` block into your model, positioning it to the right of the `Bus Builder` block and slightly above it. Leave enough space so that you can draw a connection line under the `Product` block.
3. Double-click the `Product` block to display the **Block Parameters** dialog box.