Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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International IOR Rectifier

High and Low Side Driver

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
- Separate logic supply range from 3.3V to 20V
- Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

|	
V_{OFFSET}	600V max.
$I_{O+/-}$	2A / 2A
V_{OUT}	10 – 20V
Ton/off (typ.)	120 & 94 ns
Delay Matching (typ.)	20 ns

Description

The IR25607 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

Package Options

16 Lead SOIC Wide Body

Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR25607SPBF	SO16W	Tube	45	IR25607SPBF
IR25607SPBF	SO16W	Tape and Reel	1000	IR25607STRPBF

Typical Connection Diagram
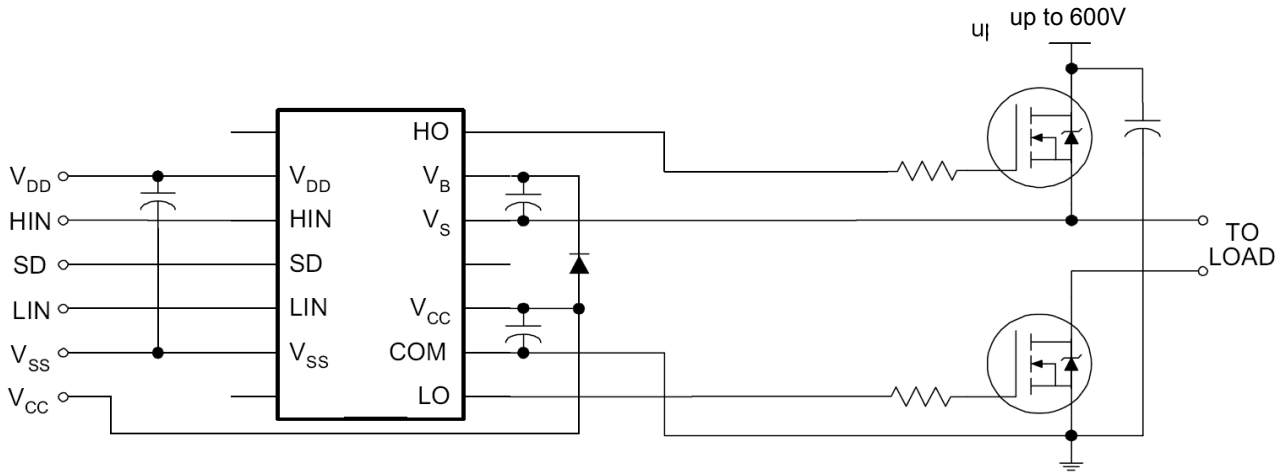
(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	-0.3	625	V
V_S	High side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage	-0.3	V_{SS} + 25	
V_{SS}	Logic supply offset voltage	V_{CC} – 25	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS} -0.3	V_{DD} + 0.3	
dVs/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ T_A ≤ +25°C	—	1.25	W
Rth_{JA}	Thermal resistance, junction to ambient	—	100	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	†	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{DD}	Logic supply voltage	V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic supply offset voltage	-5 ††	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient temperature	-40	125	°C

† Logic operational for VS of -5 to +600V. Logic state held for VS of -5V to -VBS. (Please refer to Design Tip DT97-3 for more details).

†† When V_{DD} < 5V, the minimum V_{SS} offset is limited to -V_{DD}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, CL = 1000 pF, V_{SS} = COM and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
ton	Turn-on propagation delay	—	120	150		V_S = 0V
toff	Turn-off propagation delay	—	94	125		V_S = 600V
tsd	Shutdown propagation delay	—	110	140	ns	V_S = 600V
tr	Turn-on rise time	—	25	35		
tf	Turn-off fall time	—	17	25		
MT	Delay matching, HS & LS turn-on/off	—	—	20		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	9.5	—	—		
V_{IL}	Logic "0" input voltage	—	—	6.0	V	
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50		V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{CC} supply current	—	15	30	μA	V_{IN} = 0V or V_{DD}
I_{IN+}	Logic "1" input bias current	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" input bias current	—	—	1		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.5	8.6	9.7		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.0	8.2	9.4	V	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	2	2.5	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 μs
I_{O-}	Output low short circuit pulsed current	2	2.5	—		V_O = 15V, V_{IN} = V_{DD} PW ≤ 10 μs

Functional Block Diagram
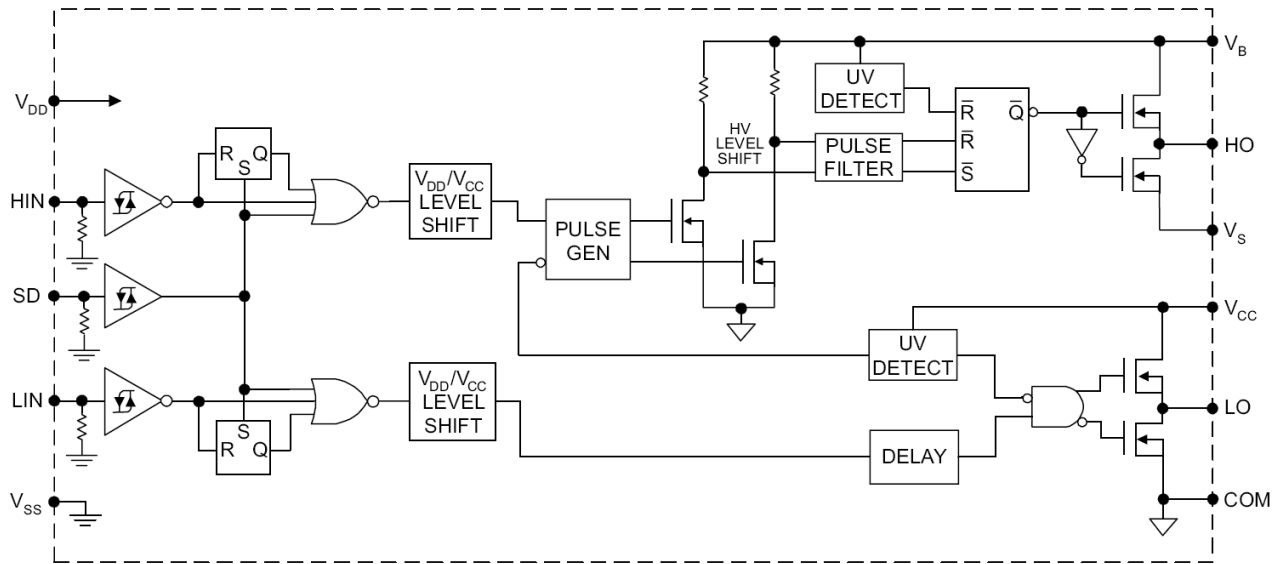
Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments
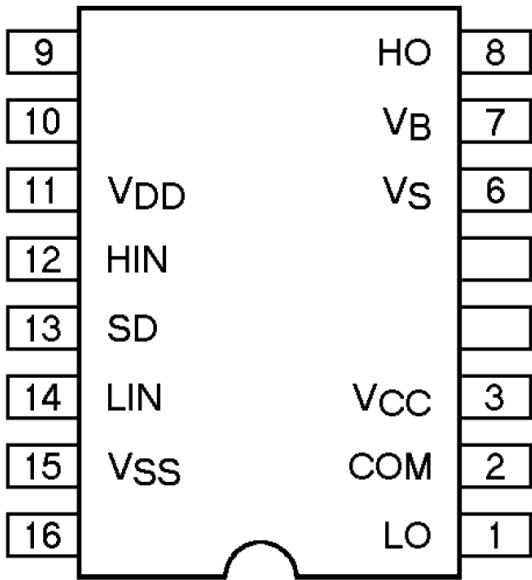
Application Information and Additional Details
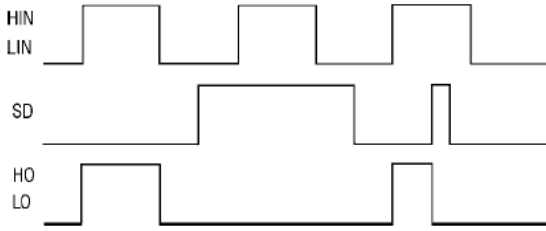
Figure 1. Input/Output Timing Diagram
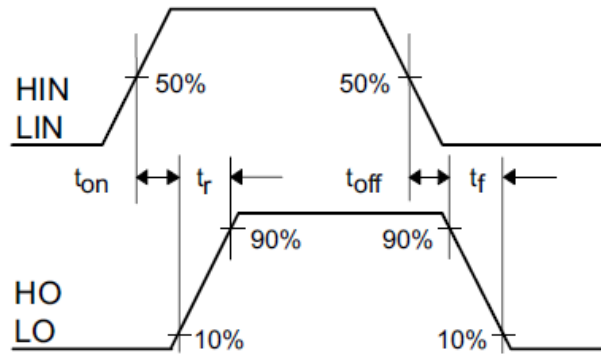
Figure 2. Switching Time Waveform Definitions
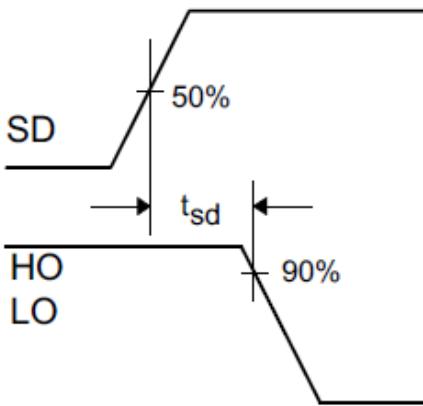
Figure 3. Shutdown Waveform Definitions
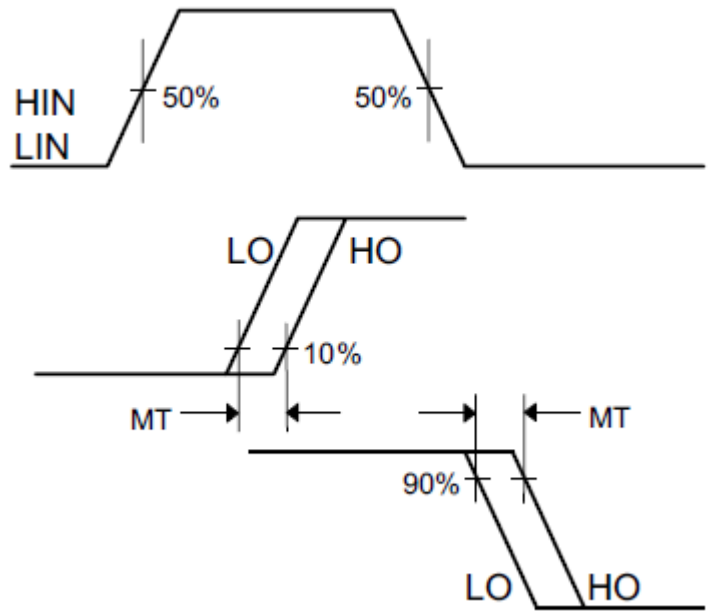
Figure 4. Delay matching Waveform Definitions
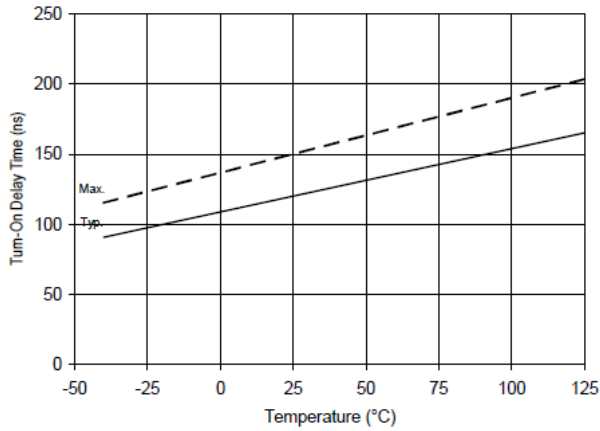
Figure 5A. Turn On Time vs. Temperature
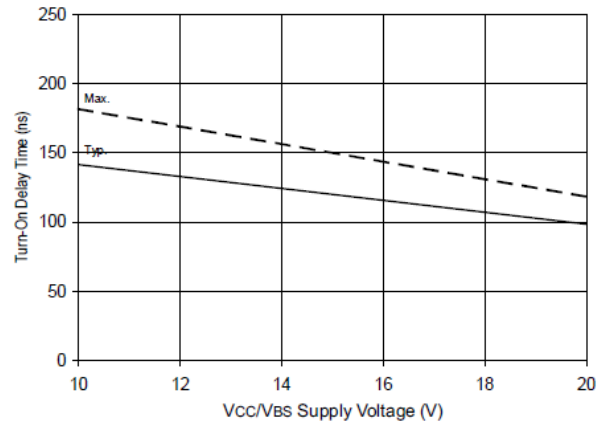
Figure 5B. Turn On Time vs. V_{CC}/V_{BS} Supply Voltage
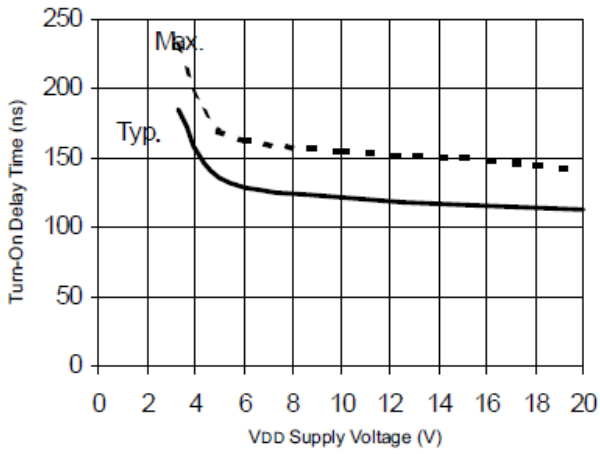
Figure 5C. Turn On Time vs. V_{DD} Supply Voltage
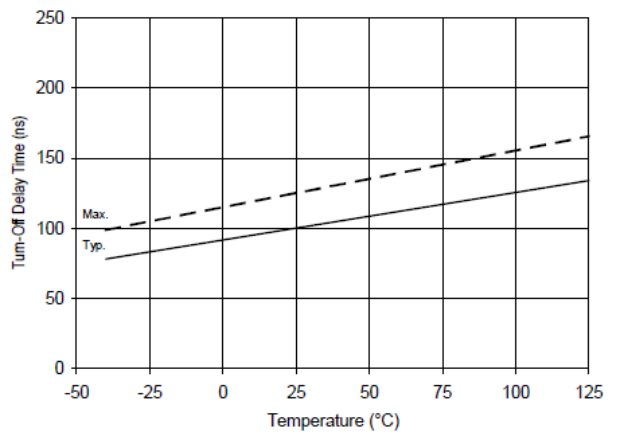
Figure 6A. Turn Off Time vs. Temperature
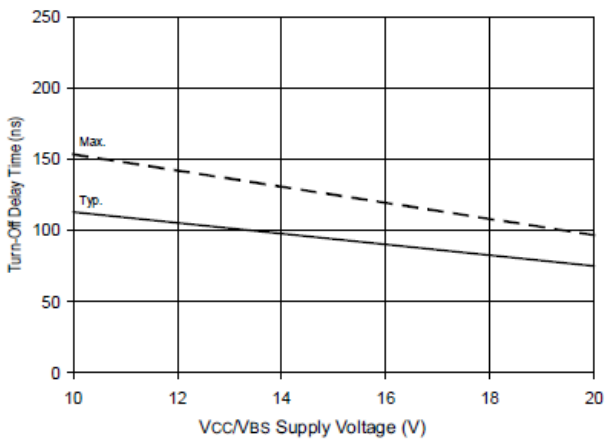
Figure 6B. Turn Off Time vs. V_{CC}/V_{BS} Supply Voltage
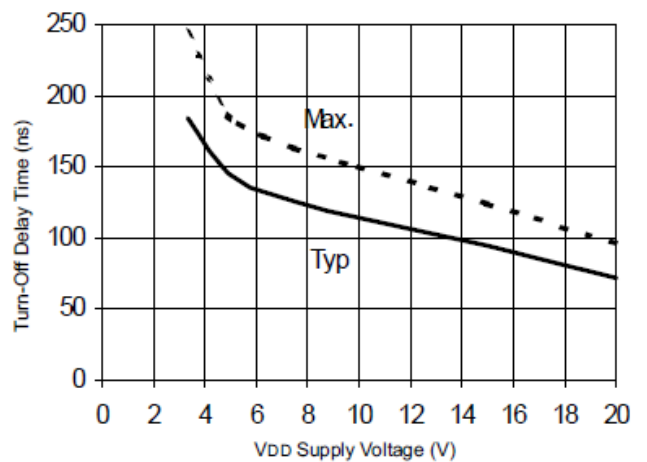
Figure 6C. Turn Off Time vs. V_{DD} Supply Voltage
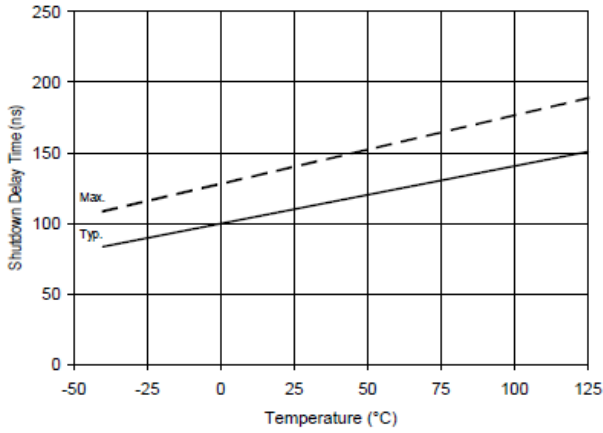
Figure 7A. Shutdown Time vs. Temperature
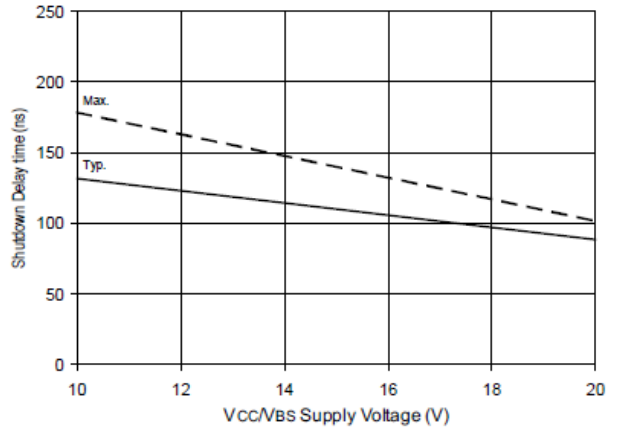
Figure 7B. Shutdown Time vs. V_{CC}/V_{BS} Supply Voltage
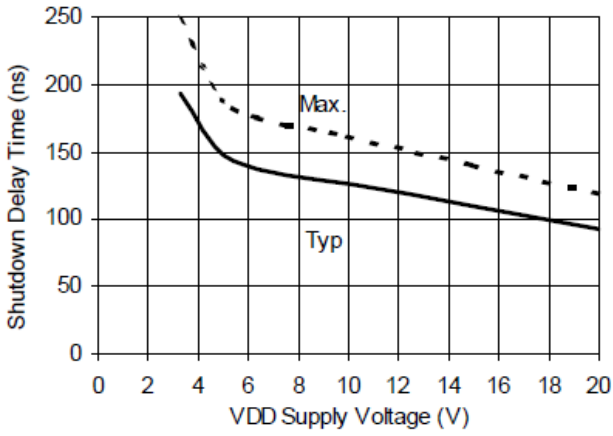
Figure 7C. Shutdown Time vs. V_{DD} Supply Voltage
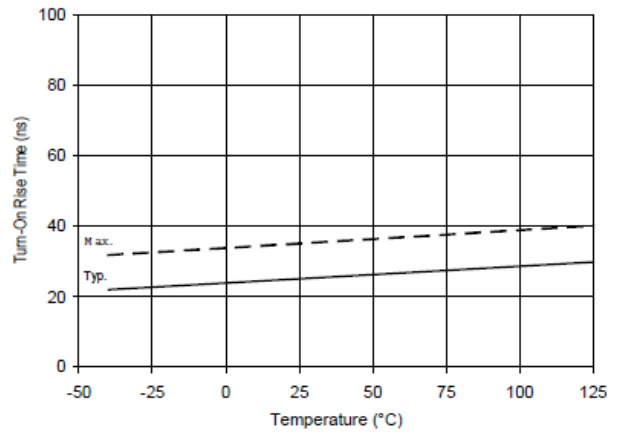
Figure 8A. Turn On Rise Time vs. Temperature
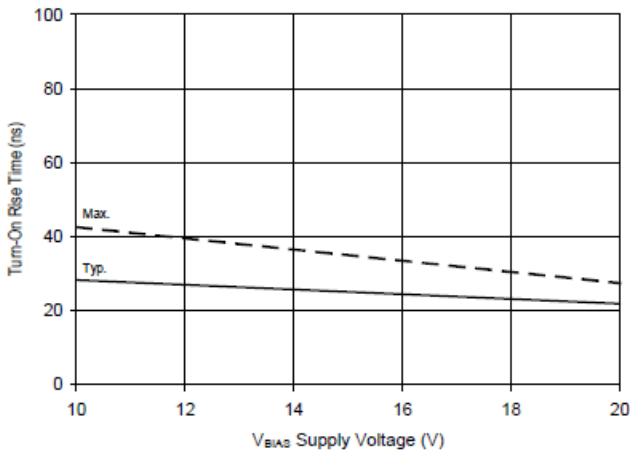
Figure 8B. Turn On Rise Time vs. Voltage
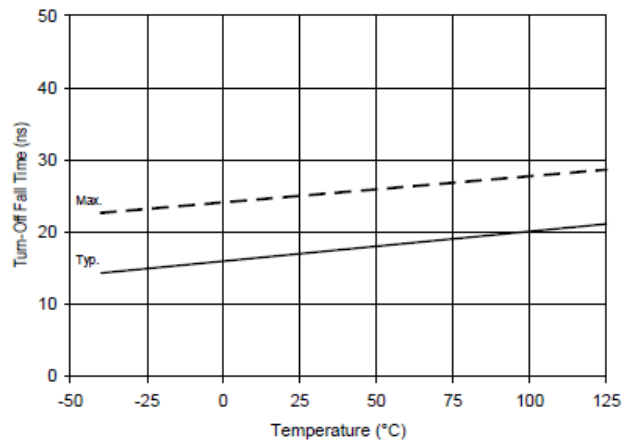
Figure 9A. Turn Off Fall Time vs. Temperature
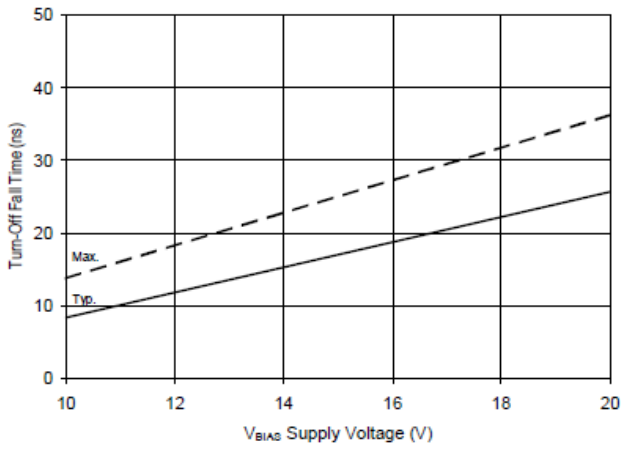
Figure 9B. Turn Off Fall Time vs. Voltage
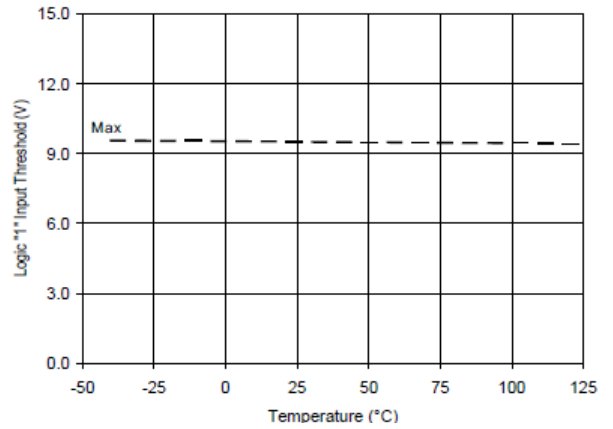
Figure 10A. logic '1' Input Threshold vs. Temperature
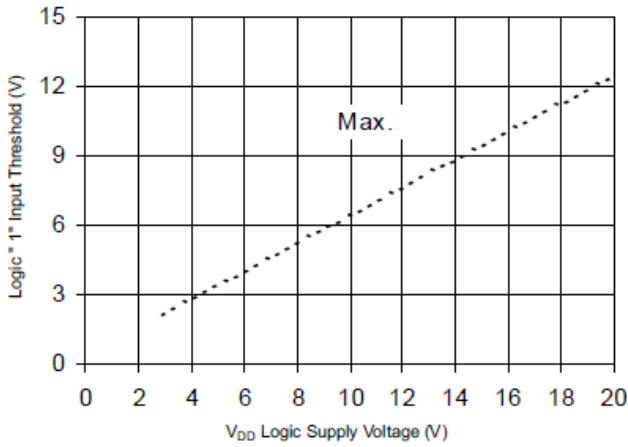
Figure 10B. Logic '1' Input Threshold vs. Voltage
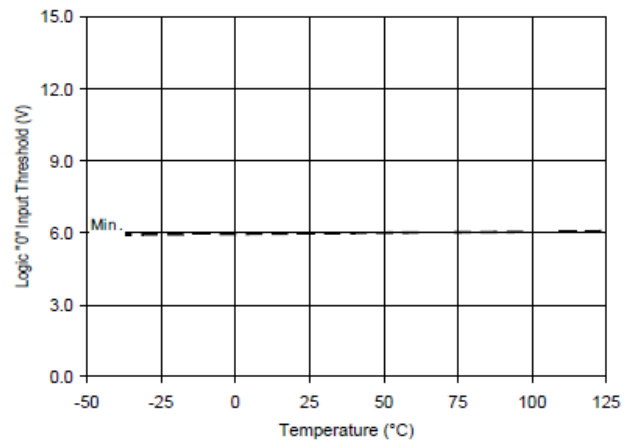
Figure 11A. Logic '0' Input Threshold vs. Temperature
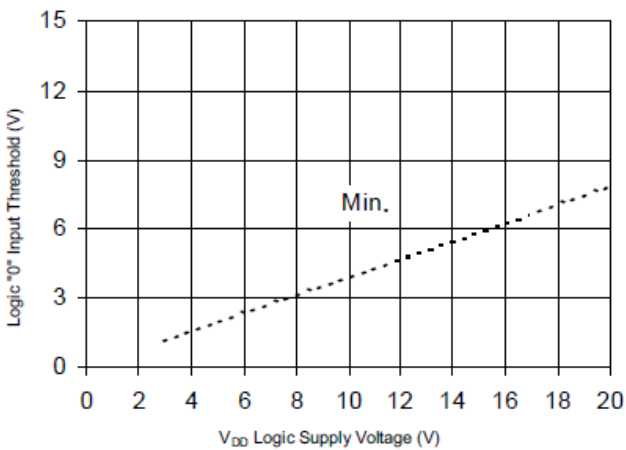
Figure 11B. Logic '0' Input Threshold vs. Voltage
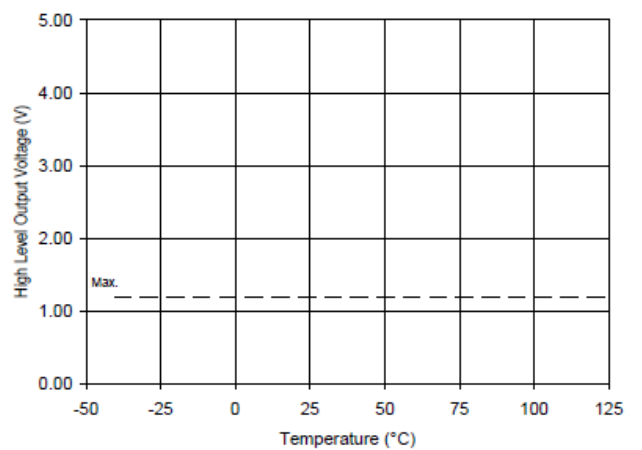
Figure 12A. High Level Output vs. Temperature
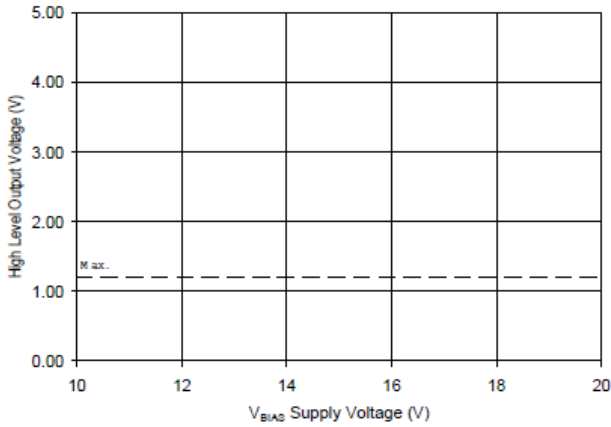
Figure 12B. High Level Output vs. Voltage
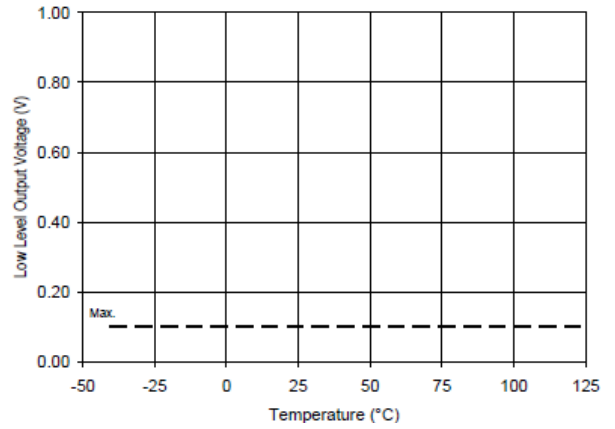
Figure 13A. Low Level Output vs. Temperature
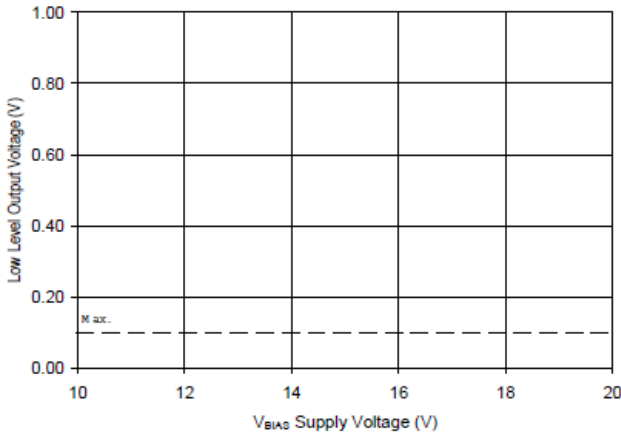
Figure 13B. Low Level Output vs. Voltage
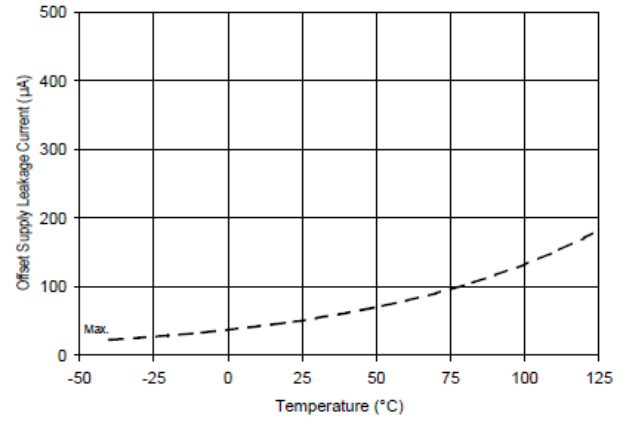
Figure 14A. Offset Supply Current vs. Temperature
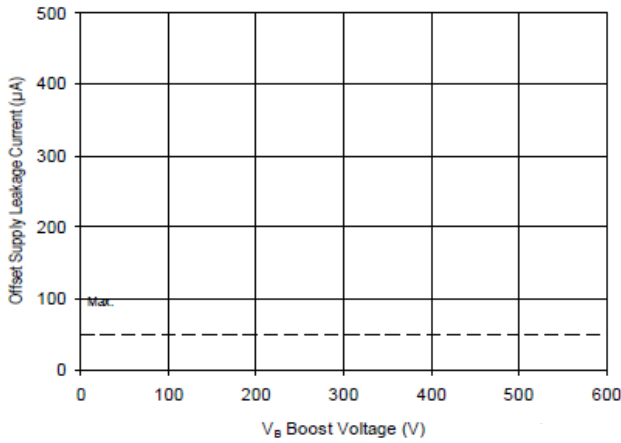
Figure 14B. Offset Supply Current vs. Voltage
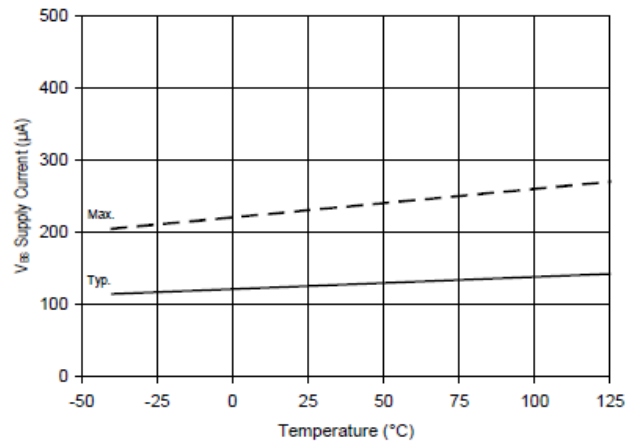
Figure 15A. V$_{BS}$ Supply Current vs. Temperature
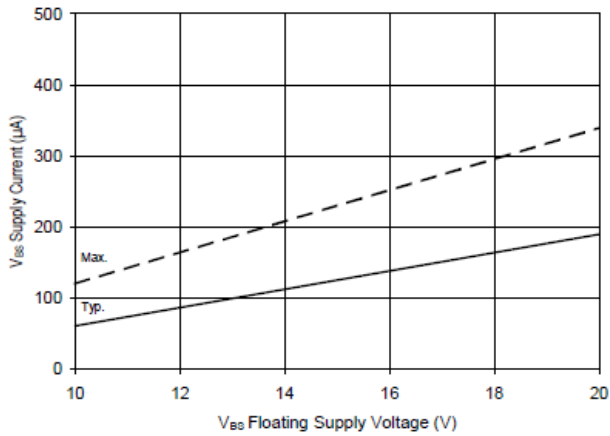
Figure 15B. V_BS Supply Current vs. Voltage
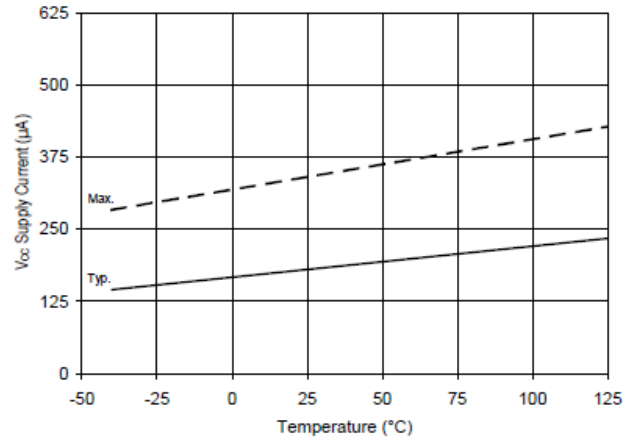
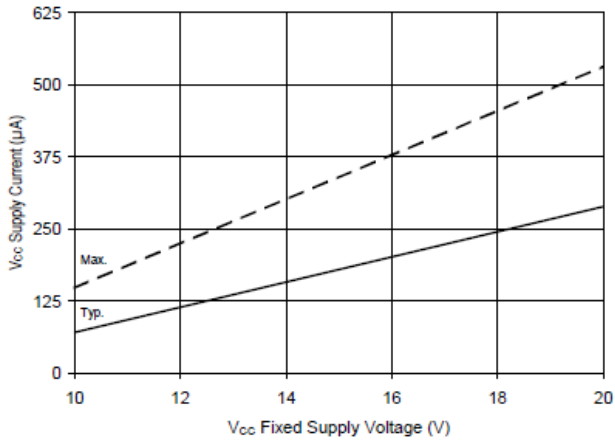**Figure 16A. V_CC Supply Current vs. Temperature**
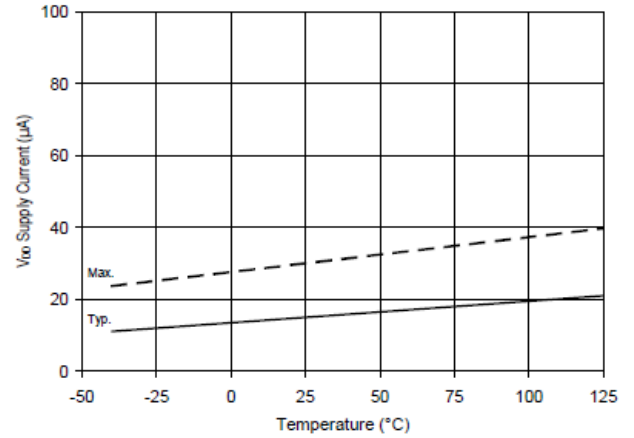

Figure 16B. V_CC Supply Current vs. Voltage

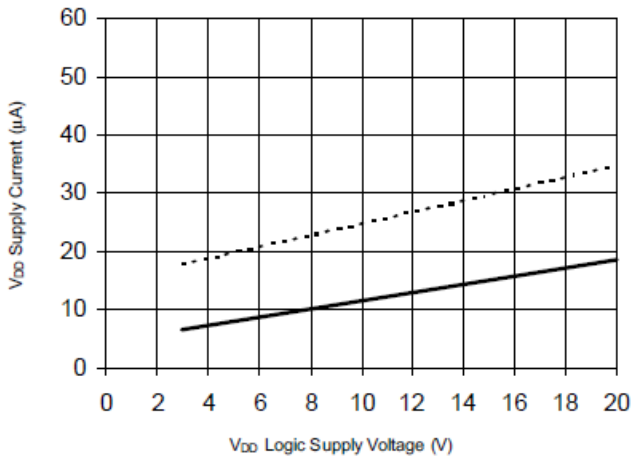**Figure 17A. V_DD Supply Current vs. Temperature**

Figure 17B. V_DD Supply Current vs. V_DD Voltage
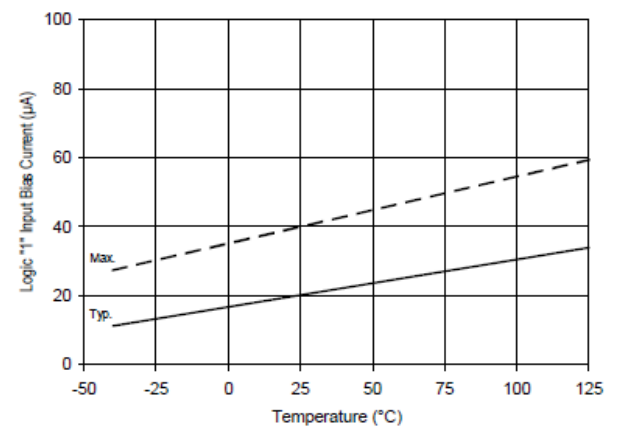

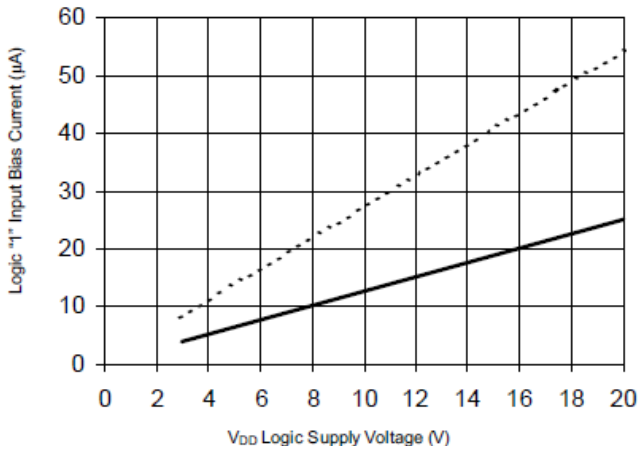**Figure 18A. Logic '1' Input Current vs. Temperature**

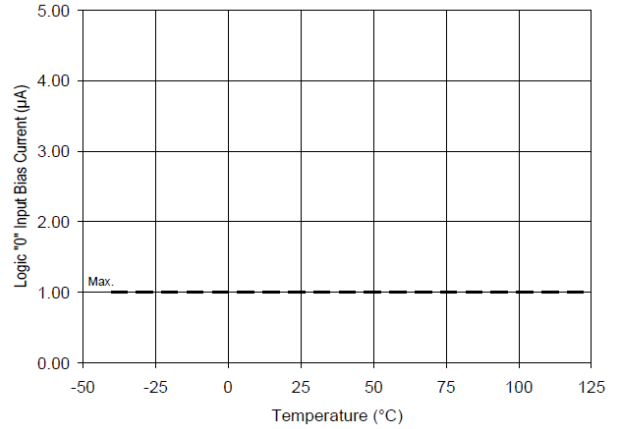**Figure 18B. Logic '1' Input Current vs. V_DD Voltage**

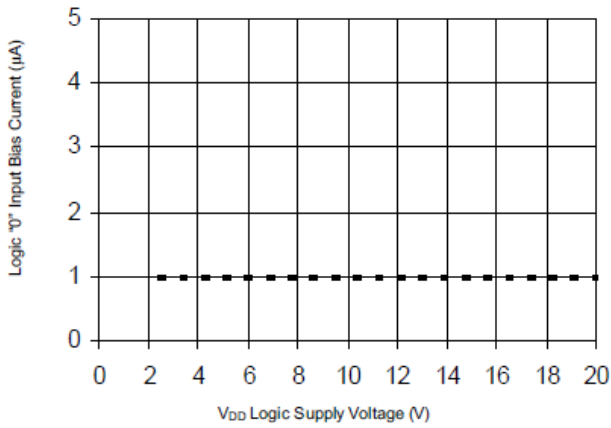**Figure 19A. Logic '0' Input Current vs. Temperature**

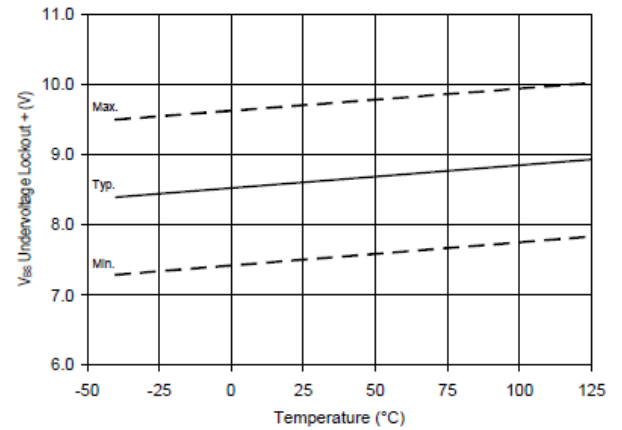**Figure 19B. Logic '0' Input Current vs. V_DD Voltage**

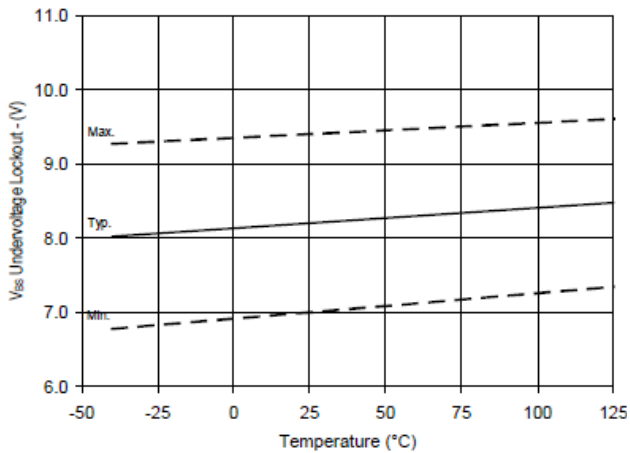**Figure 20. V_BS Undervoltage (+) vs. Temperature**

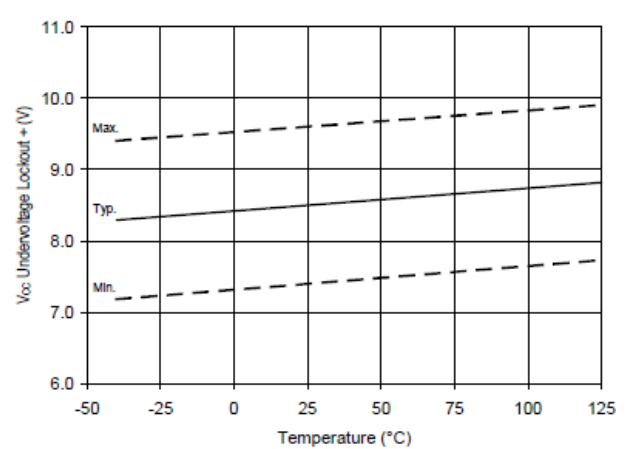**Figure 21 V_BS Undervoltage (-) vs. Temperature**

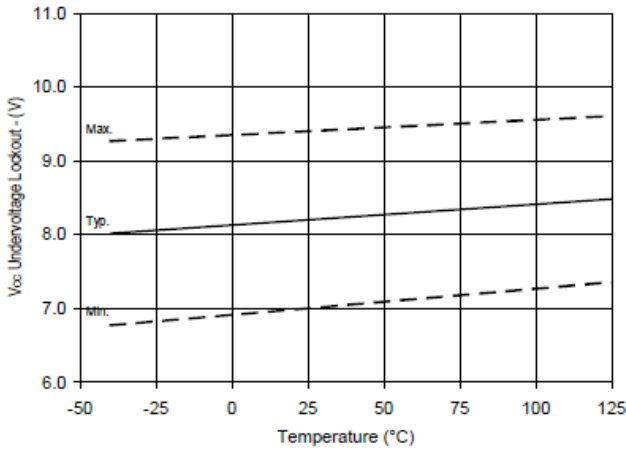**Figure 22. V_CC Undervoltage (+) vs. Temperature**
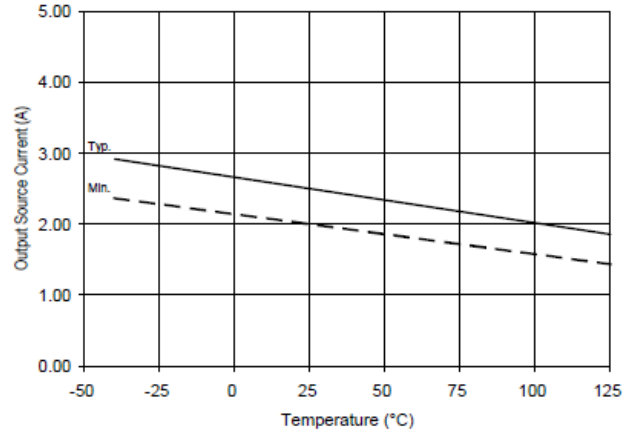
Figure 23. V_CC Undervoltage (-) vs. Temperature

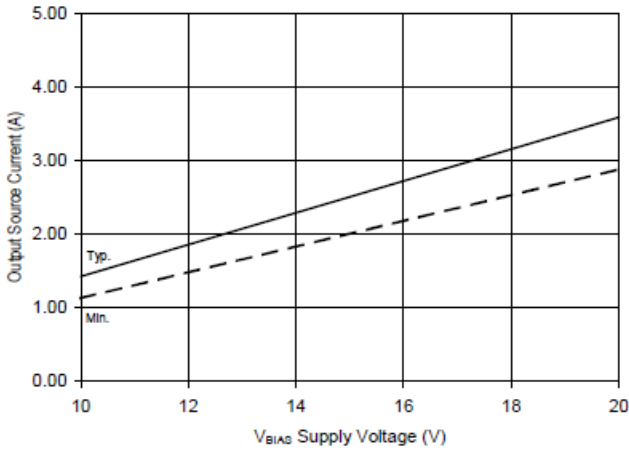**Figure 24A. Output Source Current vs. Temperature**

Figure 24B. Output Source Current vs. Voltage
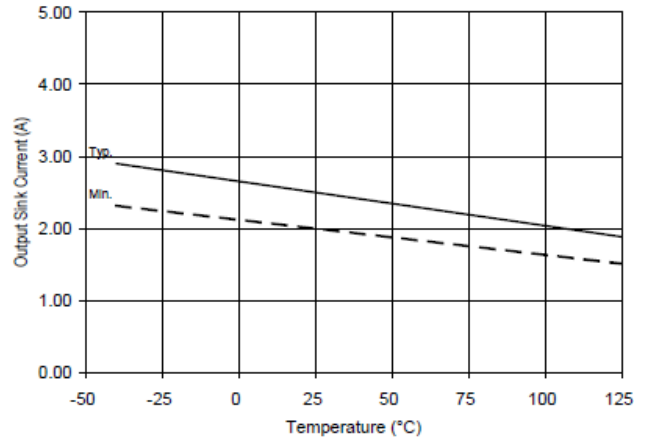

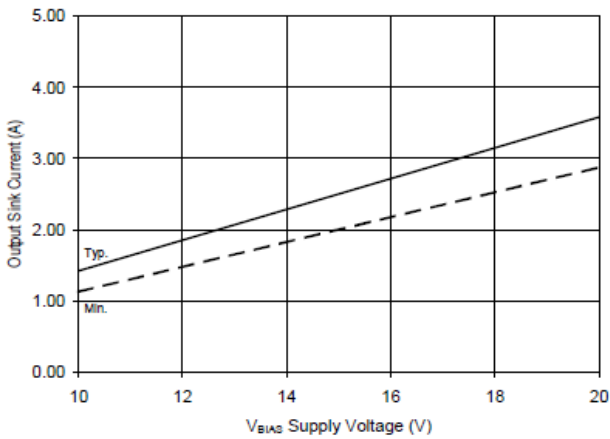**Figure 25A. Output Sink Current vs. Temperature**

Figure 25B. Output Sink Current vs. Voltage
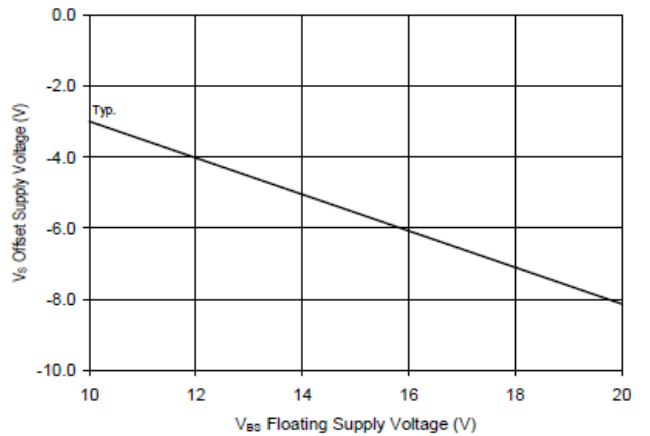
Figure 26. Maximum V_S Negative Offset vs. V_BS Supply Voltage
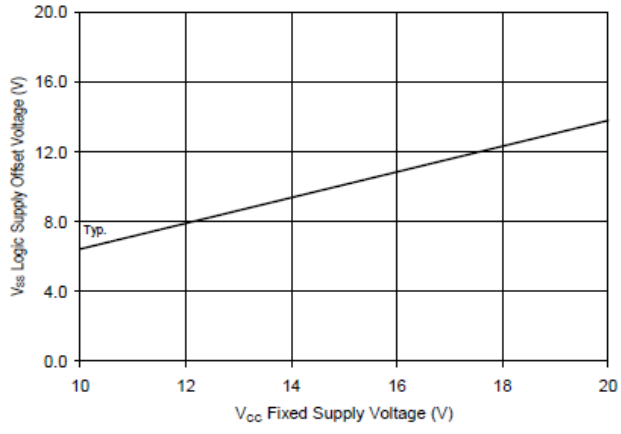
Figure 27. Maximum V$_{SS}$ Positive Offset vs. V$_{CC}$ Supply Voltage

Package Details

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

16 Lead SOIC (wide body)

Tape and Reel Details

LOADED TAPE FEED DIRECTION

NOTE : CONTROLLING
DIMENSION IN MM

CARRIER TAPE DIMENSION FOR 16SOICN

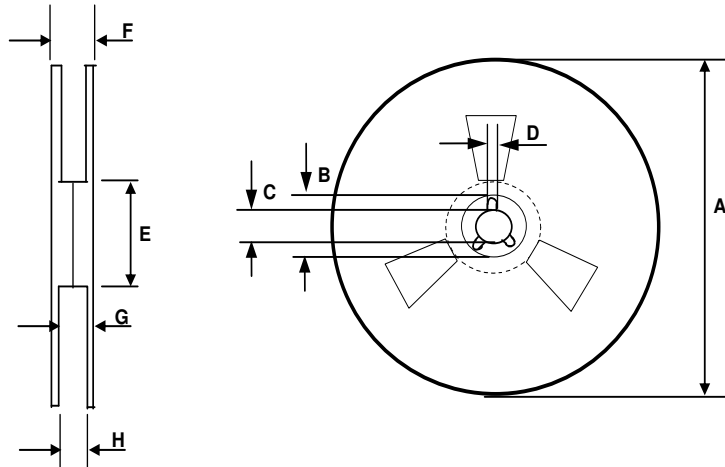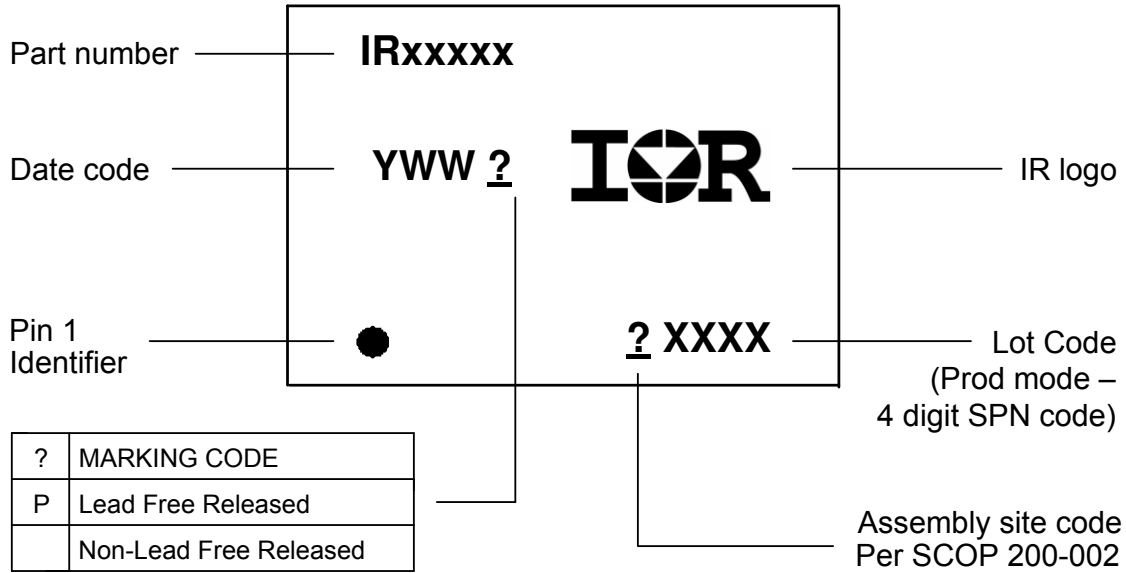| Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information

Part number ——	**IRxxxxx**
Date code ——	**YWW ?**
	IΩR — IR logo
Pin 1 Identifier ——	●
	? XXXX — Lot Code (Prod mode – 4 digit SPN code)

?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Assembly site code
Per SCOP 200-002

Qualification Information†

Qualification Level	Industrial†† (per JEDEC JESD 47)
	Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level	MSL3††† (per IPC/JEDEC J-STD-020)
RoHS Compliant	Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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