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IR3084

DATA SHEET
XPHASE™ VR 10/11 CONTROL IC

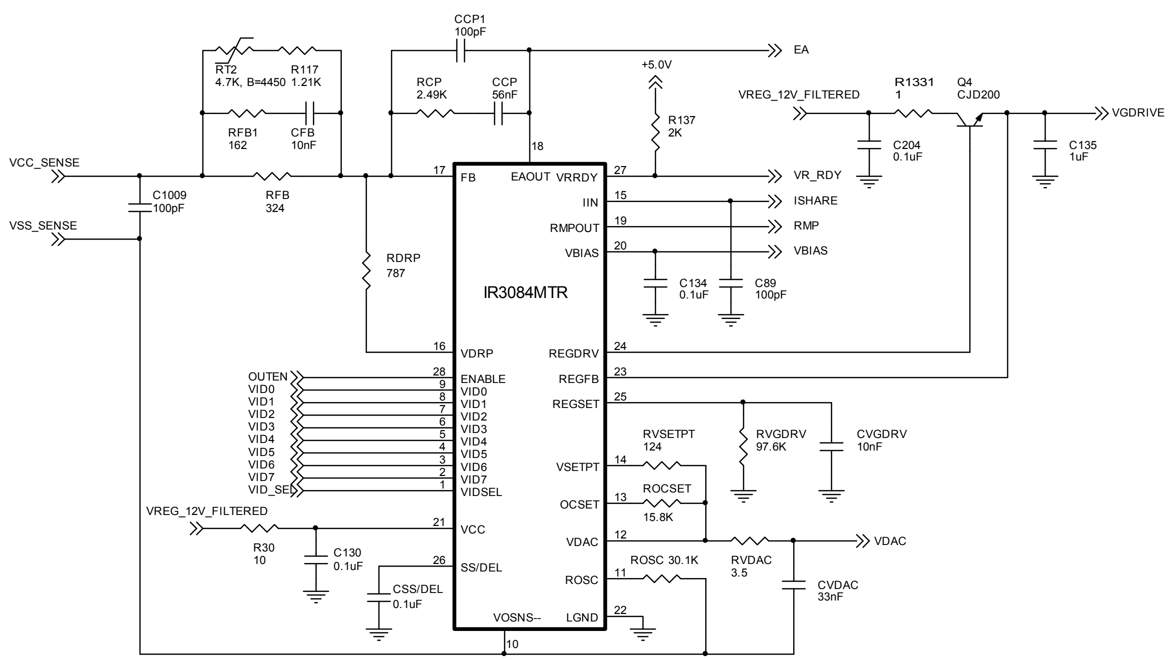
DESCRIPTION

The IR3084 Control IC combined with an IR *XPhase*™ Phase IC provides a full featured and flexible way to implement a complete VR10 or VR11 power solution. The "Control" IC provides overall system control and interfaces with any number of "Phase" ICs which each drive and monitor a single phase of a multiphase converter. The X*Phase*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

FEATURES

- 1 to X phase operation with matching Phase IC
- Supports both VR11 8-bit VID code and extended VR10 7-bit VID code
- 0.5% Overall System Setpoint Accuracy
- VID Select pin sets the DAC to either VR10 or VR11
- VID Select pin selects either VR11 or legacy VR10 type startups
- Programmable VID offset and Load Line output impedance
- Programmable VID offset function at the Error Amp's non-inverting input allowing zero offset
- Programmable Dynamic VID Slew Rate
- ±300mV Differential Remote Sense
- Programmable 150kHz to 1MHz oscillator
- Enable Input with 0.85V threshold and 100mV of hysteresis
- VR Ready output provides indication of proper operation and avoids false triggering
- Phase IC Gate Driver Bias Regulator / VRHOT Comparator
- Operates from 12V input with 9.9V Under-Voltage Lockout
- 6.9V/6mA Bias Regulator provides System Reference Voltage
- Programmable Hiccup Over-Current Protection with Delay to prevent false triggering
- Small thermally enhanced 5mm x 5mm, 28 pin MLPQ package

TYPICAL APPLICATION CIRCUIT



ORDERING INFORAMATION

DEVICE	ORDER QUANTITY
IR3084MTRPBF	3000 Tape and Reel
IR3084MPBF	100 Piece Strip

ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature……………..0 to 150°C
Storage Temperature Range………………….−65°C to 150°C
ESD Rating………………………………………HBM Class 1B JEDEC standard
Moisture Sensitivity Level………………………JEDEC Level 3 @ 260 °C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	VIDSEL	20V	−0.3V	1mA	1mA
2−9	VID7−0	20V	−0.3V	1mA	1mA
10	VOSNS−	0.5V	−0.5V	10mA	10mA
11	ROSC	20V	−0.5V	1mA	1mA
12	VDAC	20V	−0.3V	1mA	1mA
13	OCSET	20V	−0.3V	1mA	1mA
14	VSETPT	20V	−0.3V	1mA	1mA
15	IIN	20V	−0.3V	1mA	1mA
16	VDRP	20V	−0.3V	5mA	5mA
17	FB	20V	−0.3V	1mA	1mA
18	EAOUT	10V	−0.3V	20mA	20mA
19	RMPOUT	20V	−0.3V	5mA	5mA
20	VBIAS	20V	−0.3V	50mA	10mA
21	VCC	20V	−0.3V	1mA	50mA
22	LGND	n/a	n/a	50mA	1mA
23	REGFB	20V	−0.3V	1mA	1mA
24	REGDRV	20V	−0.3V	10mA	50mA
25	REGSET	20V	−0.3V	1mA	1mA
26	SS/DEL	20V	−0.3V	1mA	1mA
27	VRRDY	20V	−0.3V	1mA	20mA
28	ENABLE	20V	−0.3V	1mA	1mA

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 9.5V ≤ V_{CC} ≤ 16V, −0.3V ≤ VOSNS− ≤ 0.3V, 0 °C ≤ T_J ≤ 100 °C, ROSC = 24kΩ, CSS/DEL = 0.1μF ±10%

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDAC REFERENCE					
System Set-Point Accuracy (Deviation from Tables 1 & 2 per test circuit in Figure 1 which emulates in-VR operation)	VID ≥ 1V, 10kΩ≤ROSC≤100kΩ, 25 °C ≤ T_J ≤ 100 °C	−0.5		0.5	%
	0.8V ≤ VID < 1V, 10kΩ≤ROSC≤100kΩ, 25 °C ≤ T_J ≤ 100 °C	−5		+5	mV
	0.5V≤VID<0.8V, 10kΩ≤ROSC≤100kΩ, 25 °C ≤ T_J ≤ 100 °C	−8		+8	mV
Source Current	Includes OCSET and VSETPT currents	104	113	122	μA
Sink Current	Includes OCSET and VSETPT currents	92	100	108	μA
VIDx Input Threshold		500	600	700	mV
VIDx & VIDSEL Input Bias Current	0V ≤ VIDx ≤ VCC	−5	0	5	μA
VIDx 11111x Blanking Delay	Measure Time till VRRDY drives low, Note 1	0.5	1.3	2.1	μs
VIDSEL Pull-up Voltage	VIDSEL FLOATING	1.15	1.25	1.35	V
VIDSEL Pull-up Resistance		5.0	12.5	20.0	KΩ
VIDSEL VR10/VR11 Threshold		0.55	0.62	0.69	V
VIDSEL VR11 No Boot Threshold		3.0	3.5	4.0	V
VIDSEL VR10 No Boot Threshold		7.0	7.5	8.0	V
ERROR AMPLIFIER					
Input Offset Voltage	Measure V(FB) – V(VSETPT) per test circuit in Figure 1. Applies to TBS VID codes. Note 2.	−5	0.0	5	mV
FB Bias Current		−1	−0.3	0.5	μA
VSETPT Bias Current		48.5	51	53.5	μA
DC Gain	Note 1	90	100	110	dB
Gain Bandwidth Product	Note 1	6	10		MHz
Corner Frequency	45 deg Phase Shift, Note 1		200	400	Hz
Slew Rate	Note 1	1.4	3.2	5	V/μs
Source Current		−1.2	−0.8	−0.35	mA
Sink Current		0.5	1.0	1.7	mA
Max Voltage	VBIAS–VEAOUT (ref. to VBIAS)	150	375	600	mV
Min Voltage	Normal operation or Fault mode	30	110	200	mV
VDRP BUFFER AMPLIFIER					
Input Offset Voltage	V(VDRP) – V(IIN), 0.5V ≤ V(IIN) ≤ 5V	−10	−1	6	mV
Source Current	0.5V ≤ V(IIN) ≤ 5V	−9	−7.3	−4	mA
Sink Current	0.5V ≤ V(IIN) ≤ 5V	0.2	0.88	4.1	mA
Bandwidth (−3dB)	Note 1	1	6		MHz
Slew Rate	Note 1	5	10		V/μs

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
CURRENT SENSE INPUT					
IIN Bias Current	V(SS/DEL) > 0.85V, V(EAOUT) > 0.5V	−2.0	−0.2	1.0	μA
IIN Preconditioning Pull-Down Resistance	V(SS/DEL) < 0.35V	5.6	12.5	19.4	KΩ
IIN Preconditioning RESET Threshold	V(EAOUT)	0.20	0.35	0.50	V
IIN Preconditioning SET Threshold	V(SS/DEL)	0.35	0.60	0.85	V
VBIAS REGULATOR					
Output Voltage	−5mA ≤ I(VBIAS) ≤ 0mA	6.6	6.9	7.2	V
Current Limit		−35	−20	−6	mA
Over-Current Comparator					
Input Offset Voltage	1V ≤ V(OCSET) ≤ 5V	−10	−1	10	mV
OCSET Bias Current		−53.5	−51	−48.5	μA
SOFT START AND DELAY					
Start Delay (TD1)	RDRP = ∞	1.2	1.8	2.6	ms
Soft Start Time (TD2)	RDRP = ∞	0.8	1.6	2.8	ms
VID Sample Delay (TD3)		0.2	1.0	2.5	ms
VRRDY Delay (TD4 + TD5)		0.5	1.3	2.2	ms
OC Delay Time	Note 1	150	250	350	μs
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.85	1.3	1.5	V
SS/DEL Charge Current		40	70	100	μA
SS/DEL Discharge Current		4	6.5	9	μA
Charge/Discharge Current Ratio		9.5	11.2	12.5	μA/μA
OC Discharge Current	Note 1	20	40	60	μA
Charge Voltage		3.6	3.85	4.1	V
OC/VRRDY Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL rising		80		mV
OC/VRRDY Delay Comparator Threshold	Relative to Charge Voltage, SS/DEL falling		100		mV
Delay Comparator Hysteresis			20		mV
VID Sample Delay Comparator Threshold			3.10		V
SS/DEL Discharge Comparator Threshold			215		mV
ENABLE INPUT					
Threshold Voltage	ENABLE rising	775	850	925	mV
Threshold Voltage	ENABLE falling	675	750	825	mV
Threshold Hysteresis		60	100	140	mV
Input Resistance		50	100	200	KΩ
Blanking Time	Noise Pulse < 250ns will not register an ENABLE state change. Note 1	75	250	400	ns

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VRRDY OUTPUT					
Output Voltage	I(VRRDY) = 4mA		150	300	mV
Leakage Current	V(VRRDY) = 5.5V		0	10	μA
OSCILLATOR					
Switching Frequency		450	500	550	kHz
Peak Voltage (4.8V typical, measured as % of VBIAS)		70	72	74	%
Valley Voltage (0.9V typical, measured as % of VBIAS)		10	13	15	%
DRIVER BIAS REGULATOR					
REGSET Bias Current	1.5V ≤ V(REGSET) ≤ VCC – 1.5V	−112	−99	−85	μA
Input Offset Voltage	1.5V ≤ V(REGSET) ≤ VCC – 1.5V, 100μA ≤ I(REGDRV) ≤ 10mA	−12	0	12	mV
Short Circuit Current	V(REGDRV) = 0V, 1.5V ≤ V(REGSET) ≤ VCC – 1.5V, Note 1	10	20	50	mA
Dropout Voltage	I(REGDRV) = 10mA, Note 1	0.4	0.87	1.33	V
VCC UNDER−VOLTAGE LOCKOUT					
Start Threshold		9.3	9.9	10.3	V
Stop Threshold		8.5	9.1	9.5	V
Hysteresis	Start – Stop	575	800	1000	mV
GENERAL					
VCC Supply Current		9	14	18	mA
VOSNS− Current	−0.3V ≤ VOSNS− ≤ 0.3V, All VID Codes	−1.45	−1.3	−0.75	mA

Note 1: Guaranteed by design but not tested in production

Note 2: VDAC Output is trimmed to compensate for Error Amp input offsets errors

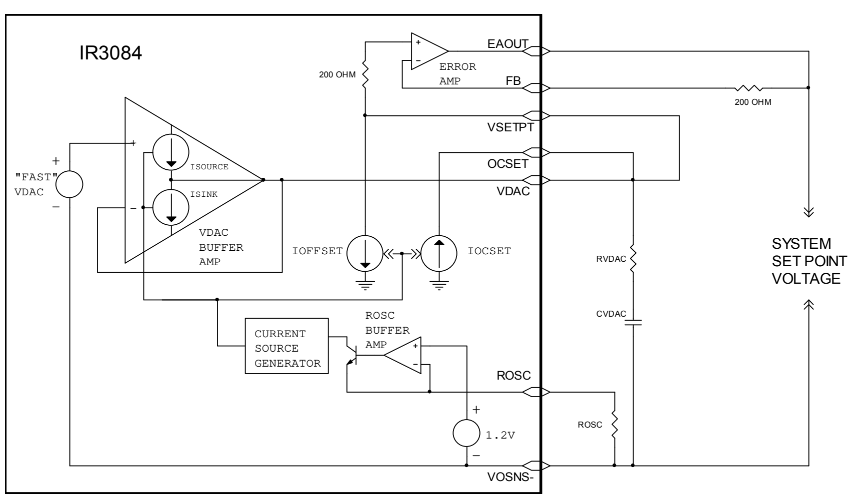


Figure 1 – System Set Point Test Circuit

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	DESCRIPTION
1	VIDSEL	Selects the DAC table and the type of Soft Start. There are 4 possible modes of operation: (1) GND selects VR10 DAC and VR11 type startup, (2) FLOAT (1.25V) selects VR11 DAC and VR11 type startup, (3) VBIAS (6.9V) selects VR11 DAC and legacy VR10 type startup, (4) VCC (12V) selects VR10 DAC and legacy VR10 type startup. Additional details are provided in the Theory of Operation section.
2−9	VID7−0	Inputs to the D to A Converter. Must be connected to an external pull-up resistor.
10	VOSNS−	Remote Sense Input. Connect to ground at the Load.
11	ROSC	Connect a resistor to VOSNS− to program oscillator frequency and OCSET, VSETPT, REGSET, and VDAC bias currents
12	VDAC	Regulated voltage programmed by the VID inputs. Connect an external RC network to VOSNS− to program Dynamic VID slew rate and provide compensation for the internal Buffer Amplifier.
13	OCSET	Programs the hiccup over-current threshold through an external resistor tied to VDAC and an internal current source. Over-current protection can be disabled by connecting a resistor from this pin to VDAC to program the threshold higher than the possible signal into the IIN pin from the Phase ICs but no greater than 5V (do not float this pin as improper operation will occur).
14	VSETPT	Error Amp non-inverting input. Converter output voltage can be decreased from the VDAC (VID) voltage with an external resistor connected to VDAC and an internal current sink. Current sensing and PWM operation are referenced to this pin.
15	IIN	Current Sense input from the Phase ICs. Prior to startup, SS/DEL<0.6V, this pin is pulled low by a 12.5K resistor to disable current balancing in the Phase ICs. When SS/DEL>0.6V and EAOUT>0.35V, this pin is released and current balancing is enabled. If current feedback from the Phase ICs is not required for implementing droop or over-current protection connect this pin to LGND. To ensure proper operation do not float this pin.
16	VDRP	Buffered IIN signal. Connect an external RC network to FB to program converter output impedance
17	FB	Inverting input to the Error Amplifier.
18	EAOUT	Output of the Error Amplifier. When Low, provides UVL function to the Phase ICs.
19	RMPOUT	Oscillator Output voltage. Used by Phase ICs to program Phase Delay
20	VBIAS	6.9V/6mA Regulated output used as a system reference voltage for internal circuitry and the Phase ICs.
21	VCC	Power Input for internal circuitry
22	LGND	Local Ground for internal circuitry and IC substrate connection
23	REGFB	Inverting input of the Bias Regulator Error Amp. Connect to the out put of the Phase IC Gate Driver Bias Regulator.
24	REGDRV	Output of the Bias Regulator Error Amp.
25	REGSET	Non-inverting input of the Bias Regulator Error Amp. Output Voltage of the Phase IC Gate Driver Bias Regulator is set by an internal current source flowing into an external resistor connected between this pin and ground.
26	SS/DEL	Controls Converter Start-up and Over-Current Timing. Connect an external capacitor to LGND to program.
27	VRRDY	Open Collector output that drives low during Start-Up and any external fault condition. Connect external pull-up.
28	ENABLE	Enable Input. A logic low applied to this pin puts the IC into Fault mode. This pin has a 100K pull-down resistor to GND.

SYSTEM THEORY OF OPERATION

XPhase™ Architecture

The *XPhase*™ architecture is designed for multiphase interleaved buck converters which are used in applications requiring small size, design flexibility, low voltage, high current and fast transient response. The architecture can be used in any multiphase converter ranging from 1 to 16 or more phases where flexibility facilitates the design trade−off of multiphase converters. The scalable architecture can be applied to other applications which require high current or multiple output voltages.

As shown in Figure 2, the *XPhase*™ architecture consists of a Control IC and a scalable array of phase converters each using a single Phase IC. The Control IC communicates with the Phase ICs through a 5−wire analog bus, i.e. bias voltage, phase timing, average current, error amplifier output, and VID voltage. The Control IC incorporates all the system functions, i.e. VID, PWM ramp oscillator, error amplifier, bias voltage, and fault protections etc. The Phase IC implements the functions required by the converter of each phase, i.e. the gate drivers, PWM comparator and latch, over−voltage protection, and current sensing and sharing.

There is no unused or redundant silicon with the *XPhase*™ architecture compared to others such as a 4 phase controller that can be configured for 2, 3, or 4 phase operation. PCB Layout is easier since the 5 wire bus eliminates the need for point−to−point wiring between the Control IC and each Phase. The critical gate drive and current sense connections are short and local to the Phase ICs. This improves the PCB layout by lowering the parasitic inductance of the gate drive circuits and reducing the noise of the current sense signal.

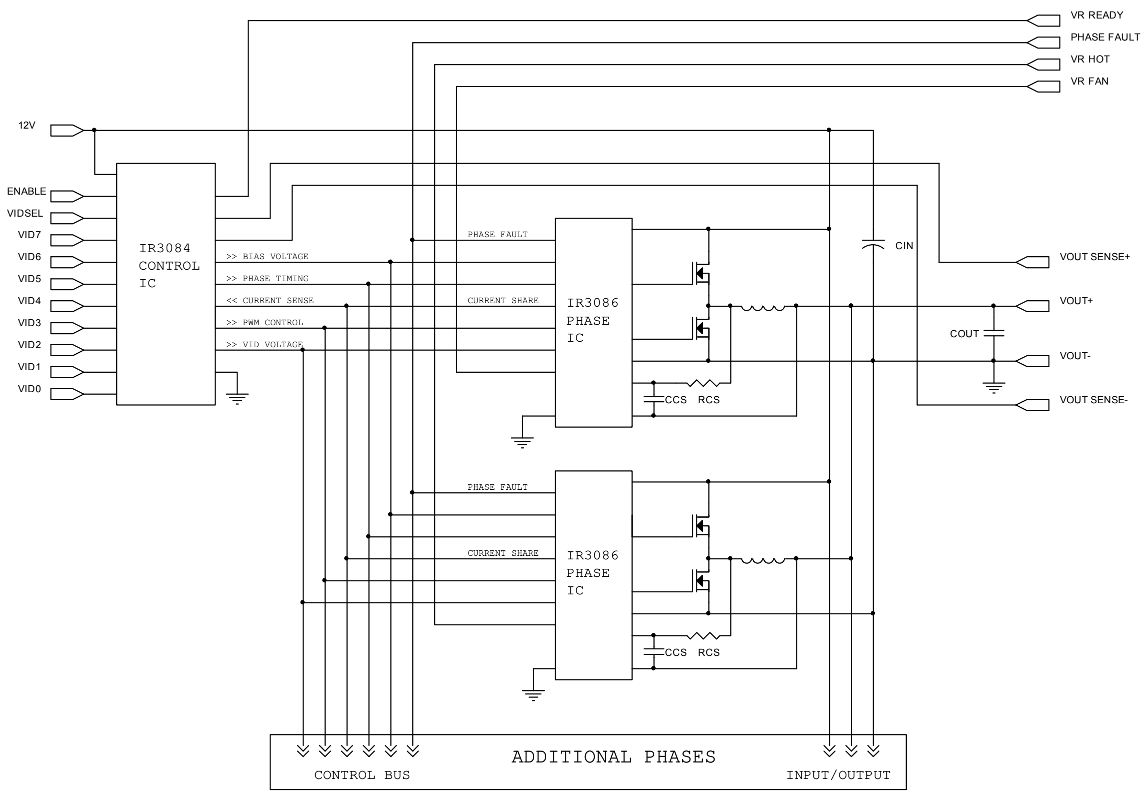


Figure 2 – System Block Diagram

PWM Control Method

The PWM block diagram of the *XPhase*™ architecture is shown in Figure 3. Feed−forward voltage mode control with trailing edge modulation is used. A high−gain wide−bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. An external RC circuit connected to the input voltage and ground is used to program the slope of the PWM ramp and to provide the feed−forward control at each phase. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to drops in the PCB related to changes in load current.

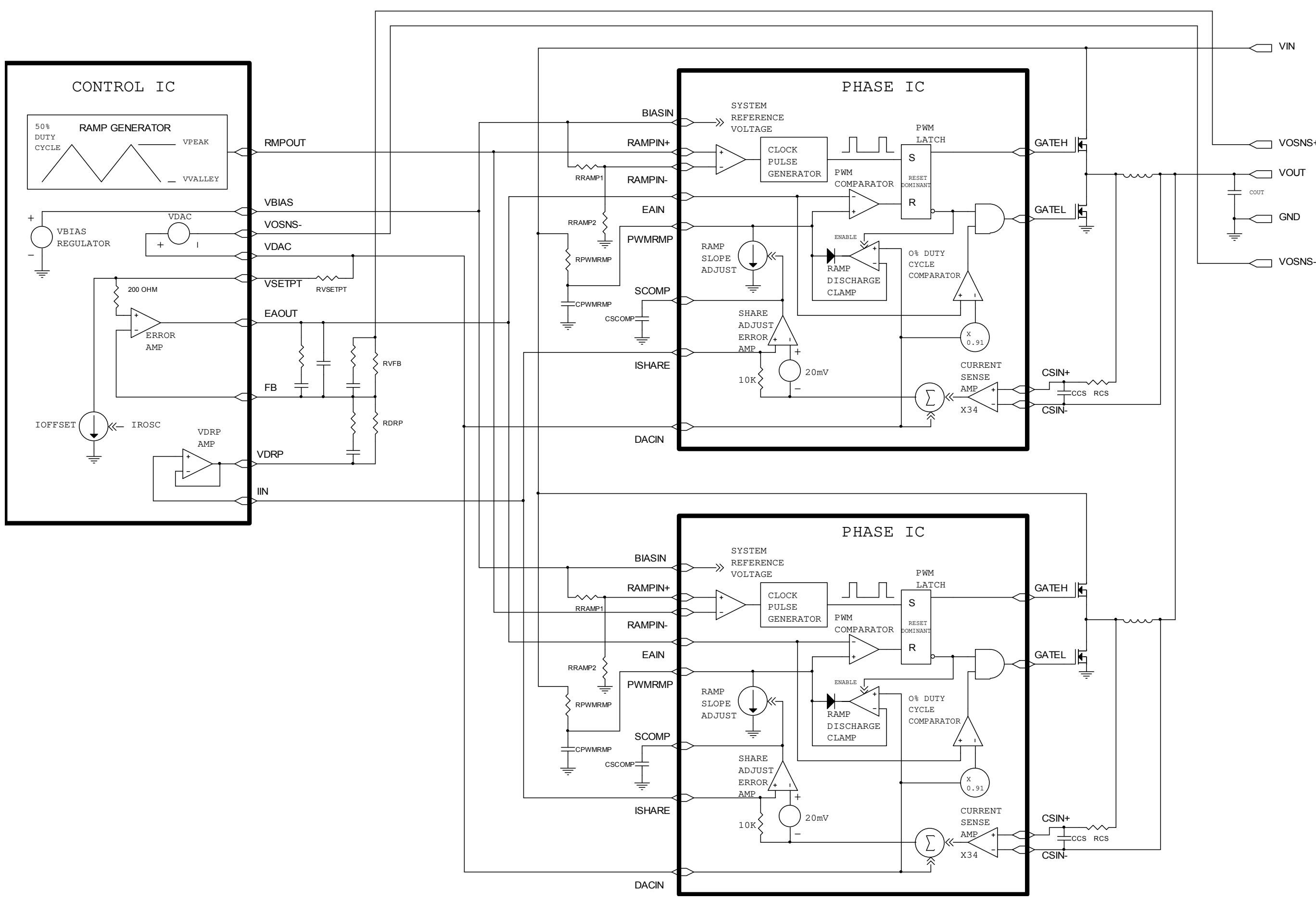


Figure 3 – IR3084 PWM Block Diagram

Frequency and Phase Timing Control

The oscillator is located in the Control IC and its frequency is programmable from 150kHz to 1MHZ by an external resistor. The output of the oscillator is a 50% duty cycle triangle waveform with peak and valley voltages of approximately 4.8V and 0.9V. This signal is used to program both the switching frequency and phase timing of the Phase ICs. The Phase IC is programmed by resistor divider RRAMP1 and RRAMP2 connected between the VBIAS reference voltage and the Phase IC LGND pin. A comparator in the Phase ICs detects the crossing of the oscillator waveform with the voltage generated by the resistor divider and triggers a clock pulse that starts the PWM cycle. The peak and valley voltages track the VBIAS voltage reducing potential Phase IC timing errors. Figure 4 shows the Phase timing for an 8 phase converter. Note that both slopes of the triangle waveform can be used for synchronization by swapping the RAMP + and – pins.

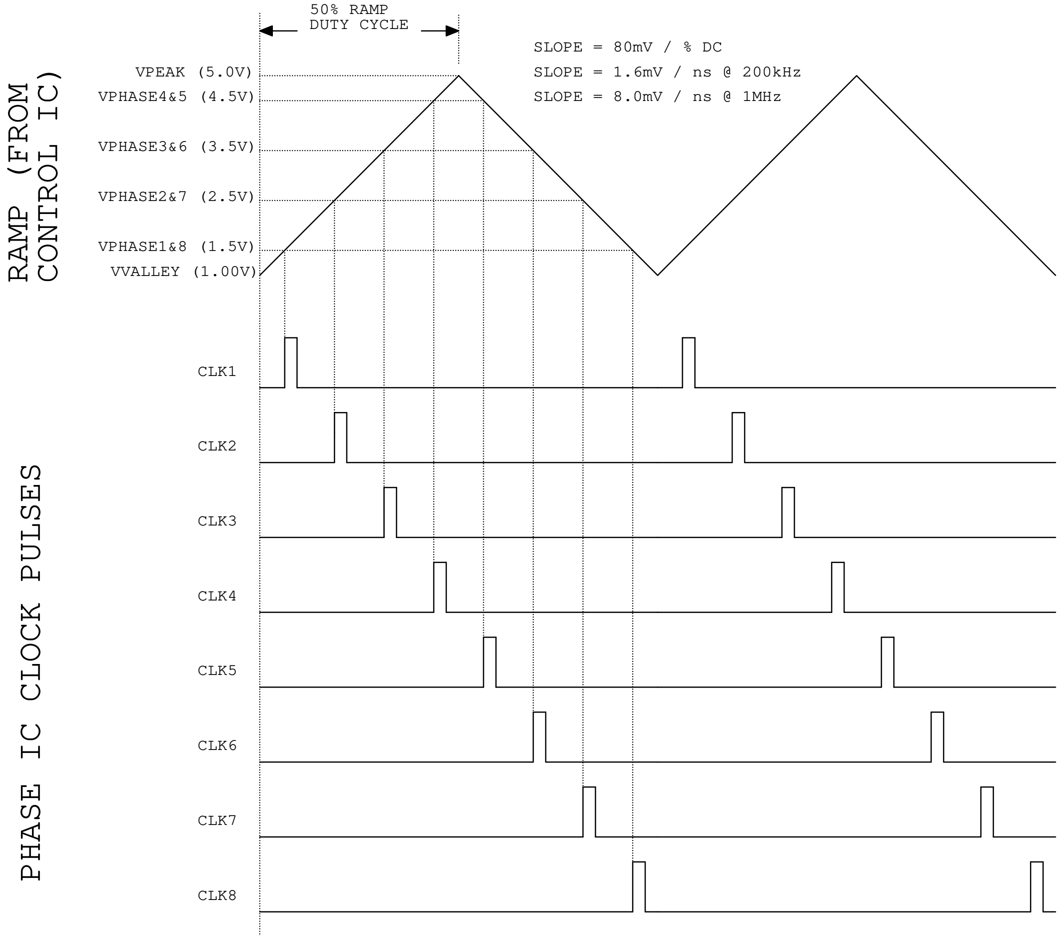


Figure 4 – 8 Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the Phase IC. Upon receiving a clock pulse, the PWM latch is set, the PWMRMP voltage begins to increase, the low side driver is turned off, and the high side driver is then turned on. When the PWMRMP voltage exceeds the Error Amp's output voltage the PWM latch is reset. This turns off the high side driver, turns on the low side driver, and activates the Ramp Discharge Clamp. The clamp quickly discharges the PWMRMP capacitor to the VDAC voltage of the Control IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amp output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amp is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response" where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / Vout$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODY\ DIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / (Vout + V_{BODY\ DIODE})$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "body braking" and is accomplished through the "0% Duty Cycle Comparator" located in the Phase IC. If the Error Amp's output voltage drops below 91% of the VDAC voltage this comparator turns off the low side gate driver.

Figure 5 depicts PWM operating waveforms under various conditions

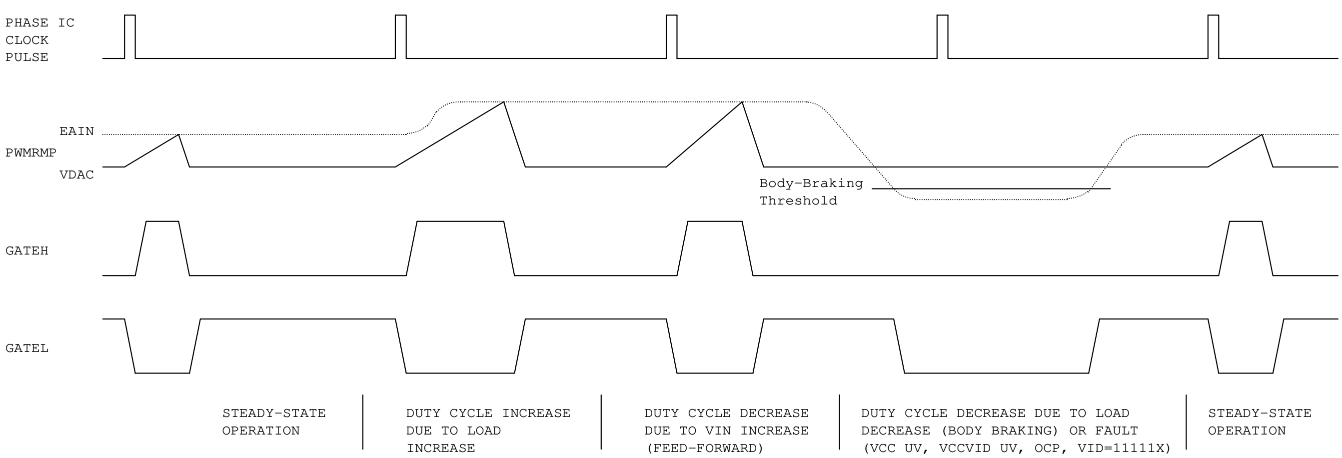


Figure 5 – PWM Operating Waveforms

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_SC_S} = i_L(s)\frac{R_L+sL}{1+sR_SC_S}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR. If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak−to−average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak−to−average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the Phase IC, as shown in Figure 6. Its gain decreases with increasing temperature and is nominally 34 at 25ºC and 29 at 125ºC (−1470 ppm/ºC). This reduction of gain tends to compensate the 3850 ppm/ºC increase in inductor DCR. Since in most designs the Phase IC junction is hotter than the inductor these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 100mV and negative up to −20mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the Control IC and other Phases through an on-chip 10KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average inductor current through all the inductors and is used by the Control IC for voltage positioning and current limit protection.

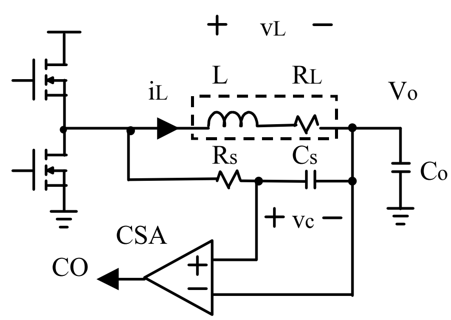


Figure 6 – Inductor Current Sensing and Current Sense Amplifier

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each Phase IC. The output of the current sense amplifier is compared with the share bus less a nominal 20mV offset. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will activate a current source that reduces the slope of its PWM ramp thereby increasing its duty cycle and output current. The crossover frequency of the current share loop can be programmed with a capacitor at the SCOMP pin so that the share loop does not interact with the output voltage loop.

IR3084 THEORY OF OPERATION

Block Diagram

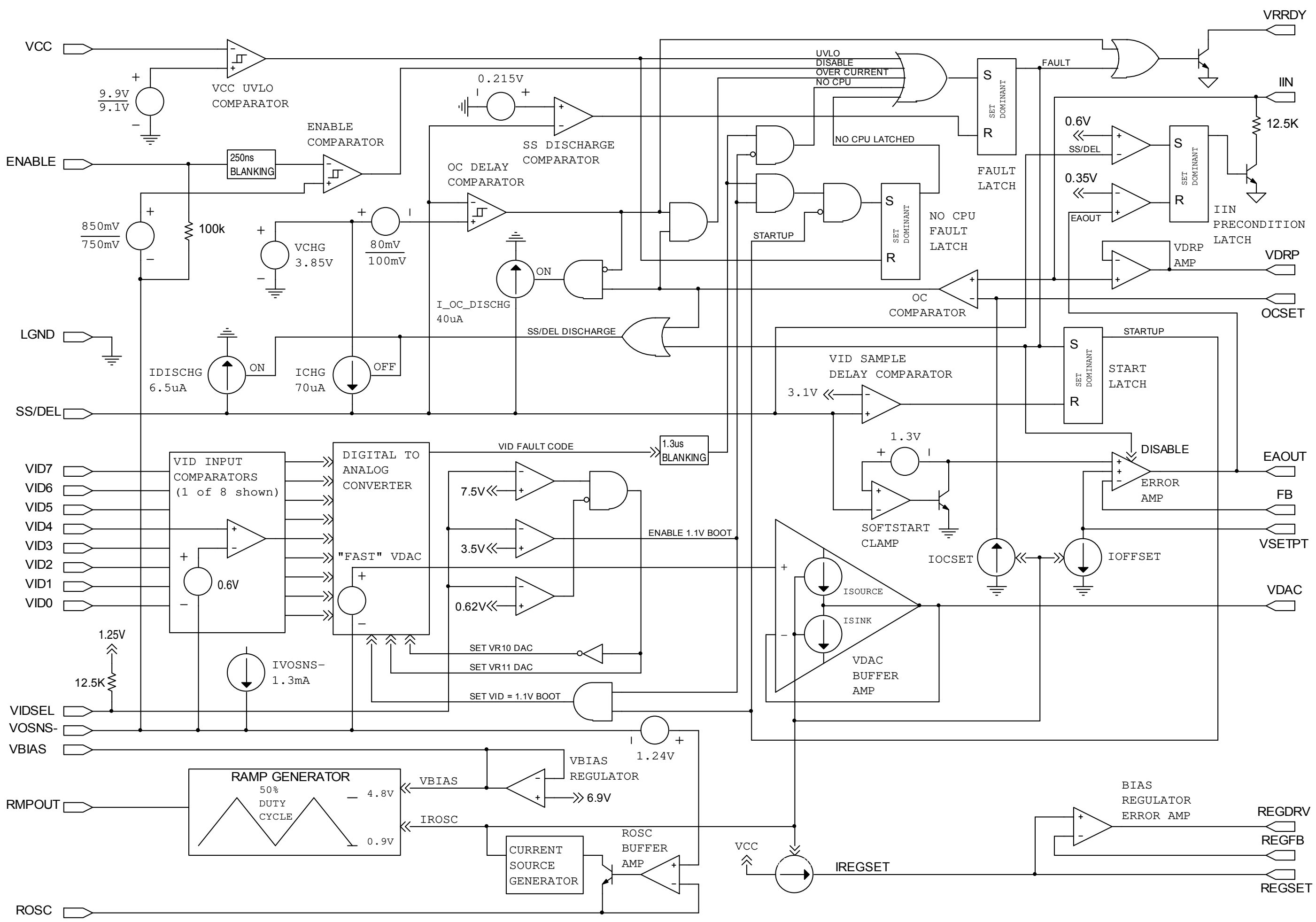


Figure 7 – IR3084 Block Diagram

VID Control

An 8−bit VID voltage compatible with VR 10 (see Table 1) and VR11 (see Table 2) is available at the VDAC pin. The VIDSEL pin configures the DAC for VR10 if grounded or connected to VCC (12V) and for VR11 if floated or connected to VBIAS (6.9V). The VIDSEL pin is internally pulled−up to 1.25V through a 12.5Kohm resistor. The VID pins require an external bias voltage and should not be floated. The VID input comparators, with 0.6V threshold, monitor the VID pins and control the 8 bit Digital−to−Analog Converter (DAC) whose output is sent to the VDAC buffer amplifier. The output of the buffer amp is the VDAC pin. The VDAC voltage is post-package trimmed to compensate for the input offsets of the Error Amp to provide a 0.5% system accuracy. The actual VDAC voltage does not represent the system set point and has a wider tolerance.

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Voltage
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375
0	1	1	1	1	0	1	1.48750
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875
1	0	1	0	0	0	1	1.36250
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250
1	1	0	1	0	0	0	1.20625

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Voltage
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	FAULT
1	1	1	1	1	0	0	FAULT
1	1	1	1	1	1	1	FAULT
1	1	1	1	1	1	0	FAULT
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375
0	0	1	0	0	0	1	0.98750
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.96250
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.88750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

Table 1 – VR10 VID Table with 6.25mV extension

Hex (VID7:VID0)	Dec (VID7:VID0)	Voltage
00	00000000	Fault
01	00000001	Fault
02	00000010	1.60000
03	00000011	1.59375
04	00000100	1.58750
05	00000101	1.58125
06	00000110	1.57500
07	00000111	1.56875
08	00001000	1.56250
09	00001001	1.55625
0A	00001010	1.55000
0B	00001011	1.54375
0C	00001100	1.53750
0D	00001101	1.53125
0E	00001110	1.52500
0F	00001111	1.51875
10	00010000	1.51250
11	00010001	1.50625
12	00010010	1.50000
13	00010011	1.49375
14	00010100	1.48750
15	00010101	1.48125
16	00010110	1.47500
17	00010111	1.46875
18	00011000	1.46250
19	00011001	1.45625
1A	00011010	1.45000
1B	00011011	1.44375
1C	00011100	1.43750
1D	00011101	1.43125
1E	00011110	1.42500
1F	00011111	1.41875
20	00100000	1.41250
21	00100001	1.40625
22	00100010	1.40000
23	00100011	1.39375
24	00100100	1.38750
25	00100101	1.38125
26	00100110	1.37500
27	00100111	1.36875
28	00101000	1.36250
29	00101001	1.35625
2A	00101010	1.35000
2B	00101011	1.34375
2C	00101100	1.33750
2D	00101101	1.33125
2E	00101110	1.32500
2F	00101111	1.31875
30	00110000	1.31250
31	00110001	1.30625
32	00110010	1.30000
33	00110011	1.29375
34	00110100	1.28750
35	00110101	1.28125
36	00110110	1.27500
37	00110111	1.26875
38	00111000	1.26250
39	00111001	1.25625
3A	00111010	1.25000
3B	00111011	1.24375
3C	00111100	1.23750
3D	00111101	1.23125
3E	00111110	1.22500
3F	00111111	1.21875
40	01000000	1.21250
41	01000001	1.20625
42	01000010	1.20000
43	01000011	1.19375
44	01000100	1.18750
45	01000101	1.18125
46	01000110	1.17500
47	01000111	1.16875
48	01001000	1.16250
49	01001001	1.15625
4A	01001010	1.15000
4B	01001011	1.14375
4C	01001100	1.13750
4D	01001101	1.13125
4E	01001110	1.12500
4F	01001111	1.11875
50	01010000	1.11250
51	01010001	1.10625
52	01010010	1.10000
53	01010011	1.09375
54	01010100	1.08750
55	01010101	1.08125
56	01010110	1.07500
57	01010111	1.06875
58	01011000	1.06250
59	01011001	1.05625
5A	01011010	1.05000
5B	01011011	1.04375
5C	01011100	1.03750
5D	01011101	1.03125
5E	01011110	1.02500
5F	01011111	1.01875
60	01100000	1.01250
61	01100001	1.00625
62	01100010	1.00000
63	01100011	0.99375
64	01100100	0.98750
65	01100101	0.98125
66	01100110	0.97500
67	01100111	0.96875
68	01101000	0.96250
69	01101001	0.95625
6A	01101010	0.95000
6B	01101011	0.94375
6C	01101100	0.93750
6D	01101101	0.93125
6E	01101110	0.92500
6F	01101111	0.91875
70	01110000	0.91250
71	01110001	0.90625
72	01110010	0.90000
73	01110011	0.89375
74	01110100	0.88750
75	01110101	0.88125
76	01110110	0.87500
77	01110111	0.86875
78	01111000	0.86250
79	01111001	0.85625
7A	01111010	0.85000
7B	01111011	0.84375
7C	01111100	0.83750
7D	01111101	0.83125
7E	01111110	0.82500
7F	01111111	0.81875

Table 2 – VR11 VID Table (Part 1)

Hex (VID7:VID0)	Dec (VID7:VID0)	Voltage
80	10000000	0.81250
81	10000001	0.80625
82	10000010	0.80000
83	10000011	0.79375
84	10000100	0.78750
85	10000101	0.78125
86	10000110	0.77500
87	10000111	0.76875
88	10001000	0.76250
89	10001001	0.75625
8A	10001010	0.75000
8B	10001011	0.74375
8C	10001100	0.73750
8D	10001101	0.73125
8E	10001110	0.72500
8F	10001111	0.71875
90	10010000	0.71250
91	10010001	0.70625
92	10010010	0.70000
93	10010011	0.69375
94	10010100	0.68750
95	10010101	0.68125
96	10010110	0.67500
97	10010111	0.66875
98	10011000	0.66250
99	10011001	0.65625
9A	10011010	0.65000
9B	10011011	0.64375
9C	10011100	0.63750
9D	10011101	0.63125
9E	10011110	0.62500
9F	10011111	0.61875
A0	10100000	0.61250
A1	10100001	0.60625
A2	10100010	0.60000
A3	10100011	0.59375
A4	10100100	0.58750
A5	10100101	0.58125
A6	10100110	0.57500
A7	10100111	0.56875
A8	10101000	0.56250
A9	10101001	0.55625
AA	10101010	0.55000
AB	10101011	0.54375
AC	10101100	0.53750
AD	10101101	0.53125
AE	10101110	0.52500
AF	10101111	0.51875
B0	10110000	0.51250
B1	10110001	0.50625
B2	10110010	0.50000
B3	10110011	0.49375
B4	10110100	0.48750
B5	10110101	0.48125
B6	10110110	0.47500
B7	10110111	0.46875
B8	10111000	0.46250
B9	10111001	0.45625
BA	10111010	0.45000
BB	10111011	0.44375
BC	10111100	0.43750
BD	10111101	0.43125
BE	10111110	0.42500
BF	10111111	0.41875

Hex (VID7:VID0)	Dec (VID7:VID0)	Voltage
C0	11000000	0.41250
C1	11000001	0.40625
C2	11000010	0.40000
C3	11000011	0.39375
C4	11000100	0.38750
C5	11000101	0.38125
C6	11000110	0.37500
C7	11000111	0.36875
C8	11001000	0.36250
C9	11001001	0.35625
CA	11001010	0.35000
CB	11001011	0.34375
CC	11001100	0.33750
CD	11001101	0.33125
CE	11001110	0.32500
CF	11001111	0.31875
D0	11010000	0.31250
D1	11010001	0.30625
D2	11010010	0.30000
D3	11010011	0.29375
D4	11010100	0.28750
D5	11010101	0.28125
D6	11010110	0.27500
D7	11010111	0.26875
D8	11011000	0.26250
D9	11011001	0.25625
DA	11011010	0.25000
DB	11011011	0.24375
DC	11011100	0.23750
DD	11011101	0.23125
DE	11011110	0.22500
DF	11011111	0.21875
E0	11100000	0.21250
E1	11100001	0.20625
E2	11100010	0.20000
E3	11100011	0.19375
E4	11100100	0.18750
E5	11100101	0.18125
E6	11100110	0.17500
E7	11100111	0.16875
E8	11101000	0.16250
E9	11101001	0.15625
EA	11101010	0.15000
EB	11101011	0.14375
EC	11101100	0.13750
ED	11101101	0.13125
EE	11101110	0.12500
EF	11101111	0.11875
F0	11110000	0.11250
F1	11110001	0.10625
F2	11110010	0.10000
F3	11110011	0.10000
F4	11110100	0.10000
F5	11110101	0.10000
F6	11110110	0.10000
F7	11110111	0.10000
F8	11111000	0.10000
F9	11111001	0.10000
FA	11111010	0.10000
FB	11111011	0.10000
FC	11111100	0.10000
FD	11111101	0.10000
FE	11111110	FAULT
FF	11111111	FAULT

Table 2 – VR11 VID Table (Part 2)

The IR3084 can accept changes in the VID code while operating and vary the DAC voltage accordingly. The sink/source capability of the VDAC buffer amp is programmed by the same external resistor that sets the oscillator frequency. The slew rate of the voltage at the VDAC pin can be adjusted by an external capacitor between VDAC pin and the VOSNS− pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifier. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

Adaptive Voltage Positioning

Adaptive Voltage Positioning (AVP) is needed to reduce the output voltage deviations during load transients and the power dissipation of the load when it is drawing high current. The circuitry related to the voltage positioning is shown in Figure 8.

Resistor R_{SETPT} is connected between the VDAC pin and VSETPT pin to set the desired amount of fixed offset voltage below the DAC voltage. The VSETPT is internally connected to the non−inverting input of the voltage error amplifier and an internal current source I_{OFFSET}, whose value is programmed by the same external resistor that programs the oscillator frequency. The voltage drop across RSETPT caused by I_{OFFSET} sets the no-load I offset voltage below the nominal DAC setting.

The voltage at the VDRP pin is a buffered version of the share bus and represents the sum of the DAC voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the resistor RDRP. Since the Error Amp will force the loop to maintain FB to be equal to the VSETPT reference voltage, a current will flow into the FB pin equal to (VDRP−VSETPT) / R_{DRP}. When the load current increases, the VDRP voltage increases accordingly. More current flows through the feedback resistor R_{FB}, and makes the output voltage lower proportional to the load current. The positioning voltage can be programmed by the resistor R_{DRP} so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to and therefore independent of the VDAC voltage.

Due to the difference between VDAC and VSETPT, the VDRP will cause extra offset voltage through RDRP and RFB. The total offset voltage is the sum of voltage across RVSETPT and the voltage drop on the RFB at no load.

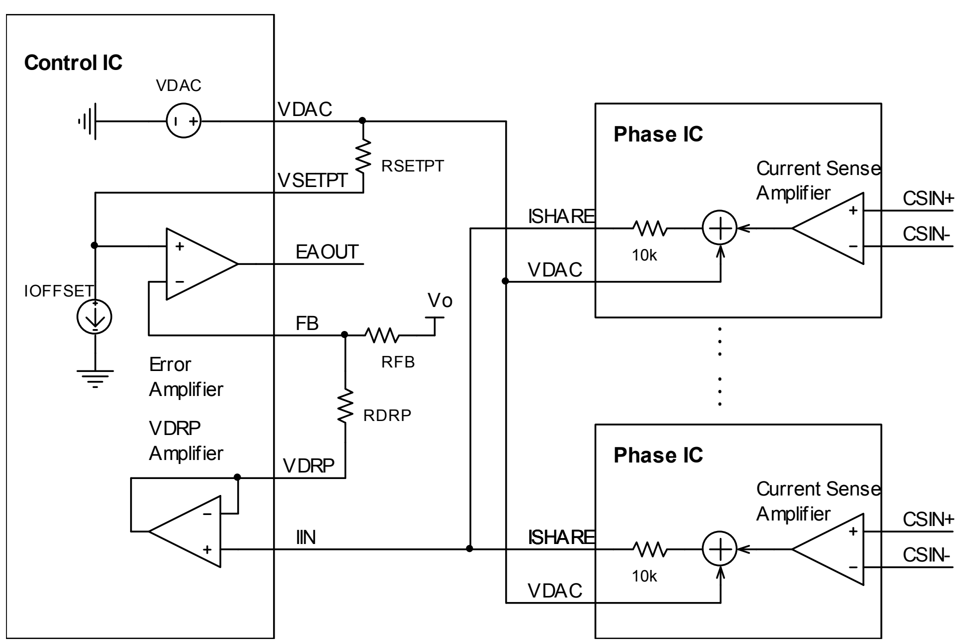


Figure 8 − Adaptive voltage positioning

Inductor DCR Temperature Correction

If the thermal compensation of the inductor DCR provided by the temperature dependent gain of the current sense amplifier is not adequate, a negative temperature coefficient (NTC) thermistor can be used for additional correction. The thermistor should be placed close to the inductor and connected in parallel with the feedback resistor, as shown in Figure 9. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

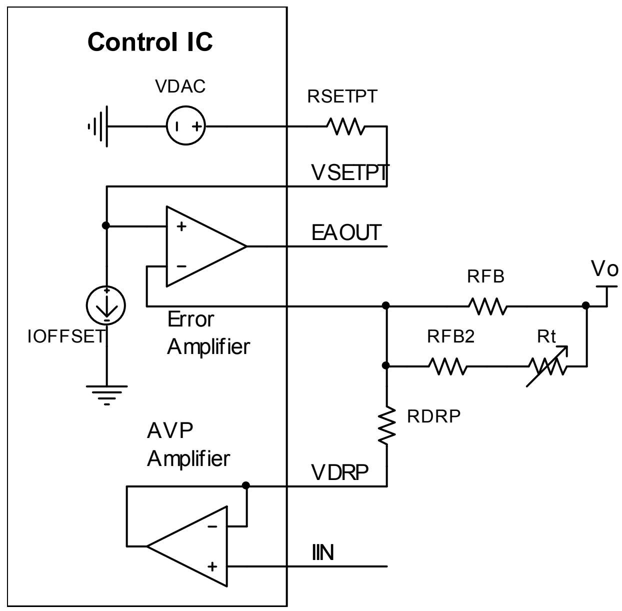


Figure 9 − Temperature compensation of inductor DCR

Remote Voltage Sensing

To compensate for impedance in the ground plane, the VOSNS− pin is used for remote sensing and connects directly to the load. The VDAC voltage is referenced to VOSNS− to avoid additional error terms or delay related to a separate differential amplifier. The capacitor connecting the VDAC and VOSNS− pins ensure that high speed transients are fed directly into the error amp without delay.

Start-up Modes

The IR3084 has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL and LGND pins controls soft start as well as over-current protection delay and hiccup mode timing. A charge current of 70uA controls the positive slope of the voltage at the SS/DEL pin.

There are two types of start-up possible: Boot Mode (VR11) and Non-Boot Mode (legacy VR10). In Boot Mode, the soft start circuitry will initially set the voltage at the VDAC pin to 1.1V and the converter's output will slowly rise, using the slew rate set by the capacitor at the SS/DEL pin, until it's equal to 1.1V. After Vcore achieves the 1.1V Boot voltage, there will be a short delay, the VID pins will be sampled, and the voltage at the VDAC pin and the converter's output will increase or decrease to the desired VID setting using the dynamic VID slew rate. In Non-Boot Mode, the soft start sequence will ramp the voltage at the VDAC pin directly to the external VID setting using the slew rate set by the capacitor at the SS/DEL pin without pausing at the 1.1V Boot voltage.

Figure 10a depicts the start-up sequence without AVP in Boot Mode (VRM11) − VIDSEL is either floating or grounded. First, the VDAC pin is charged to the 1.1V Boot voltage. Then, if there are no fault conditions, the SS/DEL capacitor will begin to be charged. Initially, the error amplifier's output will be clamped low until the voltage at the SS/DEL pin reaches 1.3V. After the voltage at the SS/DEL pin rises to 1.3V, the error amplifier's output will begin to rise and the converter's output voltage will be regulated 1.3V below the voltage at the SS/DEL pin. The converter's output voltage will slowly ramp to the 1.1V Boot voltage. The SS/DEL pin's voltage will continue to increase until it rises above the 3.1V threshold of the VID delay comparator. When the SS/DEL voltage exceeds 3.1V, the VID inputs will be sampled and the VDAC pin will transition to the level determined by the VID inputs at the dynamic VID slew rate. When the voltage on the SS/DEL pin rises above 3.77V the VRRDY Delay Comparator will allow the VRRDY signal to be asserted. SS/DEL will continue to rise until finally settling at 3.85V, indicating the end of the start-up sequence.

Figure 10b depicts the start-up sequence in Non-Boot Mode − VIDSEL is connected to VBIAS (6.9V) or to VCC (12V). First, the external VID setting is sampled and the VDAC pin is set to the desired VID voltage. Then, if there are no fault conditions, the SS/DEL capacitor will begin to charge. Initially, the error amplifier's output will be clamped low until the voltage at the SS/DEL rises to 1.3V. After the voltage at the SS/DEL pin reaches 1.3V, the error amplifier's output will begin to rise and the converter's output voltage will be regulated 1.3V below the voltage at the SS/DEL pin. As the voltage at the SS/DEL pin continues to rise, the converter's output voltage will slowly increase until it is equal to the voltage at the VDAC pin. When the voltage on the SS/DEL pin rises above 3.77V the VRRDY Delay Comparator will allow the VRRDY signal to be asserted. SS/DEL will continue to rise until finally settling at 3.85V, indicating the end of the start−up sequence.

If AVP is used (RDRP $\neq \infty$), the soft start timing will change slightly because of the resistor from the VDRP amplifier to the Error Amplifier's FB pin. During startup with AVP, the VDRP amplifier will produce a voltage at the FB pin equal to VDAC times the resistor divider formed by the droop resistor and the feedback resistor from Vcore to the FB pin. To offset the contribution from the VDRP amplifier, the voltage at the SS/DEL pin will have to rise to beyond 1.3V before the Error Amplifier's output and Vcore begin to rise. For a DAC setting of 1.3V with typical load line slope, the Error Amplifier's output will begin to rise when the voltage at the SS/DEL pin reaches approximately 1.6V. The effect of this offset will be to slightly lengthen the Start Delay (TD1) and shorten the Soft Start Ramp Time (TD2).

The following table summarizes the differences between the 4 modes associated with setting the VIDSEL pin. In addition to changing the soft start sequence, the NO_CPU code may or may not be ignored during startup and the NO_CPU code may or may not be latched.

VIDSEL Voltage	**VID Table**	**1.1V Boot Voltage During Startup?**	**Ignore NO CPU Codes During Startup?**	**Latch NO CPU Fault Code?**
GND	VR10	YES	YES	YES
FLOAT (1.2V)	VR11	YES	YES	YES
VBIAS (6.9V)	VR11	NO	NO	NO
VCC (12V)	VR10	NO	NO	NO

Table 3: 3084 Controller Functionality versus VIDSEL Voltages

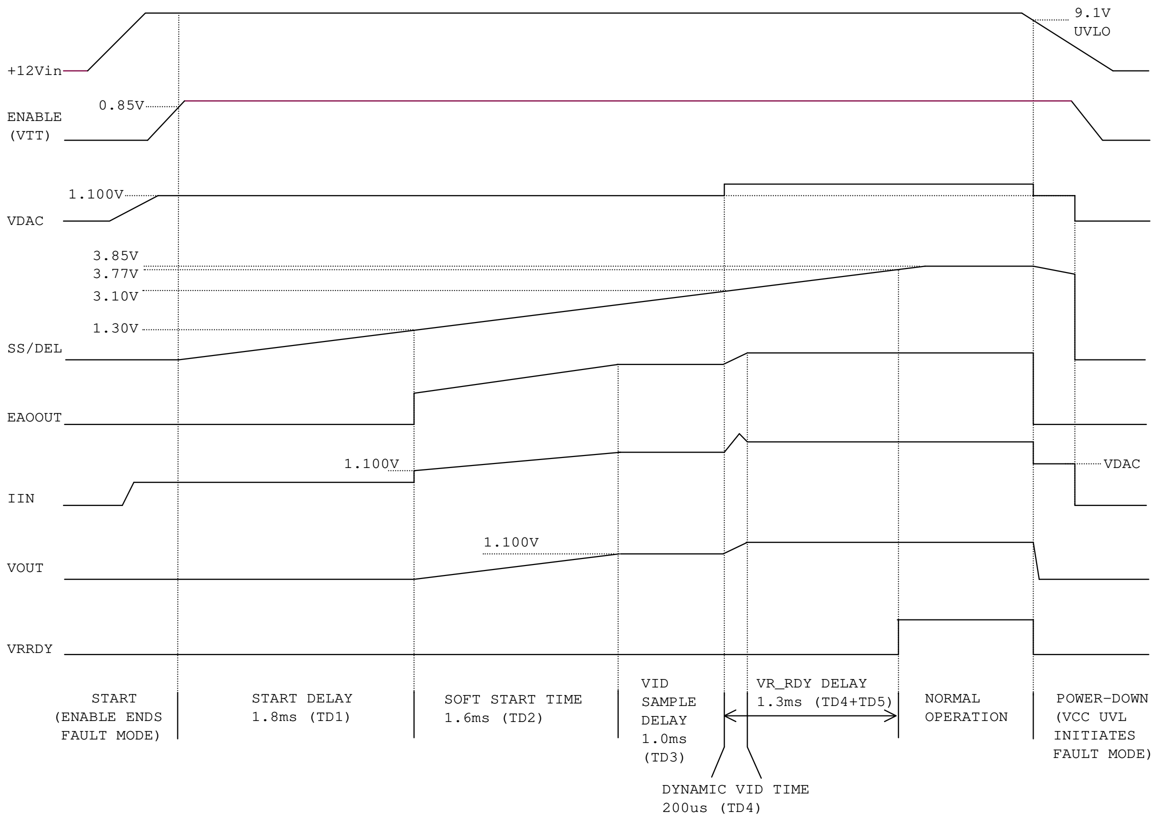


Figure 10a – Start−up Waveforms with Boot Mode (VID Setting > 1.1V)

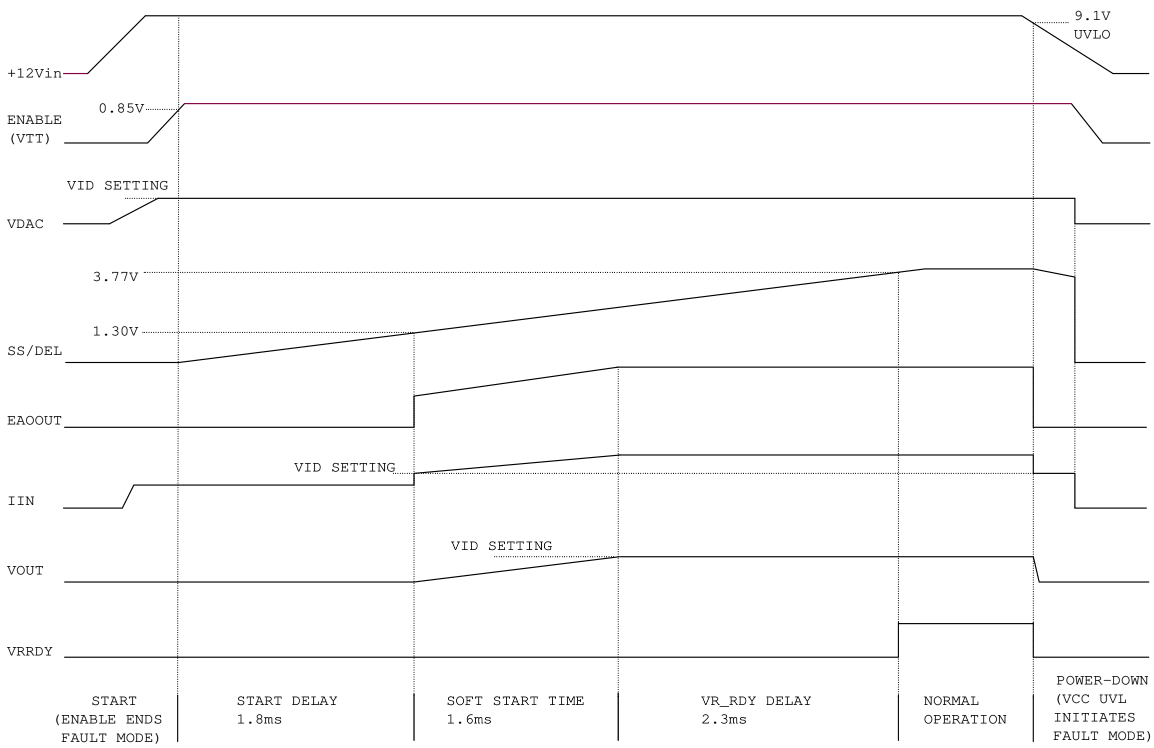


Figure 10b – Start−up Waveforms without 1.1V Boot Mode (VID Setting=1.1V)

Fault Modes

Under Voltage Lock Out, VID = FAULT, as well as a low signal on the ENABLE input immediately sets the fault latch. This causes the EAOUT pin to drive low turning off the Phase IC drivers. The VRRDY pin also drives low. The SS/DEL capacitor will discharge down to 0.215V through a 6.5uA current source. If the fault has cleared the fault latch will be reset by the discharge comparator allowing a normal start-up sequence to occur. If a VID = FAULT condition is latched it can only be cleared by cycling power to the IR3084 on and off.

Over−Current Protection Delay and Hiccup Mode

Figure 11 depicts the operating waveforms of the Over-Current protection. A delay is included if an over-current condition occurs after a successful soft start sequence. This is required because over-current conditions can occur as part of normal operation due to load transients or VID transitions. If an over-current fault occurs during normal operation it will activate the SS/DEL discharge current of 40uA but will not set the fault latch immediately. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 100mV offset of the delay comparator, the Fault latch will be set pulling the error amp's output low inhibiting switching in the phase ICs and de-asserting the VRRDY signal.

The SS/DEL capacitor will continue to discharge until it reaches 0.215V and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle the fault latch will be set without any delay and hiccup mode will begin. During hiccup mode the 10.8 to 1 charge to discharge current ratio results in a 9% hiccup mode duty cycle regardless of at what point the over-current condition occurs.

If the voltage at the SS/DEL pin is pulled below the SS/DEL to FB Input Offset Voltage (0.85V min), the converter can be disabled.

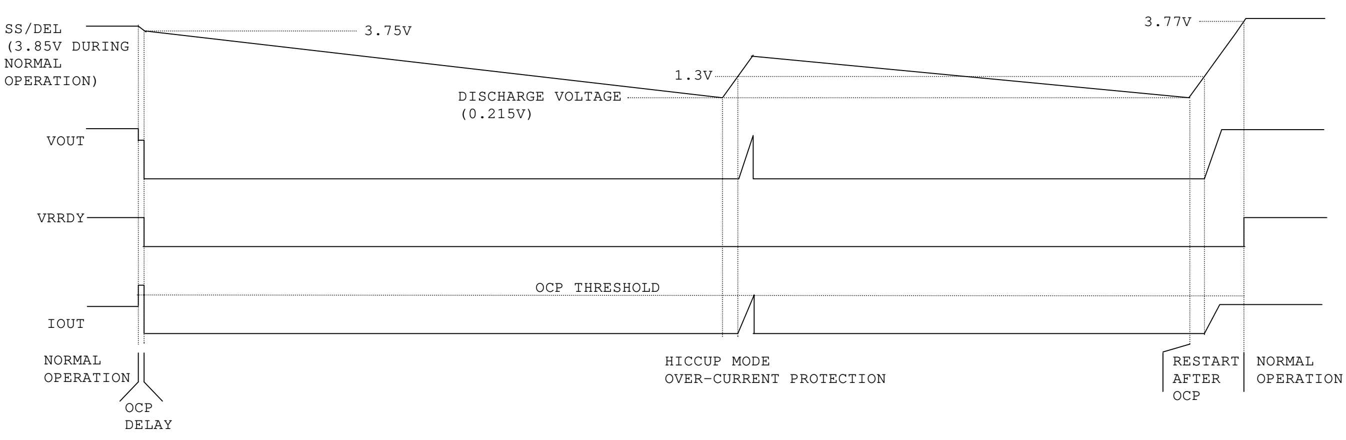


Figure 11 – Over-Current Protection Waveforms (VID = 1.1V for simplicity)

Under Voltage Lockout (UVLO)

The UVLO function monitors the IR3084's VCC supply pin and ensures that there is adequate voltage to safely power the internal circuitry. The IR3084's UVLO threshold is set higher than the minimum operating voltage of compatible Phase ICs thus providing UVLO protection for them as well. UVLO at the Phase ICs is a function of the Error Amplifier's output voltage. When the IR3084 is in UVLO, the Error Amplifier is disabled and EAOUT is at a very low voltage (<200mV) thus preventing the Phase ICs from becoming active.

During power-up, the IR3084's fault latch is reset when VCC exceeds 9.9V if there are no other faults. If the VCC voltage drops below 9.1V the fault latch will be set.

Over Current Protection (OCP)

The current limit threshold is set by a resistor connected between the OCSET and VDAC pins. If the IIN pin voltage, which is proportional to the average phase current plus DAC voltage, exceeds the OCSET voltage, the over-current protection is triggered.

VID = Fault Code (NO_CPU)

When VIDSEL is grounded or left floating, NO_CPU VID codes of 11111XX for VR10 and 0000000X, 1111111X for VR11 will set both the VID Fault Latch and the Fault Latch to disable the error amplifier. The controller will be latched OFF and a power-on reset (POR) will be required to produce a new soft start sequence. In these 2 modes, the NO_CPU codes are ignored during startup. See Table 1 for further details.

When VIDSEL is set to VBIAS (6.9V) or VCC (12V), NO_CPU VID codes of 11111XX for VR10 and 0000000X, 1111111X for VR11 will set the Fault Latch to disable the error amplifier but the VID Fault Latch will not be set. The controller will not be latched OFF and a soft start sequence will be produced when the NO_CPU code is removed and the SS/DEL voltage falls below 0.215V. In these 2 modes, the NO_CPU codes will be not be ignored during startup. See Table 1 for further details.

A 1.3µs delay is provided to prevent a NO_CPU fault condition from occurring during Dynamic VID changes.

VRRDY (Power Good) Output

The VRRDY pin is an open-collector output and should be pulled up to a voltage source through a resistor. During soft-start, the VRRDY output remains low until the converter's output voltage is in regulation and SS/DEL is above 3.77V. The VRRDY pin transitions low if the fault latch is set. A high level at the VRRDY pin indicates that the converter is in operation and has no fault, but does not ensure the output voltage is within the specification. Output voltage regulation within the design limits can logically be assured however, assuming no component failure in the system.

Load Current Indicator Output

The VDRP pin voltage represents the average phase current of the converter plus the DAC voltage. The load current can be retrieved by subtracting the VDAC voltage from the VDRP voltage.

System Reference Voltage (VBIAS)

The IR3084 supplies a 6.9V/6mA precision reference voltage from the VBIAS pin. The oscillator ramp trip points are based on the VBIAS voltage so it should be used to program the Phase ICs phase delay to minimize phase errors.

Phase IC Gate Driver Bias Regulator / VRHOT Comparator

An internal amplifier can be configured as a gate driver bias regulator to provide programmable gate driver voltage for phase ICs (Figure 12a), or a thermal monitor to provide VRHOT/VRFAN signal as required in VR11 (Figure 12b).

The internal current source IREGSET whose value is programmed by the switching frequency going through the external RSET resistor sets the gate driver voltage or the VRHOT/VRFAN threshold voltage. An NTC thermistor is used to monitor the temperature on the VRM/VRD.

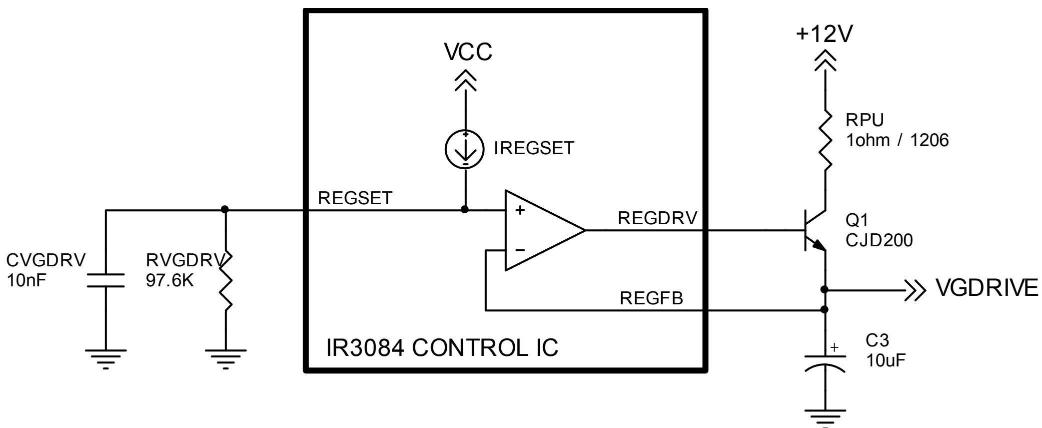


Figure 12a – IR3084 Bias Regulator configured for Gate Driver Bias Regulator

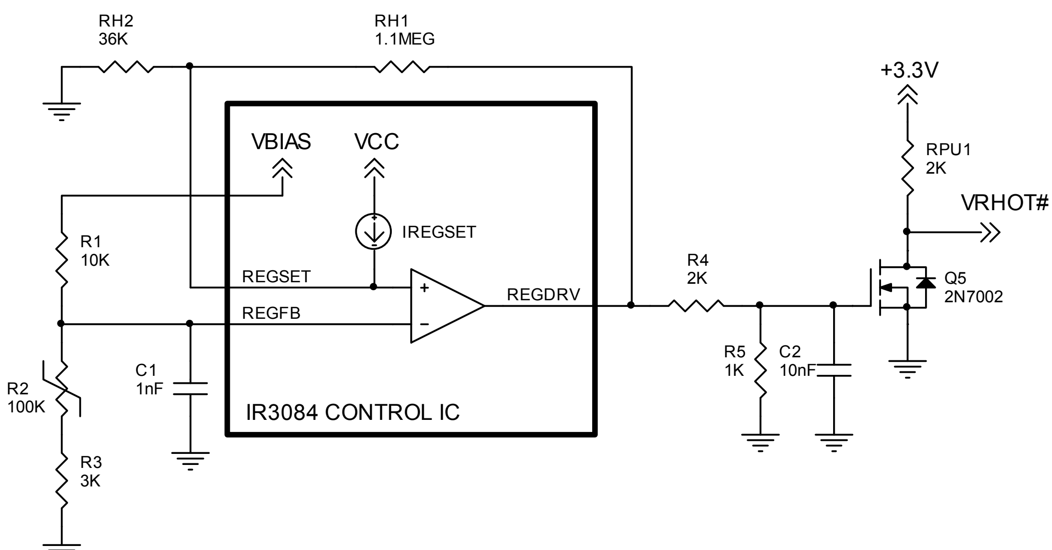


Figure 12b – IR3084 Bias Regulator configured for VRHOT# Function

PERFORMANCE CHARACTERISTICS

Figure 13: Oscillator Frequency versus ROSC

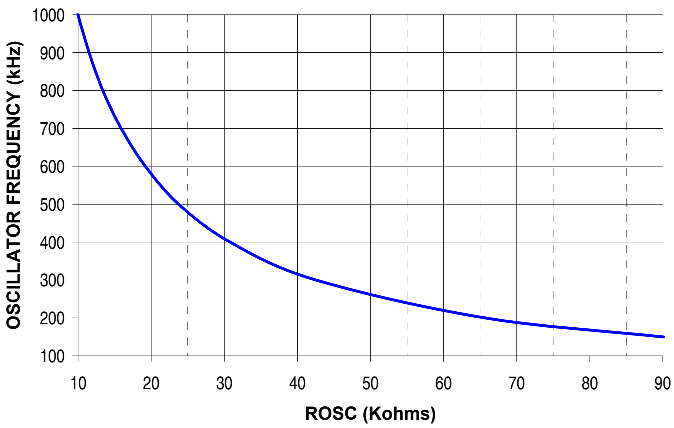


Figure 14: I(OCSET) versus ROSC

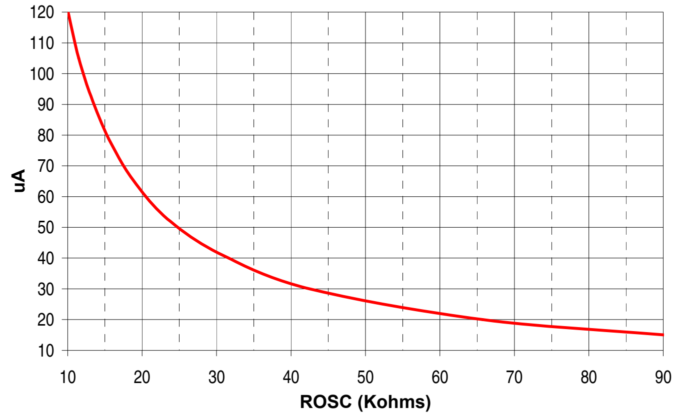


Figure 15: I(VSETPT) versus ROSC

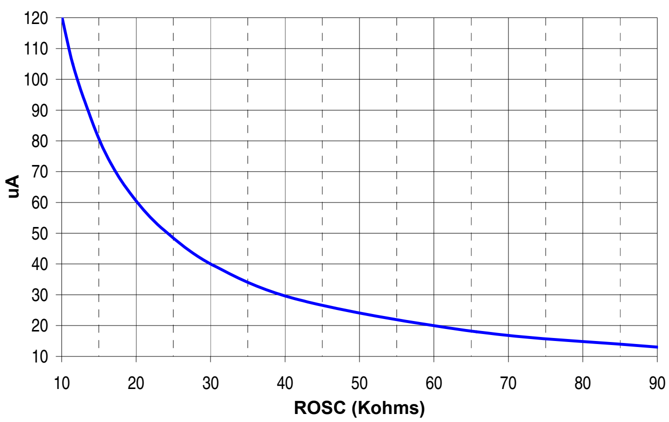


Figure 16: I(REGSET) CURRENT versus ROSC

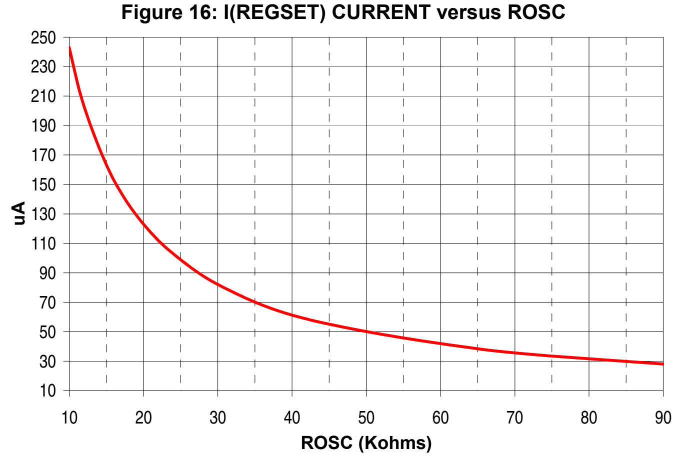


Figure 17: VDAC SINK & SOURCE CURRENT vs. ROSC

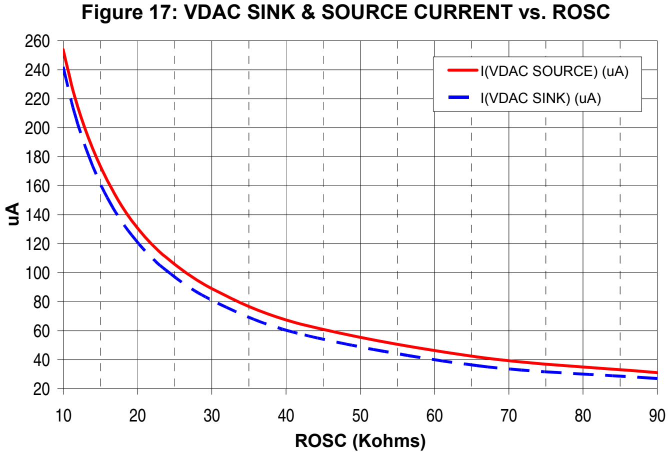
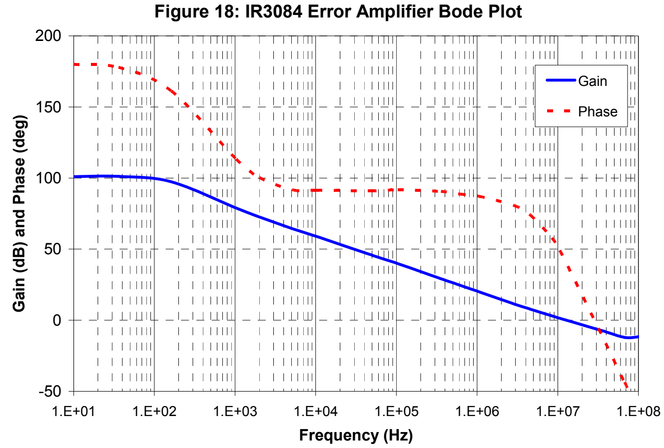


Figure 18: IR3084 Error Amplifier Bode Plot



APPLICATIONS INFORMATION

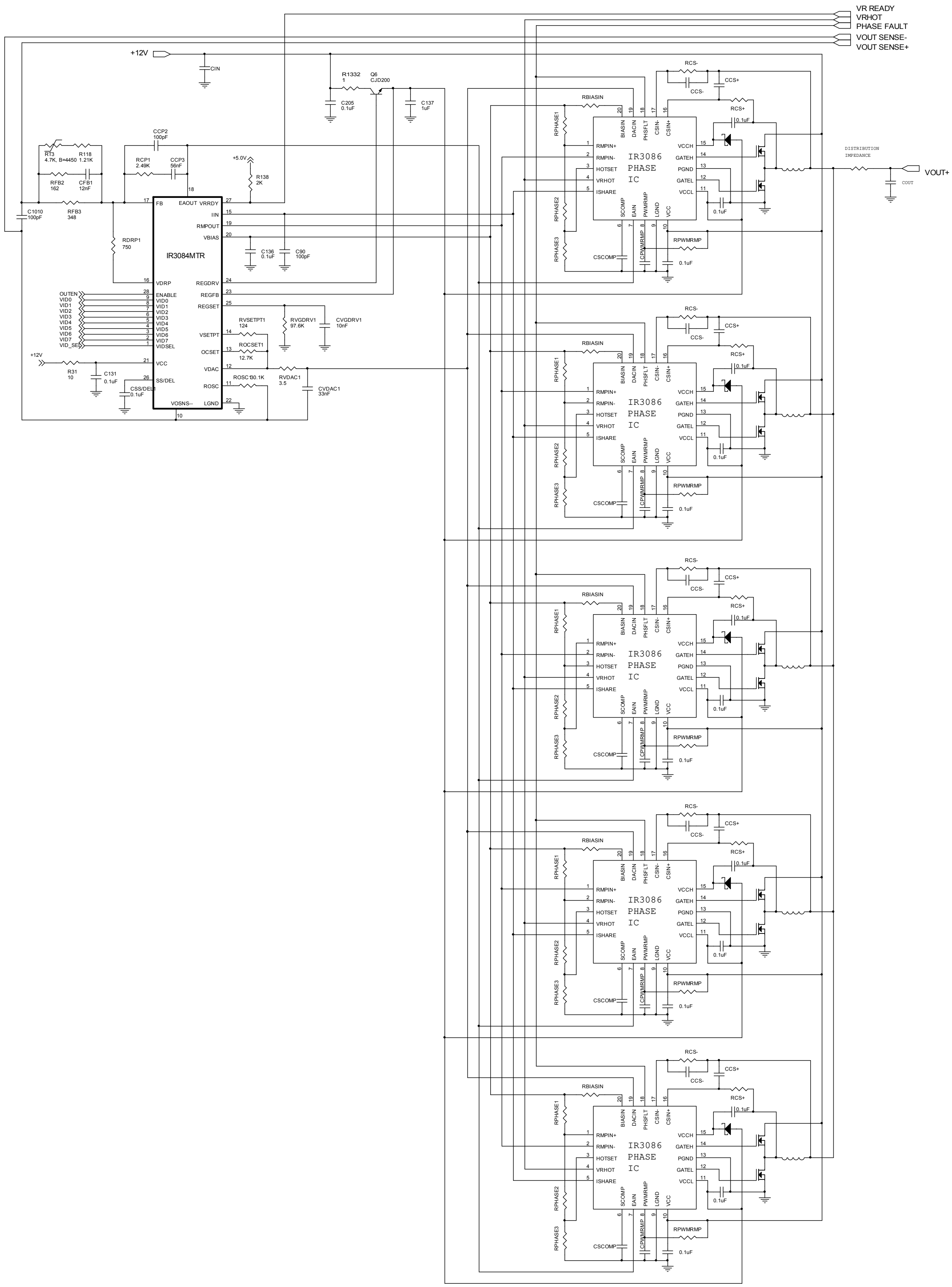


Figure 19 – IR3084/3086 5 Phase VRM/EVRD 11 Converter

DESIGN PROCEDURES – IR3084 and IR3086 Chipset

IR3084 EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

The oscillator of IR3084 generates a triangle waveform to synchronize the phase ICs, and the switching frequency of the each phase converter equals the oscillator frequency, which is set by the external resistor ROSC according to the curve in Figure 13 on page 23.

VDAC Slew Rate Programming Capacitor C_{VDAC} and Resistor R_{VDAC}

The sink and source currents of the VDAC pin are set by the value of R_{OSC}. The sink current capability of the VDAC pin is slightly less than the source current. Therefore, the VDAC sink current (I_{SINK}) should be used to calculate C_{VDAC} to insure that the dynamic VID slew rate when Vcore decreases is not too slow.

The negative slew rate of VDAC (SR_{DOWN}) is programmed by the external capacitor C_{VDAC} as shown in Equation (1). The resistor R_{VDAC} is used to compensate/stabilize the VDAC circuit and is determined by Equation (2). The positive slew rate of the VDAC voltage (SR_{UP}) is proportional to the negative slew rate of VDAC and can be calculated using Equation (3).

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} \quad (1)$$

Where: I_{SINK} is the sink current of the VDAC pin at the chosen value of R_{OSC} as shown in Figure 17 on page 23.

$$R_{VDAC} = 0.5\Omega + \frac{3.2 * 10^{-15}}{C_{VDAC}{}^2} \quad (2)$$

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} \quad (3)$$

Where: I_{SOURCE} is the source current of the VDAC pin at the chosen value of R_{OSC} as shown in Figure 17 on page 23.

The VID voltage rise or fall time during startup with Boot Mode (TD4) can be calculated using either Equation (4a) or (4b).

$$TD4 = \frac{C_{VDAC}}{I_{SOURCE}} * (VDAC - 1.1V) \qquad \text{if VDAC > 1.1V} \quad (4a)$$

$$TD4 = \frac{C_{VDAC}}{I_{SINK}} * (1.1V - VDAC) \qquad \text{if VDAC < 1.1V} \quad (4b)$$

Where: VDAC is the DAC voltage set by the VID pins.
I_{SOURCE} and I_{SINK} are the source and sink currents of the VDAC pin.
If Boot Mode is not used then TD4 = 0.