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International
IOR Rectifier

IR3092PbF

DATA SHEET

2 PHASE OPTERON, ATHLON, OR VR10.X CONTROL IC

DESCRIPTION

The IR3092 Control IC provides a full featured, single chip solution to implement robust power conversion solutions for three different microprocessor families; 1) AMD Opteron, 2) AMD Athlon or 3) Intel VR10.X family of processors. The user can select the appropriate VID range with a single pin. PWM Control and 2 phase gate drive functions are integrated into a single IC. In addition to CPU power, the IR3092 offers a compact, efficient solution for high current POL converters.

FEATURES

- 5 bit or 6 bit VID with 0.5% overall system accuracy
- Selectable VID Code for AMD Opteron, AMD Athlon or Intel VR10.X
- Programmable Slew Rate response to “On-the-Fly” VID Code Changes
- 3.5A Gate Drive Capability
- Programmable 100KHz to 540KHz oscillator
- Programmable Voltage Positioning (can be disabled)
- Programmable Softstart
- Programmable Hiccup Over-Current Protection with Delay to prevent false triggering
- Simplified Powergood provides indication of proper operation and avoids false triggering
- Operates up to 21V input with 7.8V Under-Voltage Lockout
- 5V UVL with 4.3V Under-Voltage Lockout threshold
- Adjustable Voltage, 150mA Bias Regulator provides MOSFET Drive Voltage
- Enable Input
- OVP Output
- Available in a 48L MLPQ package

ORDERING INFORMATION

DEVICE	ORDER QUANTITY
IR3092MTRPbF	3000 per Reel
IR3092MPbF	100 piece strips

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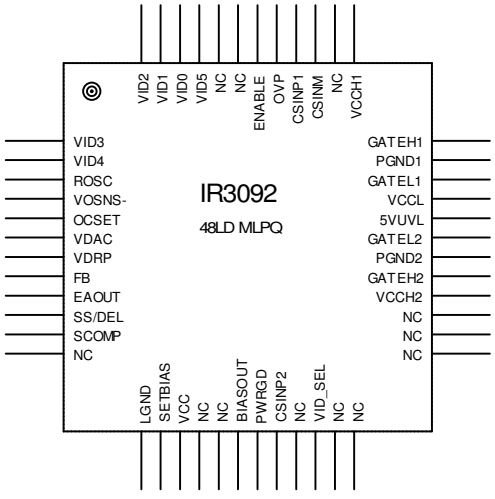
PACKAGE INFORMATION



48L MLPQ
(7 x 7 mm Body)
θ_{JA} = 27°C/W

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	VID3	Inputs to VID D to A Converter
2	VID4	Inputs to VID D to A Converter
3	ROSC	Connect a resistor to VOSNS- to program oscillator frequency and FB, OCSET, BBFB, and VDAC bias currents
4	VOSNS-	Remote Sense Input. Connect to ground at the Load.
5	OCSET	Programs the hiccup over-current threshold through an external resistor tied to VDAC and an internal current source.
6	VDAC	Regulated voltage programmed by the VID inputs. Current Sensing and Over Current Protection are referenced to this pin. Connect an external RC network to VOSNS- to program Dynamic VID slew rate.
7	VDRP	Buffered IIN signal. Connect an external RC network to FB to program converter output impedance
8	FB	Inverting input to the Error Amplifier. Converter output voltage is offset from the VDAC voltage through an external resistor connected to the converter output voltage at the load and an internal current source. Bias current is a function of ROSC. Also OVPsense.
9	EAOUT	Output of the Error Amplifier
10	SS/DEL	Controls Converter Softstart, Power Good, and Over-Current Timing. Connect an external capacitor to LGND to program the timing.
11	SCOMP	Compensation for the Current Share control loop. Connect a capacitor to ground to set the control loop's bandwidth. Phase 2 is forced to match phase 1's current.
12	N/C	No Connect.
13	LGND	Local Ground and IC substrate connection
14	SETBIAS	External resistor to ground sets voltage at BIASOUT pin. Bias current is a function of ROSC.
15	VCC	Power for internal circuitry and source for BIASOUT regulator
16-17	N/C	No Connect.
18	BIASOUT	150mA open-looped regulated voltage set by SETBIAS for GATE drive bias.
19	PWRGD	Open Collector output that drives low during Softstart or any fault condition. Connect external pull-up.
20	CSINP2	Non-inverting input to the Phase 2 Current Sense Amplifier.
21	N/C	No Connect.
22	VID_SEL	Ground Selects VR10 VID, Float Selects OPTERON VID, VCC Selects ATHLON VID
23-27	N/C	No Connect.
28	VCCH2	Power for Phase 2 High-Side Gate Driver
29	GATEH2	Phase 2 High-Side Gate Driver Output and input to GATEL2 non-overlap comparator.
30	PGND2	Return for Phase 2 Gate Drivers
31	GATEL2	Phase 2 Low-Side Gate Driver Output and input to GATEH2 non-overlap comparator.
32	5VUVL	Can be used to monitor the driver supply voltage or 5V supply voltage when converting from 5V. An under voltage condition initiates Soft Start.
33	VCCL	Power for Phase 1 and 2 Low-Side Gate Drivers.
34	GATEL1	Phase 1 Low-Side Gate Driver Output and input to GATEH1 non-overlap comparator.
35	PGND1	Return for Phase 1 Gate Drivers
36	GATEH1	Phase 1 High-Side Gate Driver Output and input to GATEL1 non-overlap comparator.
37	VCCH1	Power for Phase 1 High-Side Gate Driver
38	NC	Not connected
39	CSINM1	Inverting input to the Phase 1Current Sense Amplifier.
40	CSINP1	Non-inverting input to the Current Sense Amplifier.
41	OVP	Output that drives high during an Over-Voltage condition.
42	ENABLE	Enable Input. A logic low applied to this pin puts the IC into Fault mode.
43-44	N/C	No Connect.
45	VID5	Inputs to VID D to A Converter
46	VID0	Inputs to VID D to A Converter
47	VID1	Inputs to VID D to A Converter
48	VID2	Inputs to VID D to A Converter

ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature……..150°C
Storage Temperature Range……..-65°C to 150°C

PIN	NAME	VMAX	VMIN	ISOURCE	ISINK
1	VID3	30V	-0.3V	1mA	1mA
2	VID4	30V	-0.3V	1mA	1mA
3	ROSC	30V	-0.5V	1mA	1mA
4	VOSNS-	0.5V	-0.5V	10mA	10mA
5	OCSET	30V	-0.3V	1mA	1mA
6	VDAC	30V	-0.3V	1mA	1mA
7	VDRP	30V	-0.3V	5mA	5mA
8	FB	30V	-0.3V	1mA	1mA
9	EAOUT	10V	-0.3V	10mA	20mA
10	SS/DEL	30V	-0.3V	1mA	1mA
11	SCOMP	30V	-0.3V	5mA	5mA
12	N/C	n/a	n/a	n/a	n/a
13	LGND	n/a	n/a	50mA	1mA
14	SETBIAS	30V	-0.3V	1mA	1mA
15	VCC	30V	-0.3V	1mA	250mA
16	N/C	n/a	n/a	n/a	n/a
17	N/C	n/a	n/a	n/a	n/a
18	BIASOUT	30V	-0.3V	250mA	1mA
19	PWRGD	30V	-0.3V	1mA	20mA
20	CSINP2	30V	-0.3V	250mA	1mA
21	N/C	n/a	n/a	n/a	n/a
22	VID_SEL	30V	-0.3V	1mA	1mA
23	N/C	n/a	n/a	n/a	n/a
24	N/C	n/a	n/a	n/a	n/a
25	N/C	n/a	n/a	n/a	n/a
26	N/C	n/a	n/a	n/a	n/a
27	N/C	n/a	n/a	n/a	n/a
28	VCCH2	30V	-0.3V	n/a	3A for 100ns, 200mA DC
29	GATEH2	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
30	PGND2	0.3V	-0.3V	3A for 100ns, 200mA DC	n/a
31	GATEL2	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
32	5VUVL	30V	-0.3V	1mA	1mA
33	VCCL	30V	-0.3V	n/a	3A for 100ns, 200mA DC
34	GATEL1	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
35	PGND1	0.3V	-0.3V	3A for 100ns, 200mA DC	n/a
36	GATEH1	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
37	VCCH1	30V	-0.3V	n/a	3A for 100ns, 200mA DC
38	N/C	n/a	n/a	n/a	n/a
39	CSINM1	30V	-0.3V	250mA	1mA
40	CSINP1	30V	-0.3V	250mA	1mA
41	OVP	30V	-0.3V	1mA	1mA
42	ENABLE	30V	-0.3V	1mA	1mA
43	N/C	n/a	n/a	n/a	n/a
44	N/C	n/a	n/a	n/a	n/a
45	VID5	30V	-0.3V	1mA	1mA
46	VID0	30V	-0.3V	1mA	1mA
47	VID1	30V	-0.3V	1mA	1mA
48	VID2	30V	-0.3V	1mA	1mA

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 7.3V ≤ V_{CC} ≤ 21V, 4V ≤ V_{CCL} ≤ 14V, 4V ≤ V_{CCHX} ≤ 28V, C_{GATEHX} =3.3nF, C_{GATELX} =6.8nF, 0°C ≤ T_J ≤ 125°C

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDAC Reference					
System Set-Point Accuracy	-0.3V ≤ VOSNS- ≤ 0.3V, Connect FB to EAOUT, Measure V(EAOUT) – V(VOSNS-) deviation from Table 1. Applies to all VID codes.		0.5		%
Source Current	R_{ROSC} = 42kΩ, VDAC=OCSET	56	62	71	µA
Sink Current	R_{ROSC} = 42kΩ, VDAC=OCSET	50	58	67	µA
VID Input Threshold, INTEL	VID_SEL=0, Referenced to VOSNS-	0.4	0.6	0.8	V
VID Input Threshold, AMD	VID_SEL=Float, Referenced to VOSNS-	1.3	1.5	1.7	V
VID_SEL OPTERON Threshold		1.0	1.2	1.4	V
VID_SEL ATHLON Threshold		3.0	3.4	3.8	V
VID_SEL Float Voltage	Tracks ATHLON threshold	2.1	2.6	3.2	V
VID_SEL Pull-up Resistance	V(VID_SEL)<2.1V	30	60	100	kΩ
VID_SEL Pull-down Resistance	V(VID_SEL)>3.2V	60	190	375	kΩ
VID Pull-up Current	VID0-5 = 1V	9	15	27	µA
VID Float Voltage	Referenced to LGND	4.5	4.9	5.2	V
VID = 11111 Fault Blanking	Delay to PWRGD assertion	0.5	1.7	4.1	µs
Error Amplifier					
Input Offset Voltage	Connect FB to EAOUT, Measure V(EAOUT)-V(VDAC). From Table 1. Applies to all VID codes and -0.3V ≤ VOSNS- ≤0.3V. Note 2.	-5	-1	3	mV
FB Bias Current	R_{ROSC} = 42kΩ	28	30.5	33	µA
DC Gain	Note 1	90	100	105	dB
Gain-Bandwidth Product	Note 1	4	7		MHz
Slew Rate	Note 1, 50mV FB signal		1.25		V/µs
Source Current		280	380	500	µA
Sink Current		.75	1.0	1.5	mA
Max Voltage		4.5	4.9	5.3	V
Min Voltage			90	150	mV
VDRP Buffer Amplifier					
Positioning Offset Voltage	V(VDRP) – V(VDAC) with CSINMX=CSINPX=0, Note 1.	-125	0	125	mV
Output Voltage Range		0.2		3.75	V
Source Current		5	10	20	mA
Sink Current		200	280	400	µA

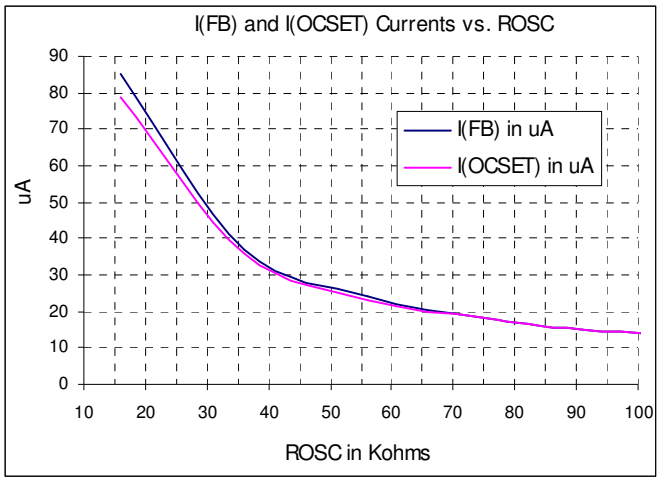
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Oscillator					
Switching Frequency	R_{ROSC} = 42kΩ	160	200	240	kHz
Phase1 to Phase2 Shift	GATEH1 rise to GATEH2 rise	155	170	190	°
BIASOUT Regulator					
SETBIAS Bias Current	R_{ROSC} = 42kΩ	105	115	125	µA
Set Point Accuracy	V(SETBIAS)-V(BIASOUT) @ 100mA	0.1	0.3	0.55	V
BIASOUT Dropout Voltage	I(BIASOUT)=100mA,Threshold when V(SETBIAS)-V(BIASOUT)=0.45V	1.2	1.8	2.5	V
BIASOUT Current Limit		150	300	450	mA
Soft Start and Delay					
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.8	1.3	1.8	V
Charge Current		25	55	75	µA
Hiccup Discharge Current		2.5	5.5	7.5	µA
OC Discharge Current		25	45	70	µA
Charge/Discharge Current Ratio		9	10	11	µA/µA
Charge Voltage		3.8	4.0	4.2	V
Delay Comparator Threshold	Relative to Charge Voltage	200	240	280	mV
Delay Comparator Hysteresis		15	30	45	mV
Discharge Comparator Threshold		200	260	350	mV
Over-Current Comparator					
Input Offset Voltage	V(OCSET)-V(VDAC), CSIN=CSINP1=CSINP2, Note 1.	-125	0	125	mV
OCSET Bias Current	R_{ROSC} = 42kΩ	28	30	33	µA
Max OCSET Set Point		3.95			V
Under-Voltage Lockout					
VCC Start Threshold		7.2	7.8	8.3	V
VCC Stop Threshold		6.7	7.3	7.8	V
VCC Hysteresis	Start – Stop	450	500	750	mV
5VUVL Start Threshold		4.05	4.3	4.55	V
5VUVL Stop Threshold		3.92	4.125	4.33	V
5VUVL Hysteresis	Start – Stop	100	175	250	mV
5VUVL Input Resistance	To LGND	24	36	72	kΩ
PWRGD Output					
Output Voltage	I(PWRGD) = 4mA		150	300	mV
Leakage Current	V(PWRGD) = 5.5V		0	10	µA
Enable Input					
Threshold, INTEL	VID_SEL=0, Referenced to VOSNS-	0.4	0.6	0.8	V
Threshold, AMD	VID_SEL=Float, Referenced to VOSNS-	1.3	1.5	1.7	V
Input Resistance		7.5	15	20	kΩ
Pull-up Voltage		2.4	3.0	3.7	V

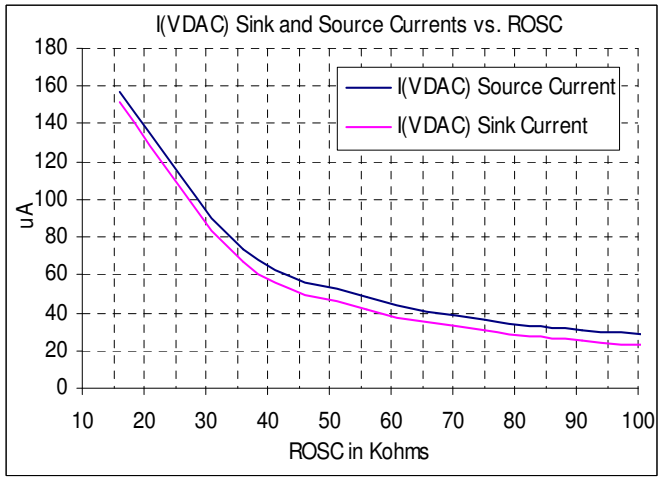
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Gate Drivers					
GATEH Rise Time	VCCHX = 12V, Measure 2V to 9V transition time, Note 1		11	40	ns
GATEH Fall Time	VCCHX = 12V, Measure 9V to 2V transition time, Note 1		11	40	ns
GATEL Rise Time	VCCL = 12V, Measure 2V to 9V transition time, Note 1		20	65	ns
GATEL Fall Time	VCCL = 12V, Measure 9V to 2V transition time, Note 1		20	65	ns
High Voltage (AC)	Measure VCCL – GATELX or VCCHX – GATEHX, Note 1		0	0.5V	V
Low Voltage (AC)	Measure GATELX or GATEHX, Note 1		0	0.5V	V
GATEL low to GATEH high delay	VCCHX = VCCL = 12V, Measure the time from GATELX falling to 2V to GATEHX rising to 2V, Note 1	20	35	60	ns
GATEH low to GATEL high delay	VCCHX = VCCL = 12V, Measure the time from GATEHX falling to 2V to GATELX rising to 2V, Note 1	20	35	60	ns
Disable Pull-Down Current	GATHX or GATELX=2V with VCC = 0V. Measure Gate pull-down current	20	35	50	μA
PWM Comparator					
Propagation Delay	VCCHX = VCCL = 12V, Measure the time from EAOUT fall crossing VDAC to GATEHX falling to 11V. (Note 1)		100	150	ns
Common Mode Input Range				4	V
Internal Ramp Start Voltage		0.45	0.7	0.9	V
Internal Ramp Amplitude		40	57	75	mV / %DTC
Current Sense Amplifier					
CSINP1&2 Bias Current		-0.5	-0.2	0.1	μA
CSINM Bias Current		-1	-0.4	0.2	μA
Input Current Offset Ratio	CSINM/CSINPX	0.7	1.7	2.6	μA/μA
Average Input Offset Voltage	(VDRP-VDAC)/GAIN withCSINX=0, Note1.	-4	0	4	mV
Offset Voltage Mismatch	Monitor I(SCOMP)	-8	0	8	mV
Gain at T_J = 25°C		22.0	23.5	25.0	V/V
Gain at T_J = 125°C		18.5	20.0	24.0	V/V
Gain Mismatch		-0.3	0	0.3	V/V
Differential Input Range		-25		75	mV
Common Mode Input Range		0		2.8	V

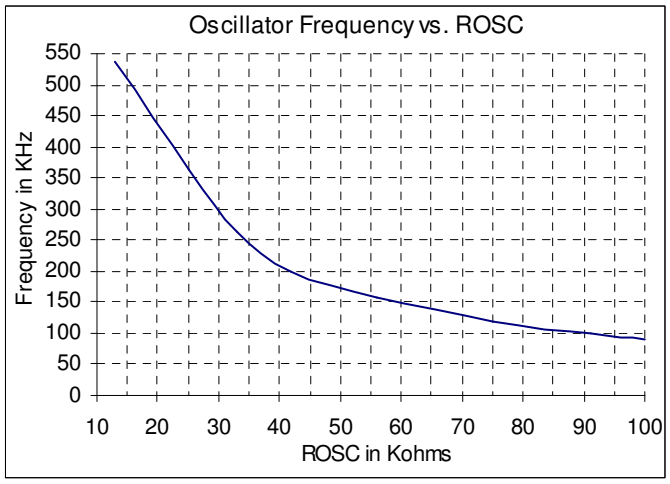
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Share Adjust Error Amplifier					
Input Offset Voltage	Note 1	-5	0	5	mV
MAX Duty Cycle Adjust Ratio	Duty Cycle of GATEH2 to GATEH1	1.5	2	3	%/%
MIN Duty Cycle Adjust Ratio	Duty Cycle of GATEH2 to GATEH1	0.6	0.5	0.4	%/%
Transconductance	Note 1	100	200	300	μA/V
SCOMP Source/Sink Current		15	28	40	μA
Equal Duty Cycle Comparator Threshold		0.45	0.7	0.85	V
Duty Cycle Match at Startup	DTC GATEH1 – DTC GATEH2	-5	0	5	%
SCOMP Precharge Current	V(SS/DEL)=0	250	420	600	μA
0% Duty Cycle Comparator					
Threshold Voltage	(Internal Ramp1 Start Voltage) – (0DC Threshold)	100	150	200	mV
Propagation Delay	VCCL = 12V. Step EAOUT from .8V to .3V and measure time to GATELX transition to < 11V.		200	320	ns
Body Braking Disable Comparator Threshold	Compare V(FB) to V(VDAC)	50	80	110	mV
OVP					
VR10 Comparator Threshold	VID_SEL=0V. Compare to V(VDAC)	120	145	180	mV
AMD Comparator Threshold	Float VID_SEL. Compare to V(VDAC)	360	480	600	mV
Propagation Delay	VCCL = 12V. V(EAOUT)=0V. Step FB 460mV above V(VDAC). Measure time to GATELX transition to >1V.		200	300	ns
Source Current		10	20		mA
Pull Down Resistance	OVP to PGND1	20	45	80	kΩ
High Voltage	I(OVP)=10mA, V(VCC)-V(OVP)	.8	1.2	1.6	V
General					
VCC Supply Current		23	29	34	mA
VOSNS- Current	-0.3V ≤ VOSNS- ≤ 0.3V, All VID Codes	2	3	4	mA
VCCHX Supply Current (12V)		3	5	7	mA
VCCHX Supply Current (28V)		5	7	9	mA
VCCL Supply Current		5	10	16	mA

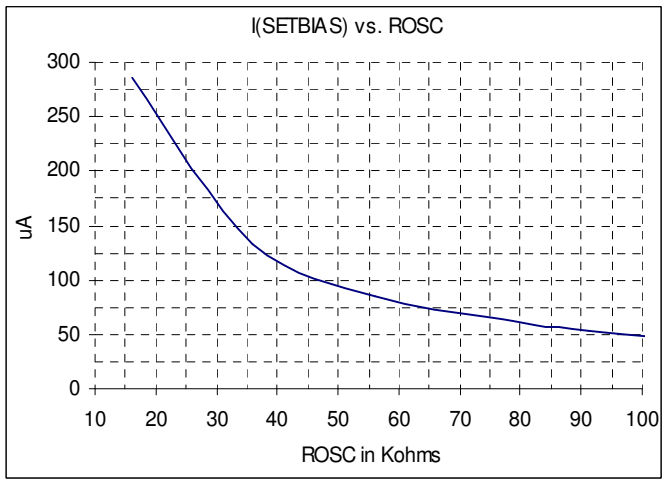
Note 1: Guaranteed by design, but not tested in production
Note 2: VDAC Output is trimmed to compensate for Error Amp input offsets errors

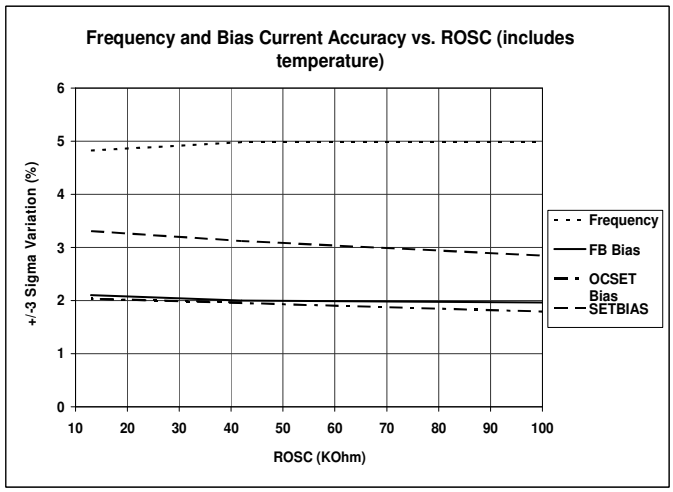
TYPICAL OPERATING CHARACTERISTICS

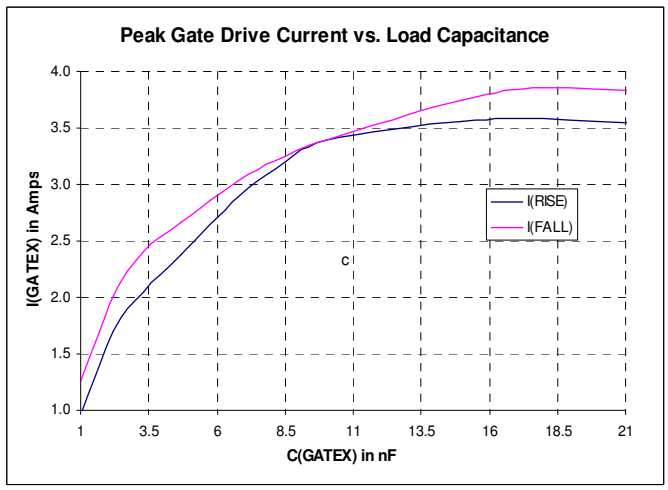












TYPICAL OPERATING CHARACTERISTICS

Error Amplifier Frequency Response

IR3092 THEORY OF OPERATION

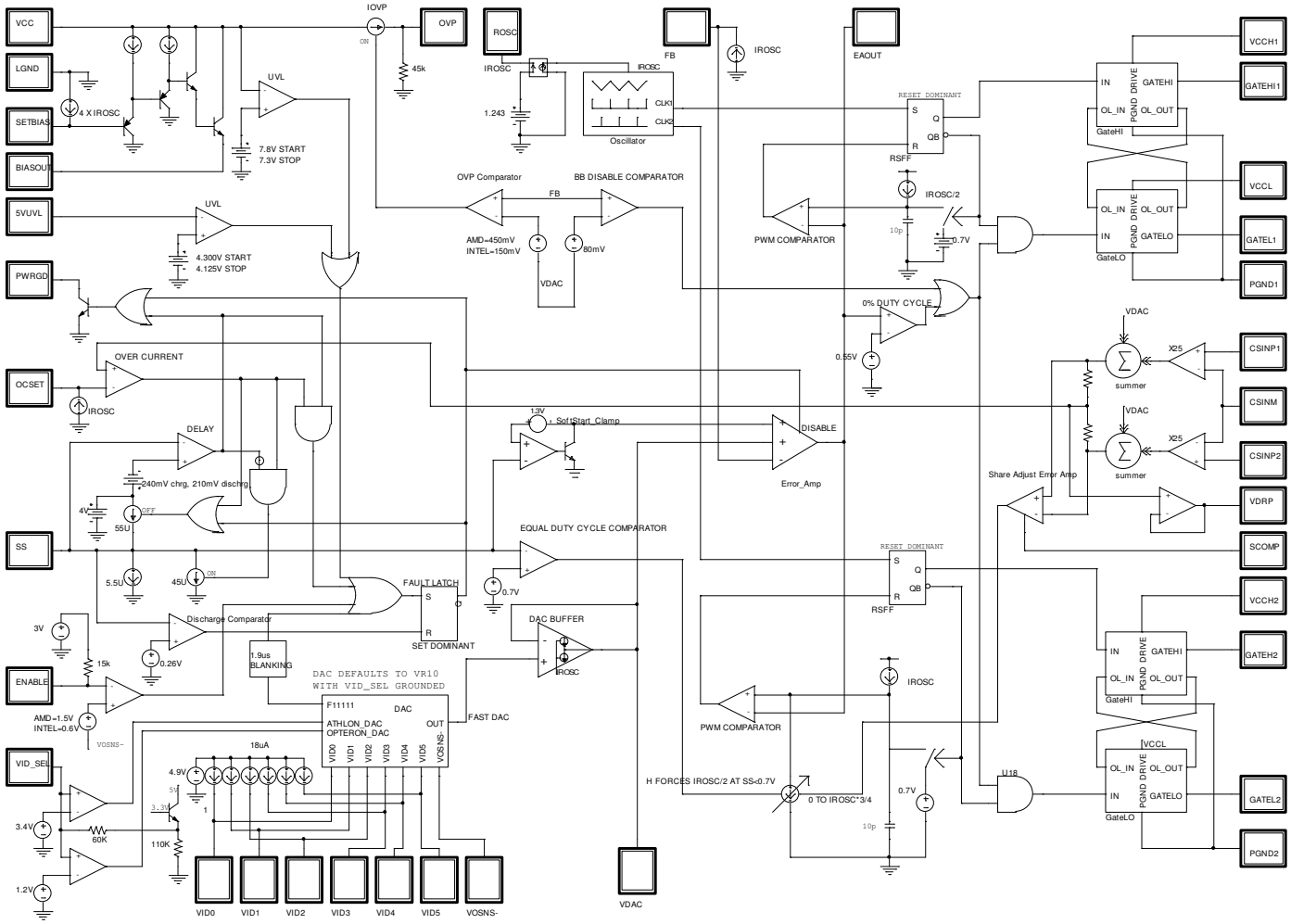


Figure 1 – IR3092 Block Diagram

PWM Operation

The IR3092 is a fully integrated 2 phase interleaved PWM control IC which uses voltage mode control with trailing edge modulation. A high-gain wide-bandwidth voltage type Error Amplifier in the control IC is used for the voltage control loop. The PWM block diagram of the IR3092 is shown in Figure 2.

Refer to Figure 3. Upon receiving a clock pulse, the RSFF is set, the internal PWM ramp voltage begins to increase, the low side driver is turned off, and the high side driver is then turned on. For phase 1, an internal 10pf capacitor is charged by a current source that's proportional to the switching frequency resulting in a ramp rate of 57mV per percent duty cycle. For example, if the steady-state operating switch node duty cycle is 10%, then the internal ramp amplitude is typically 570mV from the starting point (or floor) to the crossing of the EAOUT control voltage. When the PWM ramp voltage exceeds the Error Amplifier's output voltage, the RSFF is reset. This turns off the high side driver, turns on the low side driver, and discharges the PWM ramp to 0.7V until the next clock pulse.

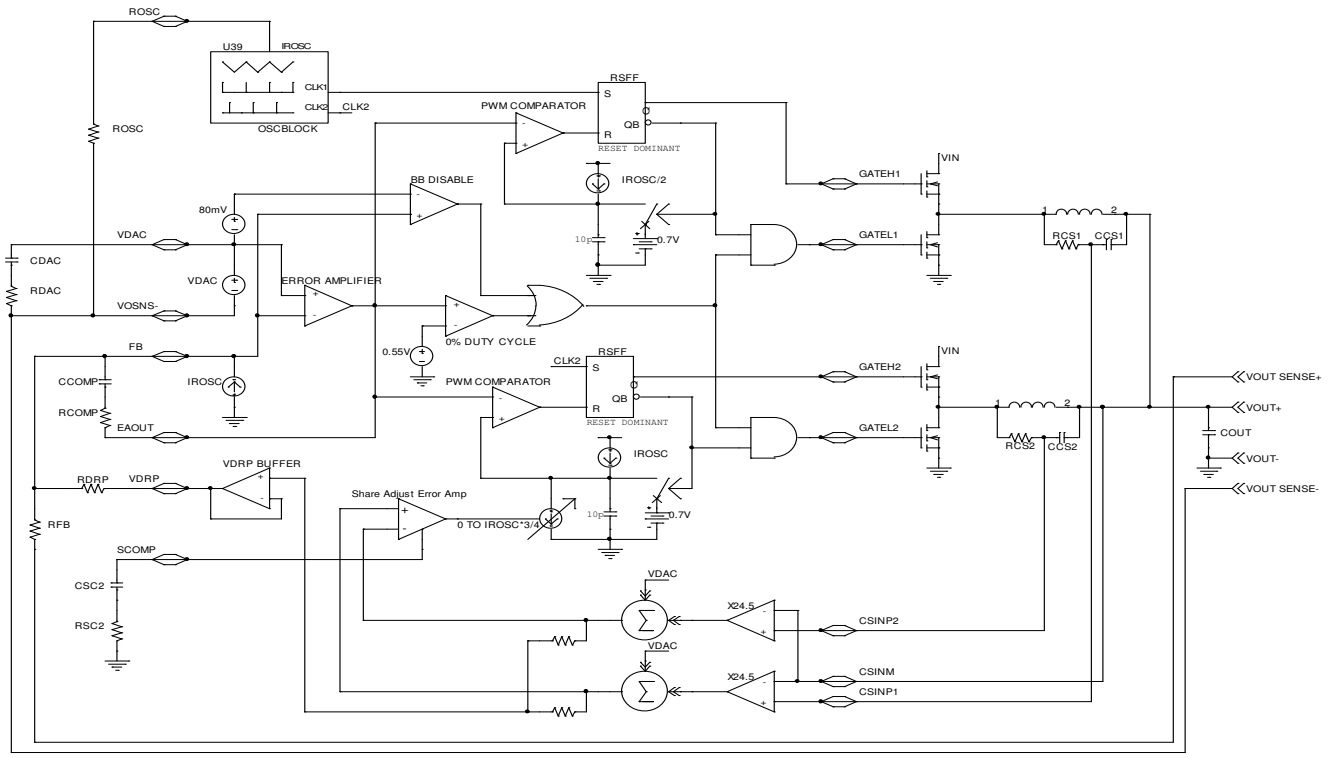


Figure 2 – PWM Block Diagram

The RSFF is reset dominant allowing both phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide “single cycle transient response” where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements.

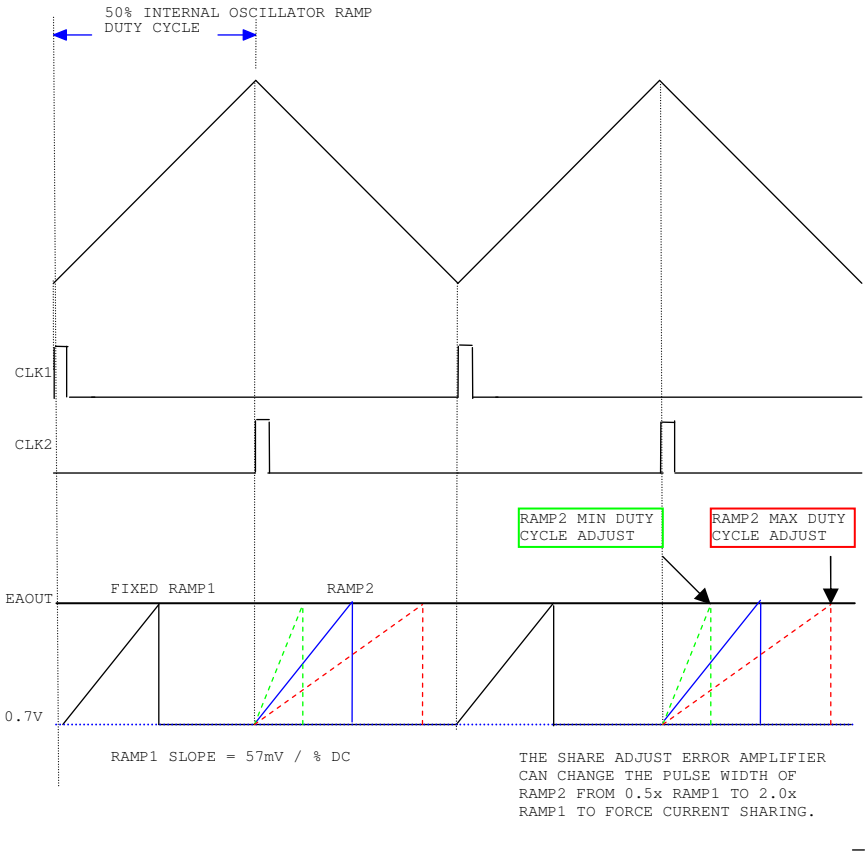


Figure 3 – 2 Phase Oscillator and PWM Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / Vout$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODY\ DIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / (Vout + V_{BODY\ DIODE})$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "body braking" and is accomplished through the "0% Duty Cycle Comparator". If the Error Amplifier's output voltage drops below 0.55V, this comparator turns off the low side gate driver.

Figure 4 depicts PWM operating waveforms under various conditions

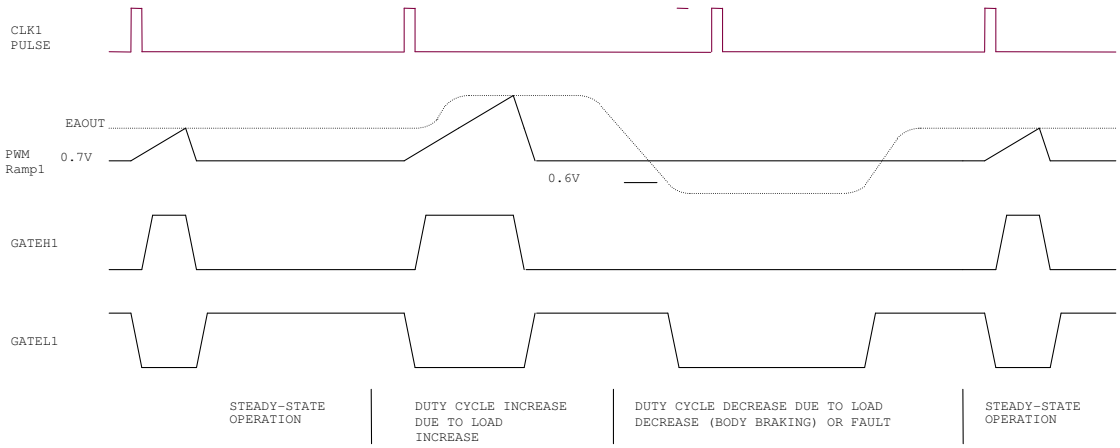


Figure 4 – PWM Operating Waveforms

Current Sense Amplifier

A high speed differential current sense amplifier is shown in Figure 5. Its gain decreases with increasing temperature and is nominally 24.5 at 25ºC and 20 at 125ºC (-1400 ppm/ºC). This reduction of gain tends to compensate the 3850 ppm/ºC increase in inductor DCR. Since in most designs the IC junction is hotter than the inductors these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 75mV and negative up to -20mV before clipping. The output of the current sense amplifier is summed with the DAC voltage which is used for over current protection, voltage positioning and current sharing.

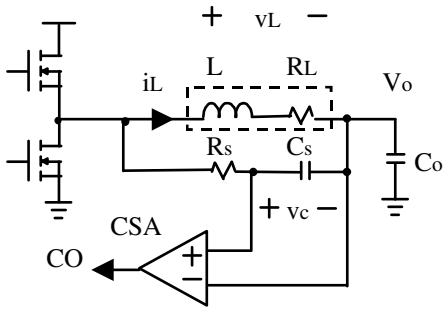


Figure 5 – Inductor Current Sensing and Current Sense Amplifier

VCC Under Voltage Lockout (UVLO)

The VCC UVLO function monitors the VCC supply pin and ensures enough voltage is available to power the internal circuitry. During power-up the fault latch is reset when VCC exceeds 7.8V and all other faults are cleared. The fault latch is set when VCC drops below 7.3V, resulting in 500mV of nominal VCC hysteresis for powering up into a load.

5VUVL Under Voltage Lockout (5VUVL)

The 5VUVL function is provided for converters using a separate voltage supply other than VCC for gate driver bias. The 5VUVL comparator prevents operation by discharging SS/DEL and forcing EAOUT low. The 5VUVL comparator has an OK threshold of 4.3V ensuring adequate gate drive voltage is present and a fault threshold of 4.125V.

Power Good Output

The PWRGD pin is an open-collector output and should be pulled up to a voltage source through a resistor. During soft start, the PWRGD remains low until the output voltage is in regulation and SS/DEL is above 3.75V. The PWRGD pin becomes low if the fault latch is set. A high level at the PWRGD pin indicates that the converter is in operation and has no fault, but does not ensure the output voltage is within the specification. Output voltage regulation within the design limits can logically be assured however, assuming no component failure in the system.

Tri-State Gate Drivers

The gate drivers can deliver over 3.5A peak current. An adaptive non-overlap circuit monitors the voltage on the GATEHX and GATELX pins to prevent MOSFET shoot-through current while minimizing body diode conduction.

The Error Amplifier output of the Control IC drives low in response to any fault condition such as VCC input under voltage or output overload. The 0% duty cycle comparator detects this and drives both gate outputs low. This tri-state operation prevents negative inductor current and negative output voltage during power-down.

The Gate Drivers revert to a high impedance “off” state at VCCL and VCCHX supply voltages below the normal operating range. An 80kΩ resistor is connected across the GATEX and PGNDX pins to prevent the GATEX voltage from rising due to leakage or other cause under these conditions.

Over Voltage Protection (OVP)

The output Over-Voltage Protection comparator monitors the output voltage through the FB pin, the positive remote sense point. If FB exceeds VDAC plus 145mV (for VR10.X, 480mV for OPTERON and ATHLON, selected with the VID_SEL pin), both GATEL pins drive high and the OVP pin sources up to 10mA. The OVP circuit over-rides the normal PWM operation and will fully turn-on the low side MOSFET within approximately 150ns. The low side MOSFET will remain ON until the over-voltage condition ceases. The lower MOSFETs alone can not clamp the output voltage however an SCR or N-MOSFET could be triggered by the OVP pin to prevent processor damage.

Error Amplifier compensation can slow down the response to an OVP condition if the voltage loop is too slow, which is usually not the case. The FB pin can only respond to an over-voltage condition once the EAOUT voltage has reached its minimum. Until then, the FB pin is modified by the falling EAOUT voltage so FB is equal to VDAC. The Error Amplifier compensation slew current generates a voltage across the RFB resistor that will mask the output voltage OVP condition. Again, for a typical fast voltage loop compensation scheme, a fairly large resistor is placed in series with the EAOUT to FB compensation capacitor to speed up the loop which results in no noticeable OVP sensing delay.

The overall system must be considered when designing for OVP. In many cases the over-current protection of the AC-DC or DC-DC converter supplying the multiphase converter will be triggered thus providing effective protection without damage as long as all PCB traces and components are sized to handle the worst-case maximum current. If this is not possible, a fuse can be added in the input supply to the multiphase converter. One scenario to be careful of is where the input voltage to the multiphase converter may be pulled below the level where the ICs can provide adequate voltage to the low side MOSFET thus defeating OVP.

A Body Braking™ Disable Comparator has been included to prevent false OVP firing during dynamic VID down changes. The BB DISABLE Comparator disables Body Braking™ when FB exceeds VDAC by 80mV. The low side MOSFETs will then be controlled to keep V(FB) and V(VOUT) within 80mV of V(VDAC), below the 150mV INTEL OVP trip point.

APPLICATIONS INFORMATION

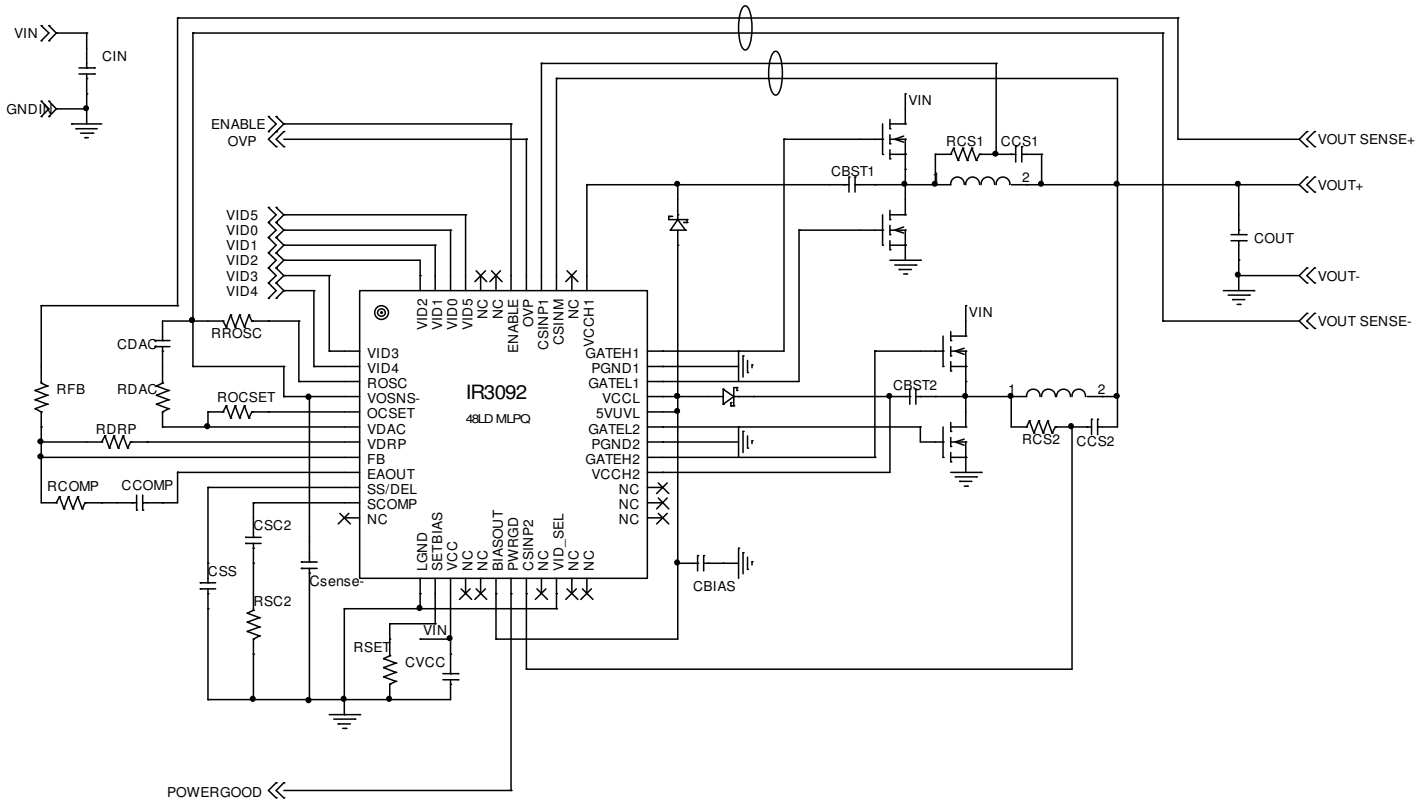


Figure 6 – System Diagram

VID Control

The IR3092 provides three different microprocessor solutions. The VID_SEL pin selects the appropriate Digital-to-Analog Converters (DAC), VID threshold voltages, and Over Voltage Protection (OVP) threshold for VR10.X, OPTERON, or ATHLON solutions. AMD VID codes are shown in Table 1; Intel VID codes are found in Table 2. The DAC output voltage is available at the VDAC pin. A detailed block diagram of the VID control circuitry can be found in Figure 7. The VID pins are internally pulled up to 4.9V by 18uA current sources. The VID input comparators have a 0.6V threshold for VR10.X or 1.5V threshold for OPTERON and ATHLON. The selected DAC voltage is provided at the Error Amplifier positive input and to the VDAC pin by the trans-conductance DAC Buffer.

The VDAC voltage is trimmed to the Error Amplifier output voltage with EAOUT tied to FB via an accurate resistor. This compensates DAC Buffer input offset, Error Amplifier input offset, and errors in the generation of the FB bias current which is based on R_{ROSC}. This trim method provides 0.5% system accuracy.

The IR3092 can accept changes in the VID code while operating and vary the VDAC voltage accordingly. The IC detects a VID change and blanks the DAC output response for 400ns to verify the new code is valid and not due to skew or noise. The sink/source capability of the VDAC buffer amp is programmed by the same external resistor that sets the oscillator frequency, R_{ROSC}. The slew rate of the voltage at the VDAC pin can be adjusted by an external capacitor between VDAC pin and the VOSNS- pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifier. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

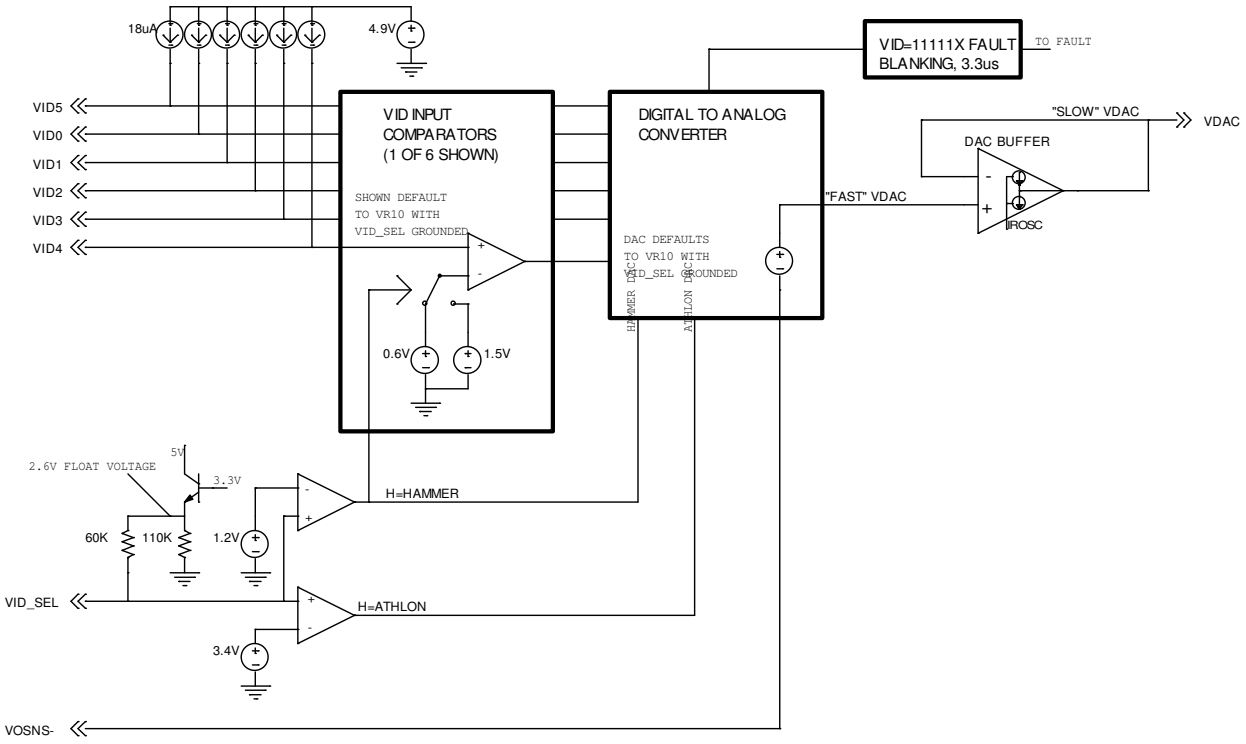


Figure 7– VID Control Block Diagram

VID = 11111X Fault

VID codes of 111111 and 111110 will set the fault latch and disable the Error Amplifier.

Slew Rate Programming Capacitor C_{DAC} and Resistor R_{DAC}

VDAC sink current I_{SINK} and source current I_{SOURCE} are determined by R_{ROSC}, and their value can be found using the curve in the Typical Operating Characteristics. The slew rate of VDAC down-slope SR_{DOWN} can be programmed by the external capacitor C_{DAC} as defined in Equation (1) and shown in Figure 6. Resistor R_{DAC} is used to compensate VDAC circuit and is determined by Equation (2). The slew rate of VDAC up-slope SR_{UP} is proportional to the down-slope slew rate SR_{DOWN} and is given by Equation (3).

$$C_{DAC} = \frac{I_{SINK}}{SR_{DOWN}} \qquad (1)$$

$$R_{DAC} = 0.5 + \frac{3.2 * 10^{-15}}{C_{DAC}^{\ 2}} \qquad (2)$$

$$SR_{UP} = \frac{I_{SOURCE}}{C_{DAC}} \qquad (3)$$

Table 1A. AMD OPTERON VID

VID_SEL Open. V(VDAC) is pre-positioned 50mV higher than Vout values listed below for load positioning.

Vout is measured at EAOUT with ROSC=42K and a 1690 ohm resistor connecting FB to EAOUT to cancel the 50mV pre-position offset.

VID4	VID3	VID2	VID1	VID0	Vout (V)
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	OFF[4]

Table 1B. AMD ATHLON VID

VIDSEL to VCC. V(VDAC) is pre-positioned 50mV higher than Vout values listed below for load positioning.

Vout is measured at EAOUT with ROSC=42K and a 1690 ohm resistor connecting FB to EAOUT to cancel the 50mV pre-position offset.

VID4	VID3	VID2	VID1	VID0	Vout (V)
0	0	0	0	0	1.850
0	0	0	0	1	1.825
0	0	0	1	0	1.800
0	0	0	1	1	1.775
0	0	1	0	0	1.750
0	0	1	0	1	1.725
0	0	1	1	0	1.700
0	0	1	1	1	1.675
0	1	0	0	0	1.650
0	1	0	0	1	1.625
0	1	0	1	0	1.600
0	1	0	1	1	1.575
0	1	1	0	0	1.550
0	1	1	0	1	1.525
0	1	1	1	0	1.500
0	1	1	1	1	1.475
1	0	0	0	0	1.450
1	0	0	0	1	1.425
1	0	0	1	0	1.400
1	0	0	1	1	1.375
1	0	1	0	0	1.350
1	0	1	0	1	1.325
1	0	1	1	0	1.300
1	0	1	1	1	1.275
1	1	0	0	0	1.250
1	1	0	0	1	1.225
1	1	0	1	0	1.200
1	1	0	1	1	1.175
1	1	1	0	0	1.150
1	1	1	0	1	1.125
1	1	1	1	0	1.100
1	1	1	1	1	OFF[4]

Note: 4 Output disabled (Fault mode)

Table 2. Intel VR10.X VID (VID_SEL Grounded, measured at EAOUT=FB.)

Processor Pins (0 = low, 1 = high)						Vout (V)	Processor Pins (0 = low, 1 = high)						Vout (V)
VID4	VID3	VID2	VID1	VID0	VID5		VID4	VID3	VID2	VID1	VID0	VID5	
0	1	0	1	0	0	0.8375	1	1	0	1	0	0	1.2125
0	1	0	0	1	1	0.8500	1	1	0	0	1	1	1.2250
0	1	0	0	1	0	0.8625	1	1	0	0	1	0	1.2375
0	1	0	0	0	1	0.8750	1	1	0	0	0	1	1.2500
0	1	0	0	0	0	0.8875	1	1	0	0	0	0	1.2625
0	0	1	1	1	1	0.9000	1	0	1	1	1	1	1.2750
0	0	1	1	1	0	0.9125	1	0	1	1	1	0	1.2875
0	0	1	1	0	1	0.9250	1	0	1	1	0	1	1.3000
0	0	1	1	0	0	0.9375	1	0	1	1	0	0	1.3125
0	0	1	0	1	1	0.9500	1	0	1	0	1	1	1.3250
0	0	1	0	1	0	0.9625	1	0	1	0	1	0	1.3375
0	0	1	0	0	1	0.9750	1	0	1	0	0	1	1.3500
0	0	1	0	0	0	0.9875	1	0	1	0	0	0	1.3625
0	0	0	1	1	1	1.0000	1	0	0	1	1	1	1.3750
0	0	0	1	1	0	1.0125	1	0	0	1	1	0	1.3875
0	0	0	1	0	1	1.0250	1	0	0	1	0	1	1.4000
0	0	0	1	0	0	1.0375	1	0	0	1	0	0	1.4125
0	0	0	0	1	1	1.0500	1	0	0	0	1	1	1.4250
0	0	0	0	1	0	1.0625	1	0	0	0	1	0	1.4375
0	0	0	0	0	1	1.0750	1	0	0	0	0	1	1.4500
0	0	0	0	0	0	1.0875	1	0	0	0	0	0	1.4625
1	1	1	1	1	1	OFF[4]	0	1	1	1	1	1	1.4750
1	1	1	1	1	0	OFF[4]	0	1	1	1	1	0	1.4875
1	1	1	1	0	1	1.1000	0	1	1	1	0	1	1.5000
1	1	1	1	0	0	1.1125	0	1	1	1	0	0	1.5125
1	1	1	0	1	1	1.1250	0	1	1	0	1	1	1.5250
1	1	1	0	1	0	1.1375	0	1	1	0	1	0	1.5375
1	1	1	0	0	1	1.1500	0	1	1	0	0	1	1.5500
1	1	1	0	0	0	1.1625	0	1	1	0	0	0	1.5625
1	1	0	1	1	1	1.1750	0	1	0	1	1	1	1.5750
1	1	0	1	1	0	1.1875	0	1	0	1	1	0	1.5875
1	1	0	1	0	1	1.2000	0	1	0	1	0	1	1.6000

Note: 4. Output disabled (Fault mode)

Oscillator Resistor R_{ROSC}

The oscillator frequency is programmable from 100kHz to 540kHZ with an external resistor R_{ROSC} as shown in Figure 6. The oscillator generates an internal 50% duty cycle saw tooth signal (Figure 4.) that is used to generate 180° out-of-phase timing pulses to set Phase 1 and 2 RS flip-flops. Once the switching frequency is chosen, R_{ROSC} can be determined from the curve in the I(SETBIAS) vs. Rosc curve in the Typical Operating Characteristics Section.

Soft Start, Over-Current Fault Delay, and Hiccup Mode

The IR3092 has a programmable soft-start function to limit the surge current during converter power-up. A capacitor connected between the SS/DEL and LGND pins controls soft start timing as well as over-current protection delay and hiccup mode timing.

Figure 8 depicts the various operating modes of the SS/DEL function. Under a no fault condition, the SS/DEL capacitor will charge. The SS/DEL charge soft-start duration is controlled by a 55uA charge current which charges CSS up to 4.0V. The Error Amplifier output is clamped low until SS/DEL reaches 1.3V. The Error Amplifier will then regulate the converter's output voltage to match the SS/DEL voltage less the 1.3V offset until it reaches the level determined by the VID inputs. The PWRGD signal is asserted once the SS/DEL voltage exceeds 3.75V.

VCC and 5VUVL Under Voltage Lock Outs, a VID=11111x fault, or low Enable pin immediately set the fault latch causing SS/DEL to begin discharging. The hiccup duration is controlled by a 5.5uA discharge current until the Discharge Comparator Threshold of 0.26V is reached. If the fault has cleared, the fault latch will reset allowing a normal soft-start to occur.

A delay is included if an over-current condition occurs after a successful soft start sequence. This is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions. If an over-current fault occurs during normal operation, the Over Current Comparator will initiate the discharge of the capacitor at SS/DEL but will not set the fault latch immediately. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 3.75V threshold of the delay comparator, the Fault latch will be set pulling the Error Amplifier's output low, inhibiting switching and de-asserting the PWRGD signal. An additional discharge current is introduced during an over current condition. The 5.5uA discharge current results in a long delay duration where SS/DEL discharges from its 4V peak to the 3.75V fault delay threshold. This potentially long over-current protection activation delay could result in potential power stage damage therefore an additional 45uA discharge current source assists the 5.5uA discharge current if an over current condition is occurring and the SS/DEL capacitor is above 3.75V. 30mV of hysteresis is included in the Delay Comparator to prevent PWRGD chatter when SS/DEL is at the delay threshold.

The SS/DEL capacitor will continue to discharge until it reaches 0.26V where the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle, the fault latch will be set without any delay and hiccup mode will begin. During hiccup mode the 10 to 1 charge to discharge ratio results in a 9% hiccup mode duty cycle regardless of at what point the over-current condition occurs.

The converter can be disabled if the SS/DEL pin is pulled below 0.9V.

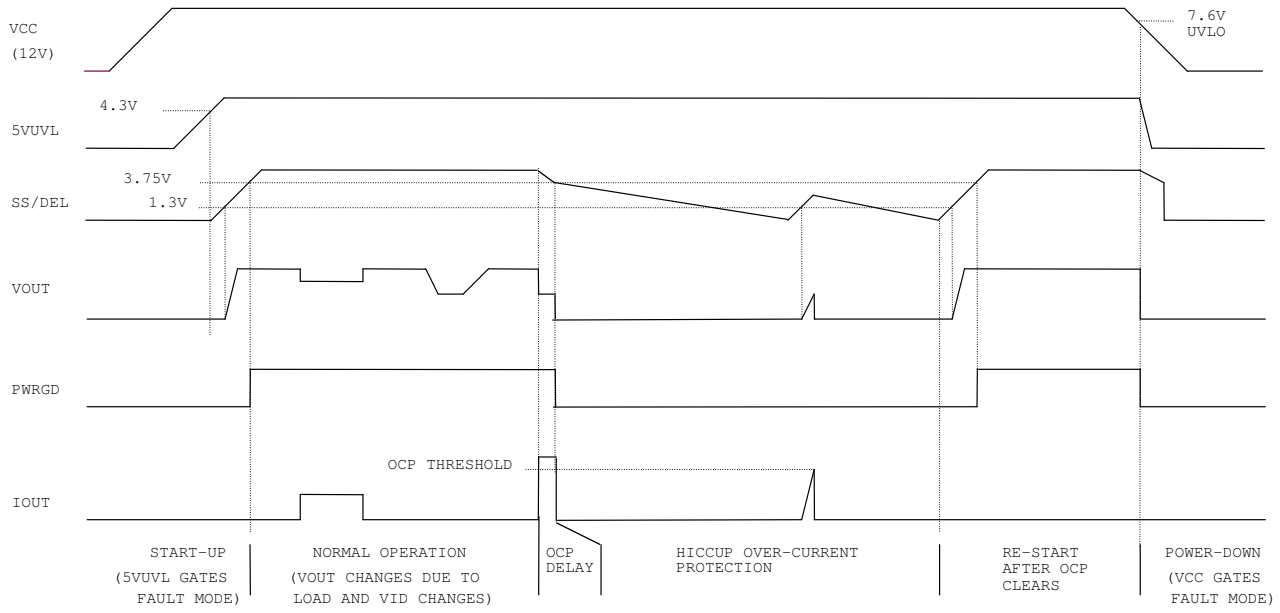


Figure 8 – Operating Waveforms

Soft-start delay time t_{SSDEL} is the time to charge SS/DEL up to 1.3V. After this the error amplifier output is released to allow the soft start. The soft start time t_{SS} represents the time during which converter voltage rises from zero to V_O. t_{SS} can be programmed by C_{SS} using equation (4).

$$C_{SS} = \frac{I_{CHG} * t_{SS}}{V_O} = \frac{55 * 10^{-6} * t_{SS}}{V_O} \qquad (4)$$

Once C_{SS} is chosen, the soft start delay time t_{SSDEL}, the over-current fault latch delay time t_{OCDEL}, and the delay time t_{VccPG} from output voltage (V_O) in regulation to Power Good are fixed and shown in equation (5), (6) and (7) respectively.

$$t_{SSDEL} = \frac{C_{SS} * \Delta V}{I_{CHG}} = \frac{C_{SS} * 1.3}{55 * 10^{-6}} \qquad (5)$$

$$t_{OCDEL} = \frac{C_{SS} * \Delta V}{I_{DISCHG}} = \frac{C_{SS} * 0.25}{50.5 * 10^{-6}} \qquad (6)$$

$$t_{VccPG} = \frac{C_{SS} * \Delta V}{I_{CHG}} = \frac{C_{SS} * (3.75 - V_O - 1.3)}{55 * 10^{-6}} \qquad (7)$$

Over Current Protection (OCP)

The current limit threshold is set by a resistor connected between the OCSET and VDAC pins. If the average Current Sense Amplifier output plus VDAC voltage exceeds the OCSET voltage, the over-current protection is triggered.

A delay is included if an over-current condition occurs after a successful soft-start sequence. This is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions. If an over-current fault occurs during normal operation, the Over Current Comparator will initiate the discharge of the capacitor at SS/DEL but will not set the fault latch immediately. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 250mV offset of the delay comparator, the Fault latch will be set pulling the Error Amplifier's output low inhibiting switching in the phase ICs and de-asserting the PWRGD signal. See Soft Start, Over-Current Fault Delay, and Hiccup Mode.

The inductor DC resistance R_L is utilized to sense the inductor current. I_{LIMIT} is the required over current limit. I_{OCSET}, the bias current of OCSET pin, is set by R_{ROSC} and is also determined by the curve in the Typical Operating Characteristics. R_{OCSET} is defined in the following Equation (8).

$$R_{OCSET} = \left(\frac{I_{LIMIT}}{2} + \frac{Vo * (Vin - Vo)}{2 * L * Vin * fsw}\right) * R_L * 23.5 / I_{OCSET} \qquad (8)$$

Adaptive Voltage Positioning

Adaptive voltage positioning is needed to reduce output voltage deviations during load transients and power dissipation of the load when it is drawing maximum current. The circuitry related to voltage positioning is shown in Figure 9. Resistor R_{FB} is connected between the Error Amplifier's inverting input pin FB and the converter's output voltage. An internal current source whose value is programmed by the same external resistor that programs the oscillator frequency, R_{ROSC}, pumps current out of the FB pin. The FB bias current develops a positioning voltage drop across R_{FB} which forces the converter's output voltage lower to V(VDAC)-I(FB)* R_{FB} to maintain a balance at the Error Amplifier inputs. R_{FB} is selected to program the desired amount of fixed offset voltage below the DAC voltage.

The voltage at the VDRP pin is an average of both phase Current Sense Amplifiers and represents the sum of the VDAC voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the resistor. The Error Amplifier forces the voltage on the FB pin to equal VDAC through the power supply loop therefore the current through RDRP is equal to (VDRP-VDAC) / R_{DRP}. As the load current increases, the VDRP voltage increases accordingly which results in an increase R_{FB} current, further positioning the output regulated voltage lower thus making the output voltage reduction proportional to an increase in load current. The droop impedance or output impedance of the converter can thus be programmed by the resistor R_{DRP}. The offset and slope of the converter output impedance are independent of the VDAC voltage.

AMD specifies the acceptable power supply regulation window as ±50mV around their specified VID tables. VR10.X specifies the VID table voltages as the absolute maximum power supply voltage. In order to have all three DAC options, the OPTERON and ATHLON DAC output voltages are pre-positioned 50mV higher than listed in AMD specs. During testing, a series resistor is placed between EAOUT and FB to cancel the additional 50mV out of the DAC. The FB bias current, equal to IROSC, develops the 50mV cancellation voltage. Trimming the VDAC voltage by monitoring V(EAOUT) with this 50mV cancellation resistor in circuit also trims out errors in the FB bias current.

The VDRP pin voltage represents the average current of the converter plus the DAC voltage. The load current can be retrieved by subtracting the VDAC voltage from the VDRP voltage.

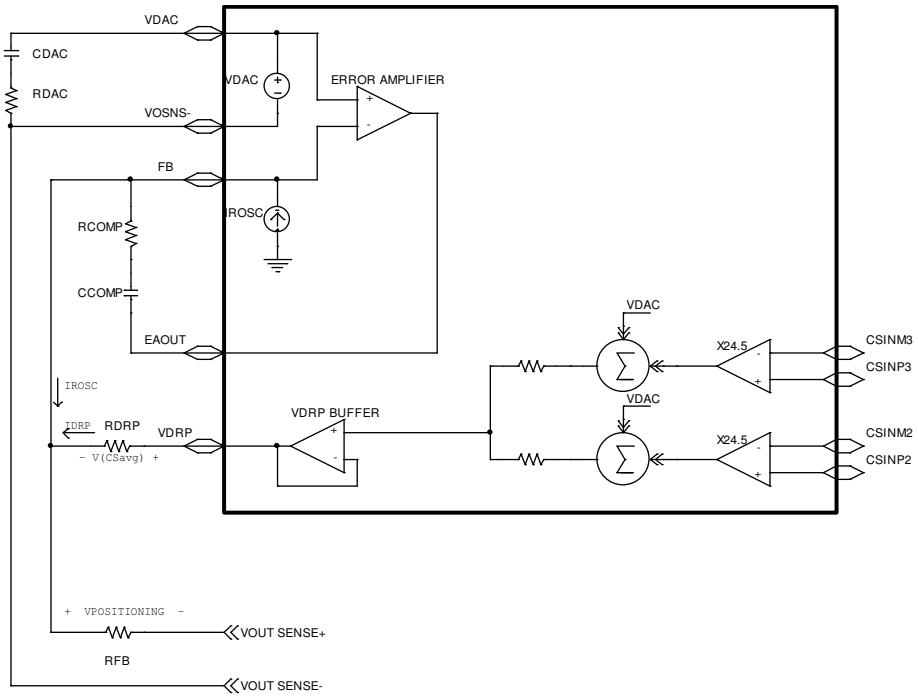


Figure 9 - Adaptive voltage positioning

A resistor R_{FB} between FB pin and the converter output is used to create output voltage offset V_{O_NLOFST} which is the difference between V_{DAC} voltage and output voltage at no load condition. An internal current source whose value is programmed by the same external resistor that programs the oscillator frequency, R_{ROSC}, pumps current I_{ROSC} out of the FB pin.

The voltage at the VDRP pin is an average of both phase Current Sense Amplifiers and represents the sum of the VDAC voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the Adaptive Voltage Positioning Resistor R_{DRP}. Adaptive voltage positioning lowers the converter voltage by $R_O * I_O$, where R_O is the required output impedance of the converter. R_{FB} and R_{DRP} are determined by (9) and (10) respectively, where R_O is the required output impedance of the converter.

$$R_{FB} = \frac{V_{O\_NLOFST}}{I_{ROSC}} \qquad (9)$$

$$R_{DRP} = \frac{R_{FB} * R_L * 23.5}{2 * R_O} \qquad (10)$$

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_SC_S} = i_L(s)\frac{R_L+sL}{1+sR_SC_S}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR. If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor R_{CS} and capacitor C_{CS} in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor C_{CS} represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but affects the AC component of the inductor current as well as the output voltage during the load current transient if adaptive voltage positioning is adopted.

Measure the inductance L and the inductor DC resistance RL. Pre-select the capacitor CCS and calculate RCS as follows.

$$R_{CS} = \frac{L/R_L}{C_{CS}} \qquad (11)$$

The bias current flowing out of the non-inverting input of the current sense amplifier creates a voltage drop across RCS, which is equivalent to an input offset voltage of the current sense amplifier. The offset affects the accuracy of converter current signal ISHARE as well as the accuracy of the converter output voltage if adaptive voltage positioning is adopted. To reduce the offset voltage, a resistor RCSO should be added between the amplifier inverting input and the converter output, as shown in Fig1. The resistor RCSO is determined by the ratio of the bias current from the non-inverting input and the bias current from the inverting input.

$$R_{CSO} = \frac{I_{CSIN+}}{I_{CSIN-}} * R_{CS} \qquad (12)$$

If RCSO is not used, RCS should be chosen so that the offset voltage is small enough. Usually RCS should be less than 2 kΩ and therefore a larger CCS value is needed.

Inductor DCR Temperature Correction

If the Current Sense Amplifier temperature dependent gain is not adequate to compensate the inductor DCR TC, a negative temperature coefficient (NTC) thermistor can be added. The thermistor should be placed close to the inductor and connected in parallel with the feedback resistor, as shown in Figure 10. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

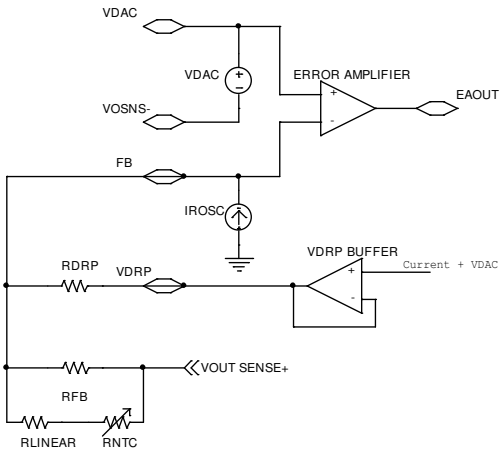


Figure 10- Temperature compensation of inductor DCR

Remote Voltage Sensing

To compensate for impedance in the ground plane, the VOSNS- pin is used for remote sensing and connects directly to the load. The VDAC voltage is referenced to VOSNS- to avoid additional error terms or delay related to a separate differential amplifier. The capacitor connecting the VDAC and VOSNS- pins ensure that high speed transients are fed directly into the Error Amplifier without delay.

Master-Slave Current Share Loop

Current sharing between phases of the converter is achieved by a Master-Slave current share loop topology. The output of the Phase 1 Current Sense Amplifier sets the reference for the Share Adjust Error Amplifier. The Share Adjust Error Amplifier will then adjust the duty cycle of PWM Ramp2 to force its input error to zero, resulting in accurate current sharing.

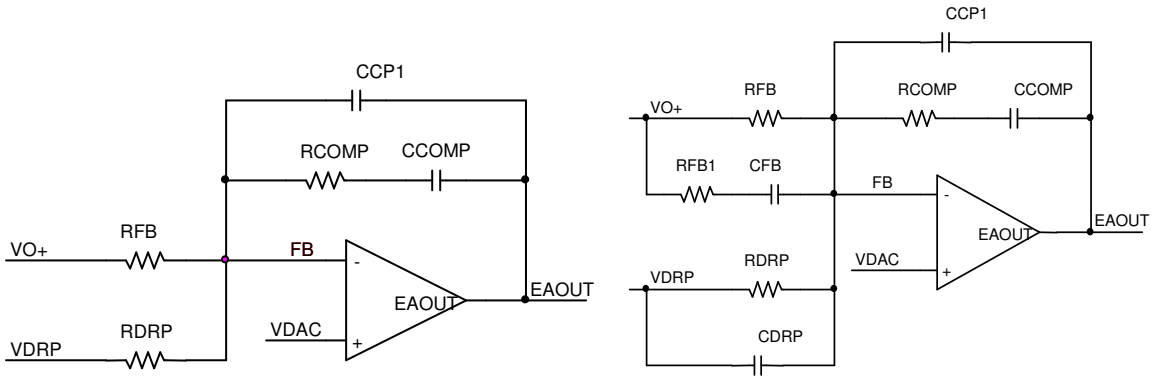
The maximum and minimum duty cycle adjust range of Ramp2 compared to Ramp1 has been limited to 0.5x and 2.0x of the master's ramp (see Figure 3.). The crossover frequency of the current share loop can be programmed with a capacitor at the SCOMP pin so that the share loop does not interact with the output voltage loop. A 22nF capacitor from SCOMP to LGND is good for most of the applications. If necessary have a 1k resistor in series with the Csc to make the current loop a little bit faster.

The SCOMP capacitor is driven by a trans-conductance stage capable of sourcing and sinking 25uA. The duty cycle of Ramp2 inversely tracks the voltage on the SCOMP pin; if V(SCOMP) increases, Ramp2's slope will increase and the effective duty cycle will decrease resulting in a reduction in Phase 2's output current. Due to the limited 25uA source current, an SCOMP pre-charge circuit has been included to pre-condition V(SCOMP) so that the duty cycle of Ramp2 is equal to Ramp1 prior to any GATEHX high pulses. The pre-condition circuit can source 400uA. The Equal Duty Cycle Comparator (see Block Diagram) activates a pre-charge circuit when SS/DEL is less than 0.7V. The Error Amplifier becomes active enabling GATEH switching when SS/DEL is above 1.3V.

Compensation of Voltage Loop

The adaptive voltage positioning is used in the computer applications to meet the load line requirements. Like current mode control, the adaptive voltage positioning loop introduces extra zero to the voltage loop and splits the double poles of the power stage, which make the voltage loop compensation much easier.

Resistors R_{FB} and R_{DRP} are chosen according to Equations (9) and (10), and the selection of compensation types depends on the capacitors used. For the applications using Electrolytic, Polymer or AL-Polymer capacitors, type II compensation shown in Figure 11 (a) is usually enough. While for the applications with only low ESR ceramic capacitors, type III compensation shown in Figure 11 (b) is preferred.



(a) Type II compensation (b) Type III compensation

Figure11 . Voltage loop compensation network

Type II Compensation

Determine the compensation at no load, the worst case condition. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, the crossover frequency of the voltage loop can be estimated by Equations (13), where C_E and R_{CE} are the equivalent capacitance and ESR of output capacitors respectively and R_{LE} is the equivalent resistance of inductor DCR.

$$f_C = \frac{R_{DRP}}{2\pi * C_E * (G_{CS} * R_{FB} * R_{LE} - R_{CE})} \qquad (13)$$

RCOMP and CCOMP have limited effect on the crossover frequency, and are used only to fine tune the crossover frequency and transient load response. Choose the desired crossover frequency fc1 around fc estimated by Equation (13) and determine RCOMP and CCOMP.

$$R_{COMP} = \frac{(2\pi * f_{C1})^2 * L_E * C_E * R_{FB}}{V_{IN} * F_M} \quad (14)$$

$$C_{COMP} = \frac{10 * \sqrt{L_E * C_E}}{R_{COMP}} \quad (15)$$

CCP1 is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough. In equation (14), VIN is the input voltage, FM is the PWM comparator gain (refer to equation (22)).

Type III Compensation

Determine the compensation at no load, the worst case condition. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, the crossover frequency of the voltage loop can be estimated by Equations (16).

$$f_C = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} \quad (16)$$

Choose the desired crossover frequency fc1 around fc estimated by Equation (16). Select other components to ensure the slope of close loop gain is -20dB/Dec around the crossover frequency. Choose resistor RFB1 according to Equation (17), and determine CFB and CDRP from Equations (18) and (19).

$$R_{FB1} = \frac{1}{2} R_{FB} \quad \text{to} \quad R_{FB1} = \frac{2}{3} R_{FB} \quad (17)$$

$$C_{FB} = \frac{1}{4\pi * f_{C1} * R_{FB1}} \quad (18)$$

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} \quad (19)$$

RCOMP and CCOMP have limited effect on the crossover frequency, and are used only to fine tune the crossover frequency and transient load response. Determine RCOMP and CCOMP from Equations (20) and (21), where FM is the PWM comparator gain defined by Equation (22).

$$R_{COMP} = \frac{(2\pi * f_{C1})^2 * L_E * C_E * R_{FB}}{V_I * F_M} \quad (20)$$

$$C_{COMP} = \frac{10 * \sqrt{L_E * C_E}}{R_{COMP}} \quad (21)$$