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FEATURES

- Single 5V to 21V application
- Wide Input Voltage Range from 1.5V to 21V with external Vcc
- Output Voltage Range: 0.6V to 0.86*PVin
- 0.5% accurate Reference Voltage
- Enhanced line/load regulation with Feed-Forward
- Programmable Switching Frequency up to 1.5MHz
- Internal Digital Soft-Start
- Enable input with Voltage Monitoring Capability
- Remote Sense Amplifier with True Differential Voltage Sensing
- Thermally compensated current limit and Hiccup Mode Over Current Protection
- Smart LDO to enhance efficiency
- External synchronization with Smooth Clocking
- Dedicated output voltage sensing for power good indication and overvoltage protection which remains active even when Enable is low.
- Enhanced Pre-Bias Start up
- Body Braking to improve transient
- Integrated MOSFET drivers and Bootstrap diode
- Thermal Shut Down
- Post Package trimmed rising edge dead-time
- Programmable Power Good Output
- Small Size 5mm x 6mm PQFN
- Operating Junction Temp: -40°C<Tj<125°C
- Lead-free, Halogen-free, and RoHS Compliant

DESCRIPTION

The IR3448 SupIRBuck® is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard PWM controller and MOSFETs make IR3448 a space-efficient solution, providing accurate power delivery for low output voltage and high current applications.

IR3448 is a versatile regulator which offers programmability of switching frequency and current limit while operating in wide input and output voltage range.

The switching frequency is programmable from 300 kHz to 1.5MHz for an optimum solution.

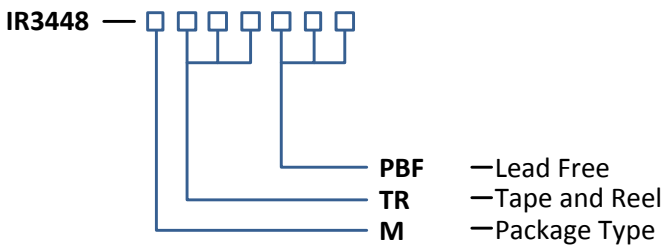
It also features important protection functions, such as Over Voltage Protection (OVP), Pre-Bias startup, hiccup current limit and thermal shutdown to give required system level security in the event of fault conditions.

APPLICATIONS

- Server Application
- Distributed Point of Load Power Architectures
- Set Top Box Application
- Power Supplies

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR3448	PQFN 5mm x 6mm	Tape and Reel	4000	IR3448MTRPBF



BASIC APPLICATION

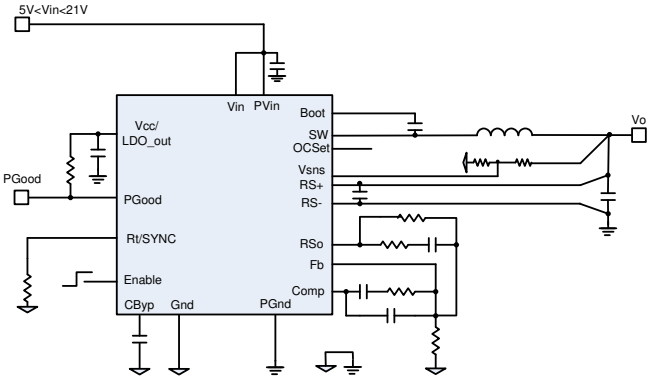


Figure 1: IR3448 Basic Application Circuit

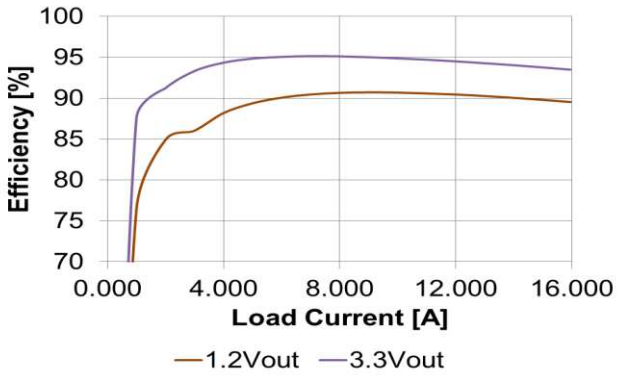
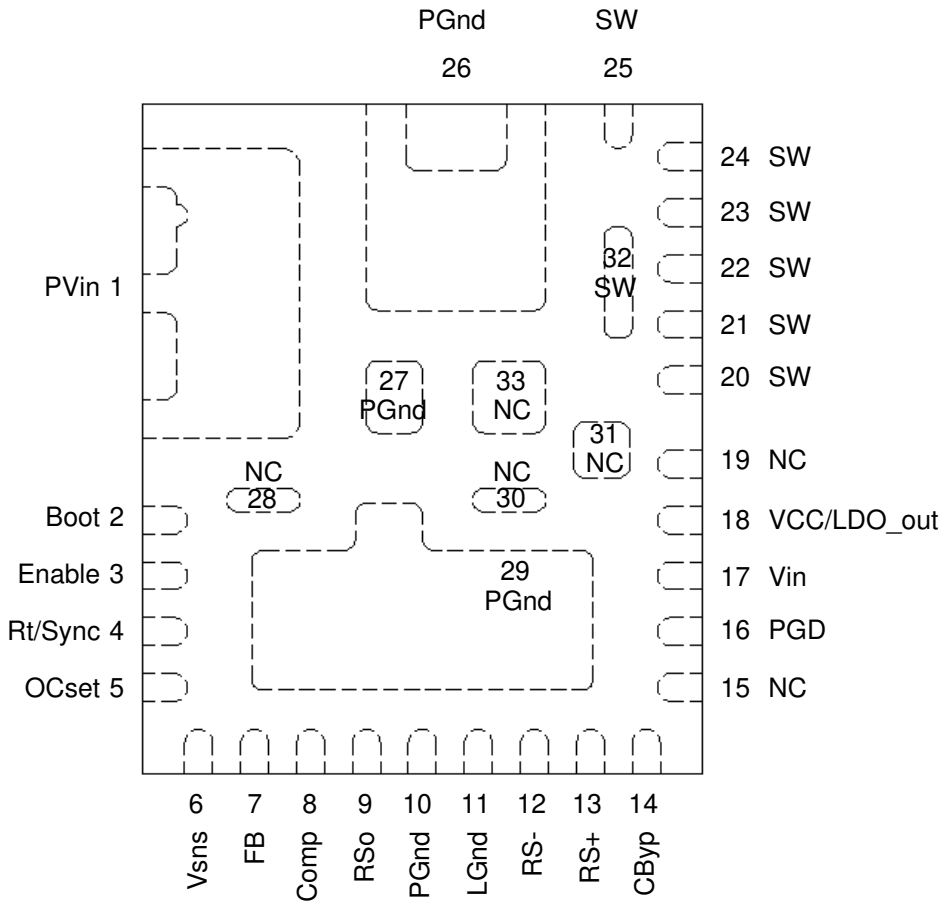


Figure 2: Efficiency [Vin=12V, Fsw=600kHz]

PIN DIAGRAM

5mm X 6mm POWER QFN
Top View



FUNCTIONAL BLOCK DIAGRAM

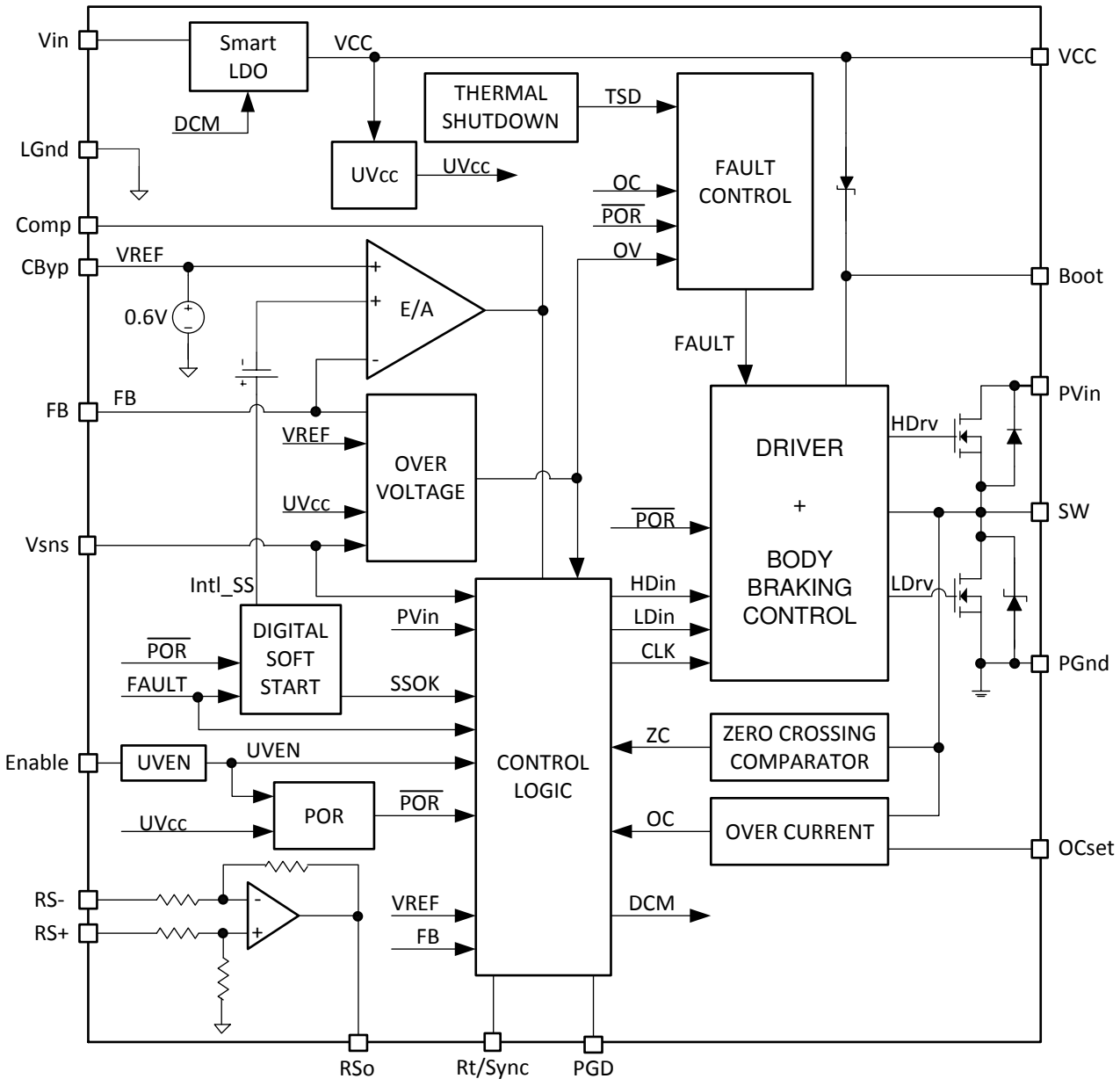


Figure 3: IR3448 Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	PVin	Input voltage for power stage. Bypass capacitors between PVin and PGND should be connected very close to this pin and PGND; also forms input to feedforward block
2	Boot	Supply voltage for high side driver
3	Enable	Enable pin to turning on and off the IC.
4	Rt/Sync	Use an external resistor from this pin to LGND to set the switching frequency, very close to the pin. This pin can also be used for external synchronization.
5	OCset	Current Limit setpoint. This pin allows the trip point to be set to one of three possible settings by either floating this pin, tying it to VCC or tying it to PGnd.
6	Vsns	Sense pin for OVP and PGood
7	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator or to the output of the remote sense amplifier, via resistor divider to set the output voltage and provide feedback to the error amplifier.
8	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to FB to provide loop compensation.
9	RSo	Remote Sense Amplifier Output
10, 26, 27, 29	PGND	Power ground. This pin should be connected to the system's power ground plane. Bypass capacitors between PVin and PGND should be connected very close to PVIN pin (pin 1) and this pin.
11	LGND	Signal ground for internal reference and control circuitry.
12	RS-	Remote Sense Amplifier input. Connect to ground at the load.
13	RS+	Remote Sense Amplifier input. Connect to output at the load.
14	Cbyp	Bypassing capacitor for internal reference voltage. A capacitor between 100pF and 180pF should be connected between this pin and LGnd.
15, 19, 28, 30, 31, 33	NC	No connection.
16	PGD	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to VCC.
17	Vin	Input Voltage for LDO.
18	VCC/LDO_out	Bias Voltage for IC and driver section, output of LDO. Add a minimum of 4.7uF bypass cap from this pin to PGnd.
20, 21, 22, 23, 24, 25, 32	SW	Switch node. This pin is connected to the output inductor.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin		-0.3V to 25V
Vin		-0.3V to 25V
VCC		-0.3V to 8V (Note 1)
SW		-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
BOOT		-0.3V to 33V
BOOT to SW		-0.3V to VCC + 0.3V (Note 2)
Input/Output pins		-0.3V to 3.9V
RS+, RS-, RSo, PGD, Enable, OCset		-0.3V to 8V (Note 1)
PGND to LGND, RS- to LGND		-0.3V to + 0.3V
Junction Temperature Range		-40°C to 150°C
Storage Temperature Range		-55°C to 150°C
ESD	Machine Model	Class A
	Human Body Model	Class 1C
	Charged Device Model	Class III
Moisture Sensitivity level		JEDEC Level 2 @ 260°C
RoHS Compliant		Yes

Note:

1. VCC must not exceed 7.5V for Junction Temperature between -10°C and -40°C.
2. Must not exceed 8V.

THERMAL INFORMATION	
Thermal Resistance, Junction to Case Top (θ_{JC_TOP})	32 °C/W
Thermal Resistance, Junction to PCB (pin 29) (θ_{JB})	2.98 °C/W
Thermal Resistance, Junction to Ambient (θ_{JA}) (Note 3)	15.4 °C/W

Note:

3. Thermal resistance (θ_{JA}) is measured with components mounted on a high effective thermal conductivity test board.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DEFINITION	MIN	MAX	UNITS
PVin	Input Bus Voltage *	1.5	21	V
Vin	Supply Voltage	5.0	21	
VCC	Supply Voltage **	4.5	7.5	
Boot to SW	Supply Voltage	4.5	7.5	
V_O	Output Voltage	0.6	0.86 * PVin	
I_O	Output Current	0	±16	A
Fs	Switching Frequency	300	1500	kHz
T_J	Junction Temperature	-40	125	°C

* SW node must not exceed 25V

** When VCC is connected to an externally regulated supply, also connect Vin.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specification apply over, 1.5V < PVin < 21V, 4.5V< VCC < 7.5V, 0°C < T_J < 125°C.
Typical values are specified at T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Loss						
Power Loss	P_{LOSS}	V_{in} = PV_{in} = 12V, V_O = 1.2V, I_O = 16A, Fs = 600kHz, L=0.400uH, T_A = 25°C, Note 4		1.94		W
MOSFET $R_{ds(on)}$						
Top Switch	Rds(on)_Top	V_{Boot} – V_{SW} = 6.8V, I_D = 16A, Tj = 25°C		6.6	8.5	mΩ
Bottom Switch	Rds(on)_Bot	VCC =6.8V, I_D = 16A, Tj = 25°C		2.2	2.9	
Reference Voltage						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		0°C < Tj < 105°C	-0.5		+0.5	%
		-40°C < Tj < 125°C	-1		+1	
Supply Current						
V_{in} Supply Current (Standby)	$I_{in(Standby)}$	Vin=21V, Enable low, No Switching		300	425	µA
V_{in} Supply Current (Dyn)	$I_{in(Dyn)}$	Vin=21V, Enable high, Fs = 600kHz			40	mA
VCC Supply Current (Standby)	$I_{cc(Standby)}$	Enable low, VCC=7V, No Switching		300	425	µA
VCC Supply Current	$I_{cc(Dyn)}$	Enable high, VCC=7V, Fs =			40	mA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
(Dyn)		600kHz				
Under Voltage Lockout						
VCC–Start–Threshold	VCC_UVLO_Start	VCC Rising Trip Level	4.0	4.2	4.4	V
VCC–Stop–Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	3.8	3.9	4.2	
Enable–Start–Threshold	Enable_UVLO_Start	Supply ramping up	1.14	1.2	1.36	V
Enable–Stop–Threshold	Enable_UVLO_Stop	Supply ramping down	0.9	1.0	1.06	
Enable leakage current	Ien	Enable=3.3V			1	µA
Oscillator						
Rt Voltage				1		V
Frequency Range	F_S	Rt=80.6k	270	300	330	kHz
		Rt=39.2k	540	600	660	
		Rt=15k	1350	1500	1650	
Ramp Amplitude	Vramp	PVin=6.8V, PVin(max) slew rate=1V/us Note 4		1.02		Vp-p
		PVin=12V, PVin(max) slew rate=1V/us Note 4		1.8		
		PVin=16V, PVin(max) slew rate=1V/us Note 4		2.4		
Ramp Offset	Ramp (os)	Note 4		0.16		V
Min Pulse Width	Tmin (ctrl)	Note 4			50	ns
Fixed Off Time		Note 4		200	230	ns
Max Duty Cycle	Dmax	Fs=300kHz, PVin=Vin=12V	86			%
Sync Frequency Range		Note 4	270		1650	kHz
Sync Pulse Duration			100	200		ns
Sync Level Threshold	High		3			V
	Low				0.6	
Error Amplifier						
Input Offset Voltage	Vos_Cbyp	VFb – VREF, VREF = 0.6V	-1.5		+1.5	%
Input Bias Current	IFb(E/A)		-0.5		+0.5	µA
Sink Current	Isink(E/A)		0.4	0.85	1.2	mA
Source Current	Isource(E/A)		4	7.5	11	mA
Slew Rate	SR	Note 4	7	12	20	V / µs
Gain-Bandwidth Product	GBWP	Note 4	20	30	40	MHz
DC Gain	Gain	Note 4	100	110	120	dB
Maximum Output Voltage	Vmax(E/A)		1.7	2	2.3	V
Minimum Output Voltage	Vmin(E/A)				100	mV
Common Mode Voltage	Vcm_Vp	Note 4	0		1.2	V
Remote Sense Differential Amplifier						
Unity Gain Bandwidth	BW_RS	Note 4	3	6.4	9	MHz
DC Gain	Gain_RS	Note 4		110		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Offset Voltage	Offset_RS	VREF=0.6V, 0°C < Tj < 85°C	-1.5	0	1.5	mV
		VREF=0.6V, -40°C < Tj < 125°C	-2		2	mV
Source Current	Isource_RS		3	13	20	mA
Sink Current	Isink_RS		0.4	1	2	mA
Slew Rate	Slew_RS	Note 4, Cload = 100pF	2	4	8	V / µs
RS+ input impedance	Rin_RS+		45	63	85	kohm
RS- input impedance	Rin_RS-	Note 4		63		kohm
Maximum Voltage	Vmax_RS	V(VCC) – V(RSo)	0.5	1	1.5	V
Minimum Voltage	Min_RS			50		mV
Internal Digital Soft Start						
Soft Start Clock	Clk_SS	Note 4	180	200	220	kHz
Soft Start Ramp Rate	Ramp(SS_Start)	Note 4	0.3	0.4	0.5	mV / µs
Bootstrap Diode						
Forward Voltage		I(Boot) = 30mA	360	520	960	mV
Switch Node						
SW Leakage Current	Isw	SW = 0V, Enable = 0V			1	µA
Internal Regulator (VCC/LDO)						
Output Voltage	VCC	Vin(min) = 7.2V, Io=0-30mA, Cload = 2.2uF, DCM=0	6.3	6.8	7.1	V
		Vin(min) = 7.2V, Io=0-30mA, Cload = 2.2uF, DCM=1	4	4.4	4.8	
VCC dropout	VCC_drop	Vin = 7V, Io=70 mA, Cload = 2.2uF			0.7	V
Short Circuit Current	Ishort	Note 4		70		mA
Zero-crossing Comparator Delay	Tdly_zc			256 / Fs		s
Zero-crossing Comparator Offset	Vos_zc	Note 4		0		mV
Body Braking						
BB Threshold	BB_threshold	Fb > Vref, Sw duty cycle, Note 3		0		%
FAULTS						
Power Good						
Power Good low upper threshold	VPG_low(upper)	Vsns Rising	115	120	125	% VREF
Power Good low Upper Threshold Falling delay	VPG_low(upper)_Dly	Vsns > VPG_low(upper)	1.5	2.5	3.5	µs
Power Good high lower threshold	VPG_high(lower)	Vsns Rising		95		% VREF
Power Good high Lower Threshold Rising Delay	VPG_high(lower)_Dly	Vsns rising		1.28		ms
Power Good low lower	VPG_low(lower)	Vsns falling		90		%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
threshold						VREF
Power Good low lower Threshold Falling delay	VPG_low(lower)_Dly	Vsns < VPG_low(lower)	101	150	199	µs
PGood Voltage Low	PG (voltage)	I_{PGood} = -5mA			0.5	V
Over Voltage Protection (OVP)						
OVP Trip Threshold	OVP (trip)	Vsns Rising	115	120	125	% VREF
OVP Fault Prop Delay	OVP (delay)	Vsns rising	1.5	2.5	3.5	µs
Over-Current Protection						
OC Trip Current	I_{TRIP}	OCSet=VCC, VCC = 6.8V, TJ = 25°C	18.9	21	23.1	A
		OCSet=floating, VCC = 6.8V, TJ = 25°C	14.8	16.5	18.2	A
		OCSet=PGnd, VCC =6.8V, TJ = 25°C	10.8	12.5	14.2	A
Hiccup blanking time	Tblk_Hiccup	Note 4		20.48		ms
Thermal Shutdown						
Thermal Shutdown		Note 4		145		°C
Hysteresis		Note 4		20		°C

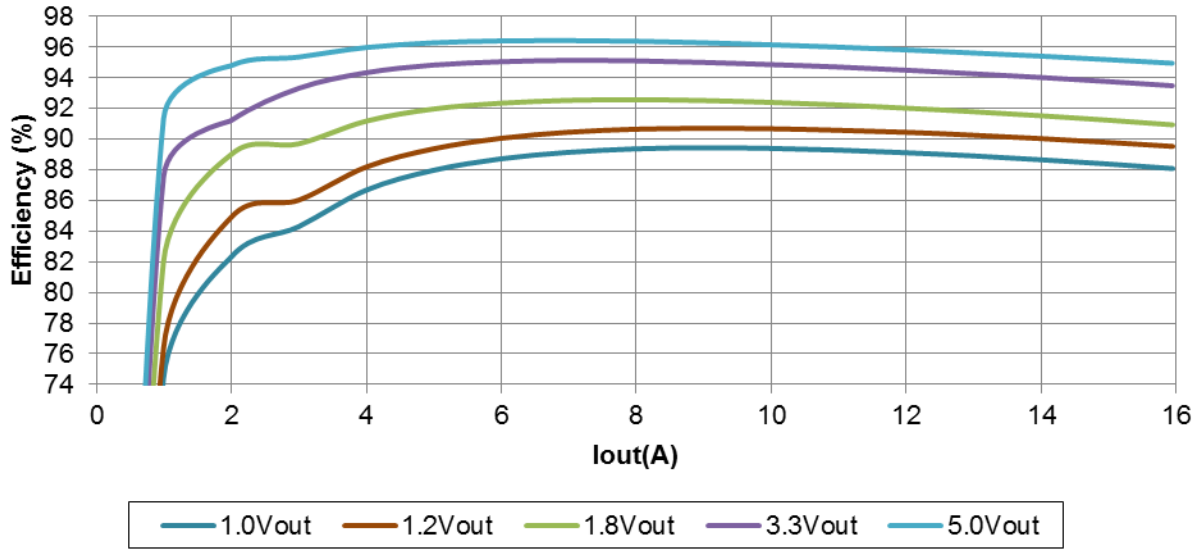
Notes:

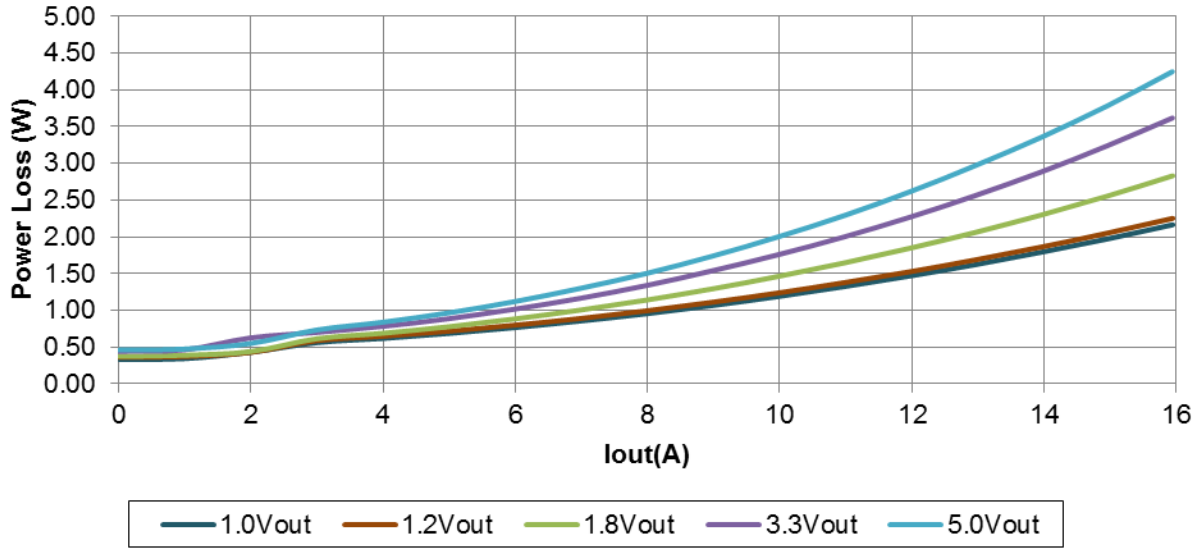
4. Guaranteed by design but not tested in production.

TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = 12V, VCC = Internal LDO, Io=0-16A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
1.0	0.4	59PR9875N (Vitec)	0.29
1.2	0.4	59PR9875N (Vitec)	0.29
1.8	0.47	7443330047 (Wurth Elektronik)	0.8
3.3	0.88	MPC1040LR88C (NEC/Tokin)	2.3
5.0	1.0	7443330100 (Wurth Elektronik)	1.35





TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 12V, Vin = VCC = 5V, Io=0-16A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
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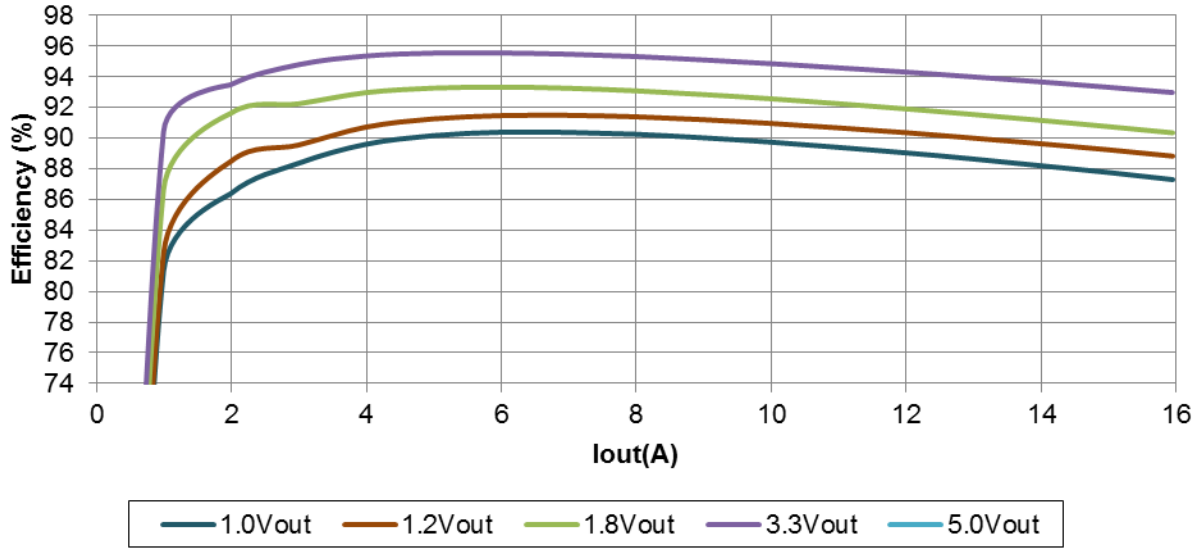
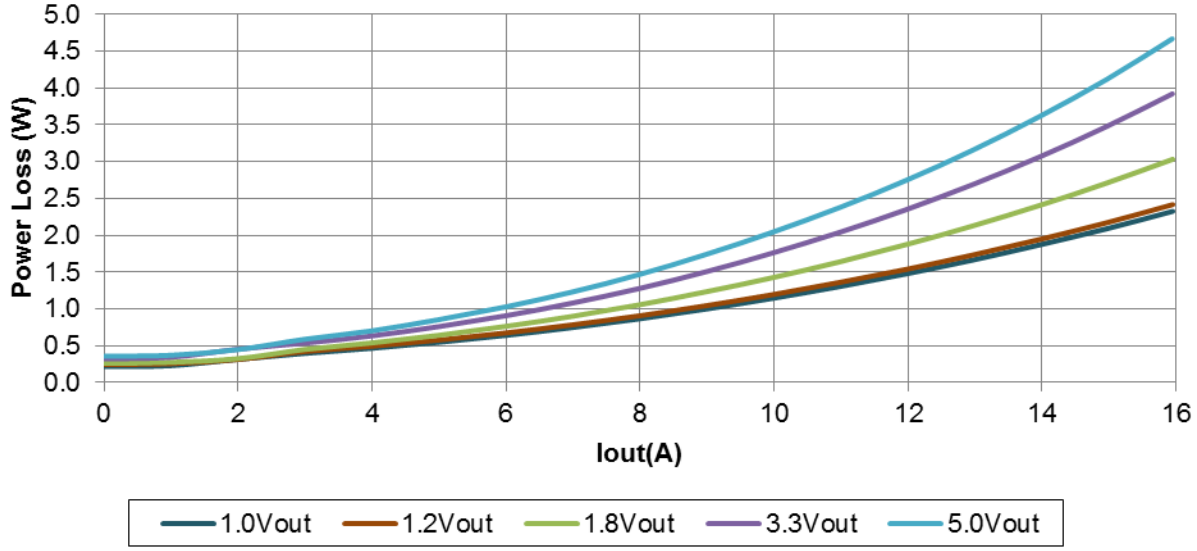
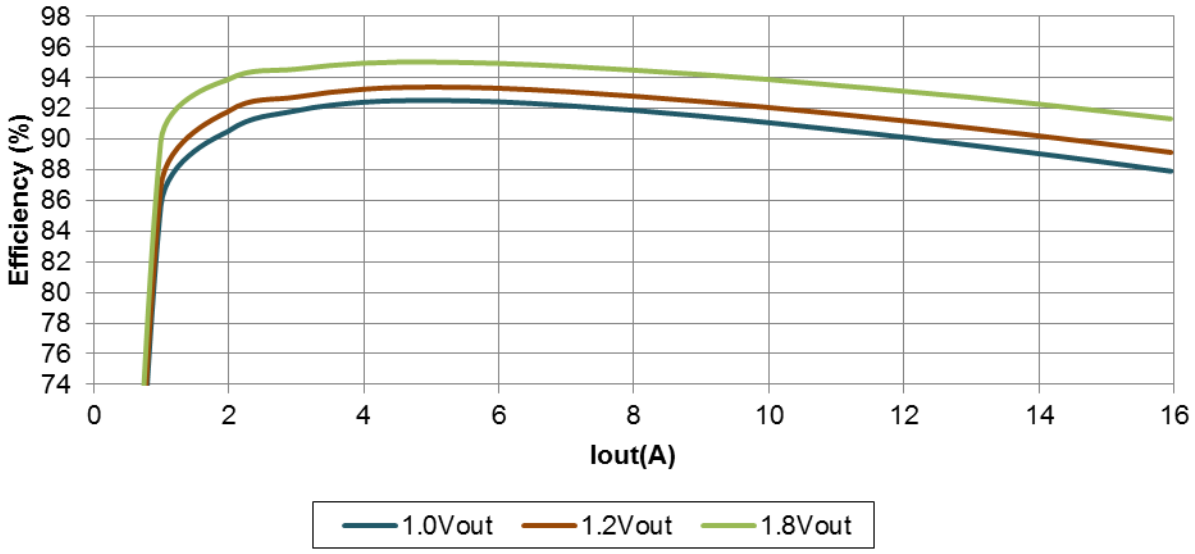


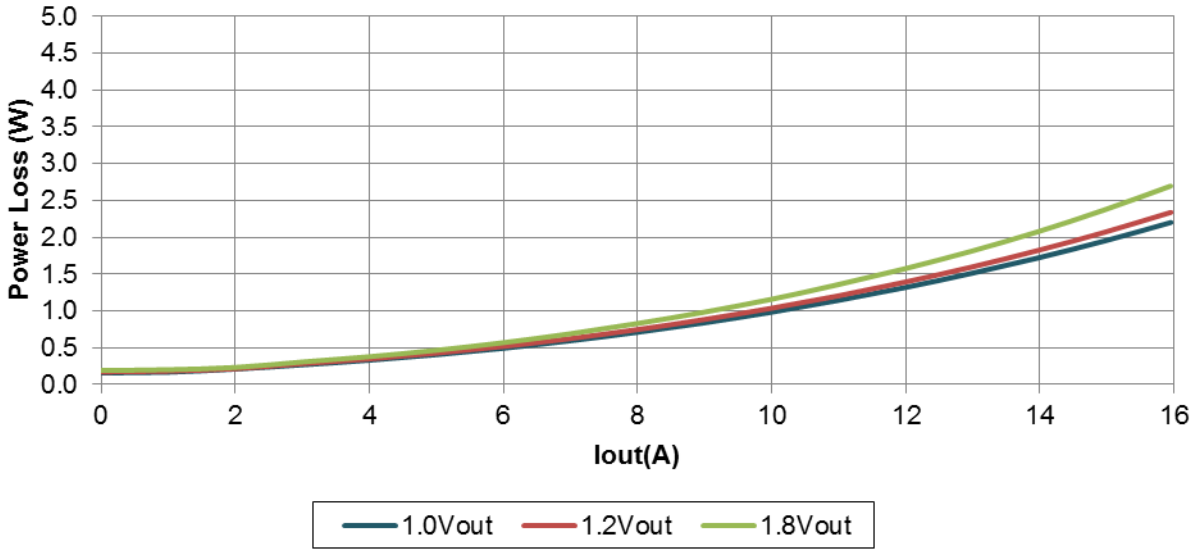


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = VCC = 5V, Io=0-16A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
1.0	0.3	59PR9874N (Vitec)	0.29
1.2	0.3	59PR9874N (Vitec)	0.29
1.8	0.4	59PR9875N (Vitec)	0.29

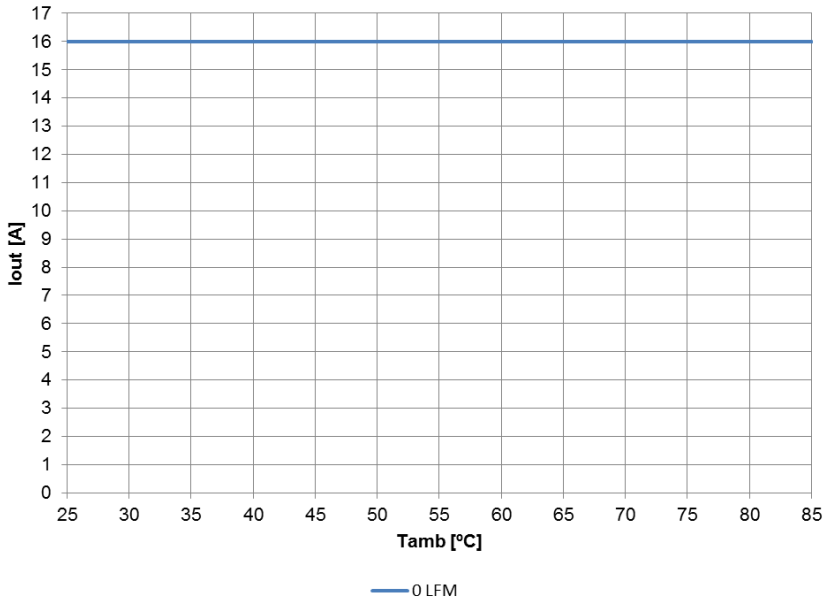




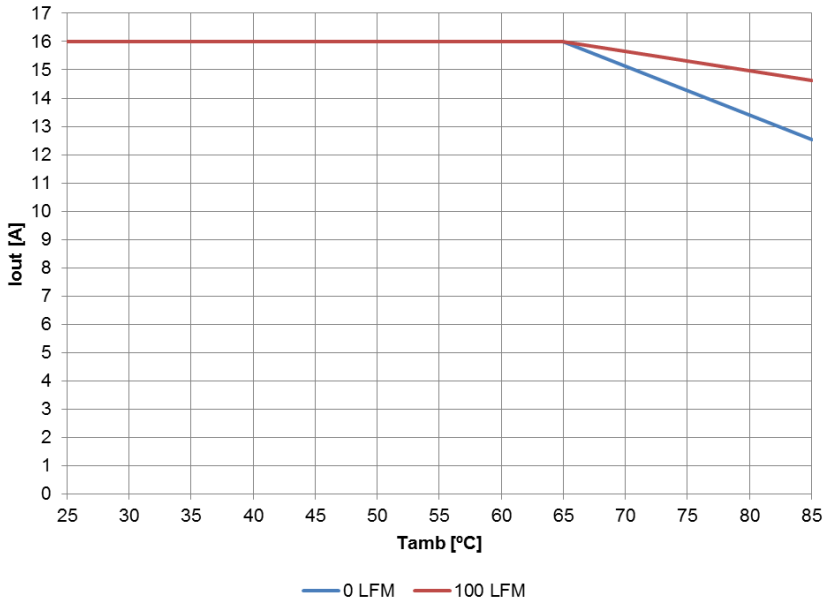
THERMAL DERATING CURVES

Measurements are done on IR3448 Evaluation board. PCB is a 6 layer board with 2 oz copper and FR4 material.

Vin=PVin=12V, Vout =1.2V, VCC=internal LDO (6.8V), Fs = 600kHz

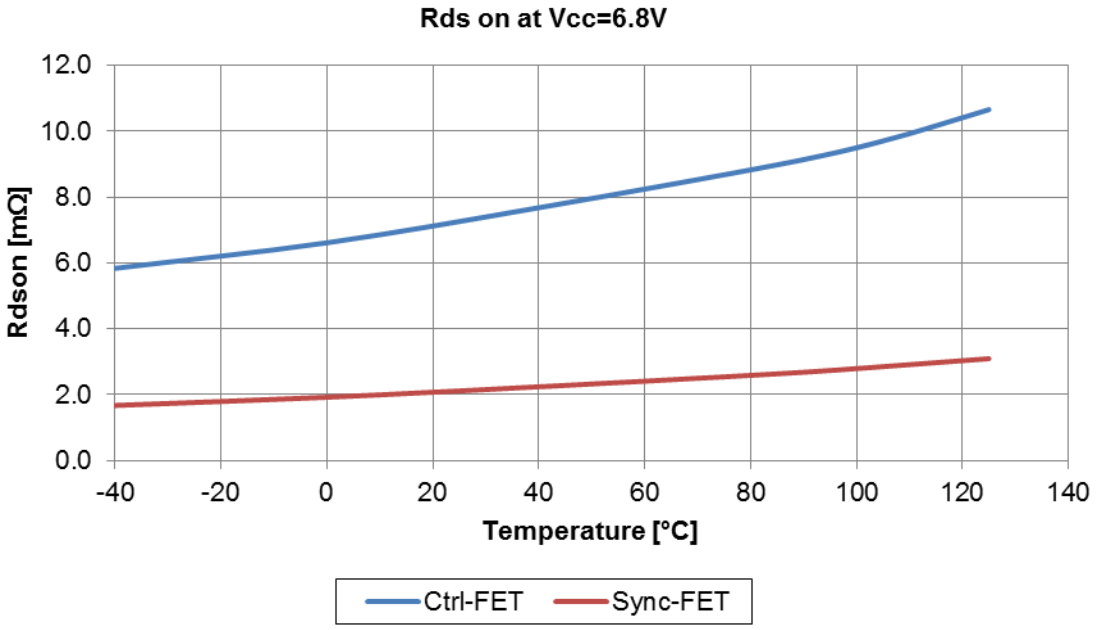


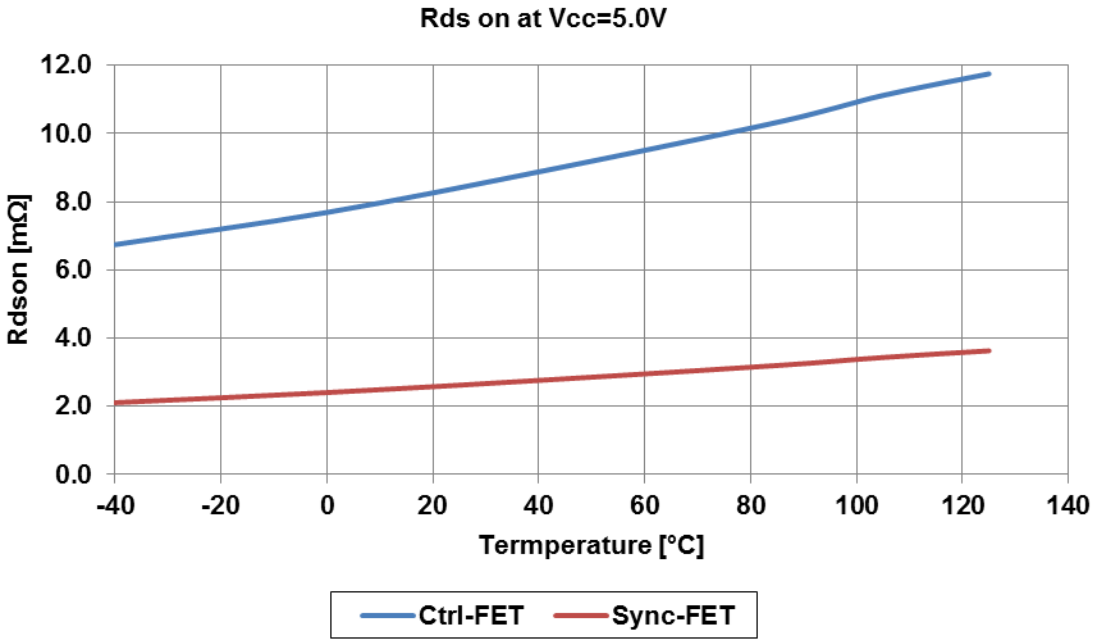
Vin=PVin=12V, Vout =5.0V, VCC=internal LDO (6.8V), Fs = 600kHz



Note: International Rectifier Corporation specifies current rating of SupIRBuck devices conservatively. The continuous current load capability might be higher than the rating of the device if input voltage is 12V typical and switching frequency is below 600kHz. However, the maximum current is limited by the internal current limit and designers need to consider enough guard bands between load current and minimum current limit to guarantee that the device does not trip at steady state condition.

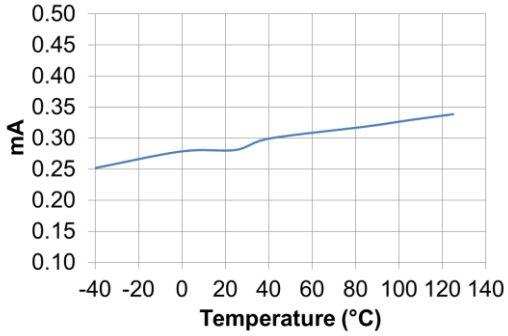
RDSON OF MOSFETS OVER TEMPERATURE



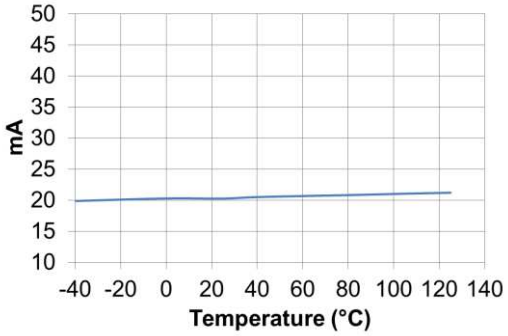


TYPICAL OPERATING CHARACTERISTICS (-40°C to +125°C)

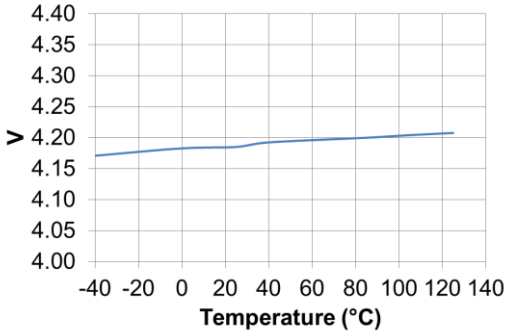
IIN (STANDBY)



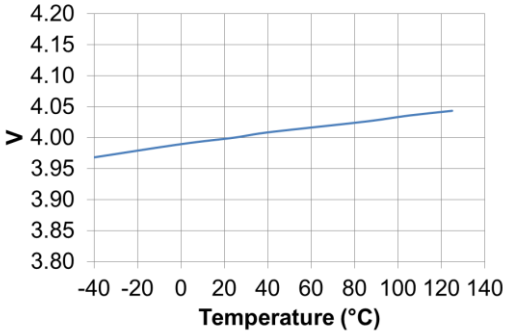
IIN (DYNAMIC) @ Fs=600kHz



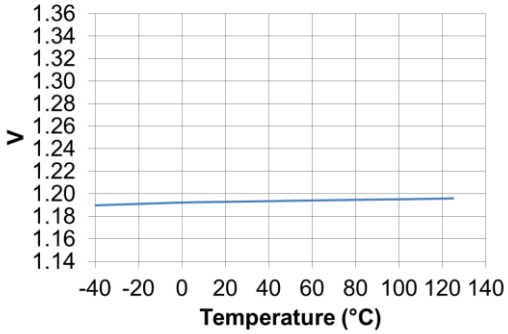
VCC_UVLO_START



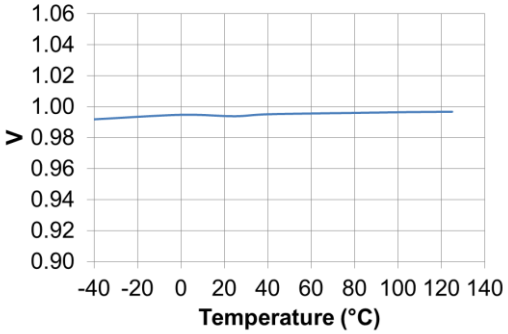
VCC_UVLO_STOP



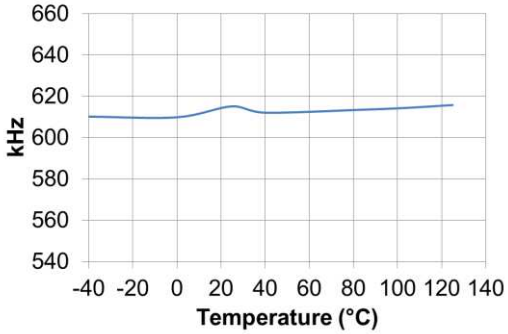
EN_UVLO_START



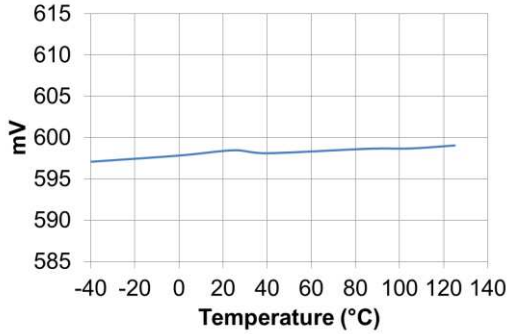
EN_UVLO_STOP

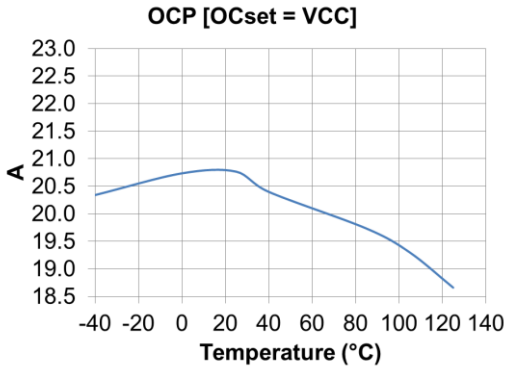


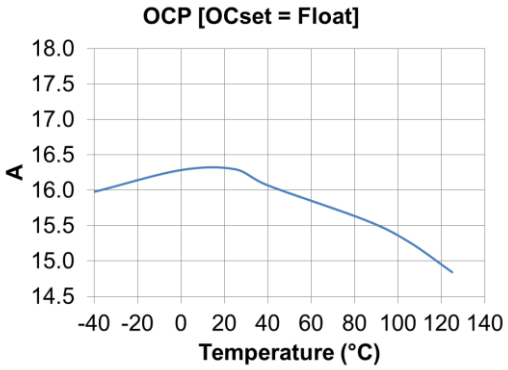
FREQUENCY [RT = 39.2kΩ]

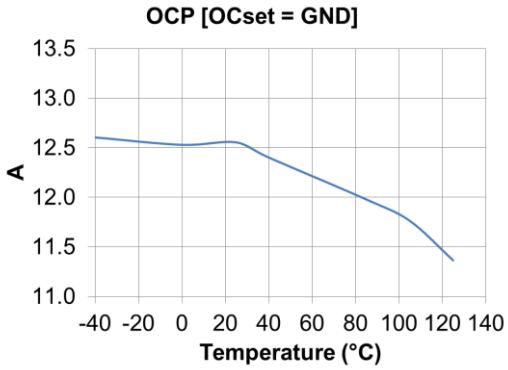


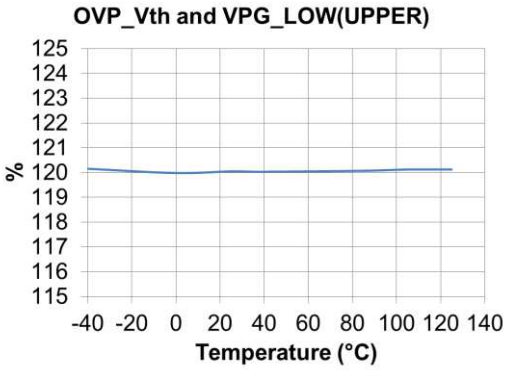
VFB

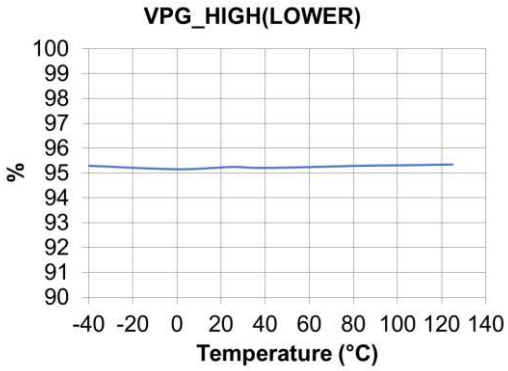


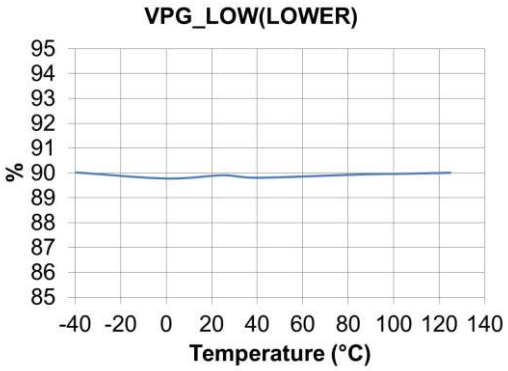

OCP [OCset = VCC]
A
23.0
22.5
22.0
21.5
21.0
20.5
20.0
19.5
19.0
18.5
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)

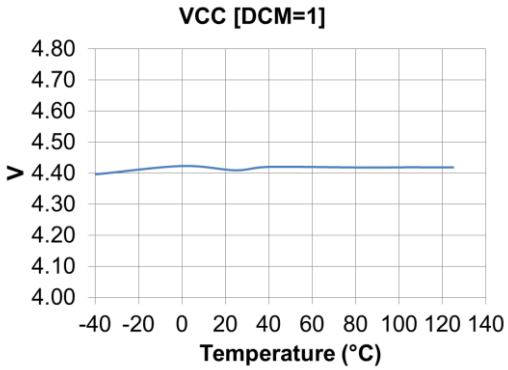

OCP [OCset = Float]
A
18.0
17.5
17.0
16.5
16.0
15.5
15.0
14.5
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)

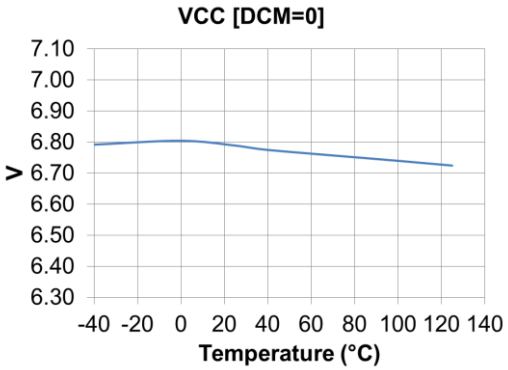

OCP [OCset = GND]
A
13.5
13.0
12.5
12.0
11.5
11.0
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)


OVP_Vth and VPG_LOW(UPPER)
%
125
124
123
122
121
120
119
118
117
116
115
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)


VPG_HIGH(LOWER)
%
100
99
98
97
96
95
94
93
92
91
90
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)


VPG_LOW(LOWER)
%
95
94
93
92
91
90
89
88
87
86
85
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)


VCC [DCM=1]
V
4.80
4.70
4.60
4.50
4.40
4.30
4.20
4.10
4.00
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)


VCC [DCM=0]
V
7.10
7.00
6.90
6.80
6.70
6.60
6.50
6.40
6.30
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)

THEORY OF OPERATION

DESCRIPTION

The IR3448 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 300kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR3448 provides precisely regulated output voltage programmed via two external resistors from 0.6V to 0.86*PVin.

The IR3448 operates with an internal bias supply (LDO) which is connected to the VCC pin. This allows operation with single supply. The bias voltage is variable according to load condition. If the output load current is less than half of the peak-to-peak inductor current, a lower bias voltage, 4.4V, is used as the internal gate drive voltage; otherwise, a higher voltage, 6.8V, is used.

This feature helps the converter to reduce power losses. The device can also be operated with an external supply from 4.5V to 7.5V, allowing an extended operating input voltage (PVin) range from 1.0V to 21V. For using the internal LDO supply, the Vin pin should be connected to PVin pin. If an external supply is used, it should be connected to VCC pin and the Vin pin should be shorted to VCC pin.

The device utilizes the on-resistance of the low side MOSFET (synchronous Mosfet) as current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

IR3448 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

UNDER-VOLTAGE LOCKOUT AND POR

The under-voltage lockout circuit monitors the voltage of VCC pin and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drops below the set thresholds. Normal operation resumes once VCC and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted the soft start sequence starts (see soft start section).

ENABLE

The Enable features another level of flexibility for startup. The Enable has precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3448 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3448 does not turn on until the bus voltage reaches the desired level Figure 4. Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold, IR3448 will be enabled. Therefore, in addition to being a logic input pin to enable the IR3448, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage (PVin). It can help prevent the IR3448 from regulating at low PVin voltages that can cause excessive input current.

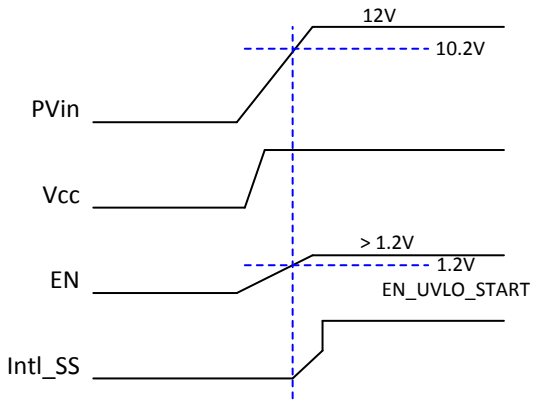


Figure 4: Normal Start up, device turns on when the bus voltage reaches 10.2V

A resistor divider is used at EN pin from PVin to turn on the device at 10.2V.

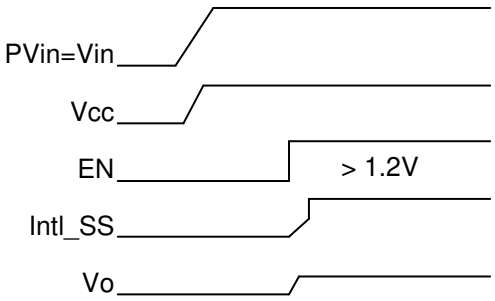


Figure 5: Recommended startup for Normal operation

Figure 5 shows the recommended startup sequence for the typical operation of IR3448 with Enable used as logic input.

PRE-BIAS STARTUP

IR3448 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. Figure 6 shows a typical Pre-Bias condition at start up. The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5% until it reaches the steady state value. The number of these startup pulses for each step is 16 and it's internally programmed. Figure 7 shows the series of 16x8 startup pulses.

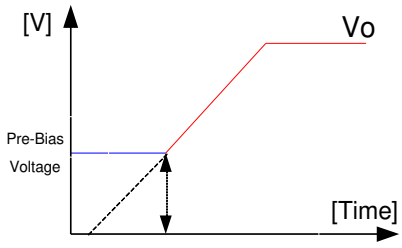


Figure 6: Pre-Bias startup

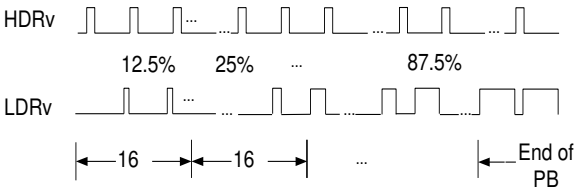


Figure 7: Pre-Bias startup pulses

SOFT-START

IR3448 has an internal digital soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and VCC rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal soft-start (Intl_SS) signal linearly rises with the rate of 0.4mV/µs from 0V to 1.5V. Figure 8 shows the waveforms during soft start. The normal Vout startup time is fixed, and is equal to:

$$Tstart = \frac{(0.75V - 0.15V)}{0.4mV/\mu S} = 1.5mS \qquad \textbf{(1)}$$

During the soft start the over-current protection (OCP) and over-voltage protection (OVP) is enabled to protect the device for any short circuit or over voltage condition.

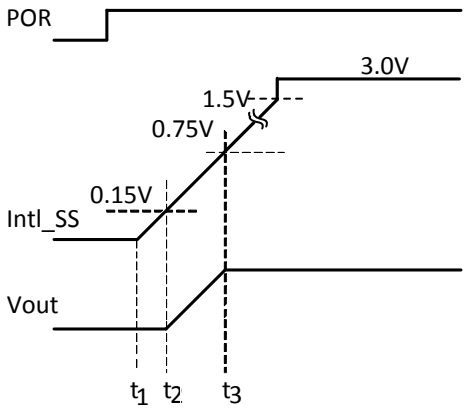


Figure 8: Theoretical operation waveforms during soft-start

OPERATING FREQUENCY

The switching frequency can be programmed between 300kHz – 1500kHz by connecting an external resistor

from R_t pin to LGnd. Table 1 tabulates the oscillator frequency versus R_t.

Table 1: Switching Frequency(Fs) vs. External Resistor(*Rt*)

Rt (KΩ)	Freq (KHz)
80.6	300
60.4	400
48.7	500
39.2	600
34	700
29.4	800
26.1	900
23.2	1000
21	1100
19.1	1200
17.4	1300
16.2	1400
15	1500

SHUTDOWN

IR3448 can be shutdown by pulling the Enable pin below its 1.0V threshold. During shutdown the high side and the low side drivers are turned off.

OVER CURRENT PROTECTION

The Over Current (OC) protection is performed by sensing the inductor current through the $R_{DS(on)}$ of the Synchronous MOSFET. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any layout related noise issues. The Over Current (OC) limit can be set to one of three possible settings by floating the OCset pin, by pulling up the OCset pin to VCC, or pulling down the OCset pin to PGnd. The current limit scheme in the IR3448 uses an internal temperature compensated current source to achieve an almost constant OC limit over temperature.

Over Current Protection circuit senses the inductor current flowing through the Synchronous MOSFET. To help minimize false tripping due to noise and transients, inductor current is sampled for about 30 nS on the downward inductor current slope approximately 12.5% of the switching period before the inductor current valley. However, if the Synchronous MOSFET is on for less than 12.5% of the switching period, the current is sampled approximately 40nS after the start of the downward slope of the inductor current. When the sampled current is higher than the OC Limit, an OC event is detected.

When an Over Current event is detected, the converter enters hiccup mode. Hiccup mode is performed by latching the OC signal and pulling the Intl_SS signal to ground for 20.48 mS (typ.). OC signal clears after the completion of hiccup mode and the converter attempts to return to the nominal output voltage using a soft start sequence. The converter will repeat hiccup mode and attempt to recover until the overload or short circuit condition is removed.

Because the IR3448 uses valley current sensing, the actual DC output current limit will be greater than OC limit. The DC output current is approximately half of peak to peak inductor ripple current above selected OC limit. OC Limit, inductor value, input voltage, output voltage and switching frequency are used to calculate the DC output current limit for the converter. Equation (2) to determine the approximate DC output current limit.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta i}{2} \quad \textbf{(2)}$$

I_{OCP} = DC current limit hiccup point
I_{LIMIT} = Current Limit Valley Point
Δi = Inductor ripple current

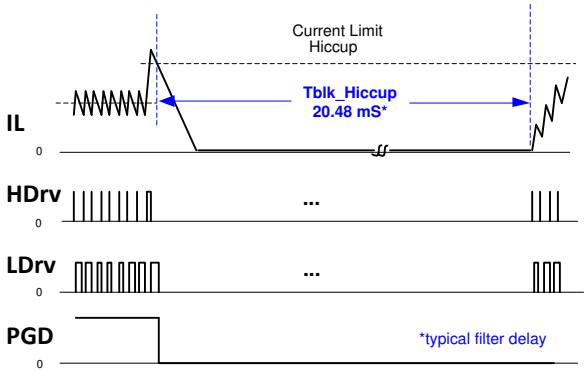


Figure 9: Timing Diagram for Current Limit Hiccup

THERMAL SHUTDOWN

Temperature sensing is provided inside IR3448. The trip threshold is typically 145°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and resets the internal soft start.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

REMOTE VOLTAGE SENSING

True differential remote sensing in the feedback loop is critical to high current applications where the output voltage across the load may differ from the output voltage measured locally across an output capacitor at the output inductor, and to applications that require die voltage sensing.

The RS+ and RS- pins of the IR3448 form the inputs to a remote sense differential amplifier (RSA) with high speed, low input offset and low input bias current which ensure accurate voltage sensing and fast transient response in such applications.

The input range for the differential amplifier is limited to 1.5V below the VCC rail. Note that IR3448 incorporates a smart LDO which switches the VCC rail voltage depending on the loading. When determining the input range assume the part is in light load and using the lower VCC rail voltage.

There are two remote sense configurations that are usually implemented. Figure 10 shows a general remote sense (RS) configuration. This configuration allows the RSA to monitor output voltages above VCC. A resistor divider is placed in between the output and the RSA to provide a lower input voltage to the RSA inputs. Typically, the resistor divider is calculated to provide VREF (0.6V) across the RSA inputs which is then outputted to RSo. The input impedance of the RSA is 63 KOhms typically and should be accounted for when determining values for the resistor divider. To account for the input impedance, assume a 63 KOhm resistor in parallel to the lower resistor in the divider network. The compensation is then designed for 0.6V to match the RSo value.

Low voltage applications can use the second remote sense configuration. When the output voltage range is within the RSA input specifications, no resistor divider is needed in between the converter output and RSA. The second configuration is shown in Figure 11. The RSA is used as a unity gain buffer and compensation is determined normally.

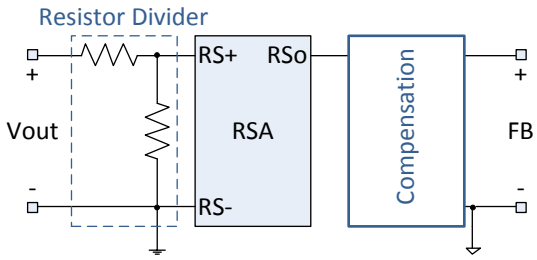


Figure 10: General Remote Sense Configuration

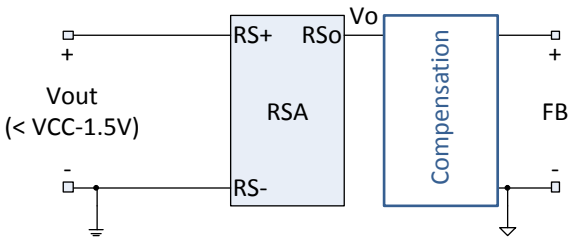


Figure 11: Remote Sense Configuration for Vout less than VCC-1.5V

EXTERNAL SYNCHRONIZATION

IR3448 incorporates an internal phase lock loop (PLL) circuit which enables synchronization of the internal oscillator to an external clock. This function is important to avoid sub-harmonic oscillations due to beat frequency for embedded systems when multiple point-of-load (POL) regulators are used. A multi-function pin, Rt/Sync, is used to connect the external clock. If the external clock is present before the converter turns on, Rt/Sync pin can be connected to the external clock signal solely and no other resistor is needed. If the external clock is applied after the converter turns on, or the converter switching frequency needs to toggle between the external clock frequency and the internal free-running frequency, an external resistor from Rt/Sync pin to LGnd is required to set the free-running frequency.

When an external clock is applied to Rt/Sync pin after the converter runs in steady state with its free-running frequency, a transition from the free-running frequency to the external clock frequency will happen. This transition is to gradually make the actual switching frequency equal to the external clock frequency, no matter which one is higher. When the external clock signal is removed from Rt/Sync pin, the switching frequency is also changed to free-running

gradually. In order to minimize the impact from these transitions to output voltage, a diode is recommended to add between the external clock and Rt/Sync pin. Figure 12 shows the timing diagram of these transitions.

An internal circuit is used to change the PWM ramp slope according to the clock frequency applied on Rt/Sync pin. Even though the frequency of the external synchronization clock can vary in a wide range, the PLL circuit keeps the ramp amplitude constant, requiring no adjustment of the loop compensation. PVin variation also affects the ramp amplitude, which will be discussed separately in Feed-Forward section.

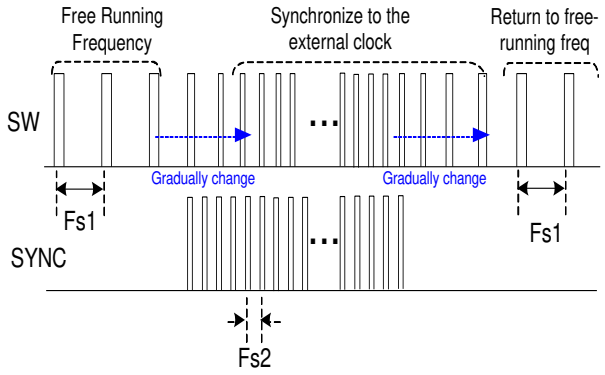


Figure 12: Timing Diagram for Synchronization to the external clock (Fs1>Fs2 or Fs1<Fs2)

FEED-FORWARD

Feed-Forward (F.F.) is an important feature, because it can keep the converter stable and preserve its load transient performance when PVin varies. The PWM ramp amplitude (Vramp) is proportionally changed with PVin to maintain PVin/Vramp almost constant throughout PVin variation range (as shown in Figure 13). The PWM ramp amplitude is adjusted to 0.15 of PVin. Thus, the control loop bandwidth and phase margin can be maintained constant. Feed-forward function can also minimize impact on output voltage from fast PVin change. F.F. is disabled when PVin<6.2V and the PWM ramp is typically 0.9V. For PVin<6.2V, PVin voltage should be accounted for when calculating control loop parameters.

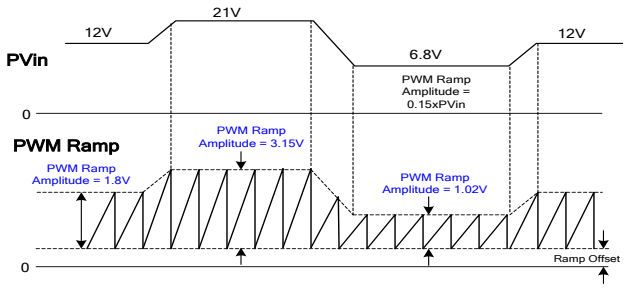


Figure 13: Timing Diagram for Feed-Forward (F.F.) Function

SMART LOW DROPOUT REGULATOR (LDO)

IR3448 has an integrated low dropout (LDO) regulator which can provide gate drive voltage for both drivers. In order to improve overall efficiency over the whole load range, LDO voltage is set to 6.8V (typ.) at mid- or heavy load condition to reduce Rds(on) and thus MOSFET conduction loss; and it is reduced to 4.4V (typ.) at light load condition to reduce gate drive loss.

The smart LDO selects its output voltage according to the load condition by sensing the inductor current (I_L). At light load condition, the inductor current can fall below zero as shown in Figure 14. A zero crossing comparator is used to detect when the inductor current falls below zero at the LDrv Falling Edge. If the comparator detects zero crossing events for 256 consecutive switching cycles, the smart LDO reduces its output to 4.4V. The LDO voltage will remain low until a zero crossing is not detected. Once a zero crossing is not detected, the counter is reset and LDO voltage returns to 6.8V. Figure 14 shows the timing diagram. Whenever the device turns on, LDO always starts with 6.8V, then goes to 4.4V / 6.8V depending upon the load condition. However, if only Vin is applied with Enable low, the LDO output is 4.4V.

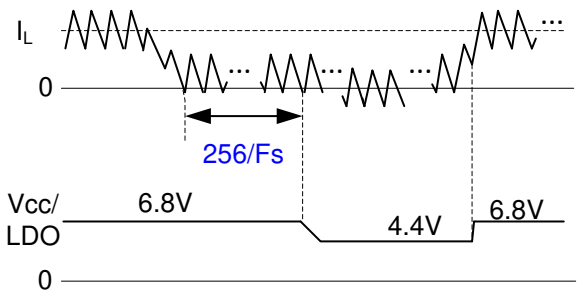


Figure 14: Time Diagram for Smart LDO

Users can configure the IR3448 to use a single supply or dual supplies. Depending on the configuration used the PVin, Vin and VCC pins are connected differently. Below several configurations are shown. In an internally biased configuration, the LDO draws from the Vin pin and provides a gate drive voltage, as shown in Figure 15. By connecting Vin and PVin together as shown in the Figure 16, IR3448 is an internally biased single supply configuration that runs off a single supply.

IR3448 can also use an external supply to provide gate drive voltage for the drivers instead of the internal LDO. To use an external bias, connected Vin and VCC to the external bias. PVin can use a separate rail as shown in Figure 17 or run off the same rail as Vin and VCC.

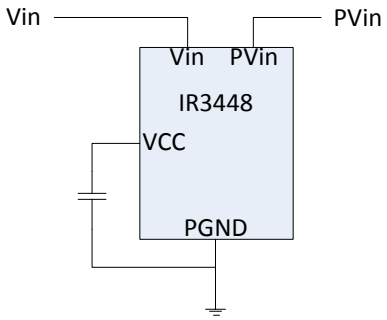


Figure 15: Internally Biased Configuration

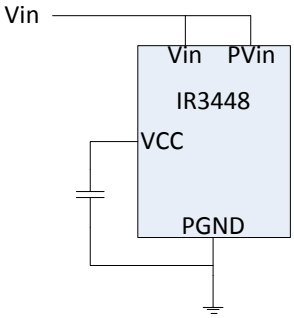


Figure 16: Internally Biased Single Supply Configuration

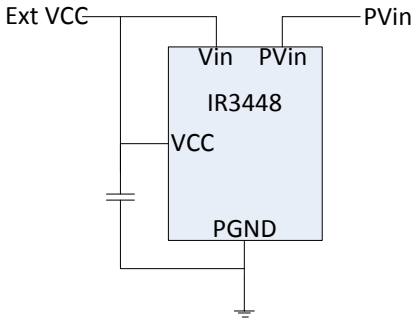


Figure 17: Externally Biased Configuration

When the Vin voltage is below 6.8V, the internal LDO enters the dropout mode at medium and heavy load. The dropout voltage increases with the switching frequency. Figure 18 shows the LDO voltage for 600kHz and 1000kHz switching frequency.

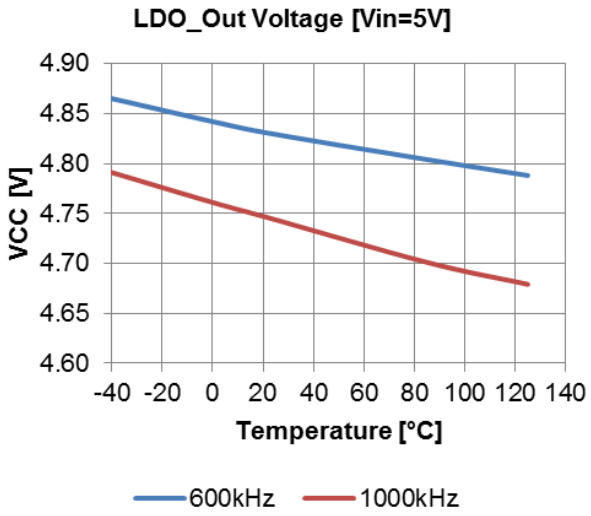


Figure 18: LDO_Out Voltage in dropout mode

CBYP

This pin reflects the internal reference voltage which is used by the error amplifier to set the output voltage. In most operating conditions this pin is only connected to an external bypass capacitor and it is left floating. A minimum 100pF ceramic capacitor is required from stability point of view

POWER GOOD OUTPUT

IR3448 continually monitors the output voltage via the sense pin (Vsns) voltage. The Vsns voltage is an input

to the window comparator with upper and lower threshold of OVP(trip) and VPG_high(lower) respectively. PGood signal is high whenever Vsns voltage is within the PGood comparator window thresholds. Hysteresis has been applied to the lower threshold, PGood signal goes low when Vsns drops below VPG_low(lower) instead of VPG_high(lower). The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation. Figure 19 show the timing diagram of the PGood signal. Vsns signal is also used by OVP comparator for detecting output over voltage condition. PGood signal is low when Enable is low.

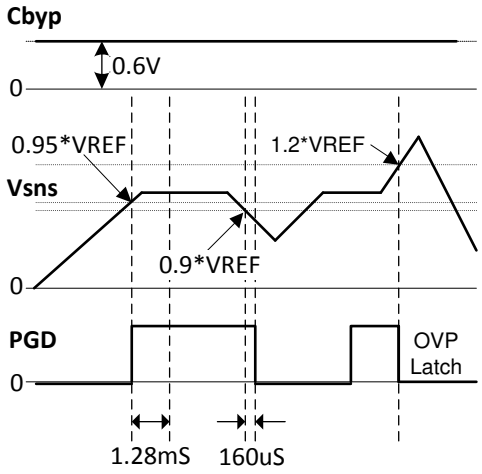


Figure 19: PGood Timing Diagram

OVER-VOLTAGE PROTECTION (OVP)

Over-voltage protection in IR3448 is achieved by comparing sense pin voltage Vsns to a pre-set threshold. When Vsns exceeds the over voltage threshold, an over voltage trip signal asserts after 2.5 uS (typ.) delay. The high side drive signal HDrv is latched off immediately and PGood flags are set low. The low side drive signal is kept on until the Vsns voltage drops below the threshold. HDrv remains latched off until a reset is performed by cycling VCC. OVP is active when enable is high or low.

Vsns voltage is set by the voltage divider connected to the output and it can be programmed externally. Figure 20 shows the timing diagram for OVP.

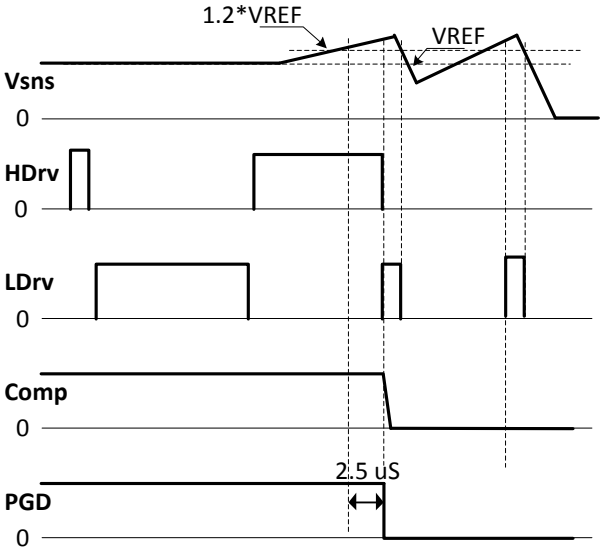


Figure 20: Timing Diagram for OVP in non-tracking mode

BODY BRAKING™

The Body Braking feature of the IR3448 allows improved transient response for step-down load transients. A severe step-down load transient would cause an overshoot in the output voltage and drive the Comp pin voltage down until control saturation occurs demanding 0% duty cycle and the PWM input to the Control FET driver is kept OFF. When the first such skipped pulse occurs, the IR3448 enters Body Braking mode, wherein the Sync FET also turned OFF. The inductor current then decays by freewheeling through the body diode of the Sync FET. Thus, with Body Braking, the forward voltage drop of the body diode provides and additional voltage to discharge the inductor current faster to the light load value as shown in equation **(3)** and equation **(4)** below:

$$\frac{di_L}{dt} = -\frac{V_o + V_D}{L}, \text{ with body braking} \quad \textbf{(3)}$$

$$\frac{di_L}{dt} = -\frac{V_o}{L}, \text{ without body braking} \quad \textbf{(4)}$$

I_L = Inductor current
V_D = Forward voltage drop of the body diode of the Sync FET.
V_o = output voltage
L = Inductor value

The Body Braking mechanism is kept OFF during pre-bias operation. Also, in the event of an extremely

severe load step-down transient causing OVP, the Body Brake is overridden by the OVP latch, which turns on the Sync FET.

MINIMUM ON TIME CONSIDERATIONS

The minimum ON time is the shortest amount of time for Ctrl FET to be reliably turned on. This is very critical parameter for low duty cycle, high frequency applications. Conventional approach limits the pulse width to prevent noise, jitter and pulse skipping. This results to lower closed loop bandwidth.

IR has developed a proprietary scheme to improve and enhance minimum pulse width which utilizes the benefits of voltage mode control scheme with higher switching frequency, wider conversion ratio and higher closed loop bandwidth, the latter results in reduction of output capacitors. Any design or application using IR3448 must ensure operation with a pulse width that is higher than the minimum on-time. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{PV_{in} \times F_s} \quad \textbf{(5)}$$

In any application that uses IR3448, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on} \quad \textbf{(6)}$$

$$t_{on(\min)} \le \frac{V_{out}}{PV_{in} \times F_s} \quad \textbf{(7)}$$

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad \textbf{(8)}$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.6V. Therefore, for $V_{out(min)}$ = 0.6V,

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad \textbf{(9)}$$

$$\therefore PV_{in} \times F_s \le \frac{0.6V}{50nS} = 12V/\mu S$$

Therefore, at the maximum recommended input voltage 21V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 571 kHz. Conversely, for operation at the maximum recommended operating frequency (1.5 MHz) and minimum output voltage (0.6V). The input voltage (PVin) should not exceed 8V, otherwise pulse skipping may happen.

MAXIMUM DUTY RATIO

A certain off-time is specified for IR3448. This provides an upper limit on the operating duty ratio at any given switching frequency. The off-time remains at a relatively fixed ratio to switching period in low and mid frequency range, while in high frequency range this ratio increases, thus the lower the maximum duty ratio at which IR3448 can operate. Figure 21 shows a plot of the maximum duty ratio vs. the switching frequency with built in input voltage feed forward mechanism.

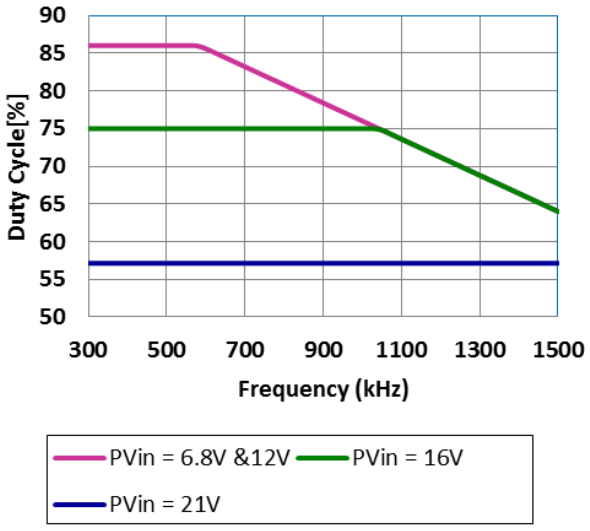


Figure 21: Maximum duty cycle vs. switching frequency

TYPICAL OPERATING WAVEFORM

DESIGN EXAMPLE

The following example is a typical application for IR3448. The application circuit is shown in Figure 28.

V_{in} = PV_{in} = 12V
F_s = 600kHz

V_o = 1.2V
I_o = 16A
Ripple Voltage = ± 1% * V_o
ΔV_o = ± 4% * Vo (for 30% load transient)

Enabling the IR3448

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage as shown in Figure 22.

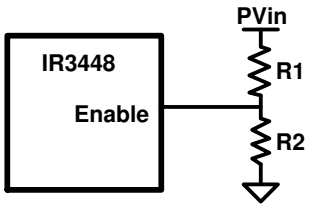


Figure 22: Using Enable pin for UVLO implementation

For a typical Enable threshold of V_{EN} = 1.2 V

$$PV_{in(\min)} \times \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2 \quad \textbf{(10)}$$

$$R_2 = R_1 \frac{V_{EN}}{PV_{in(\min)} - V_{EN}} \quad \textbf{(11)}$$

For $PV_{in\ (min)}$=9.2V, R_1=49.9K and R_2=7.5K ohm is a good choice.

Programming the frequency

For F_s = 600 kHz, select R_t = 39.2 KΩ, using Table 1.

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The FB pin is the inverting input of the error amplifier, which is internally referenced to VREF. The divider ratio is set to equal VREF at the FB pin when the output is at its desired value. When an external resistor divider is connected to the output as shown in Figure 23, the output voltage is defined by using the following equation:

$$V_o = V_{ref} \times \left(1 + \frac{R_5}{R_6}\right) \quad \textbf{(12)}$$

$$R_6 = R_5 \times \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad \textbf{(13)}$$

For the calculated values of R5 and R6, see feedback compensation section.

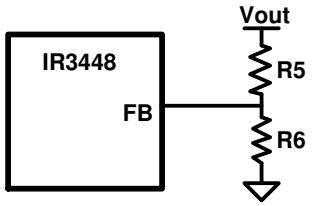


Figure 23: Typical application of the IR3448 for programming the output voltage

Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C1). The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode (Figure 24), which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C1 is approximately given as:

$$V_c \cong V_{cc} - V_D \quad \textbf{(14)}$$