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xPHASE3*TM AMD HYBRID CONTROL IC*DESCRIPTION**

The IR3514 Hybrid Control IC combined with *xPHASE3*TM Phase ICs provides a full featured and flexible way to implement a complete AMD SVID or PVID power solution. It has the ability to independently control both the VDD core and VDDNB auxiliary planes required by the CPU when operated in SVI (Serial VID Interface) mode. The IR3514 can also receive Power Savings commands through the SVI serial bus and communicate this information to the IR3507 or other Phase ICs with PSI input capabilities. When operated in PVI (Parallel VID Interface) mode, the IR3514 controls the VDD core plane through 6 Parallel VID bits and the VDDNB auxiliary plane power stage goes to high impedance. PVI/SVI selection is made by sampling VID1 input upon Enable. The IR3514 interfaces with any number of Phase ICs each driving and monitoring a single phase. The *xPHASE3*TM architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

FEATURES

- In SVI Mode (VID1=0 upon Enable)
 - 2 converter outputs for the AMD processor VDD core and VDDNB auxiliary planes
 - AMD Serial VID interface independently programs both output voltages and operation
 - Both converter outputs boot to 2-bit “Boot” VID codes which are read and stored from the SVC & SVD parallel inputs upon the assertion of the Enable input
 - PWROK input signal activates SVID after successful boot start-up
 - Both converter outputs can be independently turned on and off through SVID commands
 - Deassertion of PWROK prior to Enable causes the converter output to transition to the stored Pre-PWROK VID codes
 - Connecting the PWROK input to VCCL disables SVID and implements VFIX mode with both output voltages programmed via SVC & SVD parallel inputs per the 2 bit VFIX VID codes
 - PSI_L commands are forwarded to VDD core phase ICs
- In PVI Mode (VID1=1 upon Enable)
 - Single converter control for VDD with the VDDNB power stage in a high impedance state
 - AMD 6 bit parallel VID programs the VDD regulation voltage
- VRRDY monitors output voltages, VRRDY will deassert if any output voltage is out of spec
- 0.5% overall system set point accuracy
- Programmable Dynamic VID Slew Rates
- Programmable VID Offset (VDD output only)
- Programmable output impedance (VDD output only)
- High speed error amplifiers with wide bandwidths of 30MHz and fast slew rates of 12V/us
- Remote sense amplifiers provide differential sensing and require less than 50uA bias current
- Programmable per phase switching frequency of 250kHz to 1.5MHz
- Daisy-chain digital phase timing provides accurate phase interleaving without external components
- Hiccup over current protection with delay during normal operation
- Central over voltage detection and communication to phase ICs through the IIN (ISHARE) pin
- OVP disabled during dynamic VID down transitions to prevent false triggering
- Detection and protection of open remote sense lines
- Gate Drive and IC bias linear regulator control with programmable output voltage and UVLO
- Simplified VR Ready Output provides indication of proper operation and avoids false triggering
- Thermally enhanced 40L MLPQ (6mm x 6mm) package
- Over voltage signal to system with over voltage detection during powerup and normal operation

ORDERING INFORMATION

Device	Package	Order Quantity
IR3514MTRPBF	40 Lead MLPQ (6 x 6 mm body)	3000 per reel
* IR3514MPBF	40 Lead MLPQ (6 x 6 mm body)	100 piece strips

* Samples only

APPLICATION CIRCUIT

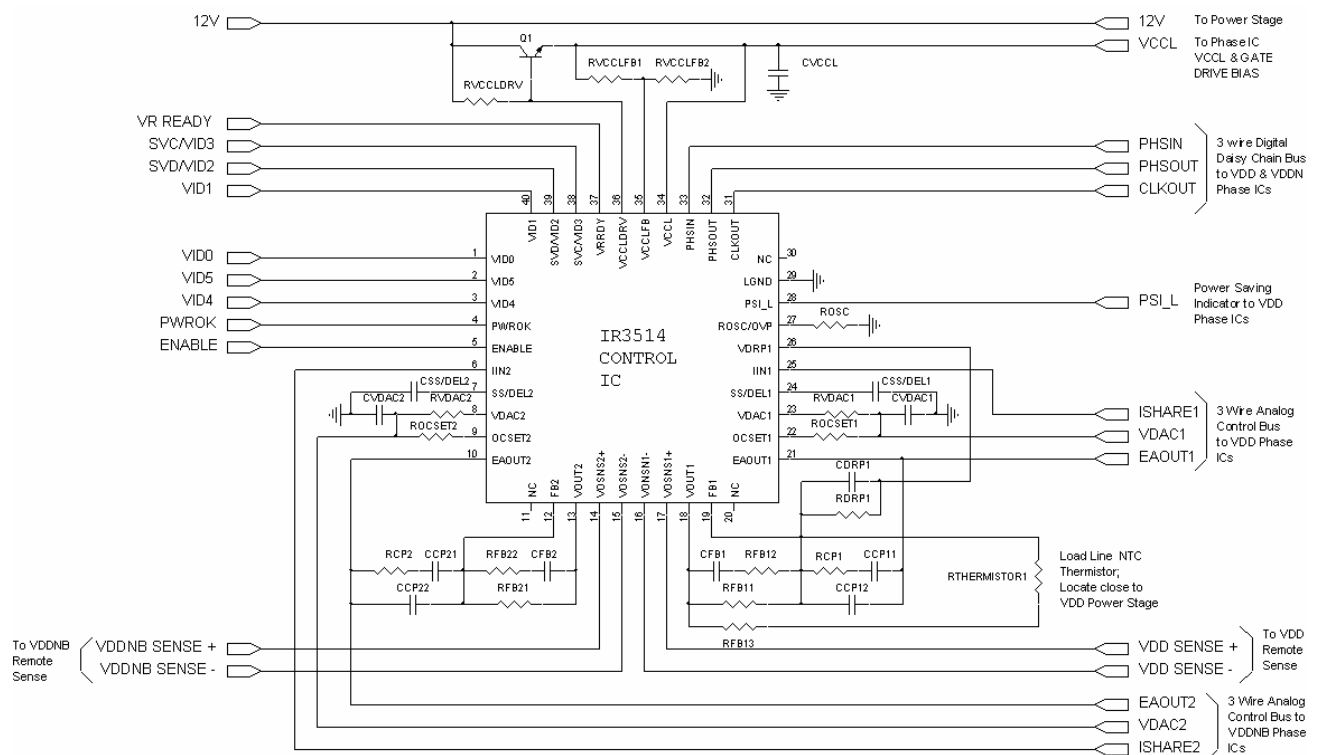


Figure 1 – IR3514 Application Circuit

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1-3	VID0, VID5, VID4	PVI VID inputs (ignored in SVI mode). Requires an external pull-up bias and should not be floated
4	PWROK	SVI System wide Power Good signal and input to the IR3514. When asserted, the IR3514 output voltage is programmed through the SVID interface protocol. Connecting this pin to VCCL enables VFIX mode upon ENABLE. Ignored in PVI.
5	ENABLE	Enable input. A logic low applied to this pin puts the IC into fault mode. In SVI mode, a logic high on the pin enables the converter and stores the SVC and SVD input states to determine either a 2-bit BOOT or VFIX VID, depending on the state of PWROK. Do not float this pin as the logic state will be undefined.
6	IIN2	SVI mode output 2 average current information input from the phase IC(s). This pin also communicates an over voltage condition to the output 2 phase ICs.
7	SS/DEL2	In SVI mode, programs the output 2 startup and over current protection delay timing. Connect an external capacitor to LGND to program.
8	VDAC2	SVI mode output 2 reference voltage programmed by SVID commands. Connect an external RC network to LGND to program the dynamic VID slew rate and provide compensation for the internal buffer amplifier. In PVI mode, VDAC2 is forced to 500mV.
9	OCSET2	Programs the SVI mode output 2 hiccup over-current threshold with an external resistor to VDAC2 and an internal ROOSC based current source. Over-current protection can be disabled by setting an over-current threshold higher than the maximum possible signal on the IIN2 pin from the phase ICs; do not exceed 5V or float this pin as improper operation will occur.
10	EAOUT2	SVI mode error amplifier 2 output. Held low in PVI mode.
11	NC	No Connection
12	FB2	Inverting input to error amplifier 2.
13	VOOUT2	Output 2 remote sense amplifier output.
14	VOSEN2+	Output 2 remote sense amplifier input. Kelvin at the load.
15	VOSEN2-	Output 2 remote sense amplifier input. Kelvin at the load return.
16	VOSEN1-	Output 1 remote sense amplifier input. Kelvin at the load return.
17	VOSEN1+	Output 1 remote sense amplifier input. Kelvin at the load.
18	VOOUT1	Output 1 remote sense amplifier output.
19	FB1	Inverting input to error amplifier 1. Converter output voltage can be programmed above the VDAC1 voltage by connecting an external resistor in series with this pin. There is an ROOSC based current sink on this pin.
20	NC	No Connection
21	EAOUT1	Error amplifier 1 output.
22	OCSET1	Programs the SVI mode output 1 hiccup over-current threshold with an external resistor to VDAC1 and an internal ROOSC based current source. Over-current protection can be disabled by setting an over-current threshold higher than the maximum possible signal on the IIN2 pin from the phase ICs, do not exceed 5V or float this pin as improper operation will occur.
23	VDAC1	Output 1 reference voltage programmed by either SVID commands or parallel VID bits. Connect an external RC network to LGND to program the dynamic VID slew rate and provide compensation for the internal buffer amplifier.
24	SS/DEL1	Programs the output 1 startup and over current protection delay timing. Connect an external capacitor to LGND to program.
25	IIN1	Output 1 average current information input from the phase IC(s). This pin also communicates an over voltage condition to the output 1 phase ICs.
26	VDRP1	Buffered output of the IIN1 signal. Connect an external RC network to FB1 to program converter output impedance.

PIN DESCRIPTION CONTINUED:

PIN#	PIN SYMBOL	PIN DESCRIPTION
27	ROSC/OVP	Connect a resistor to LGND to program oscillator frequency and OCSET1, OCSET2, FB1, VDAC1, and VDAC2 bias currents. Oscillator frequency equals switching frequency per phase. The pin voltage is 0.6V during normal operation and higher than 1.6V if over-voltage condition is detected.
28	PSI_L	Digital output to communicate PSI_L to Phase Ics.
29	LGND	Local ground for internal circuitry and IC substrate connection
30	NC	No Connection
31	CLKOUT	Clock output at switching frequency multiplied by phase number. Connect to CLKIN pins of phase ICs.
32	PHSOUT	Phase clock output at switching frequency per phase. Connect to PHSIN pin of the first phase IC.
33	PHSIN	Feedback input of phase clock. Connect to PHSOUT pin of the last phase IC.
34	VCCL	Output of the voltage regulator, and power input for clock oscillator circuitry. Connect a decoupling capacitor to LGND.
35	VCCLFB	Non-inverting input of the voltage regulator error amplifier. Output voltage of the regulator is programmed by a resistor divider connected to VCCL.
36	VCCLDRV	Output of the VCCL regulator error amplifier to control an external pass transistor. The pin senses 12V power supply through a resistor.
37	VRRDY	Open collector output. It is asserted in SVI mode when both outputs are regulated. It is asserted in PVI mode when VDD output is regulated. Connect external pull-up.
38	SVC/VID3	In SVI mode, SVC (Serial VID Clock) is an input to IR3514 that is driven by an open drain output of the processor. In PVI mode, this pin functions as the VID3 input. It requires an external pull-up and should not be floated.
39	SVD/VID2	In SVI mode, SVD (Serial VID Data) is a bidirectional signal that is an input and open drain output for both the AMD processor and the IR3514. In PVI mode, this pin functions as the VID2. It requires an external pull-up and should not be floated.
40	VID1	This pin determines the control mode of the IR3514, either SVI or PVI. SVI mode is selected if VID1=0 upon Enable. PVI mode is selected if VID1=1 upon Enable. It requires an external pull-up and should not be floated.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltages are absolute voltages referenced to the LGND pin.

Operating Junction Temperature.....0 to 150°C
 Storage Temperature Range.....-65°C to 150°C
 ESD Rating.....HBM Class 1C JEDEC Standard
 MSL Rating.....2
 Reflow Temperature.....260°C

PIN #	PIN NAME	V _{MAX}	V _{MIN}	I _{SOURCE}	I _{SINK}
1	VID0	8V	-0.3V	1mA	1mA
2	VID5	8V	-0.3V	1mA	1mA
3	VID4	8V	-0.3V	1mA	1mA
4	PWROK	8V	-0.3V	1mA	1mA
5	ENABLE	3.5V	-0.3V	1mA	1mA
6	IIN2	8V	-0.3V	5mA	1mA
7	SS/DEL2	8V	-0.3V	1mA	1mA
8	VDAC2	3.5V	-0.3V	1mA	1mA
9	OCSET2	8V	-0.3V	1mA	1mA
10	EAOUT2	8V	-0.3V	25mA	10mA
12	FB2	8V	-0.3V	1mA	1mA
13	VOUT2	8V	-0.3V	5mA	25mA
14	VOSEN2+	8V	-0.5V	5mA	1mA
15	VOSEN2-	1.0V	-0.5V	5mA	1mA
16	VOSEN1-	1.0V	-0.5V	5mA	1mA
17	VOSEN1+	8V	-0.5V	5mA	1mA
18	VOUT1	8V	-0.3V	5mA	25mA
19	FB1	8V	-0.3V	1mA	1mA
21	EAOUT1	8V	-0.3V	25mA	10mA
22	OCSET1	8V	-0.3V	1mA	1mA
23	VDAC1	3.5V	-0.3V	1mA	1mA
24	SS/DEL1	8V	-0.3V	1mA	1mA
25	IIN1	8V	-0.3V	5mA	1mA
26	VDRP1	8V	-0.3V	35mA	1mA
27	ROSC/OVP	8V	-0.3V	1mA	1mA
28	PSI_L	8V	-0.3V	1mA	10mA
29	LGND	n/a	n/a	20mA	1mA
31	CLKOUT	8V	-0.3V	100mA	100mA
32	PHSOUT	8V	-0.3V	10mA	10mA
33	PHSIN	8V	-0.3V	1mA	1mA
34	VCCL	8V	-0.3V	1mA	20mA
35	VCCLFB	3.5V	-0.3V	1mA	1mA
36	VCCLDRV	10V	-0.3V	1mA	50mA
37	VRRDY	8V	-0.3V	1mA	20mA
38	SVC/VID3	8V	-0.3V	1mA	1mA
39	SVD/VID2	8V	-0.3V	1mA	10mA
40	VID1	8V	-0.3V	1mA	1mA

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN
 $4.75V \leq VCCL \leq 7.5V$, $-0.3V \leq VOSEN-x \leq 0.3V$, $0^\circ C \leq T_J \leq 100^\circ C$, $7.75 k\Omega \leq ROSC \leq 50 k\Omega$, $CSS/DELx = 0.1\mu F$

ELECTRICAL CHARACTERISTICS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions (unless otherwise specified). Typical values represent the median values, which are related to 25°C.

IR3514 Electrical Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
PVID INTERFACE					
VIDx Input Threshold		0.85	0.95	1.05	V
VIDx Pull-down Resistance		100	175	250	kΩ
PSI_L OUTPUT					
Output Voltage	I(PSI_L) = 3mA		150	300	mV
Pull-up Resistance (to VCCL)		6	10	20	kΩ

IR3514 Electrical Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SVID Interface					
SVC & SVD Input Thresholds	Threshold Increasing	0.850	0.950	1.05	V
	Threshold Decreasing	550	650	750	mV
	Threshold Hysteresis	195	300	405	mV
Bias Current	$0V \leq V(x) \leq 3.5V$, SVD not asserted	-5	0	5	μA
SVD Low Voltage	I(SVD) = 3mA		20	300	mV
SVD Output Fall Time	$0.7 \times VDD$ to $0.3 \times VDD$, $1.425V \leq VDD \leq 1.9V$, $10 pF \leq C_b \leq 400 pF$, C_b =capacitance of one bus line (Note 1)	$20 + 0.1 \times C_b(pF)$		250	ns
Pulse width of spikes suppressed by the input filter	Note 1	97	260	410	ns
Oscillator					
PHSOUT Frequency		-10%	See Figure 2	+10%	kHz
ROSC Voltage		0.57	0.600	0.630	V
CLKOUT High Voltage	I(CLKOUT) = -10 mA, measure V(VCCL) – V(CLKOUT).			1	V
CLKOUT Low Voltage	I(CLKOUT) = 10 mA			1	V
PHSOUT High Voltage	I(PHSOUT) = -1 mA, measure V(VCCL) – V(PHSOUT)			1	V
PHSOUT Low Voltage	I(PHSOUT) = 1 mA			1	V
PHSIN Threshold Voltage	Compare to V(VCCL)	30	50	70	%
VDRP1 Buffer Amplifier					
Input Offset Voltage	$V(VDRP1) - V(IIN1)$, $0.5V \leq V(IIN1) \leq 3.3V$	-8	0	8	mV
Source Current	$0.5V \leq V(IIN1) \leq 3.3V$	2		30	mA
Sink Current	$0.5V \leq V(IIN1) \leq 3.3V$	0.2	0.4	0.6	mA
Unity Gain Bandwidth	Note 1		8		MHz
Slew Rate	Note 1		4.7		V/μs
IIN Bias Current		-1	0	1	μA

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Remote Sense Differential Amplifiers					
Unity Gain Bandwidth	Note 1	3.0	6.4	9.0	MHz
Input Offset Voltage	$0.5V \leq V(\text{VOSENx+}) - V(\text{VOSENx-}) \leq 1.6V$, Note 2	-3	0	3	mV
Source Current	$0.5V \leq V(\text{VOSENx+}) - V(\text{VOSENx-}) \leq 1.6V$	0.5	1	1.7	mA
Sink Current	$0.5V \leq V(\text{VOSENx+}) - V(\text{VOSENx-}) \leq 1.6V$	2	12	18	mA
Slew Rate	$0.5V \leq V(\text{VOSENx+}) - V(\text{VOSENx-}) \leq 1.6V$, Note 1	2	4	8	V/us
VOSEN+ Bias Current	$0.5V < V(\text{VOSENx+}) < 1.6V$		30	50	uA
VOSEN- Bias Current	$-0.3V \leq \text{VOSENx-} \leq 0.3V$, All VID Codes		30	50	uA
VOSEN+ Input Voltage Range	$V(\text{VCCL}) = 7V$			5.5	V
Low Voltage	$V(\text{VCCL}) = 7V$			250	mV
High Voltage	$V(\text{VCCL}) - V(\text{VOUTx})$		0.5	1	V
Soft Start and Delay					
Start Delay	Measure Enable to EAOUTx activation	1	2.9	3.5	ms
Start-up Time	Measure Enable activation to VRRDY	3	8	13	ms
OC Delay Time	$V(\text{IINx}) - V(\text{OCSETx}) = 500 \text{ mV}$	300	650	1000	us
SS/DELx to FBx Input Offset Voltage	With FBx = 0V, adjust V(SS/DELx) until EAOUTx drives high	0.7	1.4	1.9	V
Charge Current		-30	-50	-70	uA
OC Delay/VID Off Discharge Currents	Note 1	30	47	70	uA
Fault Discharge Current		2.5	4.5	6.5	uA
Hiccup Duty Cycle	$I(\text{Fault}) / I(\text{Charge})$	8	10	12	uA/uA
Charge Voltage		3.5	3.9	4.2	V
Delay Comparator Threshold	Relative to Charge Voltage, SS/DELx rising Note 1		80		mV
Delay Comparator Threshold	Relative to Charge Voltage, SS/DELx falling Note 1		120		mV
Delay Comparator Hysteresis	Note 1		40		mV
Discharge Comp. Threshold		150	200	300	mV
Over-Current Comparators					
Input Offset Voltage	$1V \leq V(\text{OCSETx}) \leq 3.3V$	-35	0	35	mV
OCSET Bias Current		-5%	$V_{\text{rosc}}(V) \cdot 1000 / R_{\text{osc}}(K\Omega)$	+5%	uA
2048-4096 Count Threshold	Adjust ROSC value to find threshold		11.4		kΩ
1024-2048 Count Threshold	Adjust ROSC value to find threshold		32.5		kΩ
Error Amplifiers					
System Set-Point Accuracy (Deviation from Table 1, 2, and 3 per test circuit in Figures 2A & 2B)	$VID \geq 1V$	-0.5		0.5	%
	$0.8V \leq VID < 1V$	-5		+5	mV
	$0.5V \leq VID < 0.8V$	-8		+8	mV
Input Offset Voltage	Measure $V(\text{FBx}) - V(\text{VDACx})$. Note 2 $25^\circ\text{C} \leq T_j \leq 100^\circ\text{C}$	-1	0	1	mV
FB1 Bias Current		-5%	$V_{\text{rosc}}(V) \cdot 1000 / R_{\text{osc}}(K\Omega)$	+5%	uA
FB2 Bias Current		-1	0	1	uA
DC Gain	Note 1	100	110	120	dB
Bandwidth	Note 1	20	30	40	MHz
Slew Rate	Note 1	7	12	20	V/μs
Sink Current		0.4	0.85	1	mA
Source Current		5.0	8.5	12.0	mA
Maximum Voltage	$V(\text{VCCL}) - V(\text{EAOUTx})$	500	780	950	mV

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Minimum Voltage			120	250	mV
Open Voltage Loop Detection Threshold	Measure V(VCCL) - V(EAOUT), Relative to Error Amplifier maximum voltage.	125	300	600	mV
Open Voltage Loop Detection Delay	Measure PHSOUT pulse numbers from V(EAOUTx) = V(VCCL) to VRRDY = low.		8		Pulses
Enable Input					
Blanking Time	Noise Pulse < 100ns will not register an ENABLE state change. Note 1	75	250	400	ns
VDAC References					
Source Currents	Includes I(OCSETx)	-8%	$\frac{3000 \cdot V_{rosc}(V)}{ROSC(k\Omega)}$	+8%	μA
Sink Currents	Includes I(OCSETx)	-11%	$\frac{1000 \cdot V_{rosc}(V)}{ROSC(k\Omega)}$	+11%	μA
VRRDY Output					
Under Voltage Threshold - Voutx Decreasing	Reference to VDACx	-365	-315	-265	mV
Under Voltage Threshold - Voutx Increasing	Reference to VDACx	-325	-275	-225	mV
Under Voltage Threshold Hysteresis		5	53	110	mV
Output Voltage	I(VRRDY) = 4mA		150	300	mV
Leakage Current	V(VRRDY) = 5.5V		0	10	μA
VCCL Activation Threshold	I(VRRDY) = 4mA, V(VRRDY) = 300mV		1.73	3.5	V
Over Voltage Protection (OVP) Comparators					
Threshold at Power-up		1.60	1.73	1.83	V
Voutx Threshold Voltage	Compare to V(VDACx)	100	125	150	mV
OVP Release Voltage during Normal Operation	Compare to V(VDACx)	-13	3	20	mV
Threshold during Dynamic VID down		1.66	1.72	1.78	V
Dynamic VID Detect Comparator Threshold		25	50	75	mV
Propagation Delay to IIN	Measure time from V(Voutx) > V(VDACx) (250mV overdrive) to V(IINx) transition to > 0.9 * V(VCCL).		90	180	ns
OVP High Voltage	Measure V(VCCL)-V(ROSC/OVP)	0		1.2	V
OVP Power-up High Voltage	V(VCCLDRV)=1.8V. Measure V(VCCL)-V(ROSC/OVP)	0		0.2	V
Propagation Delay to OVP	Measure time from V(Voutx) > V(VDACx) (250mV overdrive) to V(ROSC/OVP) transition to >1V.		150	300	nS
IIN Pull-up Resistance			5	15	Ω
Open Sense Line Detection					
Sense Line Detection Active Comparator Threshold Voltage		150	200	250	mV
Sense Line Detection Active Comparator Offset Voltage	$V(Voutx) < [V(VOSENx+) - V(LGND)] / 2$	35	62.5	90	mV
VOSEN+ Open Sense Line Comparator Threshold	Compare to V(VCCL)	86.5	89.0	91.5	%
VOSEN- Open Sense Line Comparator Threshold		0.36	0.40	0.44	V
Sense Line Detection Source Currents	V(Voutx) = 100mV	200	500	700	μA

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VCCL Regulator Amplifier					
Reference Feedback Voltage		1.15	1.2	1.25	V
VCCLFB Bias Current		-1	0	1	uA
VCCLDRV Sink Current		10	30		mA
UVLO Start Threshold	Compare to V(VCCL)	89.0	93.5	97.0	%
UVLO Stop Threshold	Compare to V(VCCL)	81.0	85.0	89.0	%
Hysteresis	Compare to V(VCCL)	7.0	8.25	9.5	%
ENABLE, PWROK Inputs					
Threshold Increasing		1.38	1.65	1.94	V
Threshold Decreasing		0.8	0.99	1.2	V
Threshold Hysteresis		470	620	770	mV
Bias Current	$0V \leq V(x) \leq 3.5V$, SVC not asserted	-5	0	5	uA
PWROK VFIX Mode Threshold		3.3V	$(VCCL + 3.3)(V) / 2$	VCCL	V
General					
VCCL Supply Current		4	10	15	mA

Note 1: Guaranteed by design, but not tested in production

Note 2: VDACx Outputs are trimmed to compensate for Error & Amp Remote Sense Amp input offsets

Bold Letters: Critical specs

TBD: To be determined by Applications Engineer

TBS: To be selected by the Design Engineer to facilitate the IC design

PHSOUT FREQUENCY VS RROSC CHART

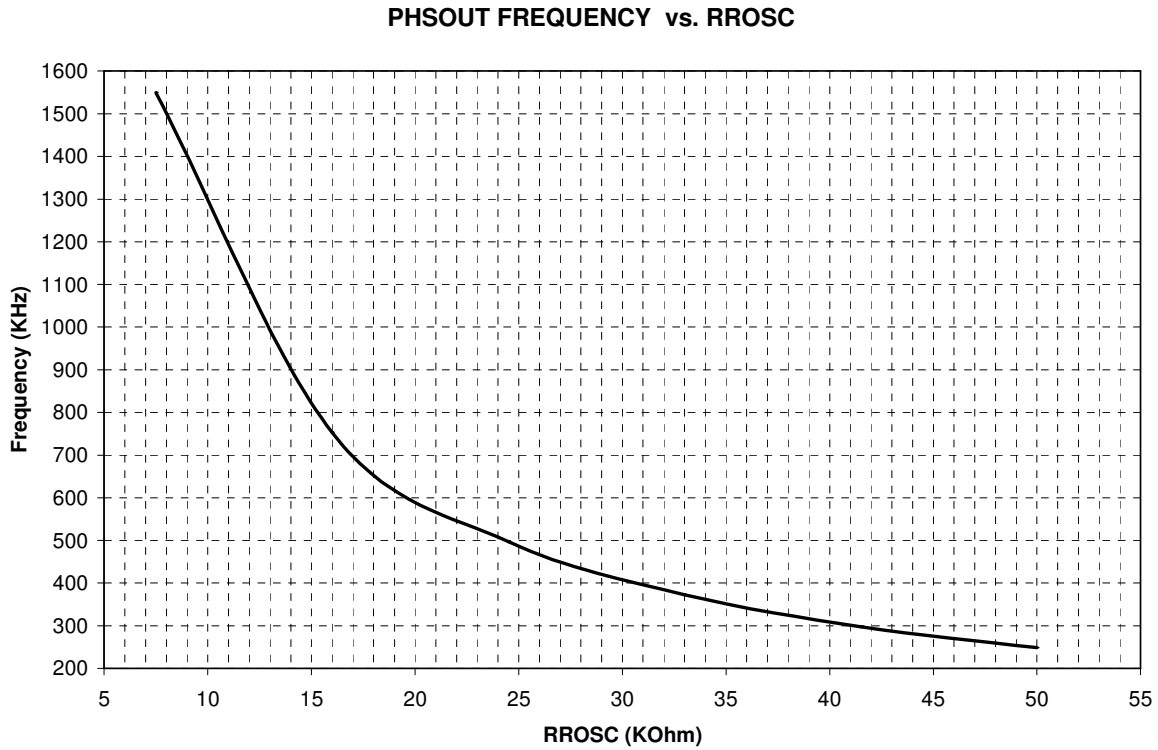


Figure 2 - PHSOUT Frequency vs. R_{ROSC} chart

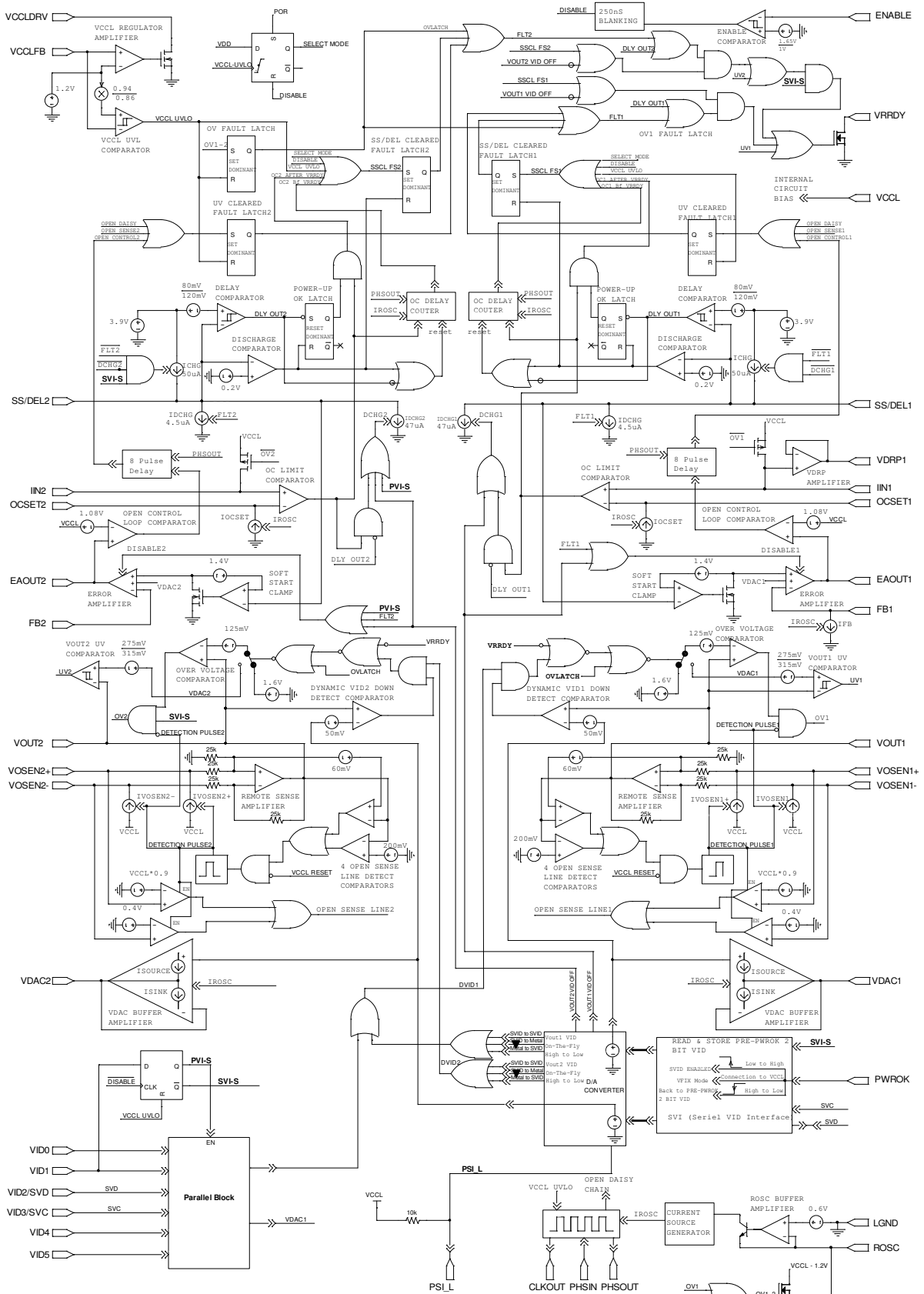


Figure 3 – IR3514 BLOCK DIAGRAM

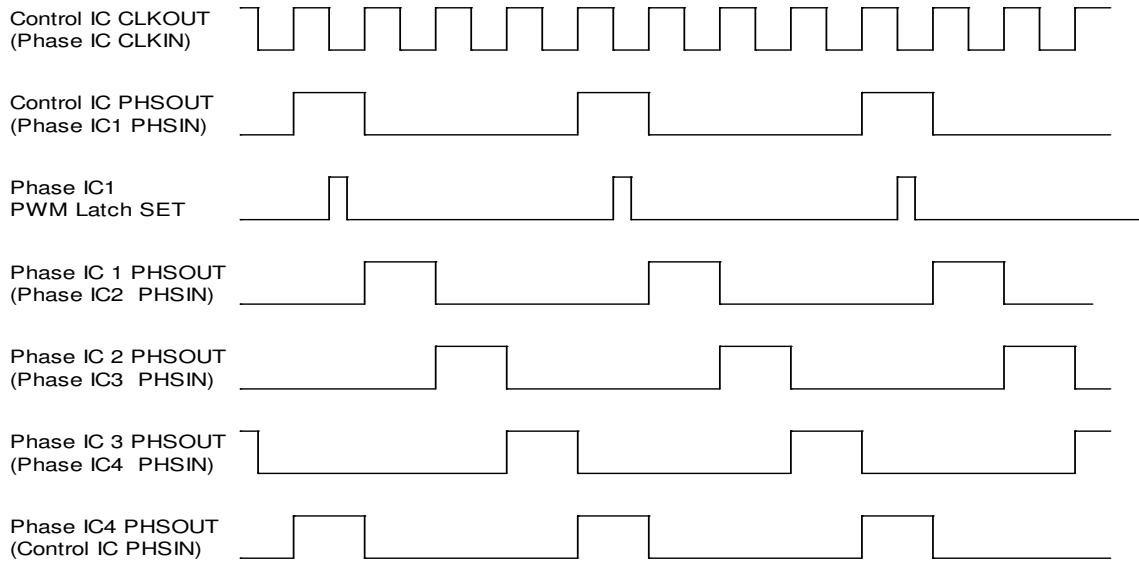


Figure 6 Four Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the phase IC. Upon receiving the falling edge of a clock pulse, the PWM latch is set. This event starts the PWM ramp voltage charge cycle, turns off the low side driver, and turns on the high side driver after a non-overlap blank time. When the PWM ramp voltage exceeds the error amplifier’s output voltage, the PWM latch is reset. This turns off the high side driver and then turns on the low side driver after the non-overlap blank time; it activates the ramp discharge clamp, which quickly discharges the internal PWM ramp capacitor to the output voltage of share adjust amplifier in phase IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go up to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide “single cycle transient response” where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage of the architecture is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Figure 7 depicts PWM operating waveforms under various conditions.

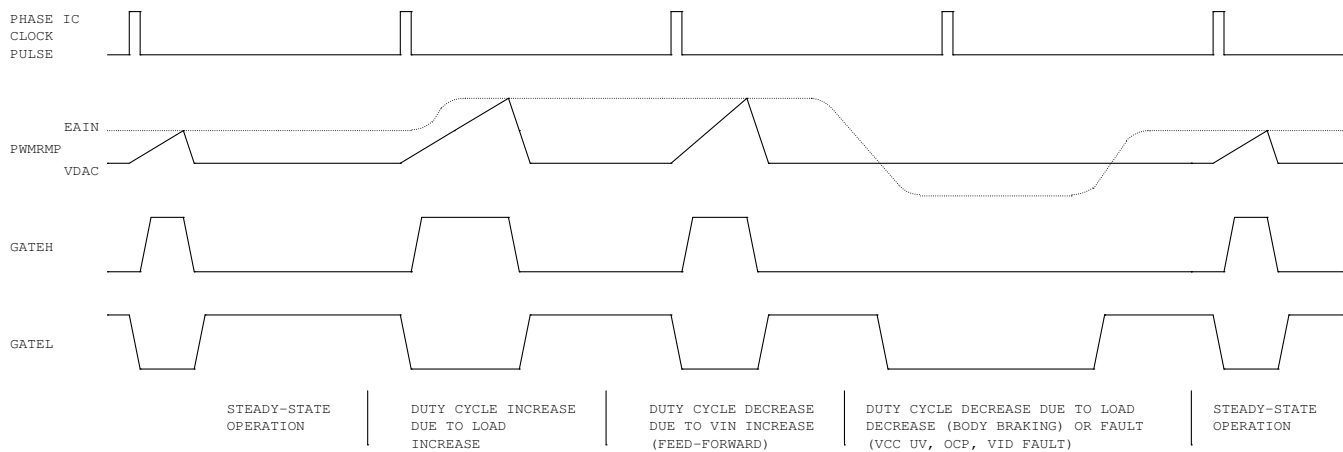


Figure 7 PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L * (I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from V_{out} to $V_{out} + V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L * (I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "body braking" and is accomplished through the "body braking comparator" located in the phase IC. If the error amplifier's output voltage drops below the VDAC voltage or a programmable voltage, this comparator turns off the low side gate driver.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 8. The equation of the sensing network is,

$$v_C(s) = v_L(s) \frac{1}{1 + sR_{CS}C_{CS}} = i_L(s) \frac{R_L + sL}{1 + sR_{CS}C_{CS}}$$

Usually, the resistor R_{CS} and capacitor C_{CS} are chosen so that the time constant of R_{CS} and C_{CS} equals the time constant of the inductor which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across C_{CS} is proportional to the current through L , and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but does affect the AC component of the inductor current.

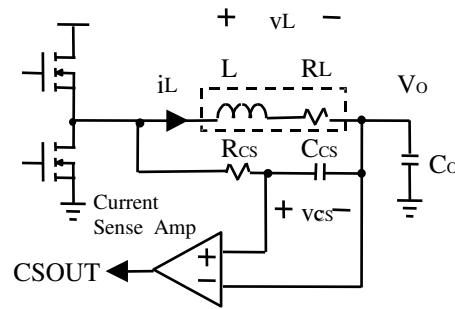


Figure 8 Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current, versus high side or low side sensing, is that the actual output current being delivered to the load is obtained rather than sensing only a peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the phase IC, as shown in Figure 8. Its gain is nominally 32.5 at 25°C, and the 3850 ppm/°C increase in inductor DCR should be compensated in the voltage loop feedback path.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the control IC and other phases through an on-chip 3KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the control IC for voltage positioning and current limit protection.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

IR3514 THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3514 is shown in Figure 3. The following discussions are applicable to either output plane unless otherwise specified.

VID Interface Configuration

The IR3514 Hybrid Control IC can operate in either SVI (Serial VID Interface) or PVI (Parallel VID Interface) mode. The state of VID1 upon ENABLE assertion determines which mode the IR3514 will operate in; VID1=0V enables the SVI Dual Plane Mode, conversely VID1="1" selects PVI Single Plane Mode.

SVI mode has the ability to independently control both the VDD core and VDDNB auxiliary planes required by the CPU. The IR3514 can also receive Power Savings commands through the SVI serial bus and communicate this information to the IR3507 or other Phase ICs with PSI input capabilities.

When operated in PVI (Parallel VID Interface) mode, the IR3514 controls the VDD core plane through 6 Parallel VID bits and the VDDNB auxiliary plane power stage goes to high impedance.

Serial VID Control (VID1="0" at ENABLE assertion)

The two Serial VID Interface (SVID) pins SVC and SVD are used to program the Boot VID voltage upon assertion of ENABLE while PWROK is de-asserted. See Table 2 for the 2-bit Boot VID codes. Both VDAC1 and VDAC2 voltages will be programmed to the Boot VID code until PWROK is asserted. The Boot VID code is stored by the IR3514 to be utilized again if PWROK is de-asserted.

Serial VID communication from the processor is enabled after the PWROK is asserted. Addresses and data are serially transmitted in 8-bit words. The IR3514 has three fixed addresses to control VDAC1, VDAC2, or both VDAC1 and VDAC2 (See Table 6 for addresses). The first data bit of the SVID data word represents the PSI bit which is passed on to the phase ICs via the IR3514 PSI_L pin. PSI_L is pulled high by an internal 10K resistor to VCCL when data bit 7 of an SVID command is high. The remaining data bits SVID[6:0] select the desired VDACx regulation voltage as defined in Table 3. SVID[6:0] are the inputs to the Digital-to-Analog Converter (DAC) which then provides an analog reference voltage to the transconductance type buffer amplifier. This VDACx buffer provides a system reference on the VDACx pin. The VDACx voltage along with error amplifier and remote sense differential amplifier input offsets are post-package trimmed to provide a 0.5% system set-point accuracy, as measured in Figures 4A and 4B. VDACx slew rates are programmable by properly selecting external series RC compensation networks located between the VDACx and the LGND pins. The VDACx source and sink currents are derived off the external oscillator frequency setting resistor, R_{ROSC}. The programmable slew rate enables the IR3514 to smoothly change the regulated output voltage throughout VID transitions resulting in a power supply input and output capacitor inrush currents, along with output voltage overshoot, to be well controlled.

The two Serial VID Interface (SVID) pins SVC and SVD can also program the VFIX VID voltage upon assertion of ENABLE while PWROK is equal to VCCL. See Table 3 for the 2-bit VFIX VID codes. Both VDAC1 and VDAC2 voltages will be programmed to the VFIX code. The SVC and SVD pins require external pull-up biasing and should not be floated.

Bits	Description
7	PSI_L: = 0 means the processor is at an optimal load for the regulator(s) to enter power-saving mode. = 1 means the processor is not at an optimal load for the regulator(s) to enter power-saving mode.
6:0	SVID[6:0] as defined in Table 4.

Table 1. Serial VID 8-Bit Data Field Encoding

Table 2 – Pre-PWROK 2 bit “metal” VID codes

SVC	SVD	Output Voltage(V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Table 3 – VFIX mode 2 bit VID Codes

SVC	SVD	Output Voltage(V)
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

Table 4 - AMD 7 BIT SVID CODES

SVID [6:0]	Voltage (V)	SVID [6:0]	Voltage (V)	SVID [6:0]	Voltage (V)	SVID [6:0]	Voltage (V)
000_0000	1.5500	010_0000	1.1500	100_0000	0.7500	110_0000	0.5000
000_0001	1.5375	010_0001	1.1375	100_0001	0.7375	110_0001	0.5000
000_0010	1.5250	010_0010	1.1250	100_0010	0.7250	110_0010	0.5000
000_0011	1.5125	010_0011	1.1125	100_0011	0.7125	110_0011	0.5000
000_0100	1.5000	010_0100	1.1000	100_0100	0.7000	110_0100	0.5000
000_0101	1.4875	010_0101	1.0875	100_0101	0.6875	110_0101	0.5000
000_0110	1.4750	010_0110	1.0750	100_0110	0.6750	110_0110	0.5000
000_0111	1.4625	010_0111	1.0625	100_0111	0.6625	110_0111	0.5000
000_1000	1.4500	010_1000	1.0500	100_1000	0.6500	110_1000	0.5000
000_1001	1.4375	010_1001	1.0375	100_1001	0.6375	110_1001	0.5000
000_1010	1.4250	010_1010	1.0250	100_1010	0.6250	110_1010	0.5000
000_1011	1.4125	010_1011	1.0125	100_1011	0.6125	110_1011	0.5000
000_1100	1.4000	010_1100	1.0000	100_1100	0.6000	110_1100	0.5000
000_1101	1.3875	010_1101	0.9875	100_1101	0.5875	110_1101	0.5000
000_1110	1.3750	010_1110	0.9750	100_1110	0.5750	110_1110	0.5000
000_1111	1.3625	010_1111	0.9625	100_1111	0.5625	110_1111	0.5000
001_0000	1.3500	011_0000	0.9500	101_0000	0.5500	111_0000	0.5000
001_0001	1.3375	011_0001	0.9375	101_0001	0.5375	111_0001	0.5000
001_0010	1.3250	011_0010	0.9250	101_0010	0.5250	111_0010	0.5000
001_0011	1.3125	011_0011	0.9125	101_0011	0.5125	111_0011	0.5000
001_0100	1.3000	011_0100	0.9000	101_0100	0.5000	111_0100	0.5000
001_0101	1.2875	011_0101	0.8875	101_0101	0.5000	111_0101	0.5000
001_0110	1.2750	011_0110	0.8750	101_0110	0.5000	111_0110	0.5000
001_0111	1.2625	011_0111	0.8625	101_0111	0.5000	111_0111	0.5000
001_1000	1.2500	011_1000	0.8500	101_1000	0.5000	111_1000	0.5000
001_1001	1.2375	011_1001	0.8375	101_1001	0.5000	111_1001	0.5000
001_1010	1.2250	011_1010	0.8250	101_1010	0.5000	111_1010	0.5000
001_1011	1.2125	011_1011	0.8125	101_1011	0.5000	111_1011	0.5000
001_1100	1.2000	011_1100	0.8000	101_1100	0.5000	111_1100	OFF
001_1101	1.1875	011_1101	0.7875	101_1101	0.5000	111_1101	OFF
001_1110	1.1750	011_1110	0.7750	101_1110	0.5000	111_1110	OFF
001_1111	1.1625	011_1111	0.7625	101_1111	0.5000	111_1111	OFF

AMD 6-Bit Parallel VID Control (VID1="1" at ENABLE assertion)

PVI mode is enabled if VID1 is equal to logic 1 when ENABLE is asserted. VID1 can then be used along with the other VIDx bits to program VDACC1 to AMD 6-bit Parallel VID codes shown in Table 5. Output 2 is shut down with VID2 defaulting to 0.5V, SS/DEL2 is held at 0V, and EAOUT2 = 0V which places all Output 2 phase ICs in high impedance mode. All Output 2 fault and OVP communication to VRRDY, ROOSC and IIN2 are disabled. PWROK and PSI_L bits are ignored in PVI mode. Pins VID0, VID1, VID4 and VID5 have 175 kΩ resistors to LGND and require external pull-up biasing. VID2/SVD and VID3/SVC do not have internal resistor pull downs and also require external pull-up biasing.

Table 5 – AMD 6-BIT PVID TABLE

VID5	VID4	VID3	VID2	VID1	VID0	Vout (V)	VID5	VID4	VID3	VID2	VID1	VID0	Vout(V)
0	0	0	0	0	0	1.5500	1	0	0	0	0	0	0.7625
0	0	0	0	0	1	1.5250	1	0	0	0	0	1	0.7500
0	0	0	0	1	0	1.5000	1	0	0	0	1	0	0.7375
0	0	0	0	1	1	1.4750	1	0	0	0	1	1	0.7250
0	0	0	1	0	0	1.4500	1	0	0	1	0	0	0.7125
0	0	0	1	0	1	1.4250	1	0	0	1	0	1	0.7000
0	0	0	1	1	0	1.4000	1	0	0	1	1	0	0.6875
0	0	0	1	1	1	1.3750	1	0	0	1	1	1	0.6750
0	0	1	0	0	0	1.3500	1	0	1	0	0	0	0.6625
0	0	1	0	0	1	1.3250	1	0	1	0	0	1	0.6500
0	0	1	0	1	0	1.3000	1	0	1	0	1	0	0.6375
0	0	1	0	1	1	1.2750	1	0	1	0	1	1	0.6250
0	0	1	1	0	0	1.2500	1	0	1	1	0	0	0.6125
0	0	1	1	0	1	1.2250	1	0	1	1	0	1	0.6000
0	0	1	1	1	0	1.2000	1	0	1	1	1	0	0.5875
0	0	1	1	1	1	1.1750	1	0	1	1	1	1	0.5750
0	1	0	0	0	0	1.1500	1	1	0	0	0	0	0.5625
0	1	0	0	0	1	1.1250	1	1	0	0	0	1	0.5500
0	1	0	0	1	0	1.1000	1	1	0	0	1	0	0.5375
0	1	0	0	1	1	1.0750	1	1	0	0	1	1	0.5250
0	1	0	1	0	0	1.0500	1	1	0	1	0	0	0.5125
0	1	0	1	0	1	1.0250	1	1	0	1	0	1	0.5000
0	1	0	1	1	0	1.0000	1	1	0	1	1	0	0.4875
0	1	0	1	1	1	0.9750	1	1	0	1	1	1	0.4750
0	1	1	0	0	0	0.9500	1	1	1	0	0	0	0.4625
0	1	1	0	0	1	0.9250	1	1	1	0	0	1	0.4500
0	1	1	0	1	0	0.9000	1	1	1	0	1	0	0.4375
0	1	1	0	1	1	0.8750	1	1	1	0	1	1	0.4250
0	1	1	1	0	0	0.8500	1	1	1	1	0	0	0.4125
0	1	1	1	0	1	0.8250	1	1	1	1	0	1	0.4000
0	1	1	1	1	0	0.8000	1	1	1	1	1	0	0.3875
0	1	1	1	1	1	0.7750	1	1	1	1	1	1	0.3750

Output 1 (VDD) Adaptive Voltage Positioning

The IR3514 provides Adaptive Voltage Positioning (AVP) on the output1 plane only. AVP helps reduce the peak to peak output voltage excursions during load transients and reduces load power dissipation at heavy load. The circuitry related to the voltage positioning is shown in Figure 9. Resistor R_{FB1} is connected between the error amplifiers inverting input pin FB1 and the remote sense differential amplifier output, VOUT1. An internal current sink on the FB1 pin along with R_{FB1} provides programmability of a fixed offset voltage above the VDACC1 voltage. The offset voltage generated across R_{FB1} forces the converter's output voltage higher to maintain a balance at the error amplifiers inputs. The FB1 sink current is derived by the external resistor R_{ROSC} that programs the oscillator frequency.

The VDRP1 pin voltage is a buffered reproduction of the IIN1 pin which is connected to the current share bus ISHARE. The voltage on ISHARE represents the system average inductor current information. At each phase IC, an RC network across the inductor provides current information which is gained up 32.5X and then added to the VDACC_x voltage. This phase current information is provided on the ISHARE bus via a 3K resistor in the phase ICs.

Output 1 Inductor DCR Temperature Compensation

A negative temperature coefficient (NTC) thermistor can be used for output1 inductor DCR temperature compensation. The thermistor should be placed close to the output1 inductors and connected in parallel with the feedback resistor, as shown in Figure 10. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

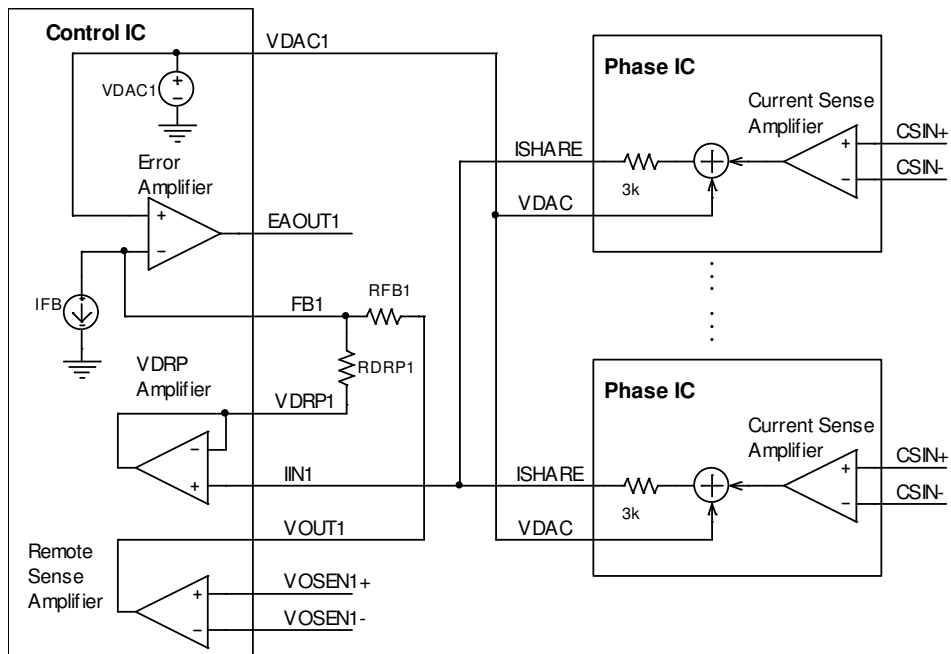


Figure 9 Adaptive voltage positioning

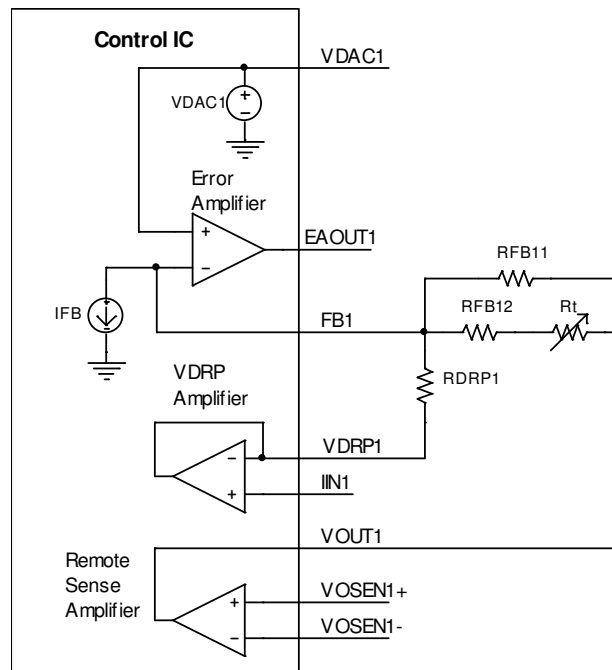


Figure 10 Temperature compensation of Output1 inductor DCR

Remote Voltage Sensing

VOSENX+ and VOSENX- are used for remote sensing and connected directly to the load. The remote sense differential amplifiers with high speed, low input offset and low input bias current ensure accurate voltage sensing and fast transient response.

Start-up Sequence

The IR3514 has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL_x and LGND pins controls soft start timing, over-current protection delay and hiccup mode timing. Constant current sources and sinks control the charge and discharge rates of the SS/DEL_x.

Figure 11 depicts the SVID start-up sequence. If the ENABLE input is asserted and there are no faults, the SS/DEL_x pin will begin charging, the pre-PWROK 2 bit Boot VID codes are read and stored, and both VDAC pins transition to the pre-PWROK Boot VID code. The error amplifier output EAOUT_x is clamped low until SS/DEL_x reaches 1.4V. The error amplifier will then regulate the converter's output voltage to match the V(SS/DEL_x)-1.4V offset until the converter output reaches the 2-bit Boot VID code. The SS/DEL_x voltage continues to increase until it rises above the threshold of Delay Comparator where the VRRDY output is allowed to go high. The SVID interface is activated upon PWROK assertion and the VDAC_x along with the converter output voltage will change in response to any SVID commands.

The PVI Single Plane Mode start-up sequence is the same as the SVID startup sequence with the exceptions that only SS/DEL1 will be allowed to charge and there is no Boot VID voltage. PWROK is ignored.

The Error Amplifier output EAOUT_x is clamped low until SS/DEL_x reaches 1.4V. The error amplifier will then regulate the converter's output voltage to match the SS/DEL_x voltage less the 1.4V offset until the converter output reaches the pre-PWROK 2 bit metal VID code. The SS/DEL_x voltage continues to increase until it rises above the threshold of Delay Comparator. The VRRDY output is then de-asserted (allowed to go high). Upon PWROK assertion the SVID interface is activated and VDAC_x and converter output will change in response to any SVID commands.

VCCL under voltage, over current, or a low signal on the ENABLE input immediately sets the fault latch, which causes the EAOUT pin to drive low, thereby turning off the phase IC drivers. The VRRDY pin also drives low and SS/DEL_x discharges to 0.2V. If the fault has cleared, the fault latch will be reset by the SS/DEL_x discharge comparator allowing another soft start charge cycle to occur.

Other fault conditions, such as output over voltage, open VOSNS sense lines, or an open phase timing daisy chain set a different group of fault latches that can only be reset by cycling VCCL power. These faults discharge SS/DEL_x, pull down EAOUT_x and drive VRRDY low.

SVID OFF codes turn off the converter by discharging SS/DEL_x and pulling down EAOUT_x but do not drive VRRDY low. Upon receipt of a non-off SVID code the converter will re-soft start and transition to the voltage represented by the SVID code as shown in Figure 11.

The converter can be disabled by pulling the SS/DEL_x pins below 0.6V.

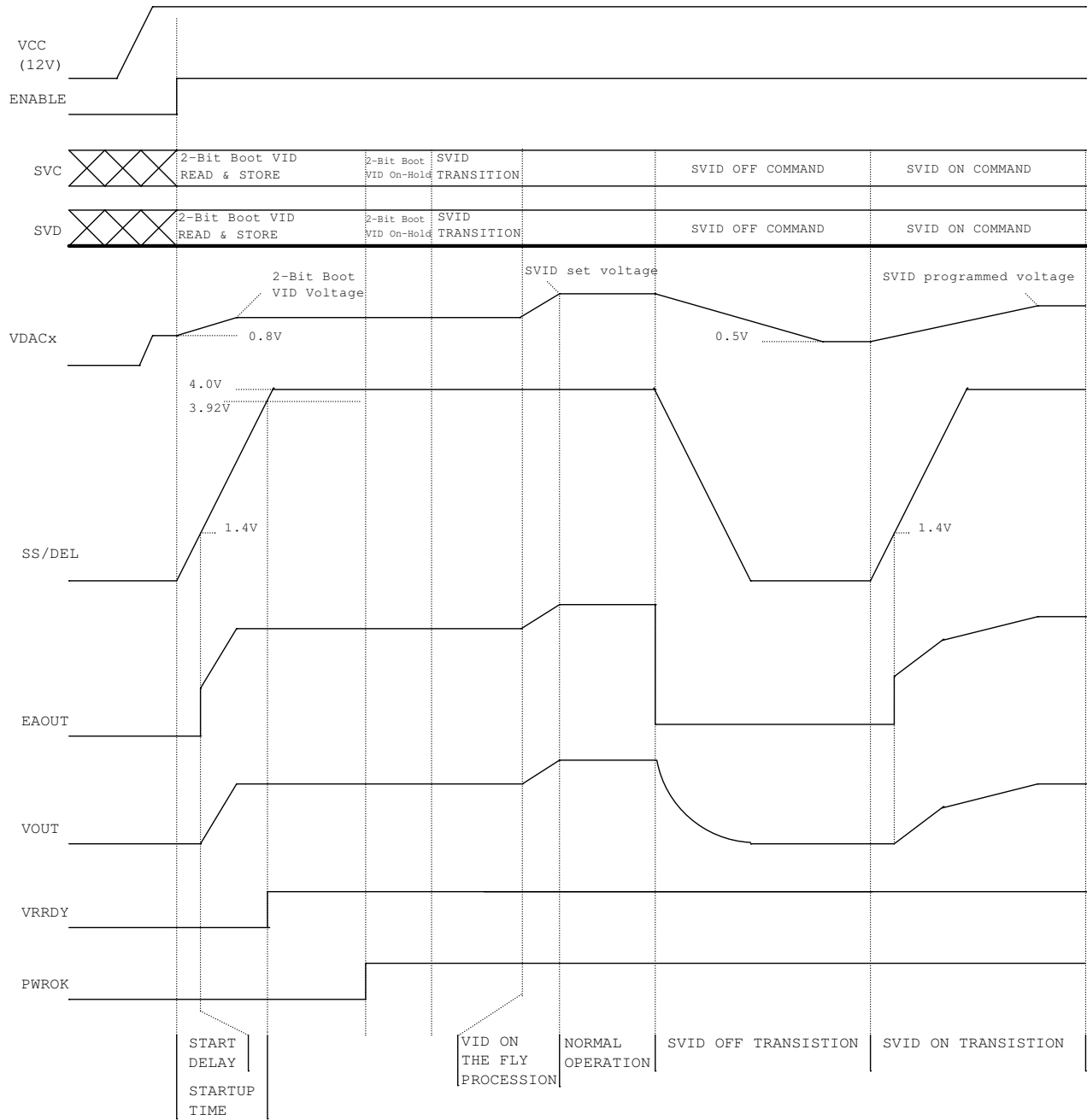


Figure 11 SVID Start-up Sequence Transitions

Serial VID Interface Protocol and VID-on-the-fly Transition

The IR3514 supports the AMD SVI bus protocol and the AMD Server and desktop SVI wire protocol which is based on fast-mode I²C. SVID commands from an AMD processor are communicated through SVID bus pins SVC and SVD. The SVC pin of the IR3514 does not have an open drain output since AMD SVID protocol does not support slave clock stretching.

The IR3514 transitions from a 2-bit Boot VID mode to SVI mode upon assertion of PWROK. The SMBus *send byte* protocol is used by the IR3514 VID-on-the-fly transactions. The IR3514 will wait until it detects a start bit which is defined as an SVD falling edge while SVC is high. A 7bit address code plus one write bit (low) should then follow the start bit. This address code will be compared against an internal address table and the IR3514 will reply with an acknowledge ACK bit if the address is one of the three stored addresses otherwise the ACK bit will not be sent out. The SVD pin is pulled low by the IR3514 to generate the ACK bit. Table 6 has the list of addresses recognized by the IR3514.

The processor should then transmit the 8-bit data word immediately following the ACK bit. Data bit 7 is the PSI_L bit which is followed by the 7Bit AMD code. The IR3514 replies again with an ACK bit once the data is received. If the received data is not a VID-OFF command, the IR3514 immediately changes the DAC analog outputs to the new target. VDACC1 and VDACC2 then slew to the new VID voltages. See Figure 12a and 12b for a send byte examples.

Table 6 - SVI Send Byte Address Table

SVI Address [6:0] + Wr	Description
110xx100b	Set VID only on Output 1
110xx010b	Set VID only on Output 2
110xx110b	Set VID on both Output 1 and Output 2

Note: 'x' in the above Table 4 means the bit could be either '1' or '0'.

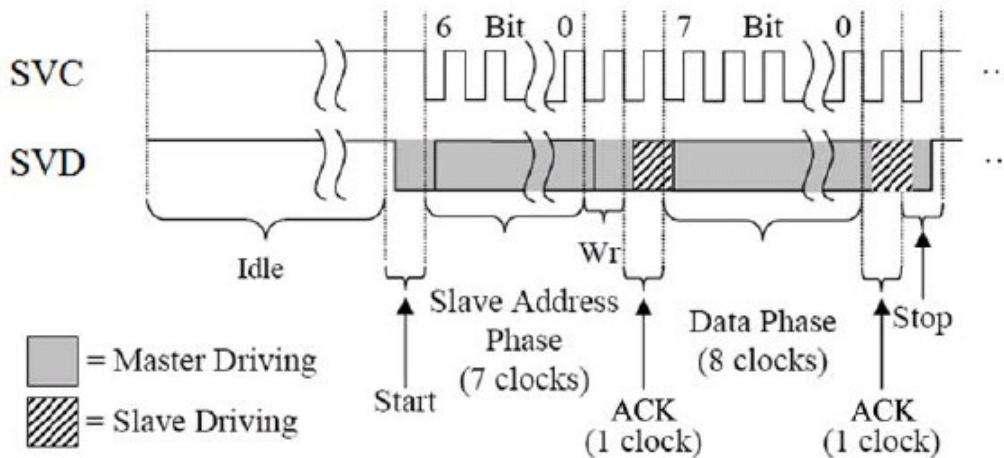


Figure 12a Send Byte Example

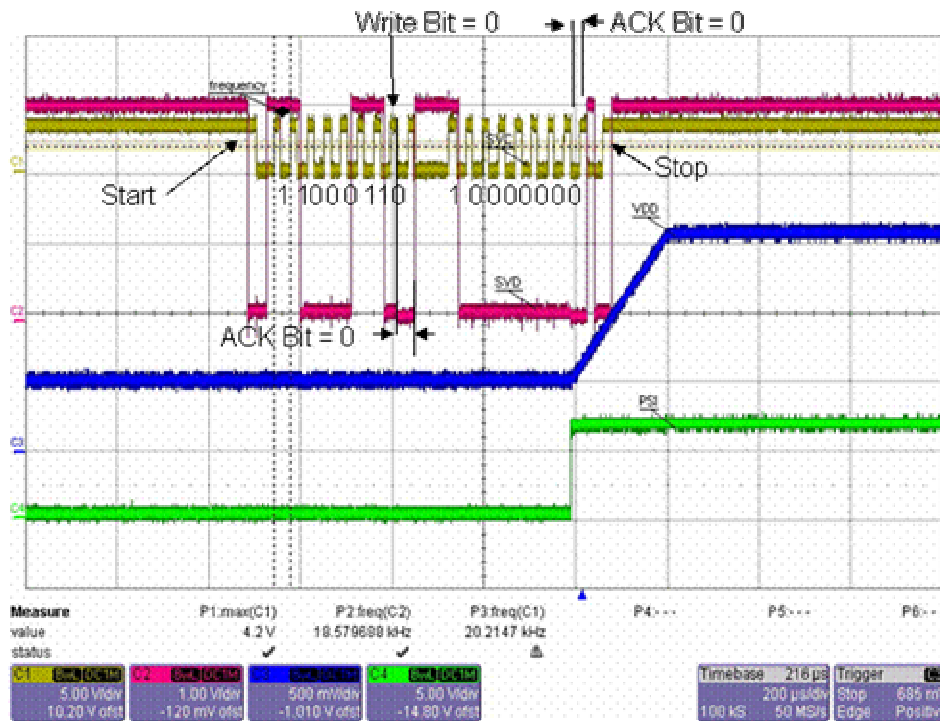


Figure 12b Sending 1.55 VID to both outputs and turning off PSI mode

Over-Current Hiccup Protection after Soft Start

The over current limit threshold is set by a resistor connected between OCSETx and VDACCx pins. Figure 13 shows the hiccup over-current protection with delay after VRRDY is asserted. The delay is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions.

If the IINx pin voltage, which is proportional to the average current plus VDACCx voltage, exceeds the OCSETx voltage after VRRDY is asserted, it will initiate the discharge of the capacitor at SS/DELx through the discharge current 47uA. If the over-current condition persists long enough for the SS/DELx capacitor to discharge below the 120mV offset of the delay comparator, the fault latch will be set pulling the error amplifier's output low and inhibiting switching in the phase ICs and de-asserting the VRRDY signal. The SS/DEL capacitor will then continue to discharge through the 4.5uA discharge current until it reaches 200 mV and the fault latch is reset allowing a normal soft start to occur. The output current is not controlled during the delay time. If an over-current condition is again encountered during the soft start cycle, the over-current action will repeat and the converter will be in hiccup mode.