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FEATURES

- Dual output 3+1 phase PWM Controller
- Easiest layout and fewest pins in the industry
- Fully supports AMD® SVI1 & SVI2 with dual OCP and Intel® VR12 & VR12.5
- Overclocking & Gaming Mode
- Switching frequency from 200kHz to 2MHz per phase
- IR Efficiency Shaping Features including Dynamic Phase Control and Automatic Power State Switching
- Programmable 1-phase operation for Light Loads and Active Diode Emulation for Very Light Loads
- IR Adaptive Transient Algorithm (ATA) on both loops minimizes output bulk capacitors and system cost
- Auto-Phase Detection with autocompensation
- Per-Loop Fault Protection: OVP, UVP, OCP, OTP
- I2C/SMBus/PMBus system interface for telemetry of Temperature, Voltage, Current & Power for both loops
- Multiple Time Programming (MTP) with integrated charge pump for easy custom configuration
- Compatible with IR ATL and 3.3V tri-state Drivers
- +3.3V supply voltage; -40°C to 85°C ambient operation
- Pb-Free, Halogen Free, RoHS, 6x6mm, 40-pin, 0.5 mm pitch QFN

DESCRIPTION

The IR35211 is a dual loop digital multi-phase buck controller designed for CPU voltage regulation and is fully compliant to AMD® SVI1 & SVI2 Rev 1.2 & Intel[®] VR12 Rev 1.5 PWM specification and VR12.5 Rev 1.3 PWM specification.

The IR35211 includes IR's Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. IR's Dynamic Phase Control adds/drops active phases based upon load current and can be configured to enter 1-phase operation and diode emulation mode automatically or by command.

IR's unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear digital PWM algorithms, minimizes output bulk capacitors and Multiple Time Programmable (MTP) storage saves pins and enables a small package size. Device configuration and fault parameters are easily defined using the IR Digital Power Design Center (DPDC) GUI and stored in on-chip MTP.

The IR35211 provides extensive OVP, UVP, OCP and OTP fault protection and includes thermistor based temperature sensing with VRHOT signal.

The IR35211 includes numerous features like register diagnostics for fast design cycles and platform differentiation, simplifying VRD design and enabling fastest time-to-market (TTM) with "set-and-forget" methodology.

APPLICATIONS

- AMD® SVI1 & SVI2, Intel® VR12 & VR12.5 based systems
- Desktop & Notebook CPU VRs
- High Performance Graphics Processors

Base Part		Standa	Orderable	
Number	Fackage Type	Form	Quantity	Part Number
IR35211	QFN 6 mm x 6 mm	Tape and Reel	3000	IR35211MxxyyTRP ¹
IR35211	QFN 6 mm x 6 mm	Tape and Reel	3000	IR35211MTRPBF
IR35211	QFN 6 mm x 6 mm	Tray	4900	IR35211MTYPBF

ORDERING INFORMATION

Notes 1: Customer Specific Configuration File, where xx = Customer ID and yy = Configuration File (Codes assigned by IR Marketing).

1

ORDERING INFORMATION



20

SM_CLK

2

11

VINSEN

12

SV_ADDR SVT/ SV_ALERT#

VDDIO/

13

14

SV_CLK/ VIDSEL1 15

SV_DIO/ VIDSEL0

Figure 1: IR35211 Pin Diagram

16

VRHOT_ICRIT#

17

E

18

ADDR_PROT

19

SM_DIO

FUNCTIONAL BLOCK DIAGRAM





3

TYPICAL APPLICATION DIAGRAM





4

PIN DESCRIPTIONS

PIN#	PIN NAME	TYPE	PIN DESCRIPTION		
1	RCSP	A [O]	Resistor Current Sense Positive Loop#1. This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop #1.		
2	RCSM	A [O]	Resistor Current Sense Minus Loop#1. This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop #1.		
3	VRDY2	D [O]	/oltage Regulator Ready Output (Loop #2). Open-drain output that asserts high when the VR nas completed soft-start to Loop #2 boot voltage. It is pulled up to an external voltage rail through and external resistor.		
4	VSEN	A [l]	Voltage Sense Input Loop#1. This pin is connected directly to the VR output voltage of Loop #1 at the load and should be routed differentially with VRTN.		
5	VRTN	A [I]	Voltage Sense Return Input Loop#1. This pin is connected directly to Loop#1 ground at the load and should be routed differentially with VSEN.		
6	RRES	A [B]	Current Reference Resistor. A 1% 7.5kohm resistor is connected to this pin to set an internal precision current reference.		
7	TSEN1	A [I]	NTC Temperature Sense Input Loop #1. An NTC network is connected to this pin to measure temperature for VRHOT. Refer to page 44 for details.		
8	V18A	A [O]	1.8V Decoupling. A capacitor on this pin provides decoupling for the internal 1.8V supply.		
9	VRDY1	D [O]	Voltage Regulator Ready Output (Loop #1). Open-drain output that asserts high when the VR has completed soft-start to Loop #1 boot voltage. It is pulled up to an external voltage rail through and external resistor.		
			Power OK Input (AMD). An input that when low indicates to return to the Boot voltage and when high indicates to use the SVI bus to set the the output voltage.		
10	PWROK/ EN_L2/	D [l]	VR Enable for Loop 2. When configured, ENABLE for Loop 2 is an active high system input to power-on Loop 2, provided Vin and Vcc are present. ENABLE is not pulled up on the controller. When ENABLE is pulled low, the controller de-asserts VR READY2 and shuts down loop 2 only.		
			Intel Mode Pin. If configured this pin will select whether the controller is in VR12 or VR12.5 Mode. If pulled low (Logic 0) the controller will operate in VR12.5 mode, if pulled high (Logic 1) the controller will operate in VR12 mode.		
11	VINSEN	A [I]	Voltage Sense Input. This is used to detect and measure a valid input supply voltage (typically 5V-19V) to the VR. Refer to page 16 for details.		
10	VDDIO/	A [P]/	VDDIO Input (AMD). This pin provides the voltage to which the SVT line and the SVD Acknowledge are driven high.		
12	SV_ADDR	D [I]	SVID Address Input (INTEL). A resistor to ground on this pin defines the SVID address which is latched when Vcc becomes valid. Requires a 0.01μ F bypass capacitors to GND.		
	SVT/		SVI Telemetry Output (AMD). Telemetry and VOTF information output by the IR35211.		
13	SV_ALERT#	D [O]	Serial VID ALERT# (INTEL). SVID ALERT# is pulled low by the controller to alert the CPU of new VR12/12.5 Status.		
	SV CLK/		Serial VID Clock Input. Clock input driven by the CPU Master.		
14	VIDSEL1	D [I]	Parallel VID Selection. When configured in GPU parallel VID mode, this is pin is used to select the VID voltage registers.		
45	SV DIO/	D [B]/	Serial VID Data I/O. Is a bi-directional serial line over which the CPU Master issues commands to controller/s slave/s.		
15	VIDSEL0	D [I]	Parallel VID Selection. When configured in GPU parallel VID mode, this is pin is used to select the VID voltage registers.		
16	VRHOT_ICRIT#	D [O]	VRHOT_ICRIT# Output. Active low alert pin that can be programmed to assert if temperature or average load current exceeds user-definable thresholds.		
17	EN	D [I]	VR Enable Input. ENABLE is an active high system input to power-on the regulator, provided Vin and Vcc are present. ENABLE is not pulled up on the controller. When ENABLE is pulled low, the controller de-asserts VR READY and shuts down the regulator.		
18	ADDR_PROT	D [B]	Bus Address & I2C Bus Protection. A resistor to ground on this pin defines the I2C address offset which is latched when Vcc becomes valid. Subsequently, this pin becomes a logic input to enable or disable communication on the I2C bus offset when protection is enabled.		
19	SM_DIO	D [B]	Serial Data Line I/O. I2C/SMBus/PMBus bi-directional serial data line.		

Dual Output Digital Multi-Phase Controller

20	SM_CLK	D [l]	Serial Clock Input. I2C/SMBus/PMBUS serial clock line. Interface is rated to 1 MHz.	
21	NC		Do Not Connect.	
22 TSEN2/	TSEN2/	TSEN2/	A [O]/	Auxiliary Voltage Sense Input. As Auxiliary Voltage Sense, it monitors an additional power supply to ensure that both the IR35211 Vcc and other voltages (such as VCC to the driver) are operational.
	VAUXSEN	A [i]	NTC Temerature Sense Input Loop #2. An NTC network is connected to this pin to measure temperature for VRHOT. Refer to page 44 for details.	
23 - 25	PWM1 – PWM3	A [O]	Phase 1-3 Pulse Width Modulation Outputs. PWM signal pin which is connected to the input of an external MOSFET gate driver. Refer to page 33 section for unused/disabled phases. The power-up state is high-impedance until ENABLE goes active.	
26	PWM1_L2	A [O]	Loop 2 Pulse Width Modulation Outputs. PWM signal pin which is connected to the input of an external MOSFET gate driver. Refer to page 33 section for unused/disabled phases. The power-up state is high-impedance until ENABLE goes active.	
27	VRTN_L2	A [I]	Voltage Sense Return Input Loop#2. This pin is connected directly to Loop#2 ground at the load and should be routed differentially with VSEN_L2.	
28	VSEN_L2	A [I]	Voltage Sense Input Loop#2. This pin is connected directly to the VR output voltage of Loop #2 at the load and should be routed differentially with VRTN_L2.	
29	VCC	A [l]	Input Supply Voltage. 3.3V supply to power the device.	
30	RCSM_L2	A [I]	Resistor Current Sense Minus Loop#2. This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop #2.	
31	RCSP_L2	A [I]	Resistor Current Sense Positive Loop#2. This pin is connected to an external network to set the load line slope, bandwidth and temperature compensation for Loop #2.	
32	ISEN 1_L2	A [I]	Loop 2 Phase 1 Current Sense Input. Loop 2 Phase 1 sensed current input (+). Short to pin 38 if not used.	
33	IRTN 1_L2	A [I]	Loop 2 Phase 1 Current Sense Return Input. Loop 2 Phase 1 sensed current input return (-). Short to pin 37 if not used.	
34	NC		Do Not Connect.	
35	ISEN 3	A [l]	Phase 3 Current Sense Input. Phase 3 sensed current input (+). Short to pin 44 if not used.	
36	IRTN 3	A [I]	Phase 3 Current Sense Return Input. Phase 3 sensed current input return (-). Short to pin 43 if not used.	
37	ISEN 2	A [l]	Phase 2 Current Sense Input. Phase 2 sensed current input (+). Short to pin 46 if not used.	
38	IRTN 2	A [I]	Phase 2 Current Sense Return Input. Phase 2 sensed current input return (-). Short to pin 45 if not used.	
39	ISEN 1	A [I]	Phase 1 Current Sense Input. Phase 1 sensed current input (+)	
40	IRTN 1	A [I]	Phase 1 Current Sense Return Input. Phase 1 sensed current input return (-)	
41 (PAD)	GND		Ground. Ground reference for the IC. The large metal pad on the bottom must be connected to Ground.	

Note 1: A - Analog; D – Digital; [I] – Input; [O] – Output; [B] – Bi-directional; [P] - Power

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC)	GND-0.3V to 4.0V
RCSPx, RCSMx	0 to 2.2V
VSEN, VSEN_L2, VRTN, VRTN_L2, ISENx, IRTNx	GND-0.2V to 2.7V
RRES, V18A, TSEN, TSEN2, VINSEN, VAUXSEN	GND-0.2V to 2.2V
VDDIO ,SV_CLK, SV_DIO, SVT#	GND-0.3V to VCC
PWMx, VIDSELx	GND-0.3V to VCC
VRDY1, VRDY2, EN, PWROK, ADDR_PROT, VRHOT_ICRIT#	GND-0.3V to VCC
SM_DIO, SM_CLK	GND-0.3V to 5.5V
ESD Rating	
Human Body Model	2000V
Machine Model	200V
Charge Device Model	1000V
Thermal Information	
Thermal Resistance $(\theta_{JA} \& \theta_{JC})^1$	29°C/W & 3°C/W
Maximum Operating Junction Temperature	-40°C to +125°C
Maximum Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Note: 1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

Recommended Operating Ambient Temperature Range	0°C to 85°C
Supply Voltage Range	+2.90V to +3.63V

The electrical characteristics table lists the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply	VCC/GND					
Supply Voltage	V _{cc}		2.90	3.3	3.63	V
Supply Current	I _{vcc}	No PWM switching	95	105	125	mA
3.3V UVLO Turn-on Threshold			-	2.80	2.90	V
3.3V UVLO Turn-off Threshold			2.60	2.70	-	V
Input Voltage (4V-19V) Sense Input	VINSEN					
Input Impedance			1	-	-	MΩ
Input Range	V12	With 14:1 divider	0	0.857	1.1	V
UVLO Turn-on Programmable Range ¹		With 14:1 divider	-	4.5 – 15.9375	-	V
UVLO Turn-off Programmable Range ¹		With 14:1 divider	-	4.5 – 15.9375	-	V
OVP Threshold (if enabled)		Desktop mode	14.3	14.6	14.9	V
		Notebook mode	-	23.5	-	v
AUX Voltage (5V) Sense Input	VAUXSEN					
Input Impedance ¹			1	-	-	MΩ
UVLO Turn-on Threshold ¹		With 14:1 divider	4.3	4.5	4.75	V
UVLO Turn-off Threshold ¹		With 14:1 divider	3.8	4	4.3	V
Reference Voltage and DAC	•					
Boot Voltage Range ¹		AMD mode	-	0.00625 - 1.55	-	V
		Intel VR12 mode	-	0.25 – 1.52	-	V
		Intel VR12.5 mode	-	0.5 – 2.3	-	V
System Accuracy ³		VID = 2.005V-2.3V	-1.1	-	1.1	%VID
		VID = 1.0V-2.0V	-0.5	-	0.5	%VID
		VID = 0.8 - 0.995V	-5	-	5	mV
		VID = 0.25 -0.795V	-8	-	8	mV
External Reference Resistor	RRES	1% external bias resistor	-	7.5	-	kΩ
Oscillator & PWM Generator						
Internal Oscillator ¹			-	96	-	MHz
Frequency Accuracy ²			-2.5	-	2.5	%

Dual Output Digital Multi-Phase Controller

IR35211

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNIT
PWM Frequency Range ¹			-	200 to 2000	-	kHz
PWM Frequency Step Size Resolution ¹			-	0.83 - 83	-	kHz
PWM Resolution ¹			-	-	160	ps
NTC Temperature Sense	TSEN1, 2					
Output Current		For TSEN = 0 to 1.2V	96	100	104	μA
Accuracy ¹		at 100°C (ideal NTC)	96	-	104	°C
Digital Inputs – Low Vth Type 1	EN (Intel), INMODE, VR_HOT (during PoR), VIDSELx					
Input High Voltage			0.7	-	-	V
Input Low Voltage			-	-	0.35	V
Input Leakage Current		Vpad = 0 to 2V	-	-	±5	μA
Digital Inputs – Low Vth Type 2	SV_CLK, SV_DIO					
Input High Voltage			0.65	-	-	V
Input Low Voltage			-	-	0.45	V
Hysteresis			-	95	-	mV
Input Leakage Current		Vpad = 0 to 2V	-	-	±1	μA
Digital Inputs – Low Vth Type 3	PWROK					
Input High Voltage			0.9	-	-	V
Input Low Voltage			-	-	0.6	V
Input Leakage Current		Vpad = 0 to 2V	-	-	±1	μA
Digital Inputs – LVTTL	SM_DIO, SM_CLK, EN(AMD), ADDR_PROT					
Input High Voltage			2.1	-	-	V
Input Low Voltage			-	-	0.8	V
Input Leakage		Vpad = 0 to 3.6V	-	-	±1	μA
Remote Voltage Sense Inputs	VSEN, VRTN, VSEN_L2, VRTN_L2					
VSEN Input Current		VCPU = 0.5V to 1.5V	-	-250 to +250	-	μA
VRTN Input Current			-	-500	-	μA
Differential Input Voltage Range ¹		VRTN = ±100mV	-	0 to 2.6	-	V
VRTN Input CM Voltage ¹			-	-100 to 100	-	mV
Remote Current Sense Inputs	ISEN/IRTNx					
Voltage Range ¹			-	-0.1 to 2.7	-	V
Analog Address/Level Inputs	ADDR_PROT, SV_ADDR	16 levels				
Output Current ¹		Vpad = 0 to 1.2V	96	100	104	μA
CMOS Outputs – VDDIO	SVT, SV_DIO (AMD Mode)					
Pull-up On Resistance ¹			-	12	-	Ω
Output Low Voltage		I = 20mA	-	-	0.4	V

Dual Output Digital Multi-Phase Controller

IR35211

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Open-Drain Outputs – 4mA Drive	VRDY1, VRDY2, SM_DIO					
Output Low Voltage		4mA	-	-	0.3	V
Output Leakage		Vpad = 0 to 3.6V	-	-	±5	μA
Open-Drain Outputs – 20mA Drive	VR_HOT_ICRIT#, SV_DIO (INTEL), SV_ALERT					
Output Low Voltage ¹		I = 20mA	-	-	0.26	V
On Resistance ¹		I = 20mA	7	9	13	Ω
Tri-State Leakage	I _{leak}	Vpad = 0 to 3.6V	-	-	±5	μA
PWM I/O	PWMx		1	1		
Output Low Voltage (Tri-state mode)		I = -4mA	-	-	0.4	V
Output High Voltage (Tri-State mode)		l =+4mA	2.9	-	-	V
Output Low Voltage (IR ATL mode)		I = -4mA	-	-	0.4	V
Output High Voltage (IR ATL mode)		I = +4mA	1.4	-	2	V
Active Tri-State Level (IR ATL mode)		l = +4mA	2.9	-	-	V
Tri-State Leakage		ATS_EN = 0, Vpad = 0 to Vcc	-	-	±1	μA
PWM Auto-Detect Inputs (when 3.3V Vcc is	s applied) – if enabled				-	
Input Voltage High			1.3	-	-	V
Input Voltage Low			-	-	0.5	V
I2C/PMBus & Reporting						
Bus Speed ¹		Normal	-	100	-	kHz
		Fast	-	400	-	kHz
		Max Speed	-	1000	-	kHz
lout & Vout Filter ¹		Selectable	-	3.2 or 52	-	Hz
lout & Vout Update Rate ¹			-	20.8	-	kHz
Vin & Temperature Filter ¹		Selectable	-	3.2 or 52	-	Hz
Vin & Temperature Update Rate ¹			-	20.8	-	kHz
Vin Range Reporting ¹		With 14:1 divider	-	0 to 15	-	V
		With 22:1 divider	-	0 to 25	-	v
Vin Accuracy Reporting		With 1% resistors	-2	-	+2	%
Vin Resolution Reporting ¹			-	62.5	-	mV
Vout Range Reporting ¹			-	-	2.2	V
Vout Accuracy Reporting ¹		No load-line	-	±0.5	-	%
Vout Resolution Reporting ¹		Vout < 2V	-	7.8	-	mV
lout Per Phase Range Reporting ¹			0	-	62	А
lout Accuracy Reporting ¹		Maximum load, all phase active (based on DCR, NTC and # active phases)	-	±2	-	%
lout Resolution Reporting ¹		lout < 256A, Loop 1	-	0.5	-	Δ
		lout < 256A, Loop 2	-	0.25	-	
Temperature Range Reporting ¹		Loop 1, Loop 2	0	-	135	°C
Temperature Accuracy Reporting ¹		At 100°C, with ideal NTC	-3	-	3	%
Temperature Resolution Reporting ¹			-	1	-	°C

Dual Output Digital Multi-Phase Controller

IR35211

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNIT
Fault Protection						
OVP Threshold During Start-up (until output reaches 1V)			1.2	1.275	1.35	V
OVP Operating Threshold ¹ (programmable)		Relative to VID	-	150 to 500	-	mV
Output UVP Threshold ¹ (programmable)		Relative to VID	-	-150 to - 500	-	mV
OVP/UVP Filter Delay ¹			-	160	-	ns
Fast OCP Range (per phase) ¹			-	0 to 62	-	А
Fast OCP Filter Bandwidth ¹			-	60	-	kHz
Slow OCP Filter Bandwidth ¹			-	3.2/52	-	Hz
OCP System Accuracy ¹		System excluding DCR/sense resistor	-	±2	-	%
VR_HOT Range ¹			-	64 to 127	-	°C
OTP Range ¹		VR_HOT level + OTP Range	-	64 to 134	-	°C
Dynamic Phase Control						
Current Filter Bandwidth ¹		For Phase drop	-	5.3	-	kHz
Timing Information						
Automatic Configuration from MTP ¹	t ₃ -t ₂	3.3V ready to end of configuration	-	-	1	ms
Automatic Trim Time ¹	t ₄ -t ₃		-	-	4	ms
EN Delay (to ramp start) ¹			-	3	-	μs
VID Delay (to ramp start) ¹		Loop bandwidth dependent	-	5	-	μs
VRDY1/2 Delay ¹		After reaching Boot voltage	-	20	-	μs

Notes:

¹ Guaranteed by design.

² PWM operating frequency will vary slightly as the number of phases changes (increases/decreases) because of the internal calculation involved in dividing a switching period evenly into the number of active phases. ³ System accuracy is for a temperature range of 0°C to +85°C. Accuracies will derate by a factor of 1.5x for temperatures outside the 0°C to

+85°C range.

GENERAL DESCRIPTION

The IR35211 is a flexible, dual-loop, digital multiphase PWM buck controller optimized to convert a 12V input supply to the core voltage required by Intel and AMD high performance microprocessors and DDR memory. It is easily configurable for 1-3 phase operation on Loop #1 and 0-1 phase operation on Loop #2.

The unique partitioning of analog and digital circuits within the IR35211 provides the user with easy configuration capability while maintaining the required accuracy and performance. Access to on-chip Multiple Time Programming memory (MTP) to store the IR35211 configuration parameters enables power supply designers to optimize their designs without changing external components.

The IR35211 controls two independent output voltages. Each voltage is controlled in an identical fashion, so that the user can configure and optimize each control loop individually. Unless otherwise described, the following functions are performed on the IR35211 on each control loop independently.

OPERATING MODES

The IR35211 can be used for Intel VR12/12.5, AMD SVI1/SVI2, DDR Memory and GPU designs without significant changes to the external components (Bill of Materials). The required mode is selected in MTP and the pin-out, VID table and relevant functions are automatically configured. This greatly reduces time-to-market and eliminates the need to manage and inventory 6 different PWM controllers.

DIGITAL CONTROLLER & PWM

A linear Proportional-Integral-Derivative (PID) digital controller provides the loop compensation for system regulation. The digitized error voltage from the highspeed voltage error ADC is processed by the digital compensator. The digital PWM generator uses the outputs of the PID and the phase current balance control signals to determine the pulse width for each phase on each loop. The PWM generator has enough resolution to ensure that there are no limit cycles. The compensator coefficients are user configurable to enable optimized system response. The compensation algorithm uses a PID with two additional programmable poles. This provides the digital equivalent of a Type III analog compensator.

ADAPTIVE TRANSIENT ALGORITHM (ATA)

Dynamic load step-up and load step-down transients require fast system response to maintain the output voltage within specification limits. This is achieved by a unique adaptive non-linear digital transient control loop based on a proprietary algorithm.

MULTIPLE TIME PROGRAMMING MEMORY

The multiple time programming memory (MTP) stores the device configuration. At power-up, MTP contents are transferred to operating registers for access during device operation. MTP allows customization during both design and high-volume manufacturing. MTP integrity is verified by cyclic redundancy code (CRC) checking on each power up. The controller will not start in the event of a CRC error.

The IR35211 offers up to 8 writes to configure basic device parameters such as frequency, fault operation characteristics, and boot voltage. This represents a significant size and component saving compared to traditional analog methods. The following pseudo-code illustrates how to write the MTP:

write data
Set MTP Command Register = WRITE,
Line Pointer = An unused line
Poll MTP Command Register until Operation = IDLE.

verify data was written correctly
Issue a READ Command; then poll OTP Operation Register
till Operation = IDLE
Verify that the Read Succeeded

INTERNAL OSCILLATOR

The IR35211 has a single 96MHz internal oscillator that generates all the internal system clock frequencies required for proper device function. The oscillator frequency is factory trimmed for precision and has extremely low jitter (Figure 4) even in light-load mode (Figure 5). The single internal oscillator is used to set the same switching frequency on each loop.

Dual Output Digital Multi-Phase Controller

IR35211



Figure 4: Persistence plot of a 3Φ, 50A system



Figure 5: Persistence plot in 1Φ, 10A

HIGH-PRECISION VOLTAGE REFERENCE

The internal high-precision voltage reference supplies the required reference voltages to the VID DACs, ADCs and other analog circuits. This factory trimmed reference is guaranteed over temperature and manufacturing variations.

HIGH PRECISION CURRENT REFERENCE

An on-chip precision current reference is derived using an off-chip precision resistor connected to the RRES pin of the IR35211. RRES must be a $7.5k\Omega$, 1% tolerance resistor, placed very close to the controller pin to minimize parasitics.

VOLTAGE SENSE

An error voltage is generated from the difference between the target voltage, defined by the VID and load line (if implemented), and the differential, remotely sensed, output voltage. For each loop, the error voltage is digitized by a high-speed, highprecision ADC. An anti-alias filter provides the necessary high frequency noise rejection. The gain and offset of the voltage sense circuitry for each loop is factory trimmed to deliver the required accuracy.

CURRENT SENSE

Lossless inductor DCR or precision resistor current sensing is used to accurately measure individual phase currents. Using a simple off-chip thermistor, resistor and capacitor network for each loop, a thermally compensated load line is generated to meet the given power system requirement. A filtered voltage, which is a function of the total load current and the target load line resistance, is summed into each voltage sense path to accomplish the Active Voltage Positioning (AVP) function.

VID DECODER

The VID decoder receives a VID code from the CPU that is converted to an internal code representing the VID voltage. This block also outputs the signal for VR disable if a VID shutdown code has been received. The VID code is 8 bits in AMD SVI2 & Intel VR12/VR12.5 mode and 7 bits in AMD SVI1 mode.

MOSFET DRIVER, POWER STAGE AND DRMOS COMPATIBILITY

The output PWM signals of the IR35211 are designed for compatibility with the CHL85xx family of active trilevel (ATL) MOSFET drivers. CHL85xx drivers have a fast disable capability which enables any phase to be turned off on-the-fly. It supports power-saving control modes, improved transient response, and superior on the fly phase dropping without having to route multiple output disable (ODB or SMOD) signals.

In addition, the IR35211 provides the flexibility to configure PWM levels to operate with external MOSFET drivers, Power Stages or driver-MOSFET (DrMOS) devices that support Industry standard +3.3V tri-state signaling.

I2C & PMBUS INTERFACE

An I2C or PMBus interface is used to communicate with the IR35211. This two-wire serial interface consists of clock and data signals and operates as fast as 1MHz. The bus provides read and write access to the internal registers for configuration and monitoring of operating parameters and can also be used to program on-chip non-volatile memory (MTP) to store operating parameters.

To ensure operation with multiple devices on the bus, an exclusive address for the IR35211 is programmed into MTP. The IR35211, additionally, supports pinprogramming of the address.

To protect customer configuration and information, the I2C interface can be completely locked to provide no access or configured for limited access with a 16bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry only mode which allows reads from the telemetry registers only.

The IR35211 provides a hardware pin security option to provide extra protection. The protect pin is shared with the ADDR pin and is automatically engaged once the address is read. The pin must be driven high to disable protection. The pin can be enabled or disabled by a configuration setting in MTP.

The IR35211 supports the packet error checking (PEC) protocol and a number of PMBus commands to monitor voltages and currents. Refer to the PMBus Command Codes in Table 63.

IR DIGITAL POWER DESIGN CENTER (DPDC) GUI

The IR DPDC GUI provides the designer with a comprehensive design environment that includes screens to calculate VR efficiency and DC error budget, design the thermal compensation networks and feedback loops, and produce calculated Bode plots and output impedance plots. The DPDC environment is a key utility for design optimization, debug, and validation of designs that save designer significant time, allowing faster time-to-market (TTM).

The DPDC also allows real-time design optimization and real-time monitoring of key parameters such as output current and power, input current and power, efficiency, phase currents, temperature, and faults.

The IR DPDC GUI allows access to the system configuration settings for switching frequency, MOSFET driver compatibility, soft start rate, VID table, PSI, loop compensation, transient control system parameters, input under-voltage, output over-voltage, output under-voltage, output over-current and overtemperature.

PROGRAMMING

Once a design is complete, the DPDC produces a complete configuration file.

The configuration file can be re-coded into an I2C/PMBus master (e.g. a Test System) and loaded into the IR35211 using the bus protocols described on page 50. The IR35211 has a special in-circuit programming mode that allows the MTP to be loaded at board test in mass production without powering on the entire board.

REAL-TIME MONITORING

The IR35211 can be accessed through the use of PMBus Command codes (described in Table 63) to read the real time status of the VR system including input voltage, output voltage, input and output current, input and output power, efficiency, and temperature.

THEORY OF OPERATION

OPERATING MODE

The IR35211 changes its pin-out and functionality based on the user-selected operating mode, allowing one device to be used for multiple applications without significant BoM changes. This greatly reduces the user's design cycles and TTM.

The functionality for each operating mode is completely configurable by simple selections in MTP. The mode configuration is shown in Table 1.

TABLE 1: MODE SELECTION

Mode	Description
VR12	Intel® VR12 (Selected via MTP or external INMODE pin pulled high).
VR12.5	Intel® VR12.5 (Selected via MTP or external INMODE pin pulled low).
Memory	Intel® VR12 compliant memory VR with Loop 2 output voltage ½ Loop 1 output voltage.
SVI2.0	AMD® SVI2.0 (Selected via MTP or external SVT pin).
SVI1.0	AMD® SVI1.0 (Selected via MTP or external SVT pin).
GPU Parallel	GPU VR with external VID select pins.
GPU Serial	GPU VR with Serial VID interface.

DEVICE POWER-ON AND INITIALIZATION

The IR35211 is powered from a 3.3V DC supply. Figure 6 shows the timing diagram during device initialization. An internal LDO generates a 1.8V rail to power the control logic within the device. During initial startup, the 1.8V rail follows the rising 3.3V supply voltage, proportional to an internal resistor tree. The internal oscillator becomes active at t_7 as the 1.8V rail is ramping up. Until soft-start begins, the IR35211 PWM outputs are disabled in a high impedance state to ensure that the system comes up in a known state.

The controller comes out of power-on reset (POR) at t_2 when the 3.3V supply is high enough for the internal bias central to generate 1.8V. At this time, if enabled in MTP and when the VINSEN voltage is valid, the controller will detect the populated phases by sensing the voltage on the PWM pins. If the voltage is less than the Auto Phase Detect threshold (unused PWMs are grounded), the controller assumes the phase is

unpopulated. Once the phase detection is complete the contents of the MTP are transferred to the registers by time t_3 and the automatic trim routines are complete by time t_4 . The register settings and number of phases define the controller performance specific to the VR configuration - including trim settings, soft start ramp rate, boot voltage and PWM signal compatibility with the MOSFET driver.



Figure 6: Controller Startup and Initialization

Once the registers are loaded from MTP, the designer can use I2C to re-configure the registers to suit the specific VR design requirements if desired.

TEST MODE

Driving the ENABLE and VR_HOT pins low engages a special test mode in which the I2C address changes to 0Ah. This allows individual in-circuit programming of the controller. This is specifically useful in multicontroller systems that use a single I2C bus. <u>Note that</u> <u>MTP will not load to the working registers until either</u> <u>ENABLE or VR HOT goes high.</u>

SUPPLY VOLTAGE

The controller is powered by the 3.3V supply rail. Once initialization of the device is complete, steady and stable supply voltage rails and a VR Enable signal (EN) are required to set the controller into an active state. A high EN signal is required to enable the PWM signals and begin the soft start sequence after the 3.3V and VIN supply rails are determined to be within the defined operating bands. The recommended decoupling for the 3.3V is shown in Figure 7.

IR35211

The Vcc pins should have a $0.1\mu F$ and $1\mu F$ X7R-type ceramic capacitors placed as close as possible to the package.



Figure 7: Vcc 3.3V decoupling

The V18A pin must have a 4.7μ F, X5R type decoupling capacitor connected close to the package as shown in Figure 8.



Figure 8: V18A decoupling

The IR35211 is designed to accommodate a wide variety of input power supplies and applications and offers programmability of the VINSEN turn-on/off voltages.

TABLE 2: VINSEN TURN-ON/OFF VOLTAGE RANGE

Threshold	Range
Turn-on	4.5V to 15.9375V in 1/16V steps ¹
Turn-off	4.5V to 15.9375V in 1/16V steps ¹

¹ Must not be programmed below 4.5V

16

The supply voltage on the VINSEN pin is compared against a programmable threshold. Once the rising VINSEN voltage crosses the turn-on threshold, EN is asserted and all PWM outputs become active. The VINSEN supply voltage is valid until it declines below its programmed turn-off level.

A 14:1 or 22:1 attenuation network is connected to the VINSEN pin as shown in Figure 9. Recommended values for a 12V system are $R_{VIN_1} = 13k\Omega$ and $R_{VIN_2} = 1k\Omega$, with a 1% tolerance or better. Recommended values for a mobile 7V-19V system are $R_{VIN_1} = 21k\Omega$ and $R_{VIN_2} = 1k\Omega$. C_{VINSEN} is required to have up to a maximum value of 10nF and a minimum 1nF for noise suppression. *Note: Use the 14:1 attenuation network to sense 5V with VAUXSEN pin, if configured.*



Figure 9: VINSEN resistor divider network

POWER-ON SEQUENCING

The VR power-on sequence is initiated when all of the following conditions are satisfied:

- IR35211 Vcc (+3.3V rail) > VCC UVLO
- Input Voltage (VINSEN rail) > Vin UVLO
- Aux Voltage (VAUXSEN rail) > VAUXSEN UVLO (if configured)
- ENABLE is HIGH
- VR has no Over-current, Over-voltage or Under-voltage faults <u>on either rail</u>
- MTP transfer to configuration registers occurred without parity error

Once the above conditions are cleared, start-up behavior is controlled by the operating mode.



Figure 10: Enable-based Startup

POWER-OFF SEQUENCING

When +12Vdc goes below controller turn-off threshold, the controller tristates all PWM's. When enable goes low the controller ramps down Vout on both loops as shown in Figure 11.



Figure 11: Enable-based Shutdown

AMD SVI2 MODE

When the power-on sequence is initiated, both rails will ramp to the configured Vboot voltage and assert the PWRGD on each loop. The soft-start occurs at the $\frac{1}{2}$ or $\frac{1}{4}$ multiplier slew rate as selected in Table 3.

TABLE 3: SLEW RATES

mV/µs	FAST rate	1/2 Multiplier	1/4 Multiplier
	10	5.0	2.50
	15	7.5	3.75
	20	10	5.00
	25	12.5	6.25

The boot voltage is decoded from the SVC and SVD levels when the EN pin is asserted high as shown in Table 4. This value is latched and will be re-used in the event of a soft reset (de-assertion and re-assertion of PwrOK). Note: VCC and VDDIO must be stable for a minimum 5ms before the IC is enabled to ensure that the Boot voltage is decoded from the SVC, SVD pins correctly.

TABLE 4: AMD SVI BOOT TABLE

Boot Voltage	SVC	SVD
1.1V	0	0
1.0V	0	1
0.9V	1	0
0.8V	1	1

Alternatively, the AMD boot voltage can be set by an MTP register instead of decoding the SVC, SVD pins as shown in Table 5. Boot values are shown in Table 16.

TABLE 5: AMD BOOT OPTIONS

MTP Boot Register	Boot Location
Bit[7] = low	Decode from SVC, SVD pins per Table 4
Bit[7] = high	Use MTP boot register bits [6:0]

PWROK De-assertion

The IR35211 responds to SVI commands on the SVI bus interface when PWROK is high. In the event that PWROK is de-asserted the controller resets the SVI state machine, drives the SVT pin high and returns to the Boot voltage, initial load line slope and offset.



Figure 12: PWROK De-assertion

SVI2 Interface

The IR35211 implements a fully compliant AMD SVI2 Serial VID interface (SVI). SVI2 is a three-wire interface between a SVI2 compliant processor and a VR. It consists of clock, data, and telemetry/alert signals. The processor will send a data packet with the clock (SVC) and data (SVD) lines. This packet has SVI commands to change VID, go to a low power state, enable and configure telemetry, change load line slope and change VID offset. The VR, when configured to do so, will send telemetry to the processor. The telemetry data consists of voltage only, or voltage and current of each output rail (VDD, VDDNB). The telemetry line (SVT) is also used as an alert signal (VOTF complete) to alert the processor when a positive going VID change is complete, or an offset or load line scale change has occurred.

VID Change

The IR35211 accepts an 8-bit VID within the SVD packet and will change the output voltage at the FAST rate specified in Table 3 of one or both of the loops based on the VID in Table 6. This is a VID-on-the-fly-request (VOTF Request).

TABLE 6: SVI2 VID TABLE

VID (Hex)	Voltage (V)								
0	1.55000	32	1.23750	64	0.92500	96	0.61250	C8	0.30000
1	1.54375	33	1.23125	65	0.91875	97	0.60625	C9	0.29375
2	1.53750	34	1.22500	66	0.91250	98	0.60000	CA	0.28750
3	1.53125	35	1.21875	67	0.90625	99	0.59375	СВ	0.28125
4	1.52500	36	1.21250	68	0.90000	9A	0.58750	CC	0.27500
5	1.51875	37	1.20625	69	0.89375	9B	0.58125	CD	0.26875
6	1.51250	38	1.20000	6A	0.88750	9C	0.57500	CE	0.26250
7	1.50625	39	1.19375	6B	0.88125	9D	0.56875	CF	0.25625
8	1.50000	3A	1.18750	6C	0.87500	9E	0.56250	D0	0.25000
9	1.49375	3B	1.18125	6D	0.86875	9F	0.55625	D1	0.24375
А	1.48750	3C	1.17500	6E	0.86250	A0	0.55000	D2	0.23750
В	1.48125	3D	1.16875	6F	0.85625	A1	0.54375	D3	0.23125
С	1.47500	3E	1.16250	70	0.85000	A2	0.53750	D4	0.22500
D	1.46875	3F	1.15625	71	0.84375	A3	0.53125	D5	0.21875
E	1.46250	40	1.15000	72	0.83750	A4	0.52500	D6	0.21250
F	1.45625	41	1.14375	73	0.83125	A5	0.51875	D7	0.20625
10	1.45000	42	1.13750	74	0.82500	A6	0.51250	D8	0.20000
11	1.44375	43	1.13125	75	0.81875	A7	0.50625	D9	0.19375
12	1.43750	44	1.12500	76	0.81250	A8	0.50000	DA	0.18750
13	1.43125	45	1.11875	77	0.80625	A9	0.49375	DB	0.18125
14	1.42500	46	1.11250	78	0.80000	AA	0.48750	DC	0.17500
15	1.41875	47	1.10625	79	0.79375	AB	0.48125	DD	0.16875
16	1.41250	48	1.10000	7A	0.78750	AC	0.47500	DE	0.16250
17	1.40625	49	1.09375	7B	0.78125	AD	0.46875	DF	0.15625
18	1.40000	4A	1.08750	7C	0.77500	AE	0.46250	E0	0.15000
19	1.39375	4B	1.08125	7D	0.76875	AF	0.45625	E1	0.14375
1A	1.38750	4C	1.07500	7E	0.76250	B0	0.45000	E2	0.13750
1B	1.38125	4D	1.06875	7F	0.75625	B1	0.44375	E3	0.13125
1C	1.37500	4E	1.06250	80	0.75000	B2	0.43750	E4	0.12500
1D	1.36875	4F	1.05625	81	0.74375	B3	0.43125	E5	0.11875
1E	1.36250	50	1.05000	82	0.73750	B4	0.42500	E6	0.11250
1F	1.35625	51	1.04375	83	0.73125	B5	0.41875	E7	0.10625
20	1.35000	52	1.03750	84	0.72500	B6	0.41250	E8	0.10000
21	1.34375	53	1.03125	85	0.71875	B7	0.40625	E9	0.09375
22	1.33750	54	1.02500	86	0.71250	B8	0.40000	EA	0.08750
23	1.33125	55	1.01875	87	0.70625	B9	0.39375	EB	0.08125
24	1.32500	56	1.01250	88	0.70000	BA	0.38750	EC	0.07500
25	1.31875	57	1.00625	89	0.69375	BB	0.38125	ED	0.06875

18

Dual Output Digital Multi-Phase Controller

IR35211

VID (Hex)	Voltage (V)								
26	1.31250	58	1.00000	8A	0.68750	BC	0.37500	EE	0.06250
27	1.30625	59	0.99375	8B	0.68125	BD	0.36875	EF	0.05625
28	1.30000	5A	0.98750	8C	0.67500	BE	0.36250	F0	0.05000
29	1.29375	5B	0.98125	8D	0.66875	BF	0.35625	F1	0.04375
2A	1.28750	5C	0.97500	8E	0.66250	C0	0.35000	F2	0.03750
2B	1.28125	5D	0.96875	8F	0.65625	C1	0.34375	F3	0.03125
2C	1.27500	5E	0.96250	90	0.65000	C2	0.33750	F4	0.02500
2D	1.26875	5F	0.95625	91	0.64375	C3	0.33125	F5	0.01875
2E	1.26250	60	0.95000	92	0.63750	C4	0.32500	F6	0.01250
2F	1.25625	61	0.94375	93	0.63125	C5	0.31875	F7	0.00625
30	1.25000	62	0.93750	94	0.62500	C6	0.31250	F6-FF	OFF
31	1.24375	63	0.93125	95	0.61875	C7	0.30625		

PSI[x]_L and TFN

PSI0_L is Power State Indicator Level 0. When this bit is asserted the IR35211 will drop to 1 phase. This will only occur if the output current is low enough (typically <20A) to enter PSI0, else the VR will remain in full phase operation.

PSI1_L is Power State Indicator Level 1. When this bit is asserted along with the PSI0_L bit, the IR35211 will enter diode emulation mode. This will only occur if the output current is low enough (typically <5A) to enter PSI1, else the VR will enter PSI0_L mode of operation.

TFN is an active high signal that allows the processor to control the telemetry functionality of the VR. If TFN=1, then the VR telemetry will be configured per Table 7.

TABLE 7: TFN TRUTH TABLE

VDD, VDDNB Domain Selector bit	Meaning	
0, 0	Telemetry is in voltage only mode.	
0, 1	Telemetry is in voltage & current mode.	
1, 0	Telemetry is disabled.	
1, 1	Reserved.	

SVT Telemetry

20

The IR35211 has the ability to sample and report voltage and current for the VDD and VDDNB domains. The IR35211 reports this telemetry serially over the SVT wire which is clocked by the processor driven SVC. If in voltage only telemetry mode then the sampled voltage for VDD and VDDNB are sent together in every SVT telemetry packet at a rate of 20kHz. If in voltage and current mode then the sampled voltage and current for VDD is sent out in one SVT telemetry packet followed by the sampled voltage and current for VDDNB in the next SVT telemetry packet at a rate of 40kHz. The voltage and current are moving averages based on the filters and update rates specified in the Electrical Specification Table. The voltage is reported as a function of the Set VID minus lout times the Load Line Resistance. The current is reported as a percentage of the lcc max register, where a value of FFh represents 100% and 00h represents 0% of the Icc_max setting. Resolution of the current reporting is 0.39% (1/256).

Load Line Slope Trim

The IR35211 has the ability for the processor to change the load line slope of each loop independently through the SVI2 bus while ENABLE and PWROK are asserted via the serial VID interface. The slope change applies to initial load line slope as set by the external RCSP/RCSM resistor network. The load line slope can be disabled or adjusted by -40%, -20%, 0%, +20%, +40%, +60%, or +80%.

Offset Trim

The IR35211 has the ability for the processor to change the offset of each loop independently while ENABLE and PWROK are asserted via the serial VID interface. The offset can be left unchanged, disabled, or changed +25mV or -25mV.

Ispike/Dual OCP Support

The IR35211 has two current limit thresholds. One threshold is for short duration current spikes (Fast OCP). When this threshold, typically a percentage above the peak processor current, is exceeded the VR quickly shuts down. The other threshold, typically a percentage above the thermal design current (TDC), is heavily filtered (Slow OCP) and shuts down the VR when the average current exceeds it. To meet AMD specifications, exceeding both thresholds will assert the OCP_L (VR_HOT) pin and delay the over-current shut down by 10usec for FAST threshold and 20usec for the SLOW threshold, typically. Figure 13 and Figure 14 show the delay action of the OCP pins.



Figure 13: OCP_L (VR_HOT) assertion with OCP_spike (Fast) threshold. OCP delay action (11usec)

IR35211



Figure 14: OCP_L (VR_HOT) assertion with OCP_TDC (Slow) threshold. OCP delay action (22usec)

Thermal Based Protection

The IR35211 can also assert the PROC_HOT_L (VR_HOT) pin when the temperature of the VR exceeds a configurable temp_max threshold (typically 100°C). If the temperature continues to rise and exceeds a second configurable threshold (OTP_thresh) then the VR will shut down and latch off. The VR can only be restarted if ENABLE or VCC is cycled.

AMD SVI Address Programming

By default, loop 1 is addressed as the VDD rail and loop 2 is addressed as the VDDNB rail which is sufficient for most applications. The IR35211 however, can also be configured with a single bit change to swap this addressing scheme so that loop 1 can be addressed as the VDDNB rail and loop 2 can be addressed as the VDD rail. This is for application where the VDDNB requires more than two phases and VDD only requires two.

AMD GPU 2-BIT VID AND SVI MODES

Boot Voltage

The boot voltage is fully programmable in MTP to the range shown in Table 8. Table 16 shows the Boot VID table.

TABLE 8: VBOOT RANGE

Loop	Boot Voltage
Loop 1	Any VID code
Loop 2	Any VID code

The IR35211 provides flexible sequencing options which are configured in MTP per Table 9.

TABLE 9: SEQUENCE MODE TABLE

Loop 1 & Loop 2 start together (default)	
Loop 2 starts when Loop 1 VRRDY=high	
Loop 1 starts when Loop 2 VRRDY=high	

Additionally, a start-up delay of values shown in Table 10 can be inserted immediately after the EN signal is driven high or in between the sequencing of the two loops (Table 11).

TABLE 10: START-UP DELAY

0.0 ms (default)	
0.25 ms	
0.5 ms	
1.0 ms	
2.5 ms	
5.0 ms	
10.0 ms	
	_

TABLE 11: DELAY POSITION

After ENABLE	
Between the 2 loops	

The slew rates for both loops are set independently. Some common start-up combinations are shown in Figure 15 and Figure 16.



Figure 15: Loop 1 & Loop 2 start together with 0.25ms delay from Enable



Figure 16: Loop 2 starts when Loop 1 VRRDY = high with 0.5ms delay between the loops

VID Voltage & Tables

International

ICR Rectifier

The IR35211 output voltage is controlled primarily by the settings in Table 12 when in PVI mode.

Function	Setting		
Loop 1 DVID speed	0 – fast*	1 – slow	
Loop 2 DVID speed	0 – fast*	1 – slow	
Loop 1 mode	0 – boot voltage*	1 – VID registers	
Loop 2 mode	0 – boot voltage*	1 – VID registers	

* Default Setting

2-Bit VID Mode of Operation

22

Initially, the loop output voltages starts up to the MTP programmed boot voltages. The output is held at this voltage until an I2C command changes the mode to read the VID registers.

Once under VID control, the Loop 1 output voltage is selected from 1 of 4 VID registers based upon the VIDSEL1/0 pins. Loop 2 VID voltage is not controllable from a VIDSEL pin. When selected to go to VID control it goes to the single loop 2 VID register value only. Refer to Table 13 for VIDSEL pins operation. The contents of the VID registers can be updated through I2C at any time and will cause an immediate change in the output voltage.

TABLE 13: VIDSEL FOR LOOP 1

Pin-based VIDSEL		VID Register
0	0	Loop 1 VID Register 0
0	1	Loop 1 VID Register 1
1	0	Loop 1 VID Register 2
1	1	Loop 1 VID Register 3

The VID registers are set according to the VID table in Table 17.

SVI Mode of Operation

Just as in 2-bit VID mode, the loop output voltages start up to the MTP programmed boot voltages as shown in Table 16. The output is held at this voltage until the PWROK pin is asserted and the controller receives an 8-bit serial VID code as shown in Table 17 to transition to another voltage.

The GPU SVI command is received via the SVC and SVD pins and is typically a 20 MHz signal that consists of a START, 8-bit VID code, ACK, and a STOP. The protocol structure is shown in Table 14.

TABLE 14: GPU SVI PROTOCOL

Bit Time	0	1	2	3	4	5	6	7	8	9	10
	Start	VID CODE (Table 17)							Ack	Stop	

The voltage will transition back to the boot voltage when the PWROK pin is de-asserted. The PWRGD signals will remain asserted during this transition time.

Vmax Function

The IR35211 incorporates a safety feature whereby the output voltage can be limited to a maximum value irrespective of the VID and offset settings (Table 15). This feature is especially useful in limiting the voltage in Overclocking mode. The maximum value for each loop is stored in MTP.

TABLE 15: VMAX SETTINGS FOR OVERCLOCKING IN GPU MODE

0.800	1.700
0.913	1.813
1.025	1.925
1.138	2.038
1.250	2.150
1.363	2.263
1.475	2.375
1.588	2.488

The Vmax has a lock function to prevent accidental overwrite. The pseudo-code below illustrates how to write a Vmax value:

Unlock & write desired Vmax value Set vmax_lock=0 Set Vmax=new value

lock to prevent overwrite Set Vmax_lock=1

TABLE 16: AMD BOOT VOLTAGE

VID (Hex)	Voltage (V)						
80	1.5500	A0	1.1500	C0	0.7500	E0	0.3500
81	1.5375	A1	1.1375	C1	0.7375	E1	0.3375
82	1.5250	A2	1.1250	C2	0.7250	E2	0.3250
83	1.5125	A3	1.1125	C3	0.7125	E3	0.3125
84	1.5000	A4	1.1000	C4	0.7000	E4	0.3000
85	1.4875	A5	1.0875	C5	0.6875	E5	0.2875
86	1.4750	A6	1.0750	C6	0.6750	E6	0.2750
87	1.4625	A7	1.0625	C7	0.6625	E7	0.2625
88	1.4500	A8	1.0500	C8	0.6500	E8	0.2500
89	1.4375	A9	1.0375	C9	0.6375	E9	0.2375
8A	1.4250	AA	1.0250	CA	0.6250	EA	0.2250
8B	1.4125	AB	1.0125	СВ	0.6125	EB	0.2125
8C	1.4000	AC	1.0000	CC	0.6000	EC	0.2000
8D	1.3875	AD	0.9875	CD	0.5875	ED	0.1875
8E	1.3750	AE	0.9750	CE	0.5750	EE	0.1750
8F	1.3625	AF	0.9625	CF	0.5625	EF	0.1625
90	1.3500	B0	0.9500	D0	0.5500	F0	0.1500
91	1.3375	B1	0.9375	D1	0.5375	F1	0.1375
92	1.3250	B2	0.9250	D2	0.5250	F2	0.1250
93	1.3125	B3	0.9125	D3	0.5125	F3	0.1125
94	1.3000	B4	0.9000	D4	0.5000	F4	0.1000
95	1.2875	B5	0.8875	D5	0.4875	F5	0.0875
96	1.2750	B6	0.8750	D6	0.4750	F6	0.0750
97	1.2625	B7	0.8625	D7	0.4625	F7	0.0625
98	1.2500	B8	0.8500	D8	0.4500	F8	0.0500
99	1.2375	В9	0.8375	D9	0.4375	F9	0.0375
9A	1.2250	BA	0.8250	DA	0.4250	FA	0.0250
9B	1.2125	BB	0.8125	DB	0.4125	FB	OFF
9C	1.2000	BC	0.8000	DC	0.4000	FC	OFF
9D	1.1875	BD	0.7875	DD	0.3875	FD	OFF
9E	1.1750	BE	0.7750	DE	0.3750	FE	OFF
9F	1.1625	BF	0.7625	DF	0.3625	FF	OFF

TABLE 17: GPU 2 BIT OR SVI

VID (Hex)	Voltage (V)								
0	1.55000	32	1.2375	64	0.92500	96	0.61250	C8	0.30000
1	1.54375	33	1.2313	65	0.91875	97	0.60625	C9	0.29375
2	1.53750	34	1.2250	66	0.91250	98	0.60000	CA	0.28750
3	1.53125	35	1.2188	67	0.90625	99	0.59375	СВ	0.28125
4	1.52500	36	1.2125	68	0.90000	9A	0.58750	CC	0.27500
5	1.51875	37	1.2063	69	0.89375	9B	0.58125	CD	0.26875
6	1.51250	38	1.2000	6A	0.88750	9C	0.57500	CE	0.26250
7	1.50625	39	1.1938	6B	0.88125	9D	0.56875	CF	0.25625
8	1.50000	3A	1.1875	6C	0.87500	9E	0.56250	D0	0.25000
9	1.49375	3B	1.1813	6D	0.86875	9F	0.55625	D1	0.24375
А	1.48750	3C	1.1750	6E	0.86250	A0	0.55000	D2	0.23750
В	1.48125	3D	1.1688	6F	0.85625	A1	0.54375	D3	0.23125
С	1.47500	3E	1.1625	70	0.85000	A2	0.53750	D4	0.22500
D	1.46875	3F	1.1563	71	0.84375	A3	0.53125	D5	0.21875
E	1.46250	40	1.1500	72	0.83750	A4	0.52500	D6	0.21250
F	1.45625	41	1.1438	73	0.83125	A5	0.51875	D7	0.20625
10	1.45000	42	1.1375	74	0.82500	A6	0.51250	D8	0.20000
11	1.44375	43	1.1313	75	0.81875	A7	0.50625	D9	0.19375
12	1.43750	44	1.1250	76	0.81250	A8	0.50000	DA	0.18750
13	1.43125	45	1.1188	77	0.80625	A9	0.49375	DB	0.18125
14	1.42500	46	1.1125	78	0.80000	AA	0.48750	DC	0.17500
15	1.41875	47	1.1063	79	0.79375	AB	0.48125	DD	0.16875
16	1.41250	48	1.1000	7A	0.78750	AC	0.47500	DE	0.16250
17	1.40625	49	1.0938	7B	0.78125	AD	0.46875	DF	0.15625
18	1.40000	4A	1.0875	7C	0.77500	AE	0.46250	E0	0.15000
19	1.39375	4B	1.0813	7D	0.76875	AF	0.45625	E1	0.14375
1A	1.38750	4C	1.0750	7E	0.76250	B0	0.45000	E2	0.13750
1B	1.38125	4D	1.0688	7F	0.75625	B1	0.44375	E3	0.13125
1C	1.37500	4E	1.0625	80	0.75000	B2	0.43750	E4	0.12500
1D	1.36875	4F	1.0563	81	0.74375	B3	0.43125	E5	0.11875
1E	1.36250	50	1.0500	82	0.73750	B4	0.42500	E6	0.11250
1F	1.35625	51	1.0438	83	0.73125	B5	0.41875	E7	0.10625
20	1.35000	52	1.0375	84	0.72500	B6	0.41250	E8	0.10000
21	1.34375	53	1.0313	85	0.71875	B7	0.40625	E9	0.09375
22	1.33750	54	1.0250	86	0.71250	B8	0.40000	EA	0.08750
23	1.33125	55	1.0188	87	0.70625	B9	0.39375	EB	0.08125
24	1.32500	56	1.0125	88	0.70000	BA	0.38750	EC	0.07500

25