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International
IOR Rectifier

IR3523

DATASHEET

XPHASE3™ DUAL OUTPUT CONTROL IC

DESCRIPTION

The IR3523 Control IC provides a full featured and flexible way to implement a complete dual output DDR & CPU VTT multiphase power solution for Intel VR11.1 motherboards. Each output interfaces with any number of *xPHASE3*™ Phase ICs each driving and monitoring a single phase. Output 1 includes a 3 bit VR11.x VID, 1.1V boot voltage and droop to implement the CPU VTT rail which is typically 1 phase. Output 2 includes a 3 bit VID for margining and supports any number of phases and DDR DIMM modules. The *xPHASE3*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

INDEPENDENT FEATURES FOR BOTH OUTPUT 1 & 2

- Enable Input
- Power Good (PG) Output
- 0.5% overall system set point accuracy
- Programmable Softstart
- High speed error amplifier with wide bandwidth of 30MHz and fast slew rate of 12V/us
- Remote sense amplifier provides differential sensing and requires less than 50uA bias current
- Programmable over current threshold triggers constant converter output current limit during start-up and hiccup protection during normal operation
- Over voltage condition communicated to phase ICs by IIN (ISHARE) and system by ROSC/OVP pins
- Detection and protection of open remote sense lines

OUTPUT 1 ADDITIONAL FEATURES

- 3 bit Intel VR11.x VID (VID4, VID3, VID2)
- Programmable VID offset
- 1.1 V Boot Voltage
- Programmable output impedance
- Programmable VID-on-the-Fly Slew Rate

OUTPUT 2 ADDITIONAL FEATURES

- 3 bit VID provides 1.5 V with ±150mV margining
- Programmable VID-on-the-Fly Slew Rate

FEATURES SHARED BY BOTH OUTPUTS 1 & 2

- Programmable per phase switching frequency of 250kHz to 1.5MHz
- Daisy-chain digital phase timing provides accurate phase interleaving without external components
- Gate Drive and IC bias linear regulator control with programmable output voltage and UVLO
- Over voltage signal to system with over voltage detection during powerup and normal operation

ORDERING INFORMATION

Device	Package	Order Quantity
IR3523MTRPBF	40 Lead MLPQ (6 x 6 mm body)	3000 per reel
* IR3523MPBF	40 Lead MLPQ (6 x 6 mm body)	100 piece strips

* Samples only

APPLICATION CIRCUIT

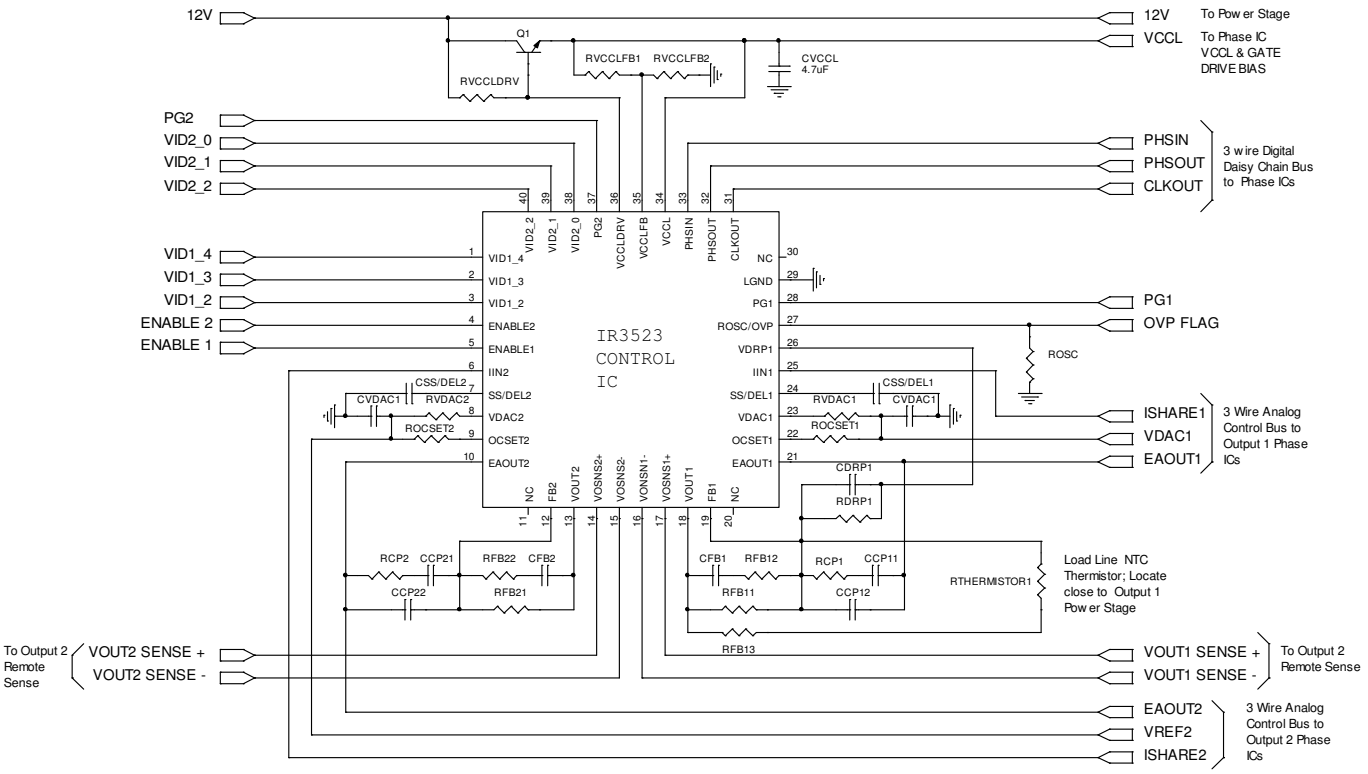

Figure 1 – IR3523 Application Circuit

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1-3	VID1_4, VID1_3, VID1_2	VID inputs for Output 1
4	ENABLE2	Enable input. A logic low applied to this pin puts output 2 into fault mode. A logic high signal on this pin enables output 2. Do not float as the logic state will be undefined.
5	ENABLE1	Enable input. A logic low applied to this pin puts output 2 into fault mode. A logic high signal on this pin enables output 2. Do not float as the logic state will be undefined.
6	IIN2	Output 2 average current input from the output 2 phase IC(s). This pin is also used to communicate over voltage condition to the output 2 phase ICs.
7	SS/DEL2	Programs output 2 startup and over current protection delay timing. Connect an external capacitor to LGND to program.
8	VDAC2	Output 2 reference voltage. Connect an external RC network to LGND to provide compensation for the internal buffer amplifier
9	OCSET2	Programs the output 2 constant converter output current limit and hiccup over-current threshold through an external resistor tied to VDAC2 and an internal current source from this pin. Over-current protection can be disabled by connecting a resistor from this pin to VDAC2 to program the threshold higher than the possible signal into the IIN pin from the phase ICs but no greater than 5V (do not float this pin as improper operation will occur).
10	EAOUT2	Output 2 error amplifier output
11,20,30	NC	No Connection

PIN#	PIN SYMBOL	PIN DESCRIPTION
12	FB2	Output 2 Error Amplifier inverting input
13	VOUT2	Output 2 remote sense amplifier output.
14	VOSEN2+	Output 2 remote sense amplifier input. Connect to output at the load.
15	VOSEN2-	Output 2 remote sense amplifier input. Connect to ground at the load.
16	VOSEN1-	Output 1 remote sense amplifier input. Connect to ground at the load.
17	VOSEN1+	Output 1 remote sense amplifier input. Connect to output at the load.
18	VOUT1	Output 1 remote sense amplifier output.
19	FB1	Inverting input to the output 1 Error Amplifier
21	EAOUT1	Output 1 error amplifier output
22	OCSET1	Programs the output 1 constant converter output current limit and hiccup over-current threshold through an external resistor tied to VDAC1 and an internal current source from this pin. Over-current protection can be disabled by connecting a resistor from this pin to VDAC1 to program the threshold higher than the possible signal into the IIN pin from the phase ICs but no greater than 5V (do not float this pin as improper operation will occur).
23	VDAC1	Output 1 reference voltage programmed by the VID inputs and error amplifier non-inverting input. Connect an external RC network to LGND to program dynamic VID slew rate and provide compensation for the internal buffer amplifier.
24	SS/DEL1	Programs output 1 startup and over current protection delay timing. Connect an external capacitor to LGND to program.
25	IIN1	Output 1 average current input from the output 1 phase IC(s). This pin is also used to communicate over voltage condition to phase ICs.
26	VDRP1	Output 1 Buffered IIN signal. Connect an external RC network to FB1 to program converter output impedance.
27	ROSC/OVP	Connect a resistor to LGND to program oscillator frequency and OCSET, VDAC1 and VREF2 bias currents. Oscillator frequency equals switching frequency per phase. The pin voltage is 0.6V during normal operation and higher than 1.6V if over-voltage condition is detected.
28	PG1	Open collector output. Asserted when Output 1 is regulated.
29	LGND	Local Ground for internal circuitry and IC substrate connection.
31	CLKOUT	Clock output at switching frequency multiplied by phase number. Connect to CLKIN pins of phase ICs.
32	PHSOUT	Phase clock output at switching frequency per phase. Connect to PHSIN pin of the first phase IC.
33	PHSIN	Feedback input of phase clock. Connect to PHSOUT pin of the last phase IC.
34	VCCL	Output of the voltage regulator, and power input for clock oscillator circuitry. Connect a decoupling capacitor to LGND.
35	VCCLFB	Non-inverting input of the voltage regulator error amplifier. Output voltage of the regulator is programmed by the resistor divider connected to VCCL.
36	VCCLDRV	Output of the VCCL regulator error amplifier to control external transistor. The pin senses the converter input voltage through a resistor.
37	PG2	Open collector output. Asserted when Output 2 output is regulated.
38, 39, 40	VID2_0, VID2_1, VID2_2	VID inputs for Output 2

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltages are absolute voltages referenced to the LGND pin.

Operating Junction Temperature……..0 to 150°C
Storage Temperature Range……-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC Standard
MSL Rating……2
Reflow Temperature……260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	VID1_4	8V	-0.3V	1mA	1mA
2	VID1_3	8V	-0.3V	1mA	1mA
3	VID1_2	8V	-0.3V	1mA	1mA
4	ENABLE2	3.5V	-0.3V	1mA	1mA
5	ENABLE1	3.5V	-0.3V	1mA	1mA
6	IIN2	8V	-0.3V	5mA	1mA
7	SS/DEL2	8V	-0.3V	1mA	1mA
8	VDAC2	3.5V	-0.3V	1mA	1mA
9	OCSET2	8V	-0.3V	1mA	1mA
10	EAOUT2	8V	-0.3V	25mA	10mA
12	FB2	8V	-0.3V	1mA	1mA
13	VOUT2	8V	-0.5V	5mA	25mA
14	VOSEN2+	8V	-0.5V	5mA	1mA
15	VOSEN2-	1.0V	-0.5V	5mA	1mA
16	VOSEN1-	1.0V	-0.5V	5mA	1mA
17	VOSEN1+	8V	-0.5V	5mA	1mA
18	VOUT1	8V	-0.5V	5mA	25mA
19	FB1	8V	-0.3V	1mA	1mA
21	EAOUT1	8V	-0.3V	25mA	10mA
22	OCSET1	8V	-0.3V	1mA	1mA
23	VDAC1	3.5V	-0.3V	1mA	1mA
24	SS/DEL1	8V	-0.3V	1mA	1mA
25	IIN1	8V	-0.3V	5mA	1mA
26	VDRP1	8V	-0.3V	35mA	1mA
27	ROSC/OVP	8V	-0.5V	1mA	1mA
28	PG1	8V	-0.3V	1mA	20mA
29	LGND	n/a	n/a	20mA	1mA
31	CLKOUT	8V	-0.3V	100mA	100mA
32	PHSOUT	8V	-0.3V	10mA	10mA
33	PHSIN	8V	-0.3V	1mA	1mA
34	VCCL	8V	-0.3V	1mA	20mA
35	VCCLFB	3.5V	-0.3V	1mA	1mA
36	VCCLDRV	10V	-0.3V	1mA	50mA
37	PG2	8V	-0.3V	1mA	20mA
38	VID2_0	8V	-0.3V	1mA	1mA
39	VID2_1	8V	-0.3V	1mA	1mA
40	VID2_2	8V	-0.3V	1mA	1mA

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN
4.75V ≤ VCCL ≤ 7.5V, -0.3V ≤ VOSEN-x ≤ 0.3V, 0 °C ≤ T_J ≤ 100 °C, 7.75 kΩ ≤ ROSC ≤ 50 kΩ, CSS/DELx = 0.1uF

ELECTRICAL CHARACTERISTICS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions (unless otherwise specified). Typical values represent the median values, which are related to 25°C.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
System Set Point Accuracy					
Deviation from Table 1 for Output 1 and deviation from Table 2 for Output 2 per test circuit in Figure 4a and 4b, respectively	Output 2 and Output 1 Output 2 at 1.8V (only)	-0.5 -1.5		0.5 1.5	% %
VIDx Interface					
Input Thresholds	Increasing	0.85	.95	1.05	V
	Decreasing (VID2_0 and VID2_1 Only)	550	650	750	mV
	Hysteresis (VID2_0 and VID2_1 Only)	190	300	410	mV
Pull-Down Resistance		100	175	250	kΩ
Oscillator					
PHSOUT Frequency		-10%	See Figure 2	+10%	kHz
ROSC Voltage		0.575	0.600	0.625	V
CLKOUT High Voltage	I(CLKOUT)= -10 mA, measure V(VCCL) – V(CLKOUT).			1	V
CLKOUT Low Voltage	I(CLKOUT)= 10 mA			1	V
PHSOUT High Voltage	I(PHSOUT)= -1 mA, measure V(VCCL) – V(PHSOUT)			1	V
PHSOUT Low Voltage	I(PHSOUT)= 1 mA			1	V
PHSIN Threshold Voltage	Compare to V(VCCL)	30	50	70	%
VDRP1 Buffer Amplifiers					
Input Offset Voltage	V(VDRP) – V(IIN), 0.5V ≤ V(IIN) ≤ 3.3V	-8	0	8	mV
Source Current	0.5V ≤ V(IIN1) ≤ 3.3V	2		30	mA
Sink Current	0.5V ≤ V(IIN1) ≤ 3.3V	0.2	0.4	0.6	mA
Unity Gain Bandwidth	Note 1		8		MHz
Slew Rate	Note 1		4.7		V/µs
IIN Bias Current		-1	0	1	µA
Remote Sense Differential Amplifiers					
Unity Gain Bandwidth	Note 1	3.0	6.4	9.0	MHz
Input Offset Voltage	0.5V≤ V(VOSENx+) - V(VOSENx-) ≤ 1.6V, Note 2	-3	0	3	mV
Source Current	0.5V≤ V(VOSENx+) - V(VOSENx-) ≤ 1.6V	0.5	1	1.7	mA
Sink Current	0.5V≤ V(VOSENx+) - V(VOSENx-) ≤ 1.6V	2	12	18	mA
Slew Rate	0.5V≤ V(VOSENx+) - V(VOSENx-) ≤ 1.6V, Note 1	2	4	8	V/us
VOSEN+ Bias Current	0.5 V < V(VOSENx+) < 1.6V		30	50	uA
VOSEN- Bias Current	-0.3V ≤ VOSENx- ≤ 0.3V, All VID Codes		30	50	uA
Low Voltage	V(VCCL) = 7V			250	mV
High Voltage	V(VCCL) – V(VOUTx)		0.5	1	V
VDAC1 & VDAC2 Outputs					
Source Currents	Includes I(OCSET)	-8%	3000*Vrosc(V)/ ROSC(kΩ)	+8%	µA
Sink Currents	Includes I(OCSET)	-11%	1000*Vrosc V)/ ROSC(kΩ)	+11%	µA

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft Start and Delay					
Start Delay	Measure Enable to EAOUTx activation	1	2.9	3.5	ms
Start-up Time	Measure Enable activation to PGx	3	8	13	ms
OC Delay Time	V(IINx) – V(OCSETx) = 500 mV	200	650	1000	us
SS/DELx to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUTx drives high	0.7	1.4	1.9	V
Charge Current		-30	-50	-70	µA
OC Delay Discharge Currents	Measure at charge voltage		47		µA
Fault Discharge Current		2.5	4.5	6.5	µA
Hiccup Duty Cycle	I(Fault) / I(Charge)	8	10	12	µA/µA
Charge Voltage (Output 1,2)		3.5	3.9	4.2	V
Delay Comparator Threshold	Relative to Charge Voltage, SS/DELx rising - Note 1		70		mV
Delay Comparator Threshold	Relative to Charge Voltage, SS/DELx falling - Note 1		135		mV
Delay Comparator Hysteresis			65		mV
VID1 Sample Delay Comparator Threshold		2.8	3.0	3.2	V
Discharge Comp. Threshold		150	200	300	mV
Error Amplifiers					
Input Offset Voltage	Measure V(FBx) – V(VDACx)). Note 2 $25\,^{o}C \le T_J \le 100\,^{o}C$	-1	0	1	mV
FB1 Bias Current		-5%	Vrosc(V)*1000 /Rosc(KΩ)	+5%	µA
FB2 Bias Current		-1	0	1	µA
DC Gain	Note 1	100	110	135	dB
Bandwidth	Note 1	20	30	40	MHz
Slew Rate	Note 1	5.5	12	20	V/µs
Sink Current		0.4	0.85	1	mA
Source Current		5.0	8.5	12.0	mA
Maximum Voltage	Measure V(VCCL) – V(EAOUTx)	500	780	950	mV
Minimum Voltage			120	250	mV
Open Control Loop Detection Threshold	Measure V(VCCL) - V(EAOUT), Relative to Error Amplifier maximum voltage.	125	300	600	mV
Open Control Loop Detection Delay	Measure PHSOUT pulse numbers from V(EAOUTx) = V(VCCL) to PGx = low.		8		Pulse
ENABLE Inputs					
Threshold Increasing		1.38	1.65	1.94	V
Threshold Decreasing		0.8	0.99	1.2	V
Threshold Hysteresis		470	620	800	mV
Bias Current	0V ≤ V(x) ≤ 3.5V	-5	0	5	uA
Blanking Time	Noise Pulse < 100ns will not register an ENABLE state change. Note 1	75	250	400	ns
PGx Outputs					
Under Voltage Threshold - Voutx Decreasing	Reference to VDAC	-365	-315	-265	mV
Under Voltage Threshold - Voutx Increasing	Reference to VDAC	-325	-275	-225	mV
Under Voltage Threshold Hysteresis		5	53	110	mV
Output Voltage	I(PGx) = 4mA		150	300	mV
Leakage Current	V(PGx) = 5.5V		0	10	µA
VCCL_DRV Activation Threshold	I(PGx) = 4mA, V(PGx) < 400mV, V(VCCL) = 0	1.0	2.0	3.6	V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Over Voltage Protection (OVP) Comparators					
Threshold at Power-up (Output 2)		1.85	1.95	2.05	V
Threshold at Power-up (Output 1)		1.39	1.47	1.55	V
Voutx Threshold Voltage	Compare to V(VDACx)	100	125	150	mV
OVP Release Voltage during Normal Operation	Compare to V(VDACx)	-25	3	25	mV
Threshold during Dynamic VID down (Output 2)		1.87	1.93	1.99	V
Threshold during Dynamic VID down (Output 1)		1.24	1.33	1.37	V
Dynamic VID Detect Comparator Threshold	Note 1	25	50	75	mV
Propagation Delay to IIN	Measure time from V(Voutx) > V(VDACx) (250mV overdrive) to V(IINx) transition to > 0.9 * V(VCCL).		90	180	ns
OVP High Voltage	Measure V(VCCL)-V(ROSC/OVP)	0		1.2	V
OVP Power-up High Voltage	V(VCCLDRV)=1.8V. Measure V(VCCL)-V(ROSC/OVP)	0		0.2	V
Propagation Delay to OVP	Measure time from V(Voutx) > V(VDAC) (250mV overdrive) to V(ROSC/OVP) transition to >1V.		150	300	ns
IIN Pull-up Resistance			5	15	Ω
Over-Current Comparators					
Input Offset Voltage	1V ≤ V(OCSETx) ≤ 3.3V	-35	0	35	mV
OCSET Bias Current		-5%	Vrosc(V)*1000/ Rosc(KΩ)	+5%	µA
2048-4096 Count Threshold	Adjust ROSC value to find threshold Note 1	11.3	16	23.1	kΩ
1024-2048 Count Threshold	Adjust ROSC value to find threshold Note 1	14.4	20	29.1	kΩ
Open Sense Line Detection					
Sense Line Detection Active Comparator Threshold Voltage		150	200	250	mV
Sense Line Detection Active Comparator Offset Voltage	V(Voutx) < [V(VOSEN+) – V(LGND)] / 2	35	60	85	mV
VOSEN+ Open Sense Line Comparator Threshold	Compare to V(VCCL)	86.5	89.0	91.5	%
VOSEN- Open Sense Line Comparator Threshold		0.36	0.40	0.44	V
Sense Line Detection Source Currents	V(Voutx) = 100mV	200	500	700	uA
VCCL Regulator Amplifier					
Reference Feedback Voltage		1.15	1.2	1.25	V
VCCLFB Bias Current		-1	0	1	uA
VCCLDRV Sink Current		10	30		mA
UVLO Start Threshold	Compare to V(VCCL)	89.0	93.5	97.0	%
UVLO Stop Threshold	Compare to V(VCCL)	81.0	85.0	89.0	%
Hysteresis	Compare to V(VCCL)	7.0	8.25	9.5	%
General					
VCCL Supply Current		4	10	15	mA

Note 1: Guaranteed by design, but not tested in production
Note 2: VDACx Outputs are trimmed to compensate for Error & Amp Remote Sense Amp input offsets

PHSOUT FREQUENCY VS RROSC CHART

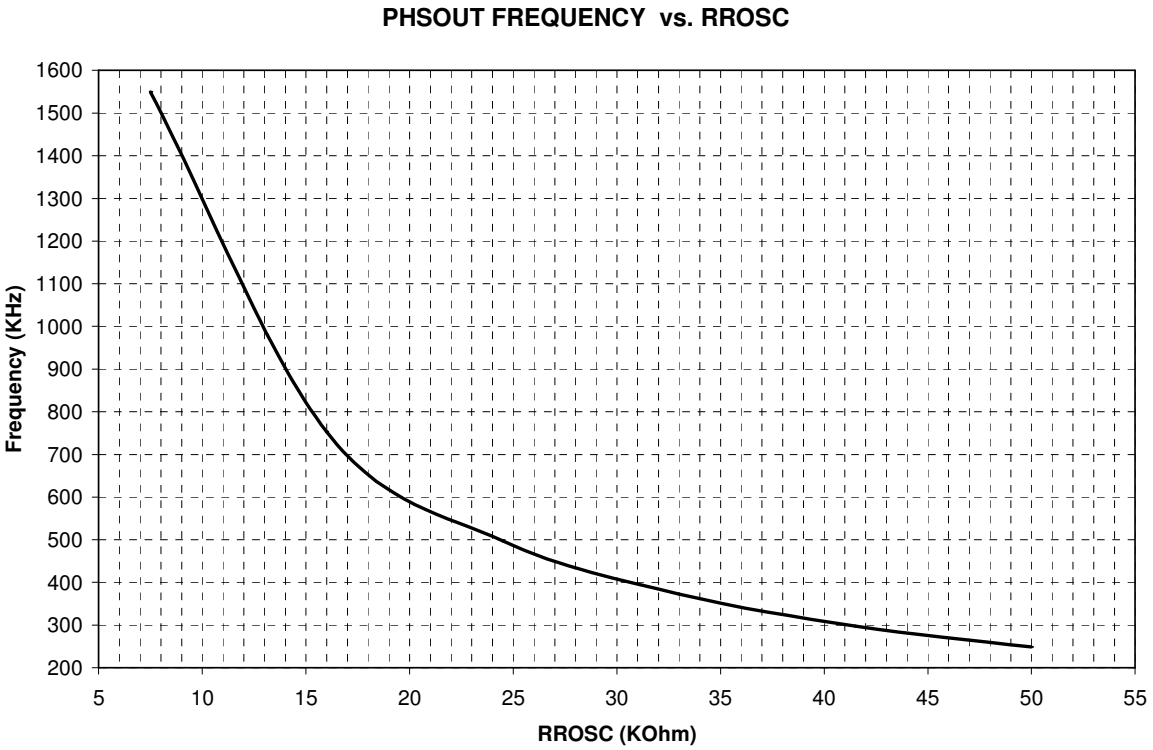

Figure 2 - PHSout Frequency vs. RROSC chart

IR3523 block diagram

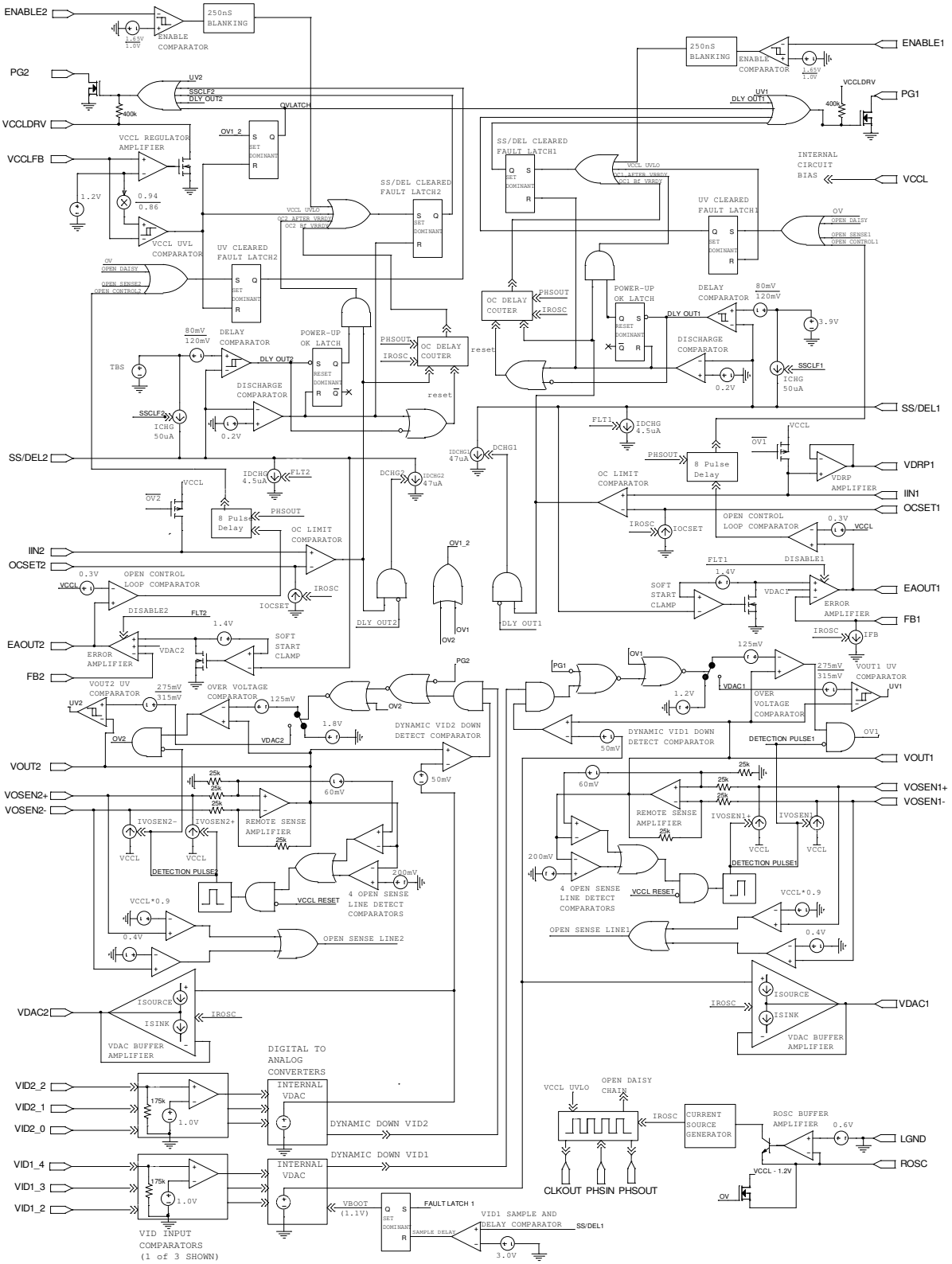

Figure 3 – IR3523 BLOCK DIAGRAM

SYSTEM SET POINT TEST

Converter output voltage is determined by the system set point voltage which is the voltage that appears at the FBx pins when the converter is in regulation. The set point voltage includes error terms for the VDAC digital-to-analog converters, Error Amp input offsets, and Remote Sense input offsets. The voltage appearing at the VDACx pins is not the system set point voltage. System set point voltage test circuits for Outputs 1 and 2 are shown in Figures 4A & 4B.

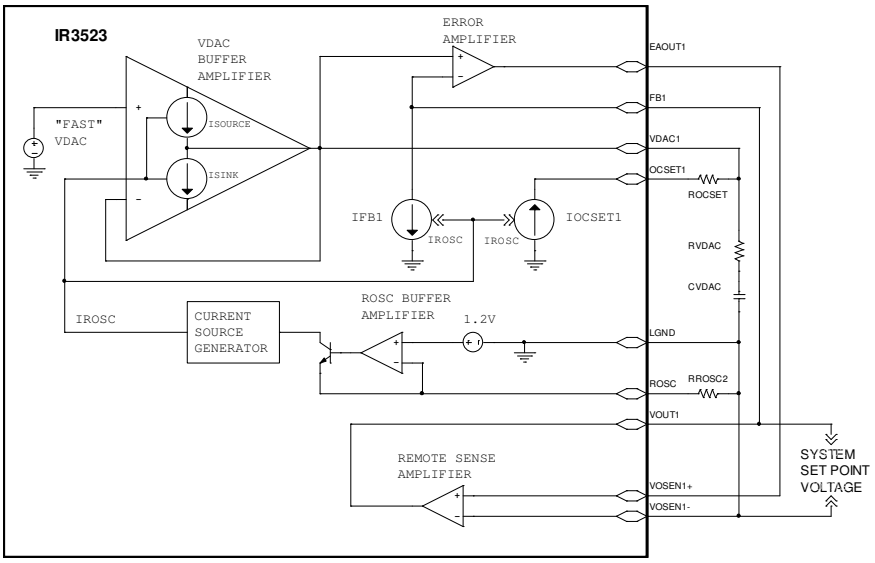

Figure 4A - Output 1 System Set Point Test Circuit

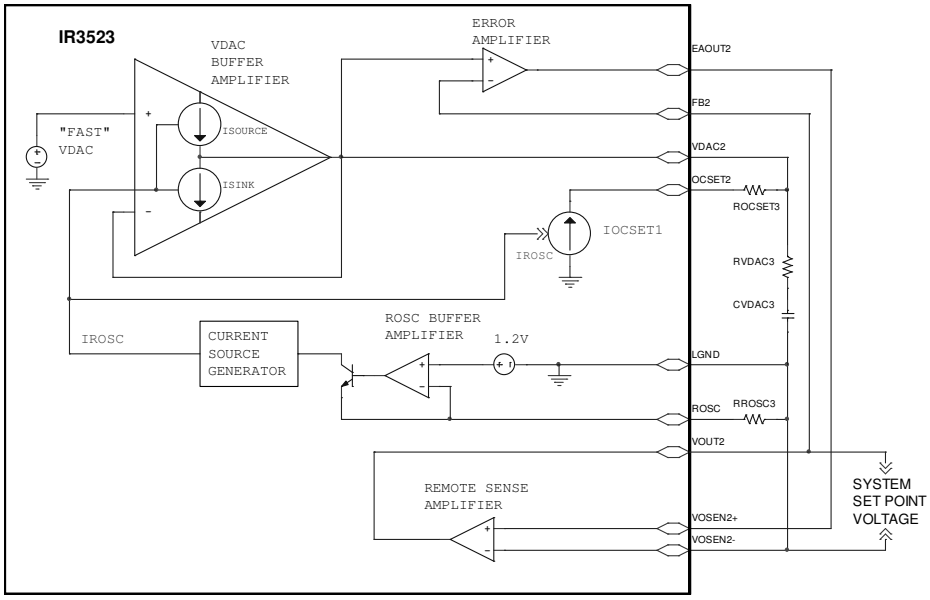

Figure 4B - Output 2 System Set Point Test Circuit

SYSTEM THEORY OF OPERATION

PWM Control Method

The PWM block diagram of the *xPHASE3*™ architecture is shown in Figure 5. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. Input voltage is sensed in phase ICs and feed-forward control is realized. The PWM ramp slope will change with the input voltage automatically compensating for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

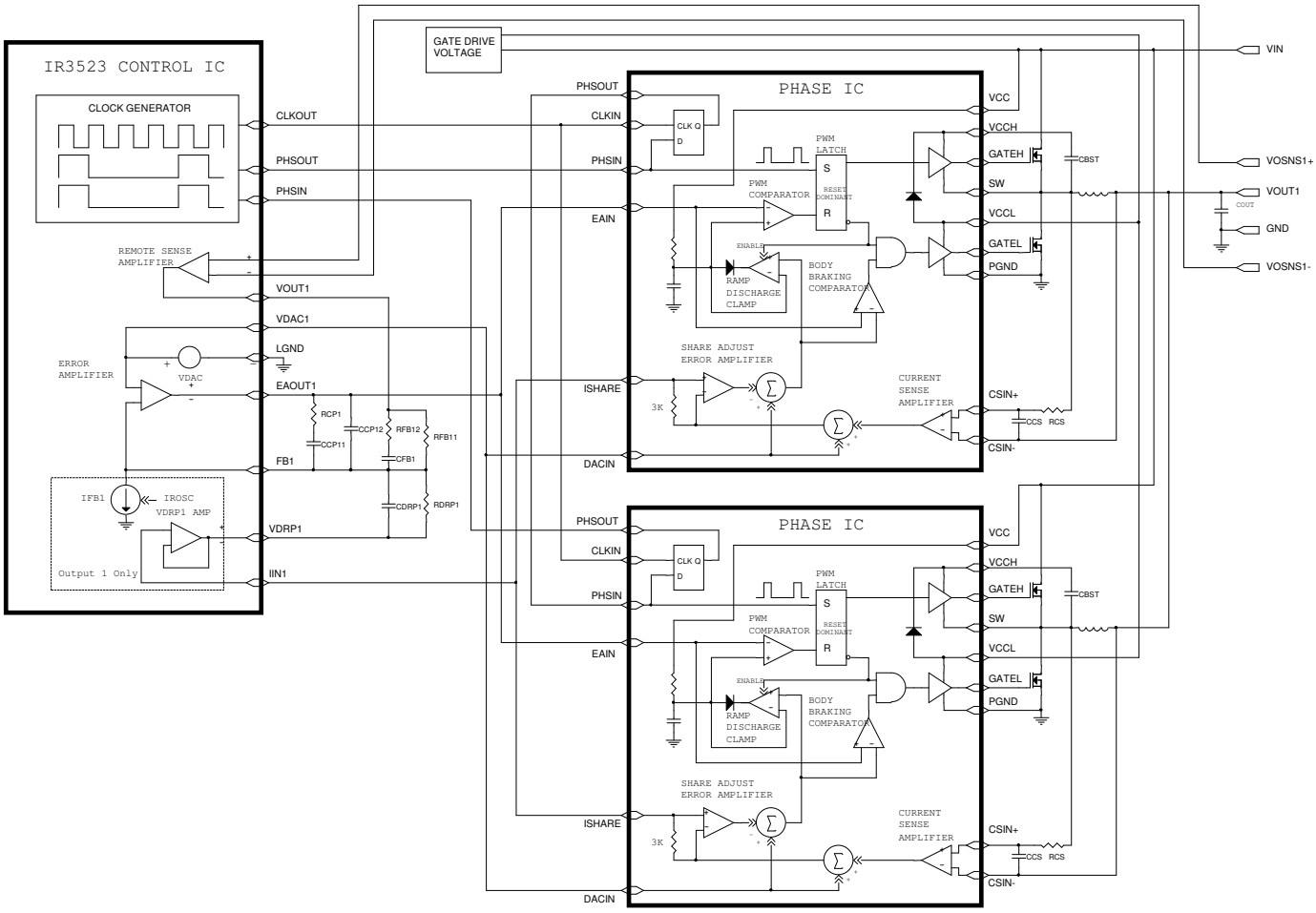

Figure 5 - PWM Block Diagram

Frequency and Phase Timing Control

The oscillator is located in the Control IC and the system clock frequency is programmable from 500kHz to 9MHZ by an external resistor. The control IC system clock signal (CLKOUT) is connected to CLKIN of all the phase ICs. The phase timing of the phase ICs is controlled by the daisy chain loop, where control IC phase clock output (PHSOUT) is connected to the phase clock input (PHSIN) of the first phase IC, and PHSOUT of the first phase IC is connected to PHSIN of the second phase IC, etc. and PHSOUT of the last phase IC is connected back to PHSIN of the control IC. During power up, the control IC sends out clock signals from both CLKOUT and PHSOUT pins and detects the feedback at PHSIN pin to determine the phase number and monitor any fault in the daisy chain loop. Figure 6 shows the phase timing for a four phase converter.

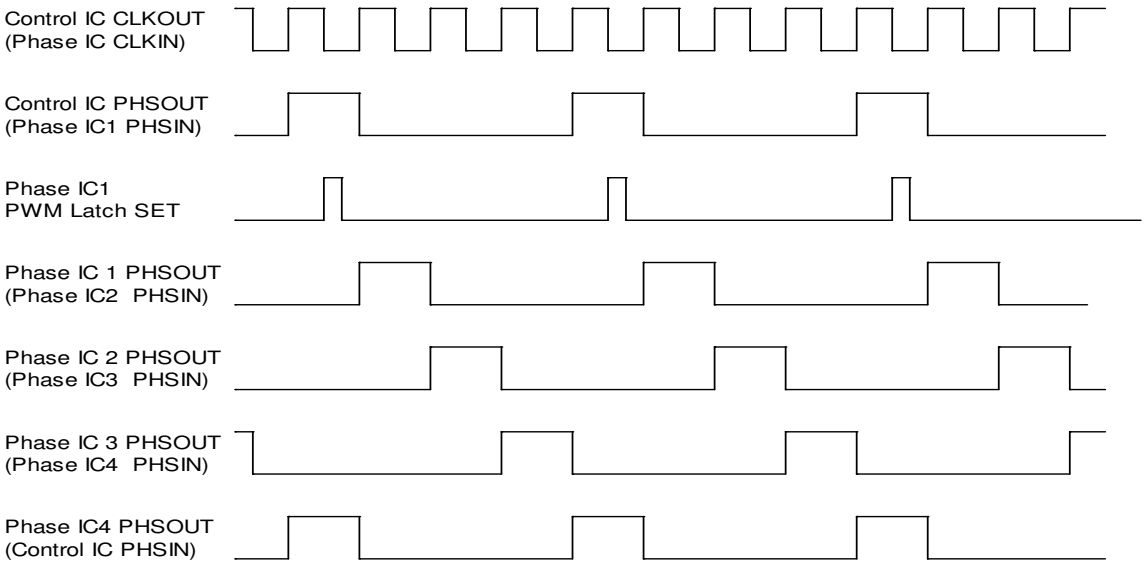

Figure 6 - Four Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the phase IC. Upon receiving the falling edge of a clock pulse, the PWM latch is set; the PWMRMP voltage begins to increase; the low side driver is turned off, and the high side driver is then turned on after the non-overlap time. When the PWMRMP voltage exceeds the error amplifier's output voltage, the PWM latch is reset. This turns off the high side driver and then turns on the low side driver after the non-overlap time; it activates the ramp discharge clamp, which quickly discharges the PWMRMP capacitor to the output voltage of share adjust amplifier in phase IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go up to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response" where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage of the architecture is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Figure 7 depicts PWM operating waveforms under various conditions.

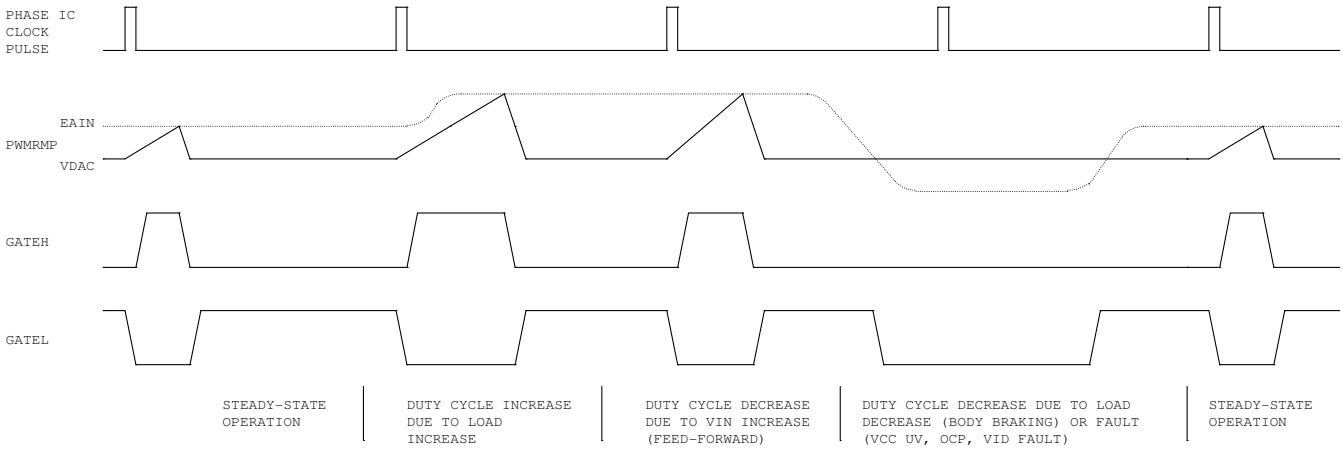

Figure 7 - PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "body braking" and is accomplished through the "body braking comparator" located in the phase IC. If the error amplifier's output voltage drops below the VDAC voltage or a programmable voltage, this comparator turns off the low side gate driver.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 8. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L+sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

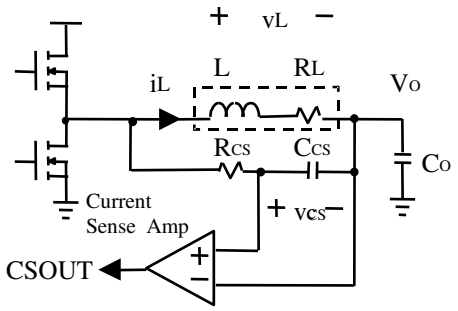

Figure 8 - Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the phase IC, as shown in Figure 8. Its gain is nominally 34 at 25ºC, and the 3850 ppm/ºC increase in inductor DCR should be compensated in the voltage loop feedback path.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the control IC and other phases through an on-chip 3KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the control IC for voltage positioning and current limit protection.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

IR3523 THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3523 is shown in Figure 3, and specific features are discussed in the following sections. All the features are described using one output but suitable for both unless otherwise specified.

VIDx Control

The IR3523 converter outputs are independently controlled by two three-bit input interfaces (see Table 1-2): VDAC1 (VOUT1) and VDAC2 (VOUT2). The VID codes are stored and then inputted to the Digital-to-Analog Converter (DAC) whose output is sent to the VDAC buffer amplifier. The output of the buffer amplifier is the VDAC pin. VDAC1 will initially boot to 1.1V when Vout1 is enabled then will transition to the stored VID1 value once SS/DEL1 reached 3.0 V. The VDAC voltage, input offsets of error amplifier and remote sense differential amplifier, are post-package trimmed to provide 0.5% system set-point accuracy. The actual VDAC voltage does not determine the system accuracy, which has a wider tolerance. The VID pins, VID2_x and VID1_x, require an external bias voltage and should not be floated.

The IR3523 can accept changes in the VID code while operating and vary DAC voltage accordingly. The sink/source capability of the VDAC buffer amplifier is programmed by the same external resistor that sets the oscillator frequency. The slew rate of the voltage at the VDAC pins can be adjusted by the external capacitors between VDAC pins and LGND pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifiers. The stepped VID transition results in a smooth analog transition of the VDAC voltage and converter output voltage. This analog transition minimizes inrush currents in the input (and output) capacitors and reduces overshoot of the output voltage.

VID1_4	VID1_3	VID1_2	VDAC1
0	0	0	**1.200**
0	0	1	**1.175**
0	1	0	**1.150**
0	1	1	**1.125**
1	0	0	**1.100**
1	0	1	**1.075**
1	1	0	**1.050**
1	1	1	**1.025**

Table 1: Output (1) 3-bit VID table

VID2_2	VID2_1	VID2_0	VDAC2
0	0	0	**1.350**
0	0	1	**1.400**
0	1	0	**1.450**
0	1	1	**1.500**
1	0	0	**1.550**
1	0	1	**1.600**
1	1	0	**1.650**
1	1	1	**1.800**

Table 2: Output (2) 3-bit VID table

Output 1 (Vtt) Adaptive Voltage Positioning

Adaptive Voltage Positioning is needed to reduce the output voltage deviations during load transients and the power dissipation of the load at heavy load. IR3523 only provides AVP on output1. The circuitry related to the voltage positioning is shown in Figure 9. Resistor R_{FB1} is connected between the error amplifier's inverting input pin FB1 and the remote sense differential amplifier output. An internal current source whose value is programmed by the same external resistor that programs the oscillator frequency sinks current from the FB1 pin. The error amplifier forces the converter's output voltage higher to maintain a balance at its inputs. R_{FB1} is selected to program the desired amount of fixed offset voltage above the DAC voltage.

The VDRP1 pin voltage is a buffered reproduction of the IIN1 pin which is connected to the current share bus ISHARE. The voltage on ISHARE represents the system average inductor current information. At each phase IC, an RC network across the inductor provides current information which is gained up 32.5X and then added to the $VDAC_X$ voltage. This phase current information is provided on the ISHARE bus via a 3K resistor in the phase ICs.

The VDRP1 pin is connected to the FB1 pin through the resistor R_{DRP1}. Since the error amplifier will force the loop to maintain FB1 to be equal to the VDAC1 reference voltage, an additional current will flow into the FB1 pin equal to (VDRP1-VDAC1) / R_{DRP1}. When the load current increases, the adaptive positioning voltage increases accordingly. More current flows through the feedback resistor R_{FB1}, and makes the output voltage lower proportional to the load current. The positioning voltage can be programmed by the resistor R_{DRP1} so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to VDAC1 and therefore independent of the VDAC1 voltage.

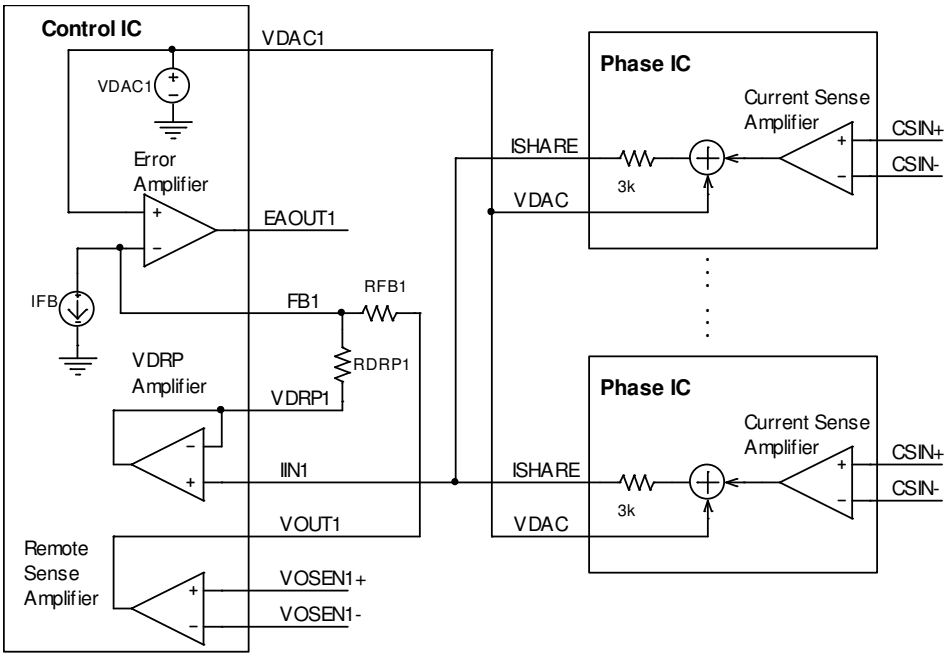

Figure 9 - Adaptive voltage positioning

Output1 Inductor DCR Temperature Compensation

A negative temperature coefficient (NTC) thermistor can be used for Output1 inductor DCR temperature compensation. The thermistor should be placed close to the Output1 inductors and connected in parallel with the feedback resistor, as shown in Figure 10. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

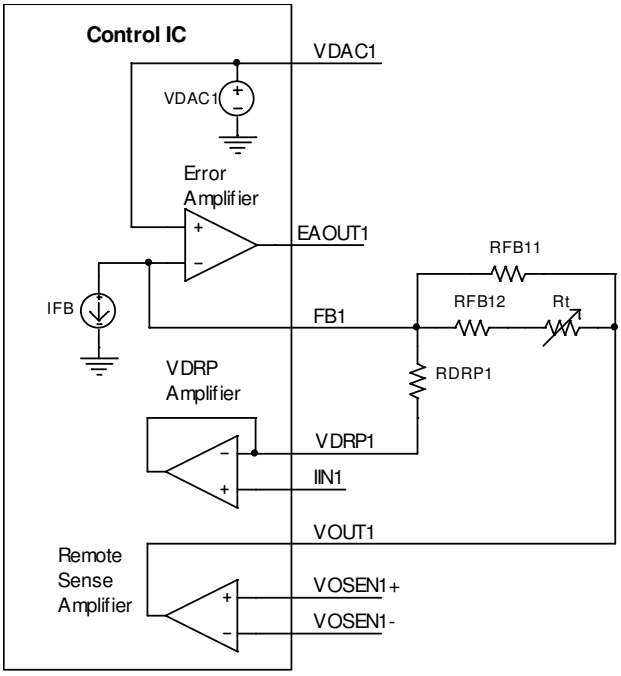

Figure 10 - Temperature compensation of Output1 inductor DCR

Remote Voltage Sensing

VOSENX+ and VOSENX- are used for remote sensing and connected directly to the load. The remote sense differential amplifiers with high speed, low input offset, and low input bias current ensure accurate voltage sensing and fast transient response.

Start-up Sequence

The IR3523 has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DELx and LGND pins controls soft start timing, over-current protection delay and hiccup mode timing. A charge current of 50uA and discharge currents of 47uA and 4.5uA control the up slope and down slope of the voltage at the SS/DEL pin respectively.

Figure 11 depicts the start-up sequence. If the ENABLE input is asserted and there are no faults, the SS/DELx pins will start charging, the VID codes are read and stored. VDAC2 transitions to the stored VID code, while VDAC1 transitions to a 1.1V internal boot voltage. The error amplifier output EAOUTx is clamped low until SS/DELx reaches 1.4 V. The error amplifier will then regulate the converter's output voltage to match the SS/DELx voltage less the 1.4 V offset until the converter VOUT2 reaches programmed VID code and VOUT1 reaches 1.1V (boot voltage). When SS/DEL1 reaches 3.0 V, VDAC1 will transition to the stored VID1 code shifting VOUT1 to the new regulation value. The SS/DELx voltage continues to increase until it rises above the threshold of Delay Comparator (3.93V). The PGx output is then de-asserted (allowed to go high).

VCCL under voltage, over current, and a low signal on the ENABLE input immediately sets a fault latch, which causes the EAOUT pin to drive low turning off the phase IC drivers. The PGx pins also drives low and SS/DELx begin to discharge until the voltage reaches 0.2 V. If the fault has cleared, the fault latch will be reset by the discharge comparator allowing a normal soft start to occur.

Other fault conditions, such as over voltage, open sense lines, and open daisy chain, set different fault latches, which start discharging SS/DELx, pull down EAOUTx voltage and drive PG low. However, the latches can only be reset by cycling VCCL power (see Table 3).

If SS/DELx pins are pulled below 0.6V, the converter can be disabled.

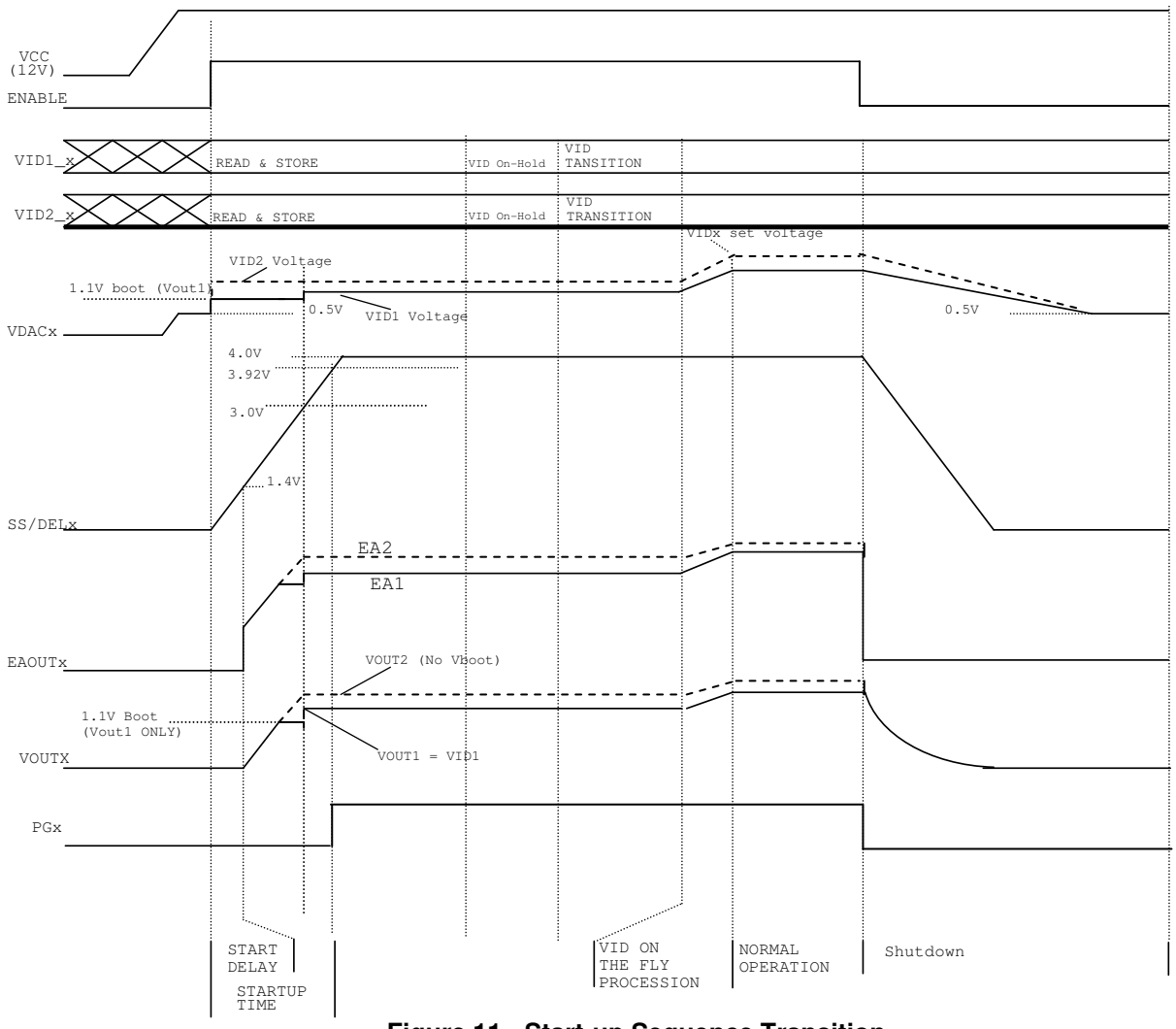

Figure 11 - Start-up Sequence Transition

Over-Current Hiccup Protection after Soft Start

The over current limit threshold is set by a resistor connected between OCSETx and VDACx pins. Figure 12 shows the hiccup over-current protection with delay after PGx is asserted. The delay is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions.

If the IINx pin voltage, which is proportional to the average current plus VDACx voltage, exceeds the OCSETx voltage after PGx is asserted, it will initiate the discharge of the capacitor at SS/DELx through the discharge current 47uA. If the over-current condition persists long enough for the SS/DELx capacitor to discharge below the 120mV offset of the delay comparator, a fault latch will be set pulling the error amplifier's output low and inhibiting switching in the phase ICs and de-asserting the PGx signal. The SS/DEL capacitor will then continue to discharge through a 4.7uA discharge current until it reaches 200 mV, and the fault latch is reset allowing a normal soft start to occur. The output current is not controlled during the delay time. If an over-current condition is again encountered during the soft start cycle, the over-current action will repeat and the converter will be in hiccup mode.

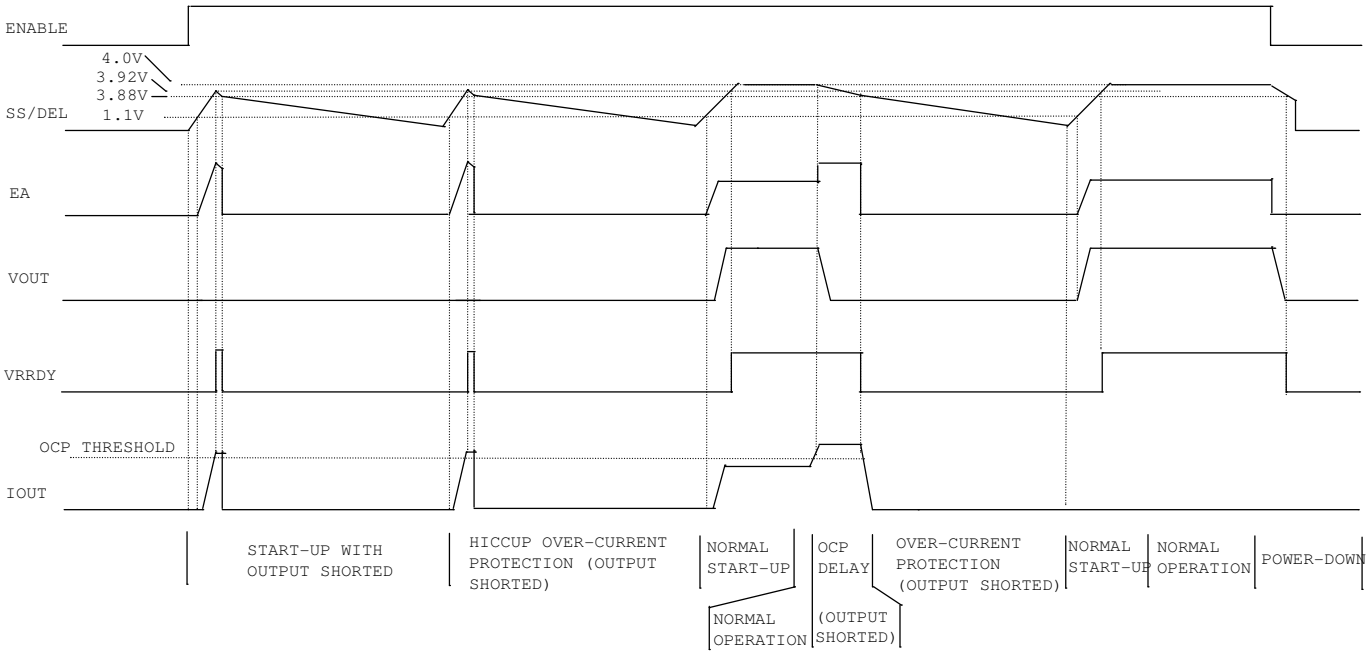

Figure 12 - Hiccup over-current waveforms

Linear Regulator Output (VCCL)

The IR3523 has a built-in linear regulator controller, and only an external NPN transistor is needed to create a linear regulator. The output voltage of the linear regulator can be programmed between 4.75V and 7.5V by the resistor divider at VCCLFB pin. The regulator output powers the gate drivers and other circuits of the phase ICs along with circuits in the control IC, and the voltage is usually programmed to optimize the converter efficiency. The linear regulator can be compensated by a 4.7uF capacitor at the VCCL pin. As with any linear regulator, due to stability reasons, there is an upper limit to the maximum value of capacitor that can be used at this pin and it's a function of the number of phases used in the multiphase architecture and their switching frequency. Figure 13 shows the stability plots for the linear regulator with 5 phases switching at 750 kHz.

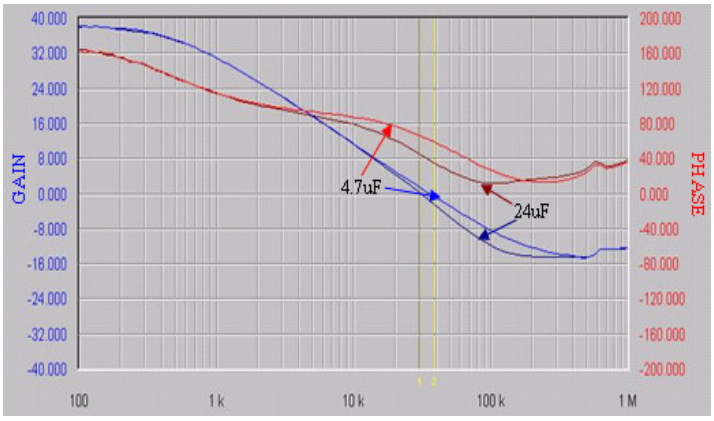

Figure 13 - VCCL regulator stability with 5 phases and PHSOUT equals 750 kHz

VCCL Under Voltage Lockout (UVLO)

The IR3523 has no under voltage lockout protection for the converter input voltage (VCC), but monitors the VCCL voltage instead. The VCCL is used to power both the control IC and phase ICs including the phase ICs internal gate drivers. During power up, the UVLO fault latch will be reset if VCCL is above 94% of the voltage set by resistor divider at VCCLFB pin. If VCCL voltage drops below 86% of the set value, the UVLO fault latch will be set.

Power Good (PG1, 2)

The PGx pin is an open-collector output and should be pulled up to a voltage source through a resistor. During soft start, the PGx remains low until the output voltage is in regulation and SS/DELx is above 3.93V. The PGx pin becomes low if any of the fault latches are triggered (See Table 3).

PGx monitors the output voltage. If any of the voltage planes fall out of regulation, PGx will become low, but the VR will continue to attempt to regulate the output voltages. Output voltage out of spec is defined as 315mV to 275mV below nominal voltage. VID on-the-fly transition, which is a voltage plane transitioning between two different VID codes, is not considered to be out of specification.

A high level at the PGx pins indicates that the converter is in operation with no fault and ensures the output voltage is within the regulation.

The PG outputs derive power from either VCCL or VCCLDRV to ensure they can assert with input voltage as low as possible.

Open Control Loop Detection

The error amplifier's output voltage is monitored to ensure the control loop is in regulation. If any fault condition forces the error amplifier output above VCCL-1.08 V for 8 switching cycles, the Open Control Loop fault latch is set. This fault latch can only be cleared by cycling power to VCCL.

Load Current Indicator Output

The VDRP pin voltage represents the average current of the converter plus the VDAC1 voltage. The load current information can be retrieved by using a differential amplifier to subtracts the VDAC1 voltage from the VDRP1 voltage.

Enable Input

Pulling the ENABLE pin below 1.0 V sets the Fault Latch. Forcing ENABLE to a voltage above 1.65V results in the 3-bit VID codes to be read and stored. SS/DEL$_X$ pins are also allowed to begin their power-up cycles as long as no fault conditions are present.

Over Voltage Protection (OVP)

Output over-voltage might occur due to a high side MOSFET short or if the output voltage sense path is compromised. If the over-voltage protection comparators sense that either VOUT$_X$ pin voltage exceeds VDAC$_X$ by 125mV, the over voltage fault latch is set which pulls the error amplifier output low turning off both converters power stage. The IR3523 communicates an OVP condition to the system by raising the ROSC pin voltage to within V(VCCL) – 1.2 V. An OVP condition is also communicated to the phase ICs by forcing the IIN pin (which is tied to the ISHARE bus and ISHARE pins of the phase ICs) to VCCL as shown in Figure 14. In each phase IC, the OVP circuit overrides the normal PWM operation to ensure the low side MOSFET turn-on within approximately 130ns. The low side MOSFET will remain on until the ISHARE pins fall below V(VCCL) - 800mV. An over voltage fault condition is latched in the IR3523 and can only be cleared by cycling the power to VCCL.

During dynamic VID down at light to no load, false OVP triggering is prevented by increasing the OVP threshold to a fixed 1.2 V (VOUT1) and 1.8 V (VOUT2) whenever a dynamic VID is detected and the difference between output voltage and the fast internal VDAC is more than 50mV, as shown in Figure 15. The over-voltage threshold is changed back to VDAC+125mV if the difference between output voltage and the fast internal VDAC is less than 50mV.

The overall system must be considered when designing for OVP. In many cases the over-current protection of the AC-DC or DC-DC converter supplying the multiphase converter will be triggered thus providing effective protection without damage as long as all PCB traces and components are sized to handle the worst-case maximum current. If this is not possible, a fuse can be added in the input supply to the multiphase converter.

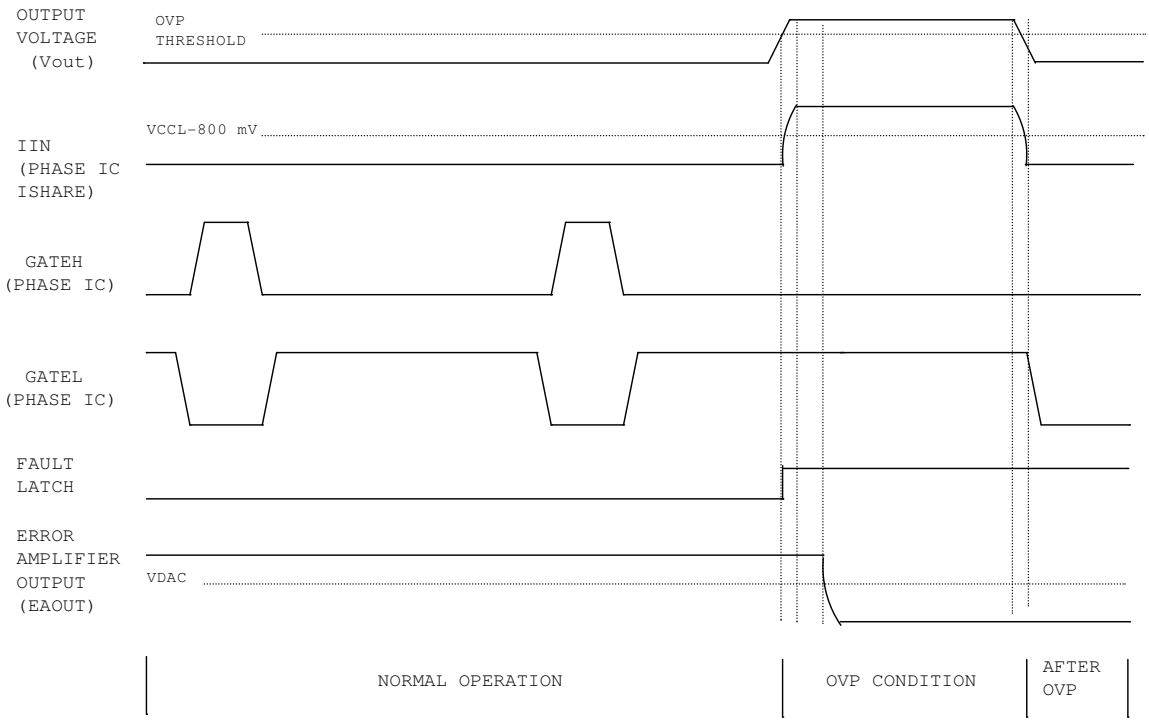

Figure 14 - Over-voltage protection during normal operation

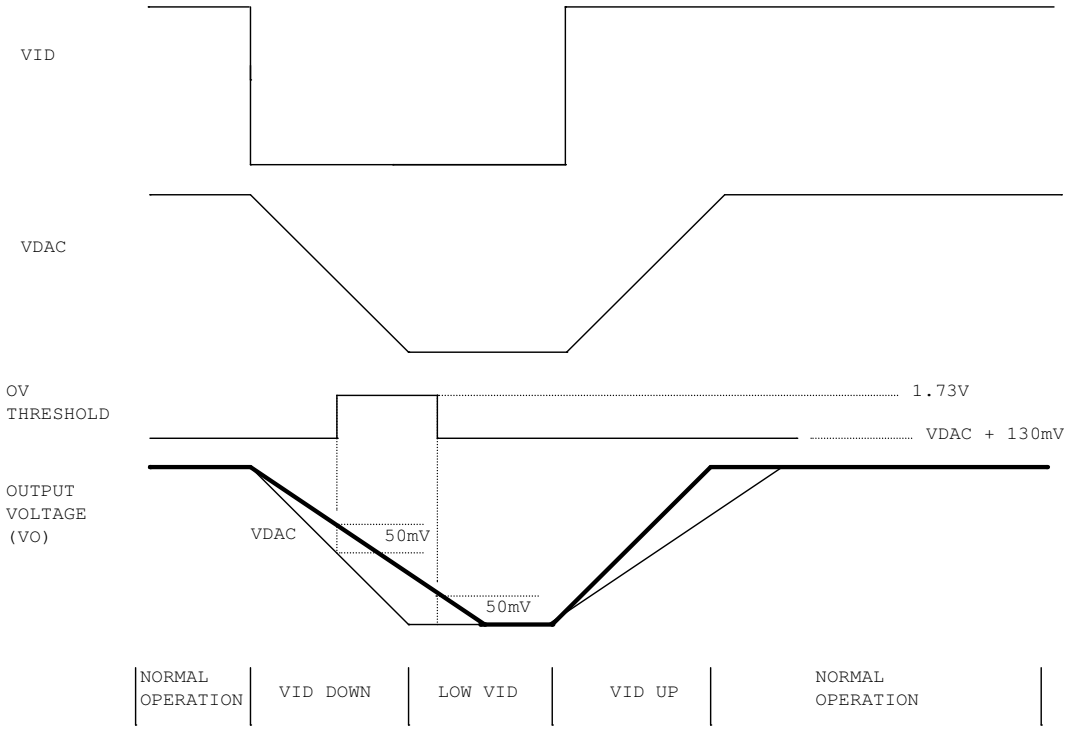

Figure 15 - Over-voltage protection during dynamic VID

Open Remote Sense Line Protection

If either remote sense line $VOSEN_X+$ or $VOSEN_X-$ is open, the output of Remote Sense Amplifier ($VOUT_X$) drops. The IR3523 continuously monitors the $VOUT_X$ pin and if $VOUT_X$ is lower than 200 mV, two separate pulse currents are applied to the $VOSEN_X+$ and $VOSEN_X-$ pins to check if the sense lines are open. If $VOSEN_X+$ is open, a voltage higher than 90% of V(VCCL) will be present at $VOSEN_X+$ pin and the output of Open Line Detect Comparator will be high. If $VOSEN_X-$ is open, a voltage higher than 400mV will be present at $VOSEN_X-$ pin and the Open Line Detect Comparator output will be high. With either sense line open, the Open Sense Line Fault Latch will be set to force the error amplifier output low and immediately shut down the converter. SS/DEL_X will be discharged and the Open Sense Fault Latch can only be reset by cycling the power to VCCL.

Open Daisy Chain Protection

IR3523 checks the daisy chain every time it powers up. It starts a daisy chain pulse on the PHSOUT pin and detects the feedback at PHSIN pin. If no pulse comes back after 32 CLKOUT pulses, the pulse is restarted again. If the pulse fails to come back the second time, the open daisy chain fault is registered, and SS/DEL is not allowed to charge. The fault latch can only be reset by cycling the power to VCCL.

After powering up, the IR3523 monitors PHSIN pin for a phase input pulse equal or less than the number of phases detected. If PHSIN pulse does not return within the number of phases in the converter, another pulse is started on PHSOUT pin. If the second started PHSOUT pulse does not return on PHSIN, an open daisy chain fault is registered.

Phase Number Determination

After a daisy chain pulse is started, the IR3523 checks the timing of the input pulse at PHSIN pin to determine the phase number.

The Fault Table below describes ten different faults that can occur during normal operation and how the IR3523 IC will react to protect the supply and the load from possible damage. The fault types that can occur are listed in row one. Row two and three describes the type and the method of clearing the faults, respectively. The first four faults are latched in the UV fault and require the VCCL supply to be recycled (below UVLO threshold) to regain operation. The rest of the faults, except for UVLO Vout, are latched in a SS fault which do not need VCCL supply recycled, but instead will automatically resume operation when these fault conditions are no longer impinging on the system. Most of the faults will disable the error amplifier (EA) and discharge the soft start capacitor. All of the faults flag PGood. PGood returns to high impedance state (high) when the fault clears. The Delay row shows reaction time after detecting a fault condition. Delays are provided to minimize the possibility of nuisance faults. Additional flagged responses are used to communicate externally of a fault event (Over Voltage) so additional action can be taken.

System Fault Table

Fault Type	Open Daisy	Open Sense	Open Control	Over Voltage	Disable	UVLO (VCCL)	OC Before	OC After	UVLO (Vout)
Latch	UV Latch				SS Latch				No
Fault Clearing Method	Recycle VCCL				SS discharge below 0.2V				No
Outputs Affected	Both	Single		Both	Both	Both	Single		Single
Error Amp Disables	Yes								No
SS/DELx Discharge	Yes								No
Flags PGood	Yes								
Delays	32 Clock Pulses	No	8 PHSOUT Pulses	No	250ns Blanking Time	No	PHSOUT Pulses*	SS/DELx Discharge Threshold	No
Additional Flagged Response	No			Yes, IINx and Rosc pins pulled-up to VCCL**	No				

* Pulse number range depends on Rosc value selected (See Specifications Table)
** Clears when OV condition ends

Table 3 - IR3523 system fault responses

APPLICATIONS INFORMATION

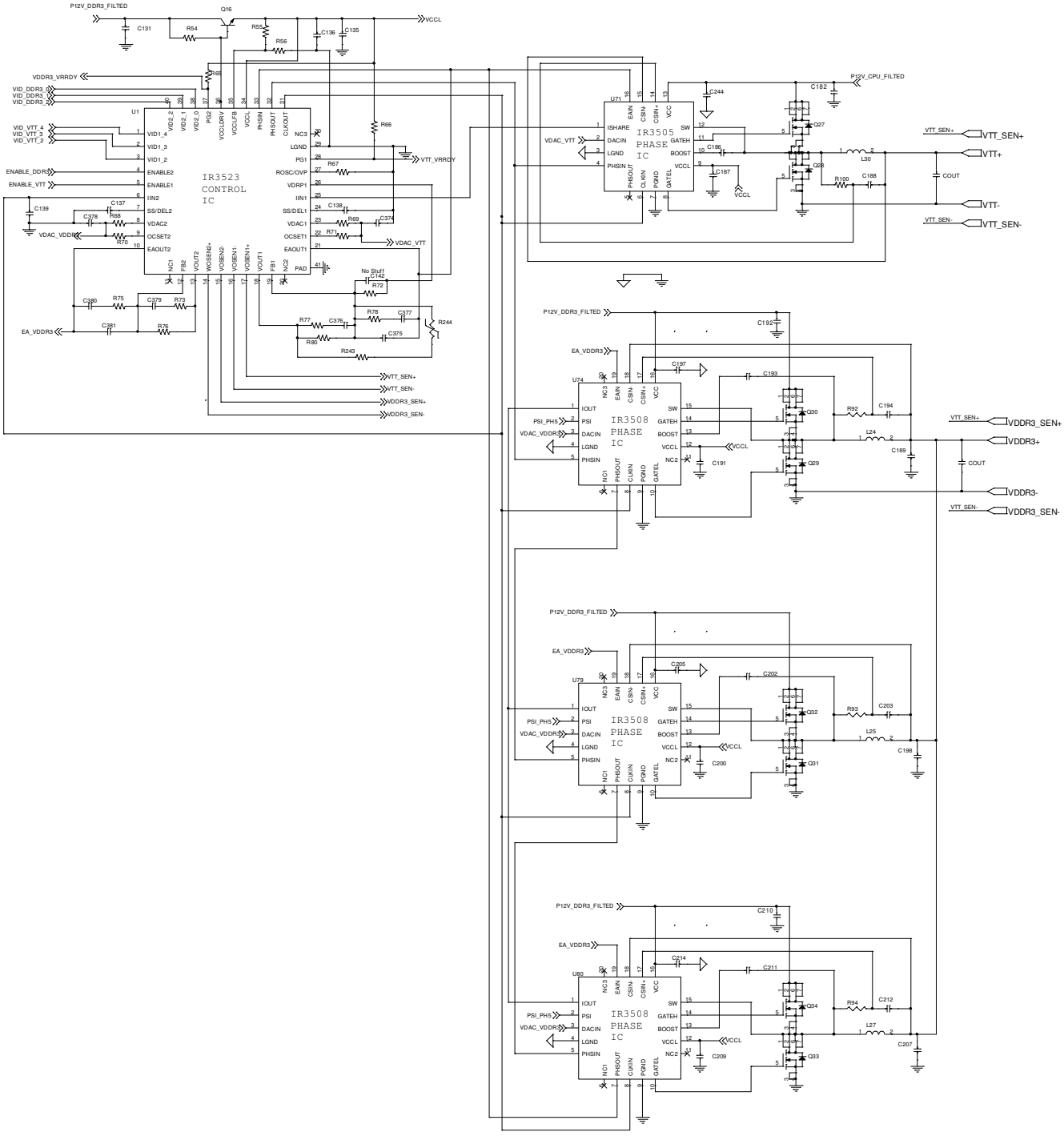

Figure 16 - IR3523 \ IR3508 Three Phases VDDR3 and a Single Phase (IR3505) Vtt One Phase Converter

DESIGN PROCEDURES - IR3523 AND IR3505 CHIPSET

IR3523 EXTERNAL COMPONENTS

All the output components are selected using one output but suitable for both unless otherwise specified.

Oscillator Resistor *Rosc*

The IR3523 generates square-wave pulses to synchronize the phase ICs. The switching frequency of the each phase converter equals the PHSOUT frequency, which is set by the external resistor RROSC, use Figure 2 to determine the RROSC value. The CLKOUT frequency equals the switching frequency multiplied by the phase number.

Soft Start Capacitor *CSS/DEL*

The Soft Start capacitor CSS/DEL programs four different time parameters, soft start delay time, soft start time, PGx delay time and over-current fault latch delay time after PGx.

SS/DELx pin voltage controls the slew rate of the converter output voltage, as shown in Figure 10. Once the ENABLE pin rises above 1.65V, there is a soft-start delay time TD1 during which SS/DEL pin is charged from zero to 1.4V. Once SS/DEL reaches 1.4V, the error amplifier output is released to allow the soft start. The soft start time, TD2, represents the time during which converter voltage rises from zero to VID2 or VOUT1's boot voltage (1.1V). The SS/DELx pins voltage rises from 1.4V to VID2 (or VOUT1 boot) plus 1.4V. Power good delay time, TD3, is the time period from between where VR reaches the VID voltage and PGx signal assertion.

Calculate CSS/DEL based on the required soft start time TD2.

$$C_{SS/DEL} = \frac{TD2 * I_{CHG}}{VID} = \frac{TD2 * 50 * 10^{-6}}{VID} \qquad (1)$$

The soft start delay time TD1 and VR ready delay time TD3 are determined by equation (2) and (3) respectively.

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{C_{SS/DEL} * 1.4}{50 * 10^{-6}} \qquad (2)$$

$$TD3 = \frac{C_{SS/DEL} * (3.93 - VID - 1.4)}{I_{CHG}} = \frac{C_{SS/DEL} * (3.93 - VID - 1.4)}{50 * 10^{-6}} \qquad (3)$$

Once CSS/DEL is chosen, use equation (4) to calculate the maximum over-current fault latch delay time tOCDEL.

$$t_{OCDEL} = 2.5 * \frac{C_{SS/DEL} * 0.12}{I_{DISCHG}} = 2.5 * \frac{C_{SS/DEL} * 0.12}{47 * 10^{-6}} \qquad (4)$$

Due to the exponential turn-on slope of the discharge current (47uA), a correction factor (X2.5) is added to the equation (4) to accurately predict over-current delay time.