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IR3628MPbF

HIGH FREQUENCY SYNCHRONOUS PWM BUCK CONTROLLER

Features

- Internal 600kHz Oscillator
- Operates with Single 5V or 12V Supply
- Programmable Over Current Protection
- Hiccup Current Limit Using MOSFET $R_{DS(on)}$ sensing
- Tracking for memory application
- Precision Reference Voltage (0.6V)
- Programmable Soft-Start
- Pre-Bias Start-up
- Thermal Protection
- 12-Lead 3x4mm MLPD Package

Applications

- DDR Application
- Storage Systems
- Embedded Telecom Systems
- Distributed Point of Load Power Architectures
- Computing Peripheral Voltage Regulator
- Graphics Card
- General DC/DC Converters

Description

The IR3628 is a PWM controller designed for high performance synchronous Buck DC/DC applications. The IR3628 drives a pair of external N-MOSFETs using a fixed 600kHz switching frequency allowing the use of small external components. The output voltage can be precisely regulated using the internal 0.6V reference voltage for low voltage applications. IR3628 provides an efficient solution for high-speed bandwidth data bus which requires a particular tracking scheme for best performance using the uncommitted error amplifier.

Protection such as Pre-Bias startup, hiccup current limit and thermal shutdown are provided to give required system level security in the event of fault conditions.

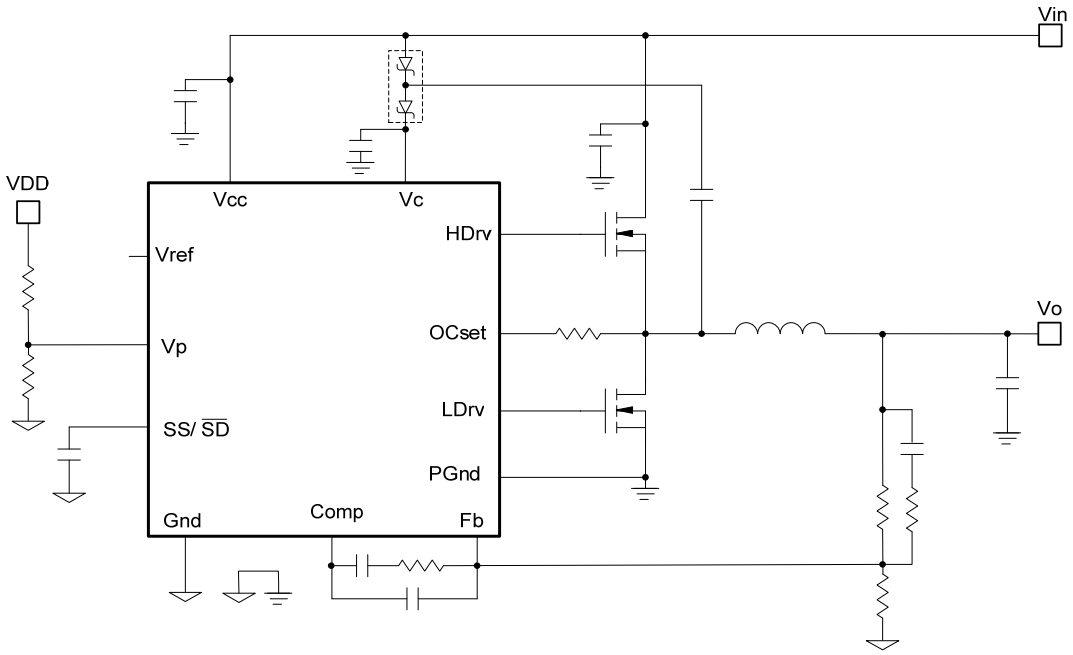


Fig. 1: Typical application Circuit

ORDERING INFORMATION

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T&R ORIANTAION
M	IR3628MPBF	12	122	-------	Figure A
M	IR3628MTRPBF	12	--------	3000	

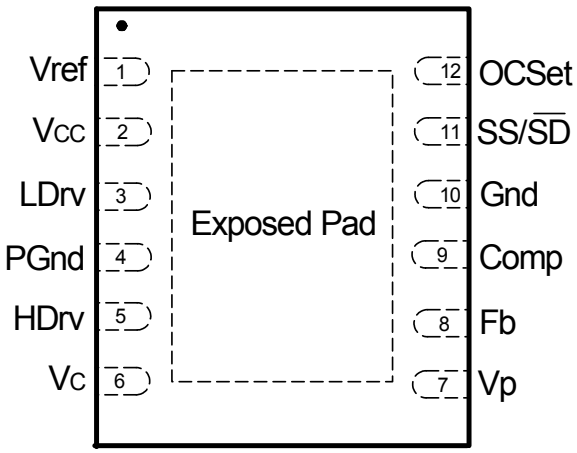
ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)

- Vcc Supply Voltage ..... -0.5V to 16V
- Vc Supply Voltage ..... -0.5V to 30V
- Vref, Vp, Fb, Comp, SS ..... -0.3V to 3.5V
- OCset 10mA
- AGnd to PGnd ..... -0.3V to +0.3V
- Storage Temperature Range ..... -65°C To 150°C
- Operating Junction Temperature Range ..... -40°C To 150°C
- ESD Classification ..... JEDEC, JESD22-A114
- Moisture Sensitivity Level ..... JEDEC Level 2 @ 260°C

Caution: *Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to "Absolute Maximum Rating" conditions for extended periods may affect device reliability.*

Package Information



12-Lead MLPD, 3x4mm

Θ_{JA} = 30° C/W *
Θ_{JC} = 2° C/W

**Exposed pad on underside is connected to a copper pad through vias for 4-layer PCB board design*

Block Diagram

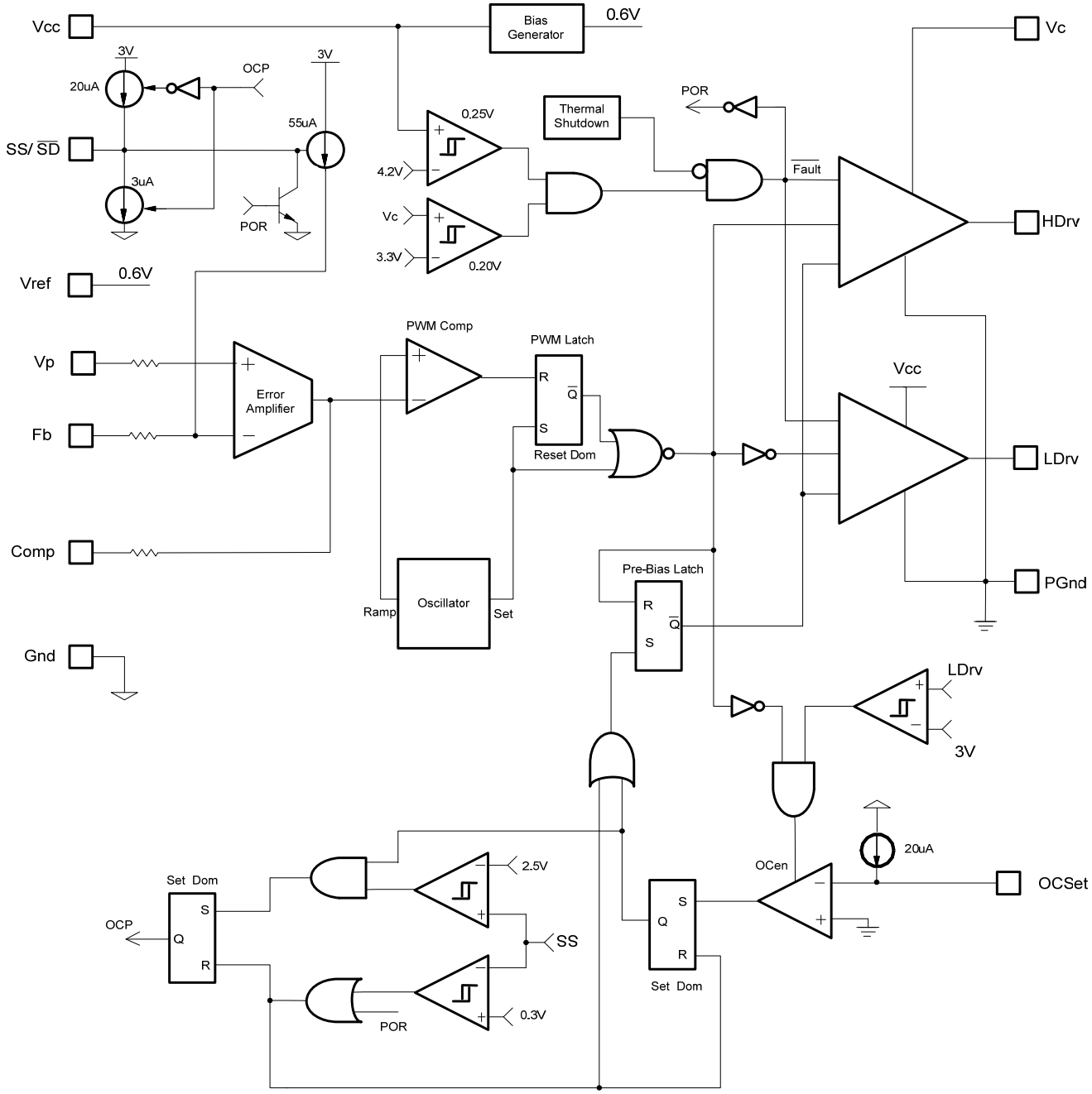


Fig. 2: Simplified block diagram of the IR3628

Pin Description

Pin	Name	Description
1	Vref	External reference voltage. Drive capability for this pin is 2uA.
2	Vcc	This pin provides power for the internal blocks of the IC as well as powers the low side driver. A minimum of 0.1uF, high frequency capacitor must be connected from this pin to power ground.
3	LDrv	Output driver for low side MOSFET
4	PGnd	Power Ground. This pin serves as a separate ground for the MOSFET drivers and should be connected to the system's power ground plane.
5	HDrv	Output driver for high side MOSFET
6	Vc	This pin powers the high side driver and must be connected to a voltage higher than bus voltage. A minimum of 0.1uF, high frequency capacitor must be connected from this pin to power ground.
7	Vp	Non inverting input of error amplifier, this pin can be used for tracking application.
8	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
9	Comp	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
10	Gnd	Signal ground for internal reference and control circuitry.
11	SS/SD	Soft start / shutdown. This pin provides user programmable soft-start function. Connect an external capacitor from this pin to ground to set the start up time of the output voltage. The converter can be shutdown by pulling this pin below 0.3V.
12	OCSet	Current limit set point. A resistor from this pin to drain of low side MOSFET will set the current limit threshold.

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{cc}	Supply Voltage	4.5	14	V
V_c	Supply Voltage	Converter voltage + 5	28	V
T_j*	Junction Temperature	-40	125	°C

*The junction Temperature for 5V application is 0°C-125°C

Electrical Specifications

Unless otherwise specified, these specification apply over V_{cc}=V_c=12V, 0°C<T_j< 105°C

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Voltage Accuracy						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		0°C<Tj<105°C	-1.5		+1.5	%
		-40°C<Tj<105°C, *Note1*	-2.5		+1.5	%
Supply Current						
V_{CC} Supply Current (Static)	$I_{CC(Static)}$	SS=0V, No Switching		10	13	mA
V_{CC} Supply Current (Dynamic)	$I_{CC(Dynamic)}$	F_s=600kHz, C_{LOAD}=1.5nF		15	25	mA
V_C Supply Current (Static)	$I_{C(Static)}$	SS=0V, No Switching		4.5	7	mA
V_C Supply Current (Dynamic)	$I_{C(Dynamic)}$	F_s=600kHz, C_{LOAD}=1.5nF		17	25	mA
Under Voltage Lockout						
V_{CC}-Start-Threshold	V_{CC}_UVLO(R)	Supply ramping up	4.0	4.2	4.4	V
V_{CC}-Stop-Threshold	V_{CC}_UVLO(F)	Supply ramping down	3.7	.9	4.1	V
V_{CC}-Hysteresis		Supply ramping up and down	0.15	0.25	0.3	V
V_C-Start-Threshold	V_C_UVLO(R)	Supply ramping up	3.1	3.3	3.5	V
V_C-Stop-Threshold	V_C_UVLO(F)	Supply ramping down	2.85	3.05	3.25	V
V_C-Hysteresis		Supply ramping up and down	0.15	0.2	0.25	V
Oscillator						
Frequency	F_S		540	600	660	kHz
Ramp Amplitude	V_{ramp}	*Note2*		1.25		V
Min Duty Cycle	D_{min}	Fb=1V			0	%
Min Pulse Width	$D_{min(ctrl)}$	F_s=600kHz, *Note2*			80	ns
Max Duty Cycle	D_{max}	F_s=600kHz, Fb=0.5V	71			%

Note1: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

Note2: Guaranteed by Design but not tested in production.

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Error Amplifier						
Fb Input Bias Current	I_{FB1}	SS=3V		-0.1	-0.5	µA
Vp Input Bias Current	I_{Vp}	SS=3V		-0.1	-0.5	µA
Fb Input Bias Current	I_{FB2}	SS=0V	40	55	70	µA
Source/Sink Current	I(source/Sink)		50	70	100	µA
Transconductance	gm		1000	1300	1600	µmho
Input Offset Voltage	Vos	Fb to Vp	-4.5	0	+4.5	mV
Vp (Common Mode Range)	Vp		0.2		1.0	V
Soft Start/SD						
Soft Start Current	I_{SS}	SS=0V	15	20	28	µA
Shutdown Output Threshold	SD				0.25	V
Over Current Protection						
OCSET Current	I_{OCSET}		15	20	26	µA
Hiccup Current	I_{Hiccup}	*Note2*		3		µA
Hiccup Duty Cycle	Hiccup(duty)	I_{Hiccup} / I_{SS} , *Note2*		15		%
Thermal Shutdown						
Thermal Shutdown Threshold		*Note2*		140		°C
Thermal Shutdown Hysteresis		*Note2*		20		°C
Output Drivers						
LO, Drive Rise Time	Tr(Lo)	CL=1.5nF, F_s=600kHz See Fig 3		30	60	ns
HI Drive Rise Time	Tr(Hi)	CL=1.5nF, F_s=600kHz See Fig 3		30	60	ns
LO Drive Fall Time	Tf(Lo)	CL=1.5nF, F_s=600kHz See Fig 3		30	60	ns
HI Drive Fall Time	Tf(Hi)	CL=1.5nF, F_s=600kHz See Fig 3		30	60	ns
Dead Band Time	Tdead	See Fig 3	10	50	100	ns

Note2: Guaranteed by Design but not tested for production.

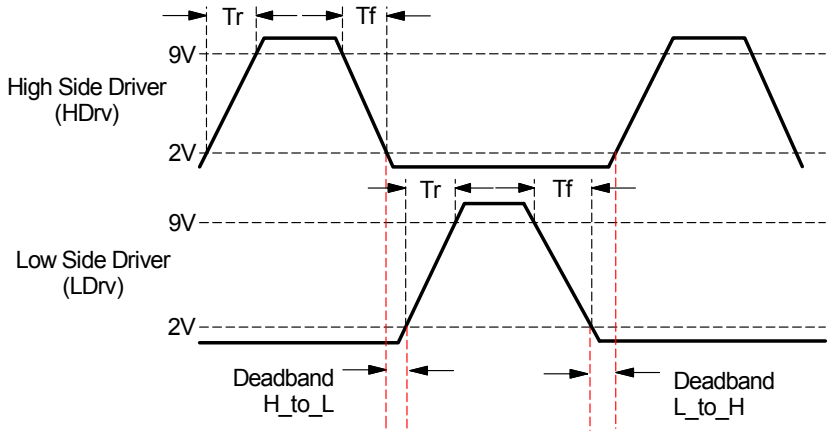
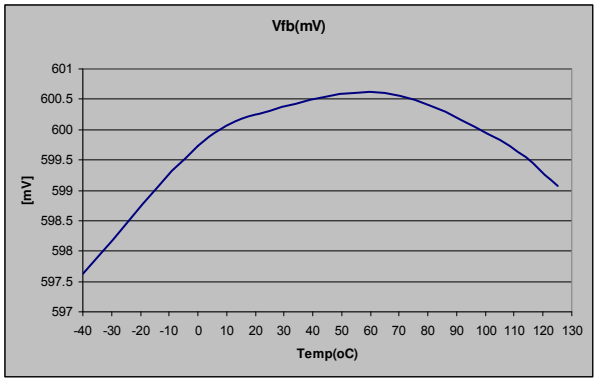
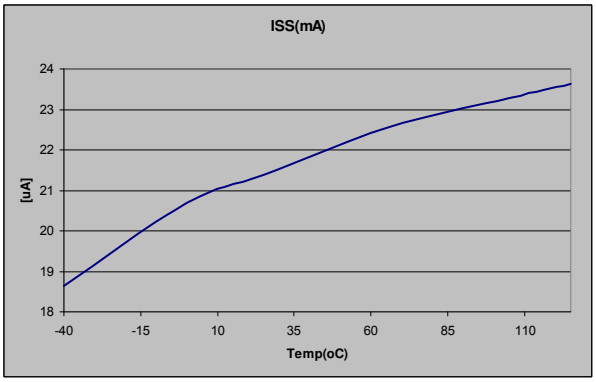
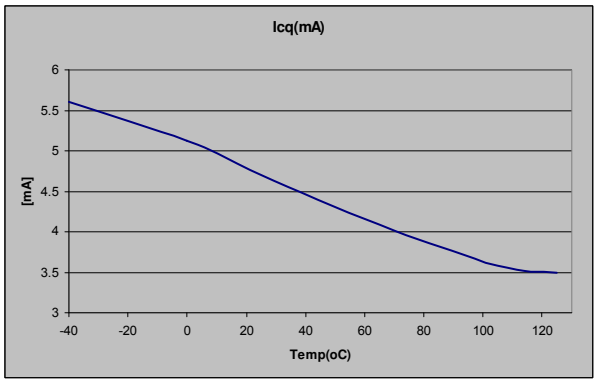


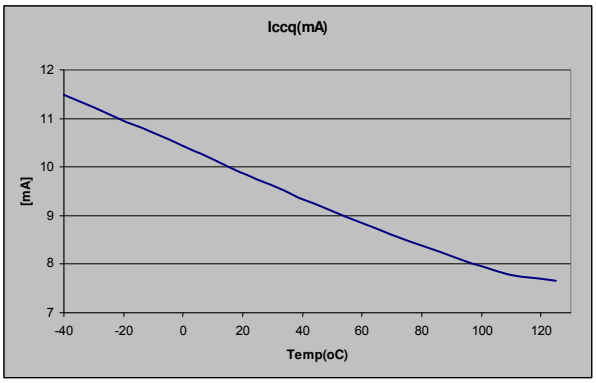
Fig. 3: Definition of Rise/Fall time and Deadband Time

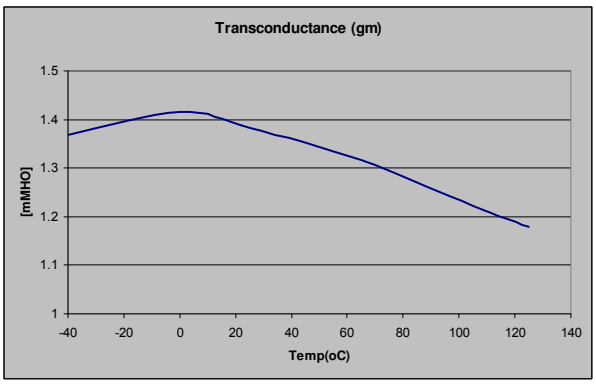
TYPICAL OPERATING CHARACTERISTICS

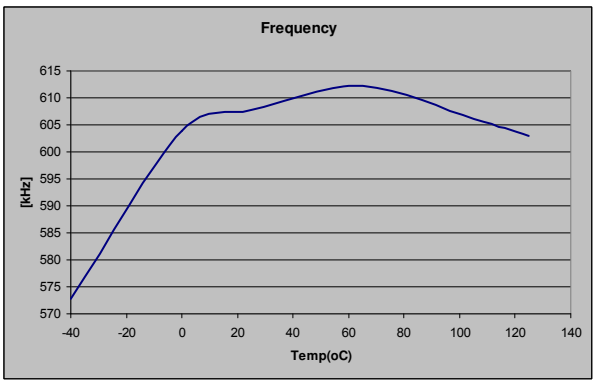


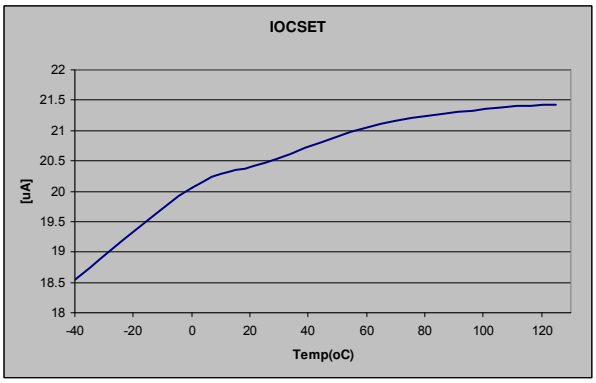


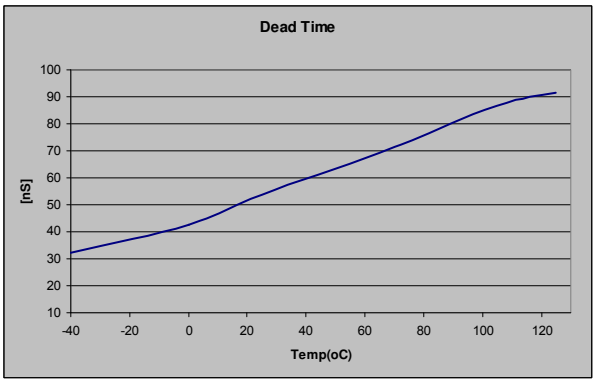












Circuit Description

THEORY OF OPEARTION

Introduction

The IR3628 is a voltage mode PWM synchronous controller and operates with a fixed 600kHz switching frequency, allowing the use of small external components. The output voltage is set by feedback pin (Fb) and the external reference voltage (0.6V). These are two inputs to error amplifier. The error signal between these two inputs is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle (D) which drivers N-channel external MOSFETs.

The timing of the IC is controlled by an internal oscillator circuit that uses on-chip capacitor to set the switching frequency.

The IR3628 operates with single input voltage from 4.5V to 12V allowing an extended operating input voltage range.

The current limit is programmable and uses on-resistance of the low-side MOSFET, eliminating the need for external current sense resistor.

Under-Voltage Lockout

The under-voltage lockout circuit monitors the two input supplies (Vcc and Vc) and assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set thresholds. Lockout occurs if Vc or Vcc fall below 3.3V and 4.2V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

Thermal Shutdown

Temperature sensing is provided inside IR3628. The trip threshold is typically set to 145°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs. Thermal shutdown is not latched and automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

Minimum Pulse Width

The time required of turning on and off the high side MOSFET is defined as “Minimum Pulse Width”. To ensure that a reliable operation is achieved the following condition needs to be met:

$$T_{on(\min)} < \frac{V_{out}}{V_{in(\max)} * F_s}$$

Shutdown

The output can be shutdown by pulling the soft-start pin below 0.3V. This can be easily done by using an external small signal transistor. During shutdown both MOSFET drivers will be turned off. Normal operation will resume by cycling soft start pin.

Error Amplifier

The IR3628 is a voltage mode controller. The error amplifier is of transconductance type. The amplifier is capable of operating with Type III compensation control scheme using low ESR output capacitance.

Pre-Bias Startup

IR3628 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated. Figure 4 shows a typical Pre-Bias condition at start up.

Depends on system configuration, specific amount of output capacitors may be required to prevent discharging the output voltage.

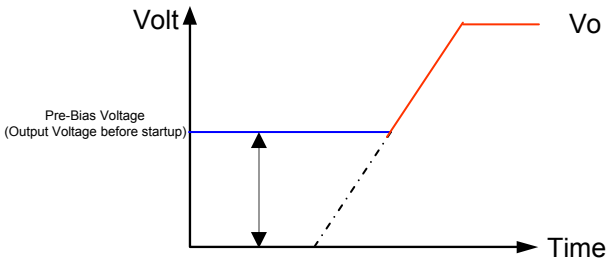


Fig. 4: Pre-Bias start up

External Reference and Tracking

IR3628 is able to operate as a stand alone converter by connecting the Vref to Vp. In this case the reference voltage is 0.6V. For tracking application the Vref can be left floating and the Vp pin will be connected to master voltage which IR3628 will track. In this case the Vp voltage is the IC’s reference voltage.

Soft-Start

The IR3628 has programmable soft-start to control the output voltage rise and limit the inrush current during start-up.

To ensure correct start-up, the soft-start sequence initiates when Vcc and Vc rise above their threshold and generate the Power On Ready (POR) signal. The soft-start function operates by sourcing current to charge an external capacitor to about 3V.

Initially, the soft-start function clamps the output of error amplifier by injecting a current (40uA) into the Fb pin and generates a voltage about 0.96V (40ux24K) across the negative input of error amplifier (see figure 5).

The magnitude of the injected current is inversely proportional to the voltage at the soft-start pin. As the soft-start voltage ramps up, the injected current decreases linearly and so does the voltage at negative input of error amplifier.

When the soft-start capacitor is around 1V, the voltage at the positive input of the error amplifier is approximately 0.6V.

The output of error amplifier will start increasing and generating the first PWM signal. As the soft-start capacitor voltage continues to go up, the current flowing into the Fb pin will keep decreasing.

The feedback voltage increases linearly as the soft start voltage ramps up. When soft-start voltage is around 2V the output voltage is reached the steady state and the injected current is zero.

Figure 6 shows the theoretical operational waveforms during soft-start.

The output voltage start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V.

The start-up time will be dependent on the size of the external soft-start capacitor and can be estimate by:

$$20\mu A * \frac{T_{start}}{C_{ss}} = 2V - 1V$$

For a given start-up time, the soft-start capacitor (nF) can be estimated as:

$$C_{SS} \cong 20\mu A * T_{start}(ms) \quad \text{--(1)}$$

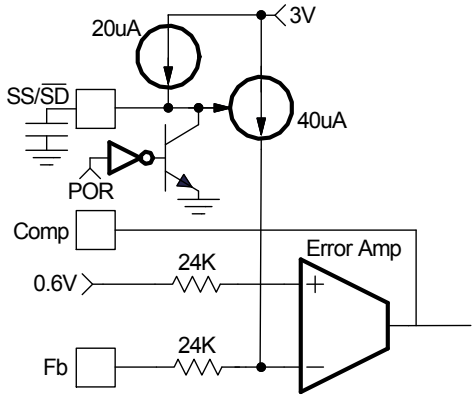


Fig. 5: Soft-Start circuit for IR3628

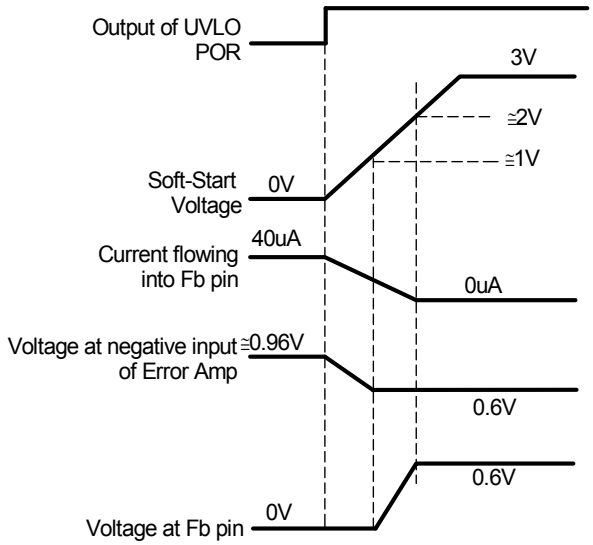


Fig. 6: Theoretical operation waveforms during soft-start

Over-Current Protection

The over current protection is performed by sensing current through the $R_{DS(on)}$ of low side MOSFET. This method enhances the converter's efficiency and reduce cost by eliminating a current sense resistor. As shown in figure 7, an external resistor (R_{SET}) is connected between OCSet pin and the drain of low side MOSFET (Q2) which sets the current limit set point.

The internal current source develops a voltage across R_{SET}. When the low side MOSFET is turned on, the inductor current flows through the Q2 and results a voltage which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) \quad --(2)$$

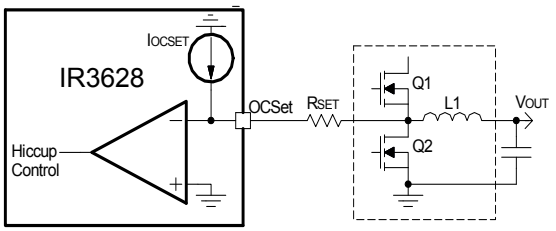


Fig. 7: Connection of over current sensing resistor

The critical inductor current can be calculated by setting:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) = 0$$

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \quad --(3)$$

An over current is detected if the OCSet pin goes below ground. This trips the OCP comparator and cycles the soft start function in hiccup mode.

The hiccup is performed by charging and discharging the soft-start capacitor in certain slope rate. As shown in figure 8 a 3uA current source is used to discharge the soft-start capacitor.

The OCP comparator resets after every soft start cycles, the converter stays in this mode until the overload or short circuit is removed. The converter will automatically recover.

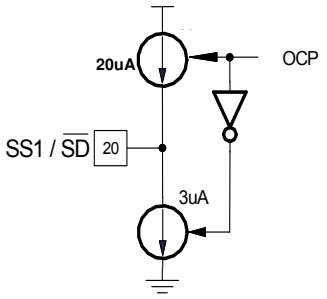


Fig. 8: 3uA current source for discharging soft-start capacitor during hiccup

The OCP circuit starts sampling current when the low gate drive is about 3V. The OCSet pin is internally clamped (~1.5V) during on time of high side MOSFET including deadtime to prevent false trigging, figure 9 shows the OCSet pin during one switching cycle. As it is shown there is about 150ns delay to mask the deadtime, since this node contains switching noises, this delay also functions as a filter.

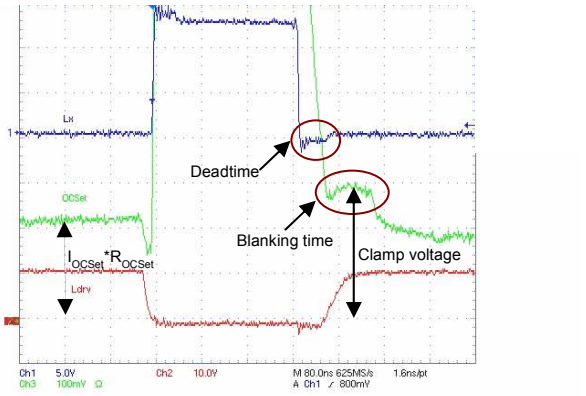


Fig. 9: OCset pin during normal condition
Ch1: Inductor point, Ch2:Ldrv, Ch3:OCSet

The value of R_{SET} should be checked in an actual circuit to ensure that the over current protection circuit activates as expected. The IR3628 current limit is designed primarily as disaster preventing, and doesn't operate as a precision current regulator.

Application Information

Design Example:

The following example is a typical application for IR3628. The application circuit is shown in page18.

$V_{in} = 12V, (13.2V, \max)$

$V_o = 0.9V$

$I_o = 10A$

$\Delta V_o \leq 30mV$ (*Output Voltage Ripple*)

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.6V. The divider is ratioed to provide 0.6V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{ref} * \left(1 + \frac{R_8}{R_9}\right) \quad --(4)$$

When an external resistor divider is connected to the output as shown in figure 10.

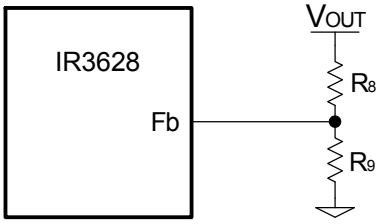


Fig. 10: Typical application of the IR3628 for programming the output voltage

Equation (4) can be rewritten as:

$$R_9 = R_8 * \left(\frac{V_{ref}}{V_O - V_{ref}}\right) \quad --(5)$$

For tracking applications replace Vref to Vp in equation (5).

For the calculated values of R_8 and R_9 see feedback compensation section.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$C_{SS} \cong 20\mu A * T_{start} \quad --(1)$$

Where T_{start} is the desired start-up time (ms)
For a start-up time of 10ms, the soft-start capacitor will be 0.2uF. Choose a ceramic capacitor at 0.22uF.

Vc supply for single input voltage

To drive the high side switch, it is necessary to supply a gate voltage at least 4V grater than the bus voltage. This is achieved by using a charge pump configuration as shown in figure 11. This method is simple and inexpensive. The operation of the circuit is as follows: when the lower MOSFET is turned on, the capacitor (C1) is pulled down to ground and charges, up to V_{BUS} value, through the diode (D1). The bus voltage will be added to this voltage when upper MOSFET turns on in next cycle, and providing supply voltage (Vc) through diode (D2). Vc is approximately:

$$V_C \cong 2 * V_{bus} - (V_{D1} + V_{D2}) \quad --(6)$$

Capacitors in the range of 0.1uF is generally adequate for most applications. The diodes must be a fast recovery device to minimize the amount of charge fed back from the charge pump capacitor into V_{BUS}. The diodes need to be able to block the full power rail voltage, which is seen when the high side MOSFET is switched on. For low voltage application, schottky diodes can be used to minimize forward drop across the diodes at start up.

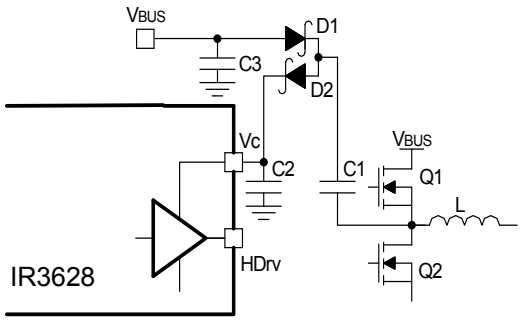


Fig. 11: Charge pump circuit to generate Vc voltage

Input Capacitor Selection

The input filter capacitor should be selected based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of upper MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \quad \text{--(7)}$$

Where: $D = \frac{V_o}{V_{in}}$

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

For Io=10A and D=0.075, the I_{RMS}=2.63A.

Ceramic capacitors are recommended due to their peak current capabilities, they also feature low ESR and ESL at higher frequency which enhance better efficiency,

Use 3x22uF, 16V ceramic capacitor from Panasonic.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi) . The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t};\ \ \Delta t = D * \frac{1}{F_s}$$

$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \quad \text{--(8)}$$

Where:

V_{in} = *Maximum input voltage*

V_o = *Output Voltage*

Δi = *Inductor ripple current*

F_s = *Switching frequency*

Δt = *Turn on time*

D = *Duty cycle*

If $\Delta i \approx 42\%(I_o)$, then the output inductor will be:

L = 0.36uH

The ETQP4LR36WFC from Panasonic provides a compact, low profile inductor suitable for this application.

Output Capacitor Selection

The voltage ripple and transient requirements determines the output capacitors types and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components, these components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR \quad \text{--(9)}$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in}}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s}$$

ΔV_o = *Output voltage ripple*

ΔI_L = *Inductor ripple current*

Since the output capacitor has major role in overall performance of converter and determine the result of transient response, selection of capacitor is critical. The IR3628 can perform well with all types of capacitors.

As a rule the capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements.

The goal for this design is to meet the voltage ripple requirement in smallest possible capacitor size. Therefore ceramic capacitor is selected due to low ESR and small size. Six of the Panasonic ECJ2FB0J226M (22uF, 6.3V, X5R and EIA 0805 case size) is a good choice.

In the case of tantalum or low ESR electrolytic capacitors, the ESR dominates the output voltage ripple, equation (9) can be used to calculate the required ESR for the specific voltage ripple.

Power MOSFET Selection

The IR3628 uses two N-Channel MOSFETs per channel. The selection criteria to meet power transfer requirements are based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{gs}), maximum output current, On-resistance $R_{DS(on)}$, and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{in}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low gate threshold voltage (V_{gs}) to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{cond} = (upperswitch) = I_{load}^2 * R_{ds(on)} * D * \vartheta$$

$$P_{cond} = (lowerswitch) = I_{load}^2 * R_{ds(on)} * (1-D) * \vartheta$$

$$\vartheta = R_{ds(on)}\ temperature\ \ dependency$$

The $R_{DS(on)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, IRF7823 is selected for control FET and IRF7832Z is selected for synchronous FET. These devices provide low on resistance in a cost effective SO8 package.

The MOSFETs have the following data:

ControlFET(IRF7823)	SyncFET(IRF7832Z)
$V_{ds} = 30V, Q_g = 14nC$	$V_{ds} = 30V, Q_g = 45nC$
$R_{ds(on)} = 8.7m\Omega @ V_{gs} = 10V$	$R_{ds(on)} = 3.8m\Omega @ V_{gs} = 10V$

The conduction losses will be: P_{con}=0.45W. The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turn-off delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{sw} = \frac{V_{ds(off)}}{2} * \frac{t_r + t_f}{T} * I_{load} \quad ---(10)$$

Where:

$V_{ds(off)}$ = Drain to source voltage at the off time

t_r = Rise time

t_f = Fall time

T = Switching period

I_{load} = Load current

The switching time waveforms is shown in figure18.

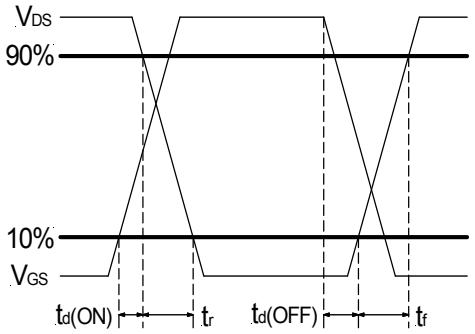


Fig. 18: switching time waveforms

From IRF7832Z data sheet:

tr = 13ns

tf = 14ns

These values are taken under a certain condition test. For more details please refer to the IRF7832Z data sheet.

By using equation (10), we can calculate the switching losses. P_{sw}=0.74W

The reverse recovery loss is also another contributing factor in control FET switching losses. This is equivalent to extra current requires to remove the minority charges from synchronous FET. The reverse recovery loss can be expressed as:

$$P_{Qrr} = Q_{rr} * t_{rr} * F_s$$

$$Q_{rr} : ReverseRecoveryCharge$$

$$t_{rr} : ReverseRecoveryTime$$

$$F_s : SwitchingFrequency$$

Feedback Compensation

The IR3628 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see figure 13). The resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2*\pi\sqrt{L_o * C_o}} \quad ---(11)$$

Figure 13 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

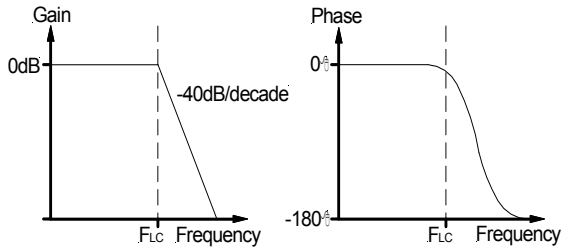


Fig. 13: Gain and Phase of LC filter

The IR3628's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The error amplifier can be compensated either in type II or typeIII compensation. When it is used in typeII compensation the transconductance properties of the error amplifier become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in figure 14.

This method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2*\pi*ESR*C_o} \quad ---(12)$$

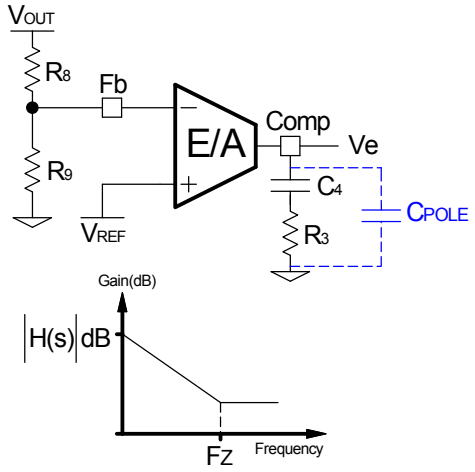


Fig. 14: TypeII compensation network and its asymptotic gain plot

The transfer function (Ve/Vo) is given by:

$$H(s) = \left(g_m * \frac{R_9}{R_9 + R_8}\right) * \frac{1 + sR_3C_4}{sC_4} \quad ---(13)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$[H(s)] = \left(g_m * \frac{R_9}{R_9 + R_8}\right) * R_3 \quad ---(14)$$

$$F_z = \frac{1}{2\pi * R_3 * C_4} \quad ---(15)$$

The gain is determined by the voltage divider and error amplifier's transconductance gain.
First select the desired zero-crossover frequency (Fo):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * (R_8 + R_9) * 1.28}{V_{in} * F_{LC}^2 * R_9 * g_m} \quad ---(15A)$$

Where:
V_{in} = Maximum Input Voltage
V_{osc} = Oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_8 and R_9 = Feedback Resistor Dividers
g_m = Error Amplifier Transconductance
1.28 = Empirical number to compensate thermal, process variations and components tolerances

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad ---(16)$$

Using equations (15) and (16) to calculate C9.
One more capacitor is sometimes added in parallel with C4 and R3. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_4 * C_{POLE}}{C_4 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_4}} \cong \frac{1}{\pi * R_3 * F_s}$$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network (typeIII). The typically used compensation network for voltage-mode controller is shown in figure 15.

In such configuration, the transfer function is given by:

$$\frac{V_e}{V_o} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m * Z_f >> 1 \text{ and } g_m * Z_{in} >> 1 \quad ---(17)$$

By replacing Z_{in} and Z_f according to figure 15, the transfer function can be expressed as:

$$H(s) = \frac{1}{sR_8(C_4 + C_3)} * \frac{(1 + sR_3C_4) * [1 + sC_7(R_8 + R_{10})]}{\left[1 + sR_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)\right] * (1 + sR_{10}C_7)}$$

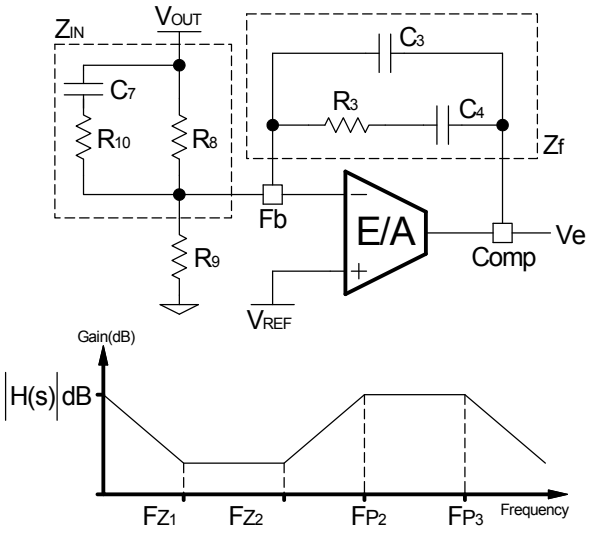


Fig.15: Compensation network with local feedback and its asymptotic gain plot

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the error amplifier output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi * R_{10} * C_7}$$

$$F_{P3} = \frac{1}{2\pi * R_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)} \cong \frac{1}{2\pi * R_3 * C_3}$$

$$F_{z1} = \frac{1}{2\pi * R_3 * C_4}$$

$$F_{z2} = \frac{1}{2\pi * C_7 * (R_8 + R_{10})} \cong \frac{1}{2\pi * C_7 * R_8}$$

Cross over frequency is expressed as:

$$F_o = R_3 * C_7 * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o}$$

Based on the frequency of the zero generated by output capacitor and its ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation types and location of crossover frequency.

Compensator type	F_{ESR} vs. F_o	Output capacitor
TypII(PI)	$F_{LC}<F_{ESR}<F_o<F_{s/2}$	Electrolytic , Tantalum
TypeIII(PID) **Method A**	$F_{LC}<F_o<F_{ESR}<F_{s/2}$	Tantalum, ceramic
TypeIII(PID) **Method B**	$F_{LC}<F_o<F_{s/2}<F_{ESR}$	Ceramic

Table1- The compensation type and location of F_{ESR} versus F_o

The details of these compensation types are discussed in application note AN-1043 which can be downloaded from IR Web-Site.

For this design we have:

V_{in}=12V
V_o=0.9V
V_{osc}=1.25V
V_{ref}=0.6V
g_m=1000umoh
L_o=0.36uH
C_o=6x22uF, ESR=2mOhm
Note: Use 16.5uF instead of 22uF for calculation, this is due to derating of ceramic capacitor
F_s=600kHz

These result to:

F_{LC}=26.6kHz
F_{ESR}=4.8MHz
$F_{s/2}$=300kHz

Select crossover frequency:

$F_o < F_{ESR}$ *and* $F_o \le (1/5 \sim 1/10) * F_s$

Fo=60kHz

Since: $F_{LC}<F_o<F_{s/2}<F_{ESR}$, typeIII method B is selected to place the pole and zeros.

The following design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient response. The DC gain will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

Desired Phase Margin: $\Theta_{max} = \frac{\pi}{3}$

$$F_{Z2} = F_o * \sqrt{\frac{1-Sin\Theta}{1+Sin\Theta}}$$
$$F_{Z2} = 16kHz$$

$$F_{P2} = F_o * \sqrt{\frac{1+Sin\Theta}{1-Sin\Theta}}$$
$$F_{P2} = 224kHz$$

Select: $F_{Z1} = 0.5 * F_{Z2}$ and $F_{P3} = 0.5 * F_s$

$$R_3 \ge \frac{2}{g_m}; R_3 \ge 2K\Omega; \text{ Select: } R_3 = 8.06K\Omega$$

Calculate C_4, C_3 and C_7 :

$$C_4 = \frac{1}{2\pi * F_{Z1} * R_3}; C_4 = 2.46nF, \text{ Select: } C_4 = 2.2nF$$

$$C_3 = \frac{1}{2\pi * F_{P3} * R_3}; C_3 = 65.8pF, \text{ Select: } C_3 = 12pF$$

$$C_7 = \frac{2\pi * F_o * L_o * C_o * V_{osc} * 1.28}{R_3 * V_{in}}; C_7 = 0.22nF,$$

Select: $C_7 = 0.22nF$

Calculate R_{10}, R_8 and R_9 :

$$R_{10} = \frac{1}{2\pi * C_7 * F_{P2}}; R_{10} = 3.23K\Omega, \text{ Select: } R_{10} = 3.24K\Omega$$

$$R_8 = \frac{1}{2\pi * C_7 * F_{Z2}} - R_{10}; R_8 = 41.76K\Omega, \text{ Select: } R_8 = 42.20K\Omega$$

$$R_9 = \frac{V_{ref}}{V_o - V_{ref}} * R_8; R_9 = 84.40K\Omega, \text{ Select: } R_9 = 84.50K\Omega$$

Programming the Current-Limit

The Current-Limit threshold can be set by connecting a resistor (R_{SET}) from drain of low side MOSFET to the OCSet pin. The resistor can be calculated by using equation (3).

The $R_{DS(on)}$ has a positive temperature coefficient and it should be considered for the worse case operation. This resistor must be placed close to the IC, place a location for small ceramic capacitor from this pin to ground for noise rejection purposes.

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \quad \text{--(3)}$$

$R_{DS(on)} = 3.8m\Omega * 1.5 = 5.7m\Omega$

$I_{SET} \cong I_{o(LIM)} = 10A * 1.5 = 15A$

(50% over nominal output current)

$R_{OCSet} = 4.27K\Omega$ Select $R_7 = 4.32K\Omega$

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas.

The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vcc and Vc should be close to respective pins. It is important to place the feedback components include feedback resistors and compensation components close to Fb and Comp pins.

In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

The MLPD is thermal enhanced package, based on thermal performance it is recommended to use 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to ground plane using vias.

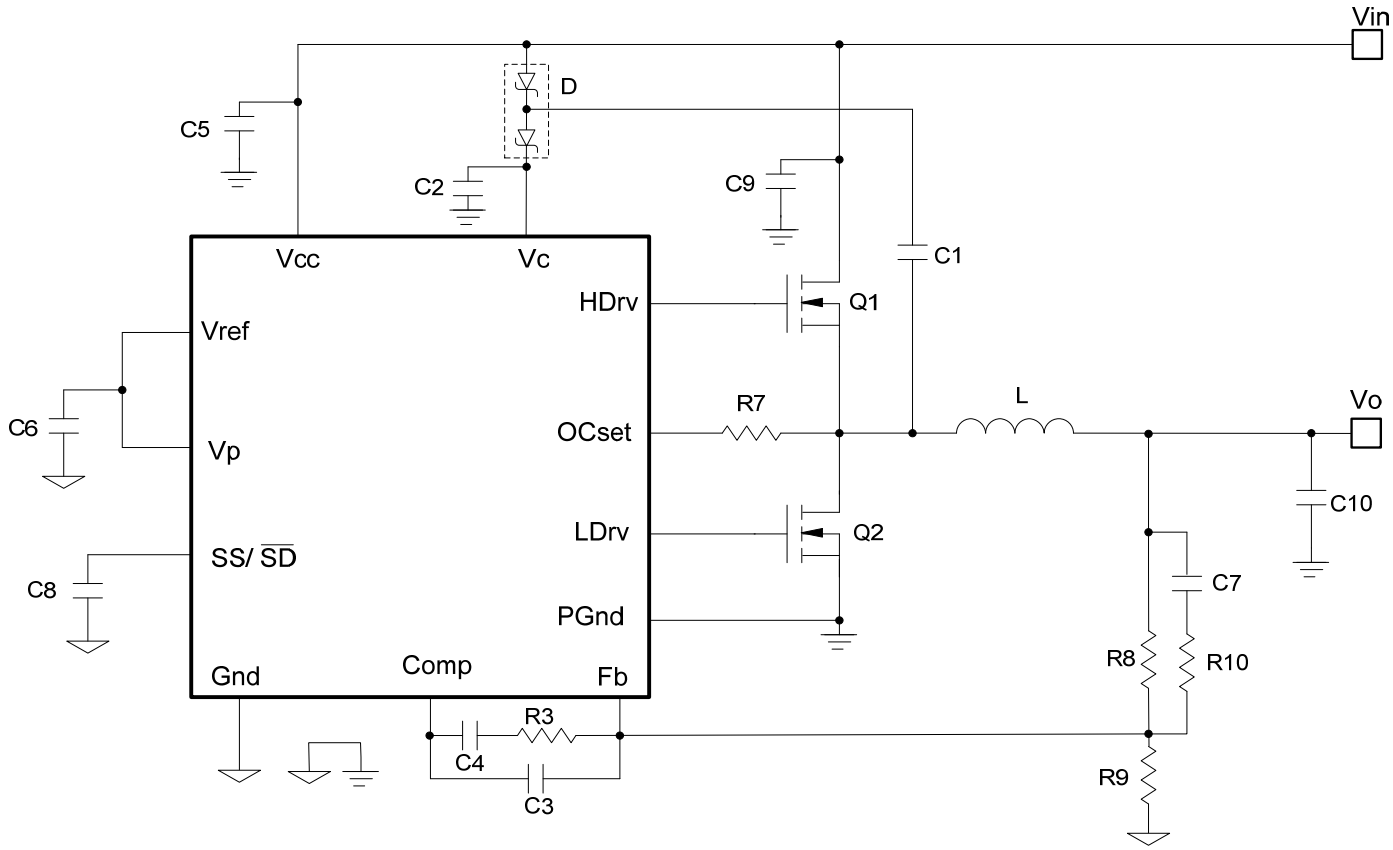


Fig.16: Application circuit for 12V to 0.9V
Using ceramic output capacitor with typeIII compensation

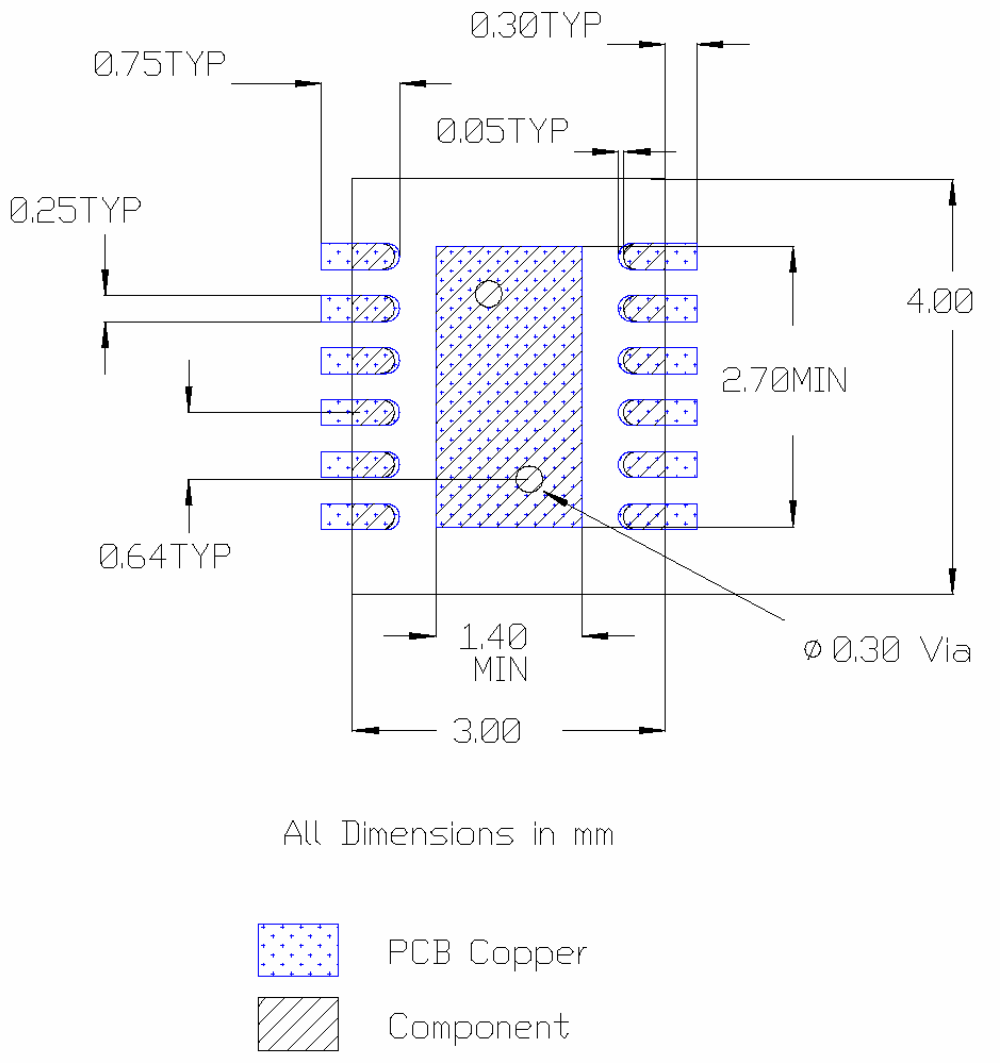
PCB Metal and Components Placement

▪ Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.

▪ Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.

▪ Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper).

▪ Two 0.30mm diameter via shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.



Solder Resist

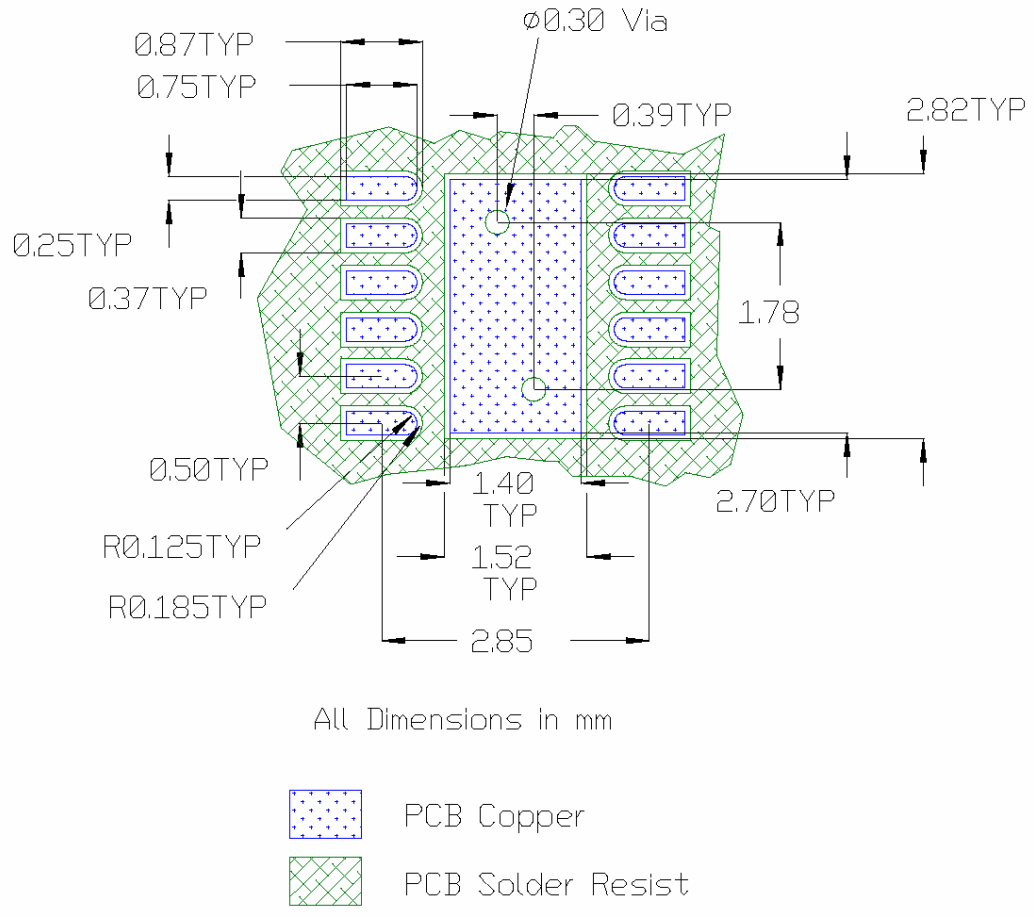
▪ The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.

▪ The minimum solder resist width is 0.13mm.
At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.

▪ The land pad should be Non Solder Mask Defined (NSMD), with a minimum pullback of the solder resist off the copper of 0.06mm to accommodate solder resist mis-alignment.

▪Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

▪Each via in the land pad should be tented or plugged from bottom boardside with solder resist.



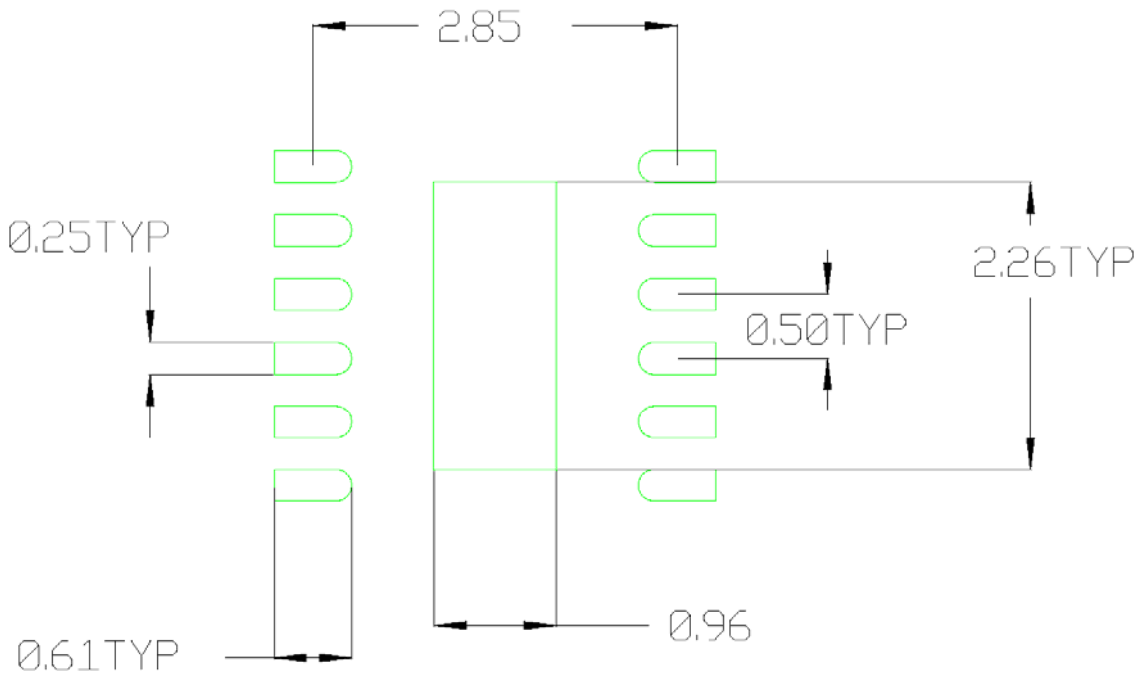
Stencil Design

▪ The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.

▪ The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.

▪ The land pad aperture should deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.

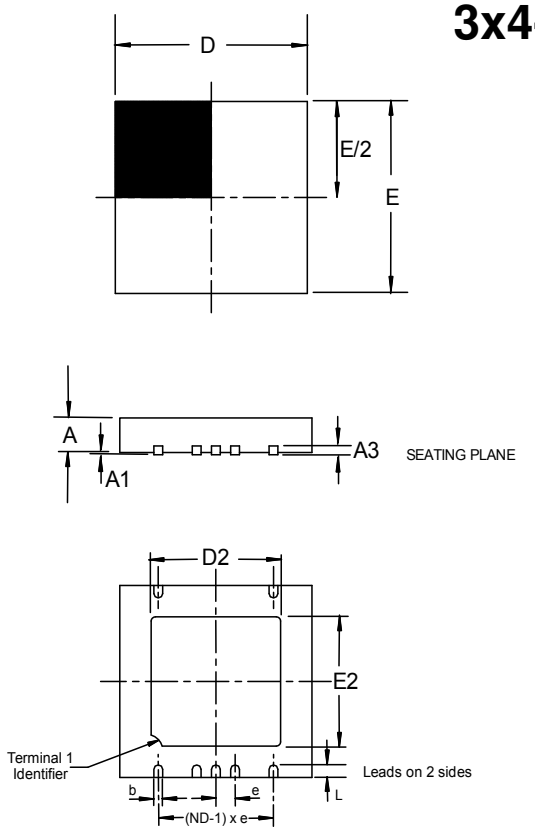
▪ The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture

All Dimensions in mm

(IR3628M) MLPD Package
3x4-12Lead



SYMBOL	VGED-4					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	.032	.035	.039
A1	0.00	0.02	0.05	.000	.0008	.0019
A3	0.20 REF			.008 REF		
b	0.18	0.25	0.30	.0071	.0096	.0118
D2	3.0	_	3.70	.118	_	.145
D	4.00 BSC			.157 BSC		
E	3.00 BSC			.118 BSC		
E2	1.40	_	1.80	.055	_	.070
L	0.30	0.40	0.50	.012	.016	.019
e	0.50 PITCH			.020 PITCH		
N	12			10		
ND	6			6		

TAPE & REEL ORIENTATION

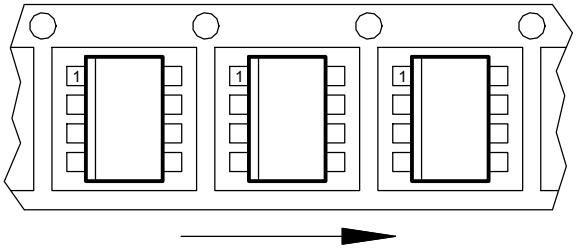


Figure A

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
This product has been designed and qualified for the Industrial market.
Visit us at www.irf.com for sales contact information
Data and specifications subject to change without notice. 08/07