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Single-input Voltage, 30A Buck Regulators with PVID

OPTIMOS IPOL IR38263

FEATURES

- Internal LDO allows single 16V operation
- Output Voltage Range: 0.5V to 0.875*PVin
- 0.5% accurate Reference Voltage
- Enhanced line/load regulation with Feedforward
- Frequency programmable by PMBus up to 1.5 MHz
- Enable input with Voltage Monitoring Capability
- Remote Sense Amplifier with True Differential Voltage Sensing
- 3 pins (PVID) to program output voltage
- Fast mode I2C and 400 kHz PMBus interface for programming, sequencing and margining output voltage, and for monitoring input voltage, output voltage, output current and temperature.
- PMBus configurable fault thresholds for input UVLO, output OVP, OCP and thermal shutdown.
- Thermally compensated pulse-by-pulse current limit and Hiccup Mode Over Current Protection
- Dedicated output voltage sensing for power good indication and overvoltage protection which remains active even when Enable is low.
- Enhanced Pre-Bias Start up
- Integrated MOSFET drivers and Bootstrap diode
- Operating junction temp: -40°C<Tj<125°C
- Thermal Shut Down
- Post Package trimmed rising edge dead-time
- PMBus Programmable Power Good Output
- Small Size 5mmx7mm PQFN
- Pb-Free (RoHS Compliant)
- External resistor allows setting up to 16 PMBus addresses

DESCRIPTION

This family of OPTIMOS IPOL devices offers easy-to-use, fully integrated and highly efficient DC/DC regulators with PVID and I2C/PMBus interface. The on-chip PWM controller and co-packaged low duty cycle optimized MOSFETs make these devices a space-efficient solution, providing accurate power delivery for low output voltage and high current applications that require a parallel VID interface.

These versatile devices offer programmability of switching frequency, output voltage, and fault/warning thresholds and fault responses while operating over a wide input range. Thus, they offer flexibility as well as system level security in event of fault conditions.

The switching frequency is programmable from 150 kHz to 1.5 MHz for an optimum solution.

The on-chip sensors and ADC along with the PVID and PMBus interfaces make it easy to monitor and report input voltage, output voltage, output current and temperature.

APPLICATIONS

- Intel® VR13 and VR12.5 based systems
- Servers and High End Desktop CPU VRs for non-core applications
- Telecom and storage applications

BASIC APPLICATION

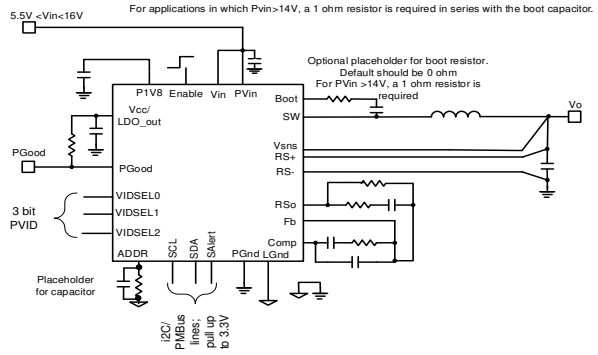


Figure 1: Typical application circuit

PIN DIAGRAM

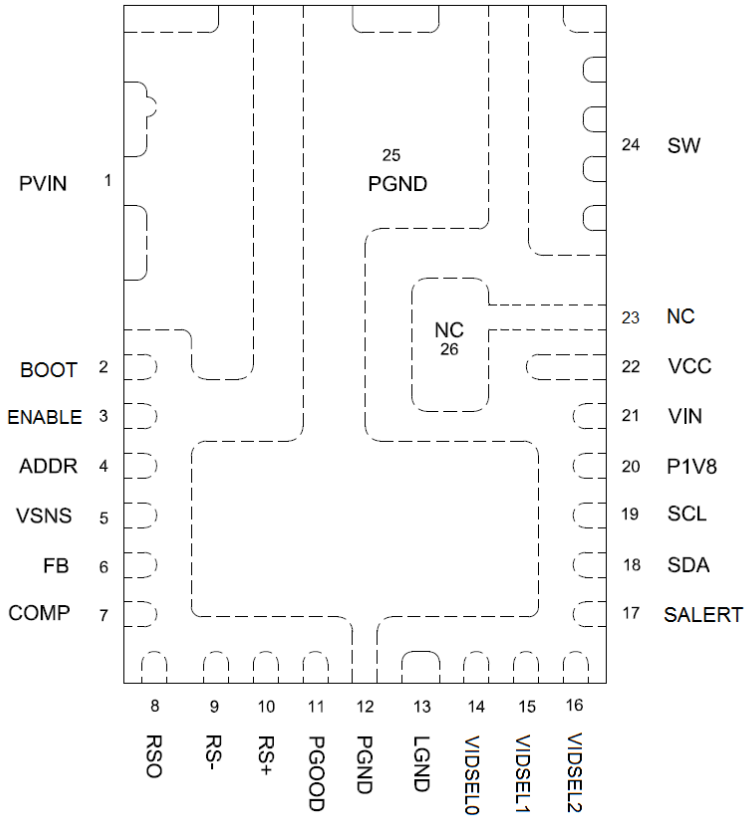


Figure 2: IR38263 Package Top View
5mm X 7mm PQFN

ORDERING INFORMATION

Package	Tape and Reel Qty	Part Number	Description
PQFN	4000	IR38263MTRPbF	30A Buck Regulator with PVID and PMBus for PVNN

FUNCTIONAL BLOCK DIAGRAM

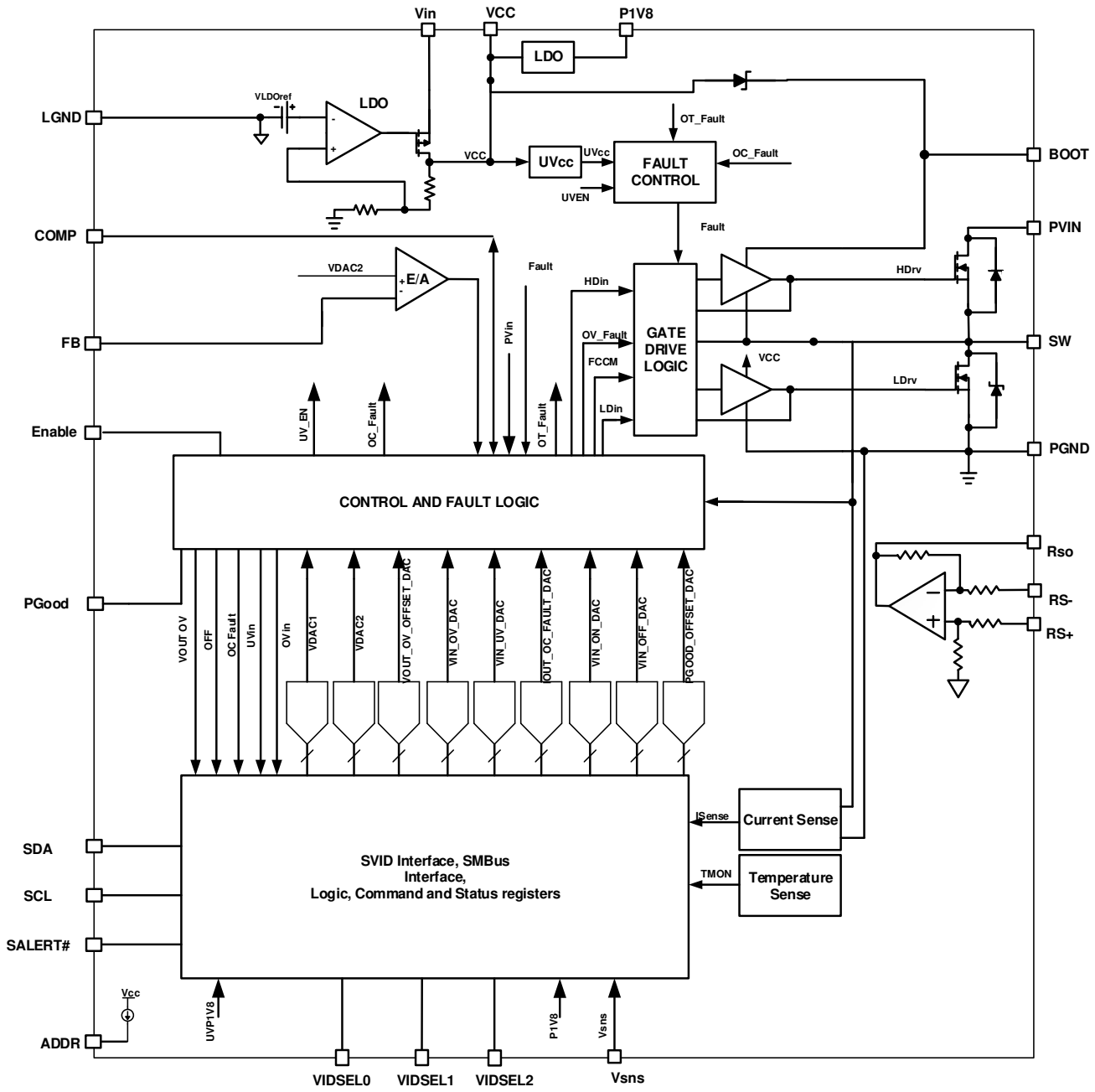


Figure 3: Simplified Block Diagram for IR38263

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	PVIN	Input voltage for power stage. Bypass capacitors between PVin and PGND should be connected very close to this pin and PGND. Typical applications use four22 uF input capacitors and a low ESR, low ESL 0.1uF decoupling capacitor in a 0603/0402 case size. A 3.3nF capacitor may also be used in parallel with these input capacitors to reduce ringing on the Sw node.
2	Boot	Supply voltage for high side driver. A 0.1uF capacitor should be connected from this pin to the Sw pin. It is recommended to provide a placement for a 0 ohm resistor in series with the capacitor. For applications in which PVin>14V, a 1 ohm resistor is required in series with boot capacitor.
3	ENABLE	Enable pin to turn on and off the IC
4	ADDR	A resistor should be connected from this pin to LGnd to set the PMBus address offset for the device. It is recommended to provide a placement for a 10 nF capacitor in parallel with the offset resistor.
5	Vsns	Sense pin for OVP and PGood. Typically connected to a local Vout capacitor at the output of the inductor.
6	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator or to the output of the remote sense amplifier, via resistor divider to set the output voltage and provide feedback to the error amplifier.
7	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to FB to provide loop compensation.
8	RSo	Remote Sense Amplifier Output. When the remote sense amplifier is used, this is connected to the feedback compensation network
9	RS-	Remote Sense Amplifier input. Connect to ground at the load.
10	RS+	Remote Sense Amplifier input. Connect to output at the load.
11	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to VCC. If the power good voltage before VCC UVLO needs to be limited to < 500 mV, use a 49.9K pullup, otherwise a 4.99K pullup will suffice.
12,25	PGND	Power ground. This pin should be connected to the system's power ground plane. Bypass capacitors between PVin and PGND should be connected very close to PVIN pin (pin 1) and this pin.
13	LGND	Signal ground for internal reference and control circuitry. This should be connected to the PGnd plane at a quiet location using a single point connection.
14	VIDSEL0	Used to select VID voltage registers. This is the LSB of the 3 bit PVID code that is internally decoded to select the register containing the target voltage. Only connect to Vcc via a 4.99KΩ resistor and do not use a direct connection. Do not exceed 6V.
15	VIDSEL1	Used to select VID voltage registers. Only connect to Vcc via a 4.99KΩ resistor and do not use a direct connection. Do not exceed 6V.
16	VIDSEL2	Used to select VID voltage registers. This is the MSB of the 3 bit PVID code that is internally decoded to select the register containing the target voltage. Only connect to Vcc via a 4.99KΩ resistor and do not use a direct connection. Do not exceed 6V.
17	SAlert#	SMBus Alert line; open drain SMBALERT# pin. This should be pulled up to 3.3V-5V with a 1K-5K resistor.
18	SDA	SMBus data serial input/output line. This should be pulled up to 3.3V-5V with a 1K-5K resistor

PIN #	PIN NAME	PIN DESCRIPTION
19	SCL	SMBus clock line. This should be pulled up to 3.3V-5V with a 1K-5K resistor
20	P1V8	This is the supply for the digital circuits; bypass with a 10uF capacitor to PGnd. A 2.2uF capacitor is valid however a10uF capacitor is recommended.
21	Vin	Input Voltage for LDO. A 1 uF capacitor is placed from this pin to PGnd. If the internal bias LDO is used, tie this pin to PVin. If an external bias voltage (typically 5V) is available for Vcc, tie the Vin pin to Vcc.
22	VCC	Bias Voltage for IC and driver section, output of LDO. Add 10 uF bypass cap from this pin to PGnd.
23,26	NC	NC
24	SW	Switch node. This pin is connected to the output inductor.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond these listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin, Vin	-0.3V to 25V
VCC	-0.3V to 6V
P1V8	-0.3V to 2 V
SW	-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
BOOT	-0.3V to 31V
BOOT to SW	-0.3V to 6V (DC) (Note 1), -0.3V to 6.5V (AC, 100ns)
PGD, other Input/output pins	-0.3V to 6V (Note 1)
PGND to GND, RS- to GND	-0.3V to + 0.3V
THERMAL INFORMATION	
Junction to Ambient Thermal Resistance Θ_{JA}	11.1 C/W (Note 2)
Junction to case top Thermal Resistance $\theta_{JC(top)}$	18.9 C/W (Note 3)
Junction to PCB Thermal Resistance Θ_{JB}	4.16 C/W (Note 4)
Junction to case top parameter $\Psi_{JT\ (top)}$	0.32 C/W (Note 2)
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C

(Voltages referenced to GND unless otherwise specified)

Note 1: Must not exceed 6V.
Note 2: Value obtained via thermal simulation under natural convention on a PVNN, IR38263 demo board. 10 layer, 7”x5.5”x0.072” PCB with 1.5 oz copper at the top and bottom layer. Inner layers 2, 3, 8 and 9 have 1 oz copper and layers 4,5,6,7 have 2 oz copper. Ta = 25C was used for the simulation.
Note 3: PCB from note 2 and package is considered in thermal simulation with Ta=25 ^{0}C. Pin 12 is considered.
Note 4: Only package is considered. Simulation is used with a cold plate that fixes top of package at Ta=25 ^{0}C.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DEFINITION	MIN	MAX	UNITS
PVin	Input Bus Voltage	1.5	16*	V
Vin	LDO supply voltage	5.3	16	
VCC	LDO output/Bias supply voltage	4.5	5.5	
Boot to SW	High Side driver gate voltage	4.5	5.5	
VO	Output Voltage	0.5	$0.875*PV_{in}$	
I_O	Output Current	0	30	A
Fs	Switching Frequency	150	1500	kHz
T_J	Junction Temperature	-40	125	°C

* SW Node must not exceed 25V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET $R_{ds(on)}$						
Top Switch	Rds(on)_Top	$V_{Boot} – V_{SW}$ = 5V, I_D = 30A, Tj = 25°C		2.2		mΩ
Bottom Switch	Rds(on)_Bot	Vcc =5V, I_D = 30A, Tj = 25°C		0.78		
Reference Voltage						
Accuracy $0^0C<Tj<85^0C$		1.25V<V_{FB}<2.555V VOUT_SCALE_LOOP=1;	-1		+1	%
		0.75V<V_{FB}<1.25V VOUT_SCALE_LOOP=1;	-0.75		+0.75	
		0.45V<V_{FB}<0.75V VOUT_SCALE_LOOP=1;	-0.5		+0.5	%
Accuracy $-40^0C<Tj<125^0C$		1.25V<V_{FB}<2.555V VOUT_SCALE_LOOP=1;	-1.6		+1.6	%
		0.75V<V_{FB}<1.25V VOUT_SCALE_LOOP=1;	-1.0		+1.0	%
		0.45V<V_{FB}<0.75V VOUT_SCALE_LOOP=1;	-2.0		+2.0	%
Supply Current						
PVin range (using external Vcc=5V)				1.5-16		V
Vin range (using internal LDO)		Fsw=600kHz		5.3-16		V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		Fsw=1.5MHz		5.5-16		
Vin range (when Vin=Vcc)			4.5	5.0	5.5	V
V_{in} Supply Current (Standby) (internal Vcc)	$I_{in(Standby)}$	Enable low, No Switching, Vin=16V, low power mode enabled		2.7	4	mA
V_{in} Supply Current (Dyn)(internal Vcc)	$I_{in(Dyn)}$	Enable high, Fs = 600kHz, Vin=16V		39	50	mA
VCC Supply Current (Standby)(external Vcc)	$I_{cc(Standby)}$	Enable low, No Switching, Vcc=5.5V, low power mode enabled		2.7	5	mA
VCC Supply Current (Dyn)(external Vcc)	$I_{cc(Dyn)}$	Enable high, Fs = 600kHz, Vcc=5.5V		39	50	mA
Under Voltage Lockout						
VCC – Start – Threshold	VCC_UVLO_Start	VCC Rising Trip Level	4.0	4.2	4.4	V
VCC – Stop – Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	3.7	3.9	4.1	
Enable – Start – Threshold	Enable_UVLO_Start	Supply ramping up	0.55	0.6	0.65	V
Enable – Stop – Threshold	Enable_UVLO_Stop	Supply ramping down	0.35	0.4	0.45	
Enable leakage current	Ien	Enable=5.5V			1	uA
Oscillator						
Ramp Amplitude	Vramp	PVin=5V, D=Dmax, Note 2		0.71		Vp-p
		PVin=12V, D=Dmax, Note 2		1.84		
		PVin=16V,D=Dmax, Note 2		2.46		
Ramp Offset	Ramp (os)	Note 2		0.22		V
Min Pulse Width	Dmin (ctrl)	Note 2		35	50	ns
Fixed Off Time		Note 2 Fs=1.5MHz		100	150	ns
Max Duty Cycle	Dmax	Fs=400kHz	86	87.5	89	%
Error Amplifier						
Input Bias Current	IFb(E/A)		-0.5		+0.5	µA
Sink Current	Isink(E/A)		0.6	1.1	1.8	mA
Source Current	Isource(E/A)		8	13	25	mA
Slew Rate	SR	Note 2	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 2	20	30	40	MHz
DC Gain	Gain	Note 2	100	110	120	dB
Maximum Voltage	Vmax(E/A)		2.8	3.9	4.3	V
Minimum Voltage	Vmin(E/A)				100	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Remote Sense Differential Amplifier						
Unity Gain Bandwidth	BW_RS	Note 2	3	6.4		MHz
DC Gain	Gain_RS	Note 2		110		dB
Offset Voltage	Offset_RS	0.5V<RS+<2.555V, 4kOhm load $27^0C<Tj<85^0C$	-1.6	0	1.6	mV
		0.5V<RS+<2.555V, 4kOhm load $-40^0C<Tj<125^0C$	-3		3	
Source Current	Isource_RS	V_RSO=1.5V, V_RSP=4V	11		16	mA
Sink Current	Isink_RS		0.4	1	2	mA
Slew Rate	Slew_RS	Note 2, Cload = 100pF	2	4	8	V/µs
RS+ input impedance	Rin_RS+		36	55	74	Kohm
RS- input impedance	Rin_RS-	Note 2	36	55	74	Kohm
Maximum Voltage	Vmax_RS	V(VCC) – V(RS+)	0.5	1	1.5	V
Minimum Voltage	Min_RS			4	20	mV
Bootstrap Diode						
Forward Voltage		I(Boot) = 40mA	150	300	450	mV
Switch Node						
SW Leakage Current	Isw	SW = 0V, Enable = 0V			1	µA
	Isw_En	SW=0; Enable= 2V		18		
Internal Regulator (VCC/LDO)						
Output Voltage	VCC	Vin(min) = 5.5V, Io=0mA, Cload = 10uF	4.8	5.15	5.4	V
		Vin(min) = 5.5V, Io=70mA, Cload = 10uF	4.5	4.99	5.2	
VCC dropout	VCC_drop	Io=0-70mA, Cload = 10uF, Vin=5.1V			0.7	V
Short Circuit Current	Ishort			110		mA
Internal Regulator (P1V8)						
Output Voltage	P1V8	Vin(min) = 4.5V, Io = 0-1mA, Cload = 2.2uF	1.795	1.83	1.905	V
1.8V UVLO Start	P1V8_UVLO_Start	1.8V Rising Trip Level	1.66	1.72	1.78	V
1.8V UVLO Stop	P1V8_UVLO_Stop	1.8V Falling Trip Level	1.59	1.63	1.68	V
Adaptive On time Mode						
Zero-crossing comparator threshold	ZC_Vth		-4	-1	2	mV
Zero-crossing comparator delay	ZC_Tdly			8/Fs		s

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
FAULTS						
Power Good						
Power Good High threshold	Power_Good_High	Vsns rising, VOUT_SCALE_LOOP=1, Vout=0.5V, PMBus mode		0.45		V
Power Good Low Threshold	Power_Good_Low	Vsns falling, VOUT_SCALE_LOOP=1, Vout=0.5V, PMBus mode		0.43		V
Power Good High Threshold Rising Delay	TPDLY	Vsns rising, Vsns > Power_Good_High		0		ms
Power Good Low Threshold Falling delay	VPG_low_Dly	Vsns falling, Vsns < Power_Good_Low	150	175	200	us
PGood Voltage Low	PG (voltage)	I_{PGood} = -5mA			0.5	V
Over Voltage Protection (OVP)						
OVP Trip Threshold	OVP (trip)	Vsns rising, VOUT_SCALE_LOOP=1, Vout=0.5V	0.57	0.605	0.63	V
OVP comparator Hysteresis	OVP (hyst)	Vsns falling, VOUT_SCALE_LOOP=1, Vout=0.5V	20	30	40	mV
OVP Fault Prop Delay	OVP (delay)	Vsns rising, Vsns-OVP(trip)>200 mV		200		ns
Over-Current Protection						
OC Trip Current	I_{TRIP}	OC limit=40, VCC = 5.05V, T_j=25^{0}C	36	40	44	A
		OC limit=16A, VCC = 5.05V, T_j=25^{0}C	12.5	16	19.5	A
OCset Current Temperature coefficient	OCSET(temp)	-40^{0}C to 125^{0}C, VCC=5.05V, Note 2		5900		ppm/°C
Hiccup blanking time	Tblk_Hiccup	Note 2		20		ms
Thermal Shutdown						
Thermal Shutdown		Note 2		145		°C
Hysteresis		Note 2		25		°C
Input Over-Voltage Protection						
PVin overvoltage threshold	$PVin_{OV}$		22	23.7	25	V
PVin overvoltage Hysteresis	$PVin_{ov\ hyst}$			2.4		V
MONITORING AND REPORTING						
I2C Bus Speed[1]				100	400	kHz
Iout & Vout filter				78		Hz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Iout & Vout Update rate				31.25		kHz
Vin & Temperature filter				78		Hz
Vin & Temperature update rate				31.25		kHz
Output Voltage Reporting						
Resolution	N_{Vout}	Note 2		1/256		V
Lowest reported Vout	Vomon_low	Vsns=0V		0		V
Highest reported Vout	Vomon_high	VOUT_SCALE_LOOP=1, Vsns=3.3V		3.3		V
		VOUT_SCALE_LOOP=0.5, Vsns=3.3V		6.6		V
		VOUT_SCALE_LOOP=0.25, Vsns=3.3V		13.2		V
		VOUT_SCALE_LOOP=0.125, Vsns=3.3V		26.4		V
Vout reporting accuracy		0^0C to 85^0C, 4.5V<Vcc<5.5V, 1V<Vsns≤ 1.5V VOUT_SCALE_LOOP=1		+/- 0.6		%
		0^0C to 85^0C, 4.5V<Vcc<5.5V, Vsns> 1.5V VOUT_SCALE_LOOP=1		+/-1		
		0^0C to 125^0C, 4.5V<Vcc<5.5V, Vsns>0.9V VOUT_SCALE_LOOP=1		+/- 1.5		
		0^0C to 125^0C, 4.5V<Vcc<5.5V, 0.5V<Vsns<0.9V VOUT_SCALE_LOOP=1		+/-3		
Iout Reporting						
Resolution	N_{Iout}	Note 2		0.0625		A
Iout (digital) monitoring Range	Iout_dig		0		40	A
Iout_dig Accuracy	I	0^0C to 125^0C, 4.5V<Vcc<5.5V, 5A < Iout <30A		+/-5		%
Temperature Reporting						
Resolution	N_{Tmon}	Note 2		1		°C
Temperature Monitoring Range	Tmon_dig		-40		150	°C
Thermal shutdown hysteresis		Note 2		25		°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Reporting						
Resolution	N_{PVin}	Note 2		1/32		V
Monitoring Range	PMBVinmon		0		21	V
Monitoring accuracy		0^0C to 85^0C, 4.5V<Vcc<5.5V, PVin>10V	-1.5		1.5	%
		-40^0C to 125^0C, 4.5V<Vcc<5.5V, PVin>14V	-1.5		1.5	
		-40^0C to 125^0C, 4.5V<Vcc<5.5V, 7V<PVin<14V	-4		4	
PMBus Interface Timing Specifications						
PMBus Operating frequency	F_{SMB}				400	kHz
Bus Free time between Start and Stop condition	T_{BUF}		1.3			us
Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	$T_{HD:STA}$		0.6			us
Repeated start condition setup time	$T_{SU:STA}$		0.6			us
Stop condition setup time	$T_{SU:STO}$		0.6			us
Data Rising Threshold			1.339		1.766	V
Data Falling Threshold			1.048		1.495	V
Clock Rising Threshold			1.339		1.766	V
Clock Falling Threshold			1.048		1.499	V
Data Rising Threshold LVT			0.7		0.9	V
Data Falling Threshold LVT			0.45		0.65	V
Clock Rising Threshold LVT			0.7		0.9	V
Clock Falling Threshold LVT			0.45		0.65	V
Data Hold Time	$T_{HD:DAT}$		300		900	ns
Data Setup Time	$T_{SU:DAT}$		100			ns
Data pulldown resistance			8	11	16	Ω
SALERT# pulldown			9	12	17	Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
resistance						
Clock low time out	$T_{TIMEOUT}$		25		35	ms
Clock low period	T_{LOW}		1.3			us
Clock High Period	T_{HIGH}		0.6		50	us
Digital Inputs – Low Vth Type 2 (VIDSELx)						
Input High Voltage			0.65	-	-	V
Input Low Voltage			-	-	0.45	V
Hysteresis			-	95	-	mV
Input Leakage Current		Vpad = 0 to 2V	-	-	±1	µA

Notes

2. Guaranteed by design but not tested in production
3. Guaranteed by statistical correlation, but not tested in production

TYPICAL APPLICATION DIAGRAMS

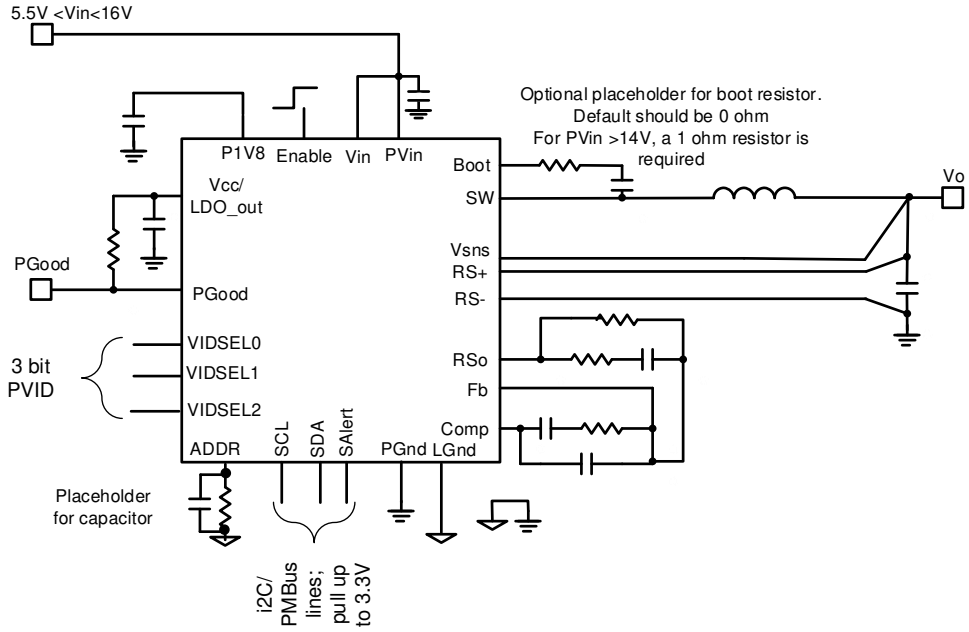


Figure 4: Using the internal LDO, Vo < 2.555V

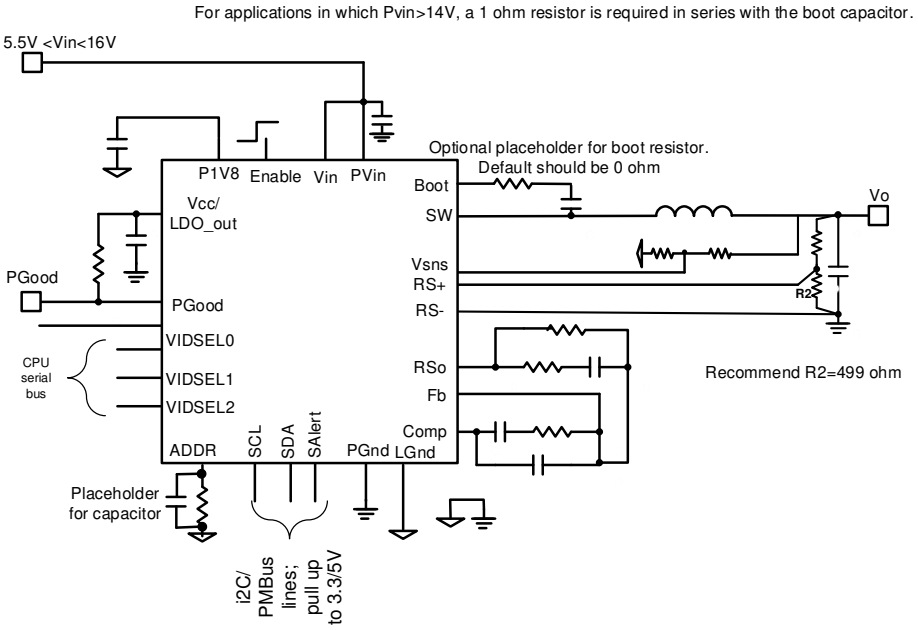


Figure 5: Using the internal LDO, Vo > 2.555V

TYPICAL APPLICATION DIAGRAMS

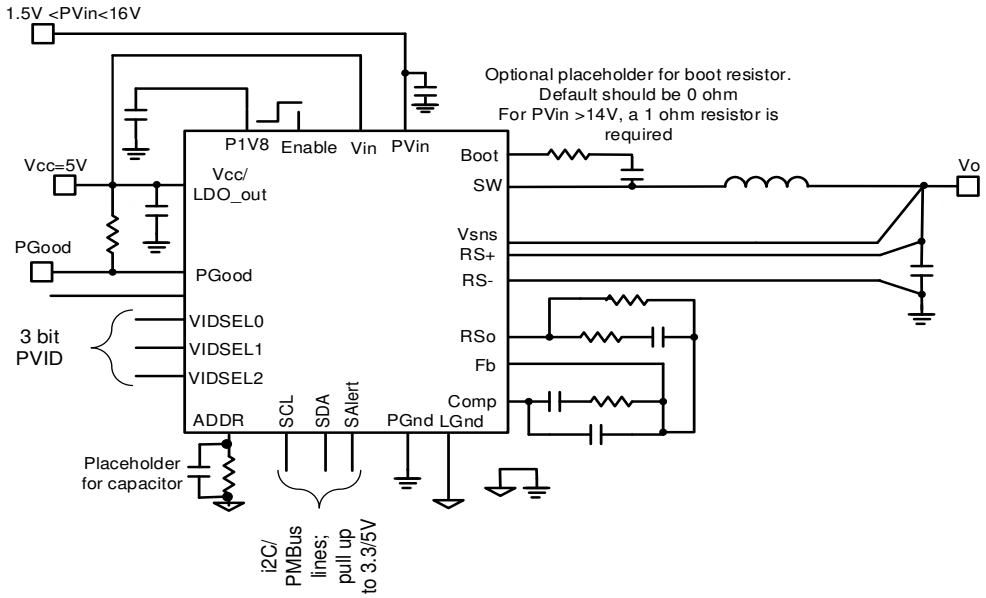


Figure 6: Using external Vcc, Vo<2.555V

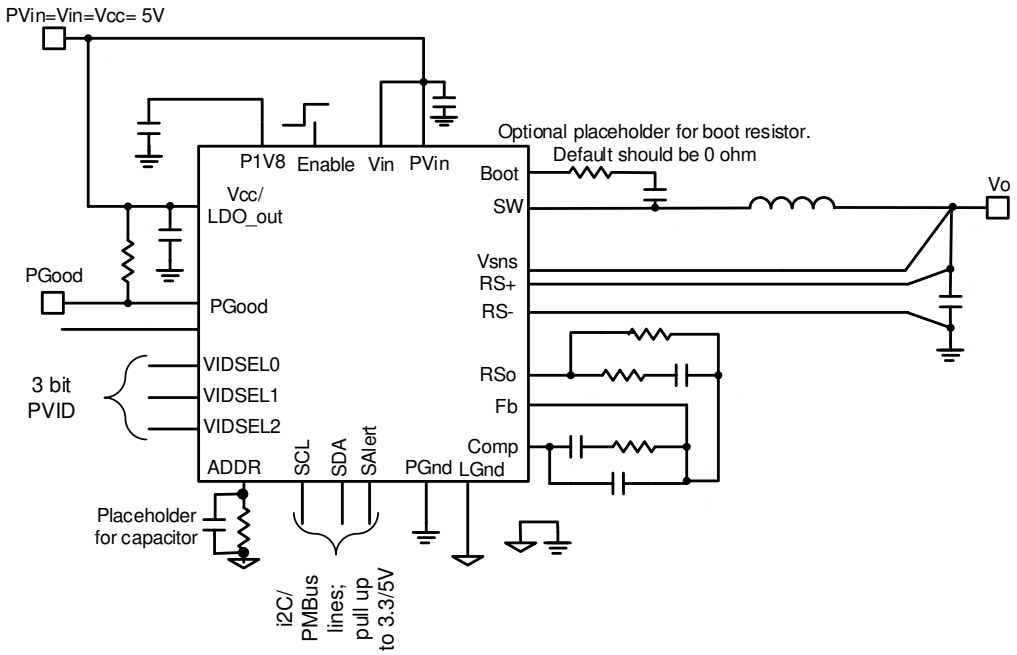
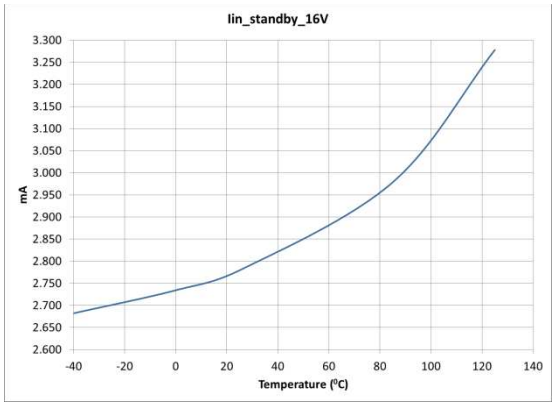
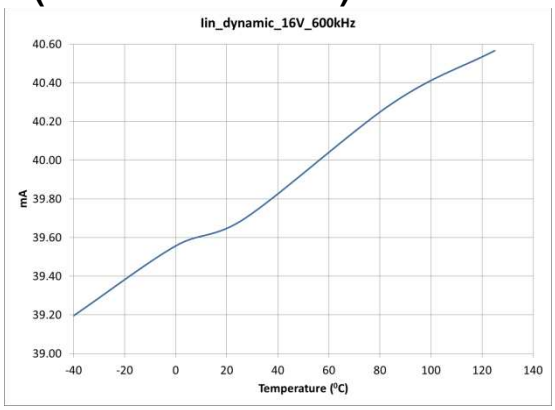
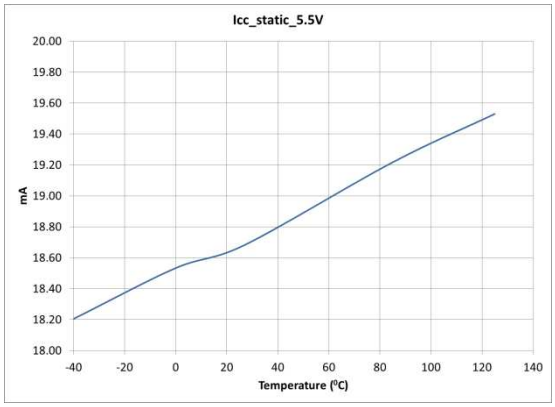


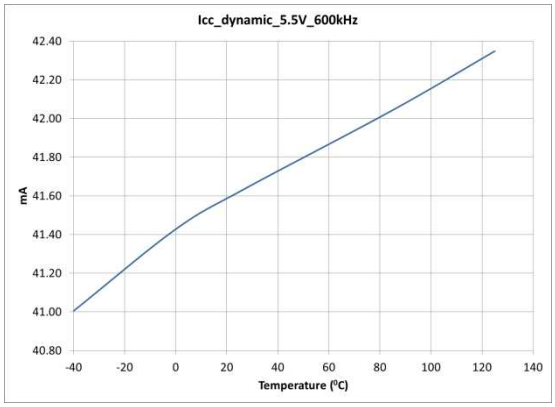
Figure 7: Single 5V application, Vo<2.555V

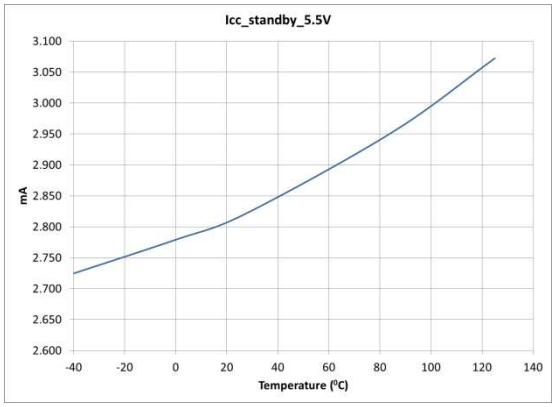
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

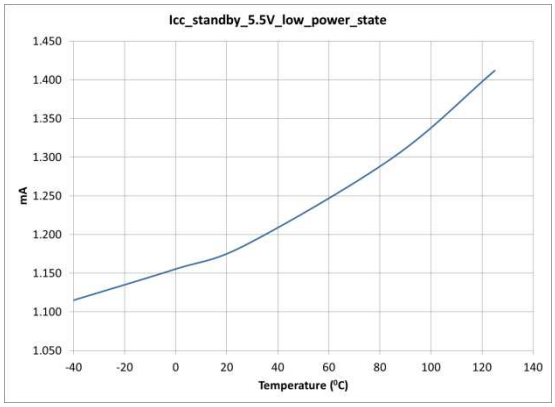




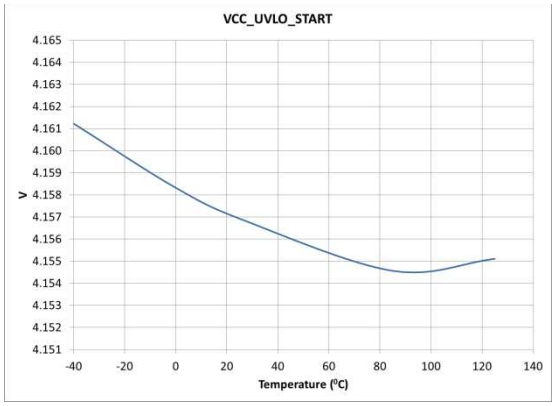


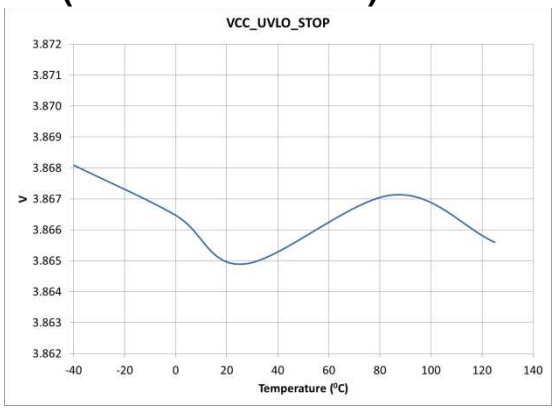


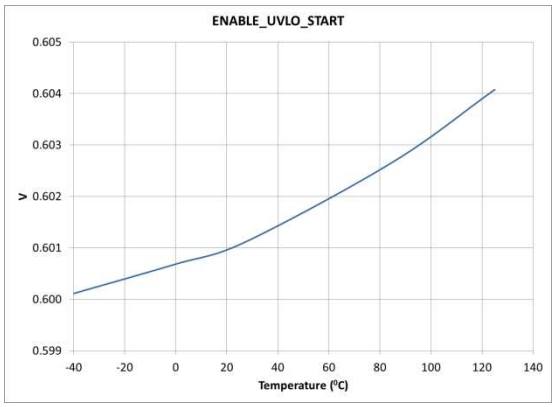


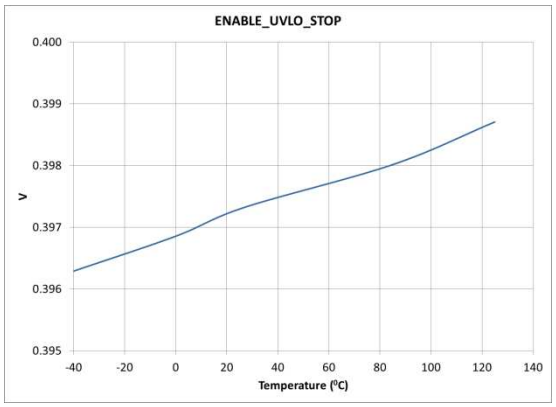


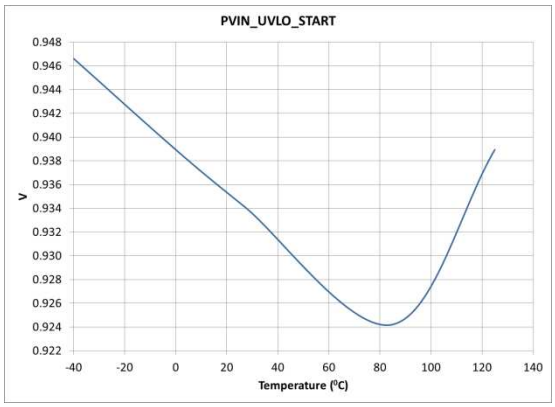
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

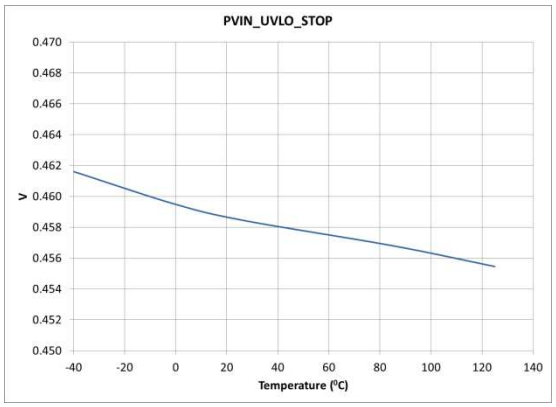












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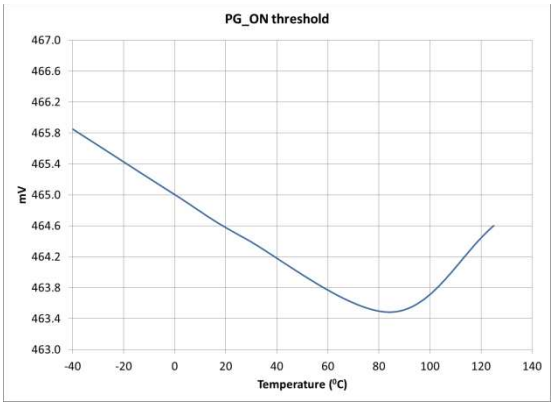
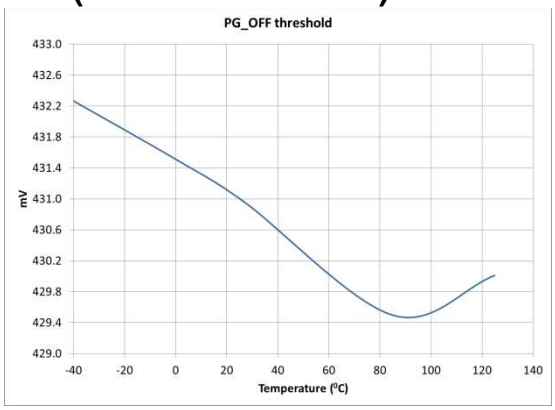
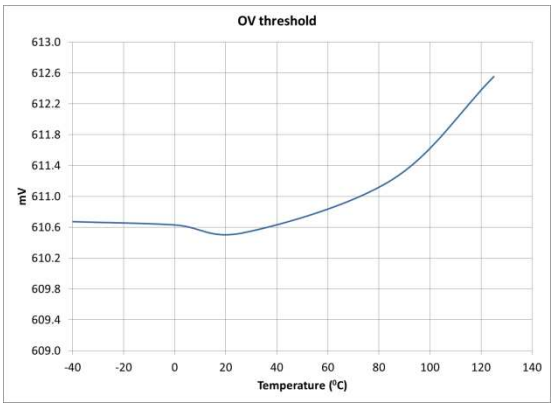
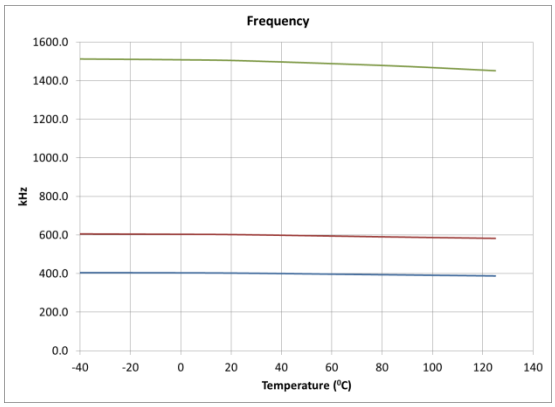
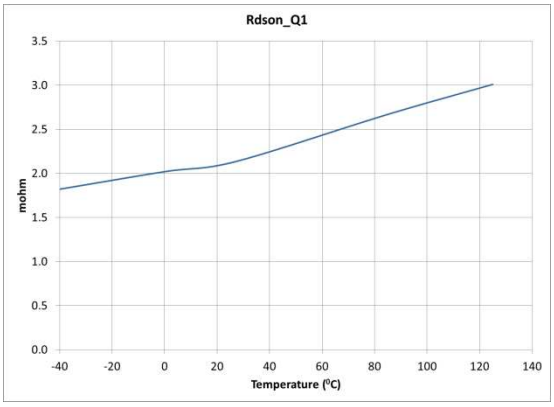
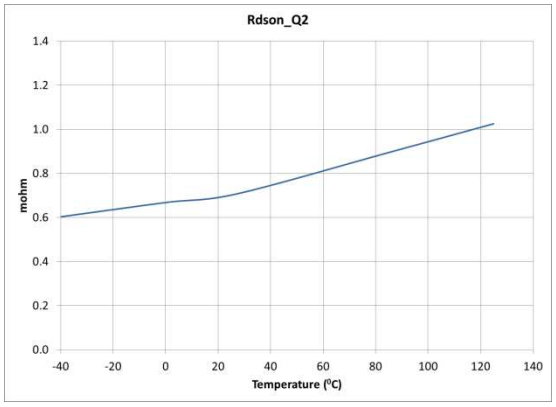




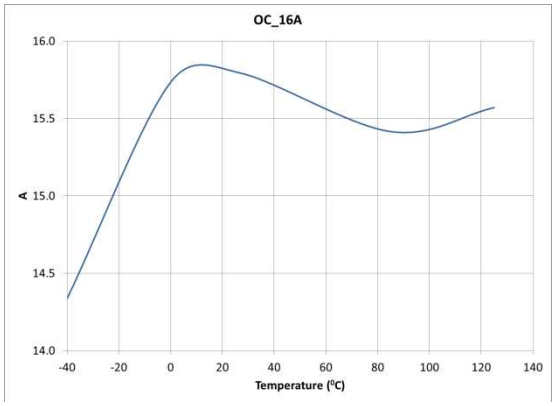


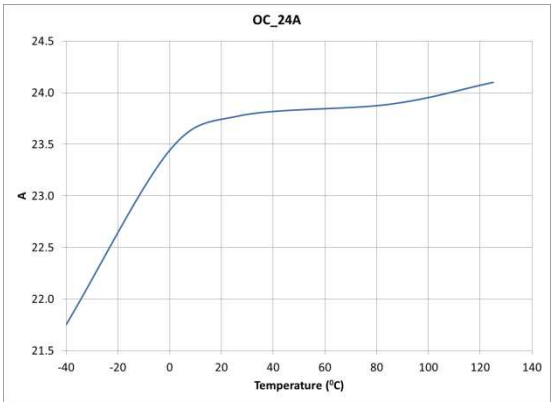


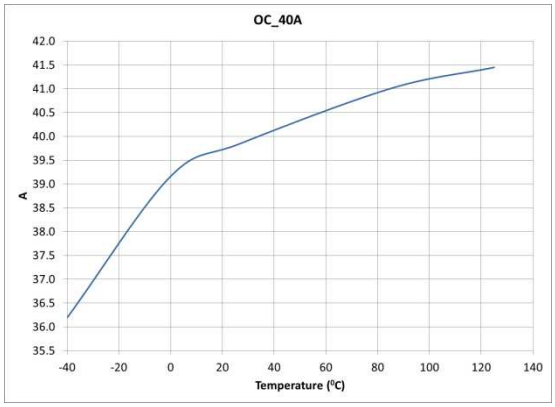




TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)



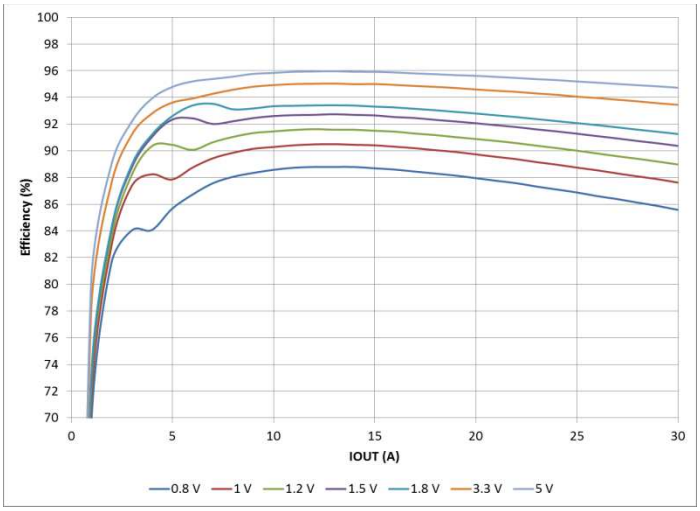


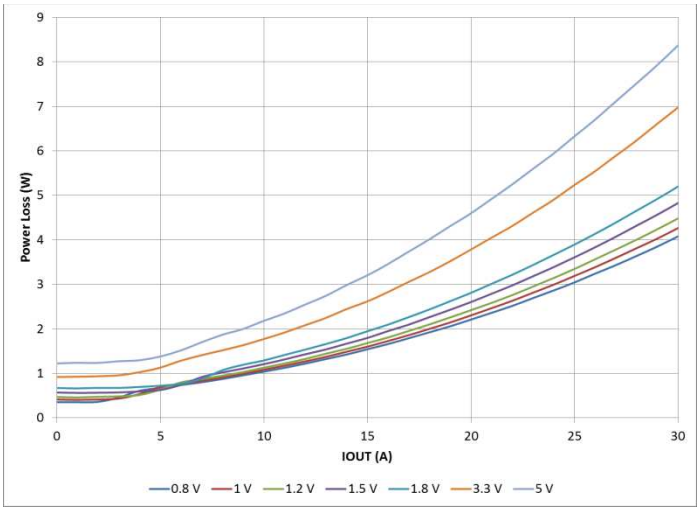


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = 12V, VCC = 5V, Io=0-30A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.8	0.15	HCB178380D-151 (Delta)	0.15
1	0.15	HCB138380D-151 (Delta)	0.15
1.2	0.15	HCB138380D-151 (Delta)	0.15
1.5	0.15	HCB138380D-151 (Delta)	0.15
1.8	0.15	HCB138380D-101 (Delta)	0.15
3.3	0.32	FP1308R3-R32-R (Cooper)	0.32
5	0.32	FP1308R3-R32-R (Cooper)	0.32

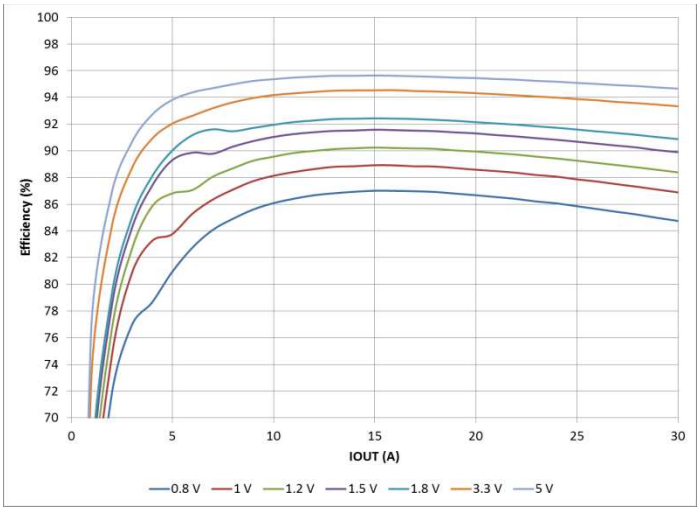


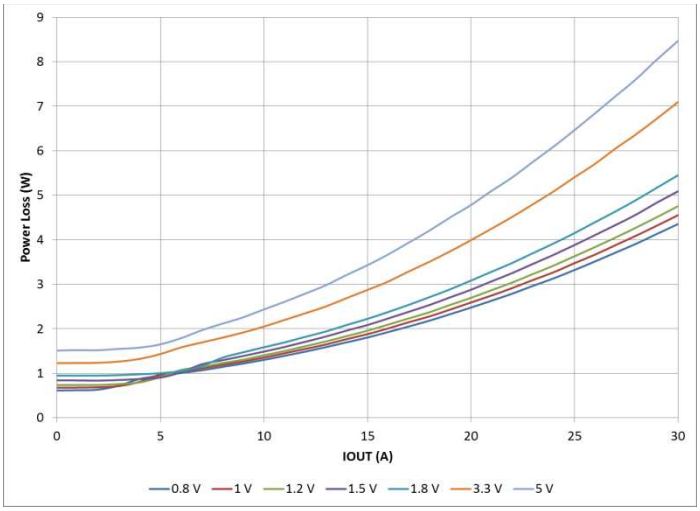


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = 12V, Internal LDO, Io=0-30A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.8	0.15	HCB178380D-151 (Delta)	0.15
1	0.15	HCB138380D-151 (Delta)	0.15
1.2	0.15	HCB138380D-151 (Delta)	0.15
1.5	0.15	HCB138380D-151 (Delta)	0.15
1.8	0.15	HCB138380D-101 (Delta)	0.15
3.3	0.32	FP1308R3-R32-R (Cooper)	0.32
5	0.32	FP1308R3-R32-R (Cooper)	0.32

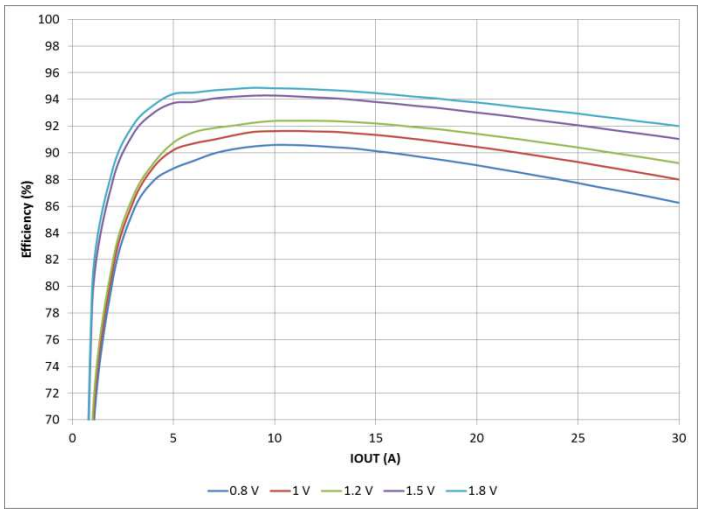


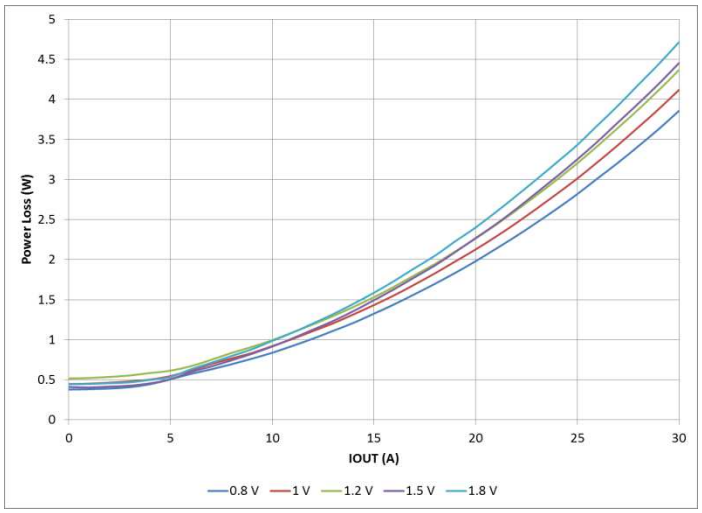


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = VCC = 5V, Io=0-30A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.8	0.1	HCB138380D-101 (Delta)	0.15
1	0.1	HCB138380D-101 (Delta)	0.15
1.2	0.15	HCB138380D-101 (Delta)	0.15
1.5	0.15	HCB138380D-151 (Delta)	0.15
1.8	0.15	HCB138380D-151 (Delta)	0.15





THEORY OF OPERATION

DESCRIPTION

The IR38263 is a 30A rated synchronous buck converter that supports PMBus communication. This device also has 3 pins that function as a parallel VID interface that can be used to set the output voltage to one of eight pre-programmed settings. They use an externally compensated fast, analog, PWM voltage mode control scheme to provide good noise immunity as well as fast dynamic response in a wide variety of applications. At the same time, the digital communication interfaces allow complete configurability of output setting and fault functions, as well as telemetry.

The switching frequency is programmable from 150 kHz to 1500 kHz and provides the capability of optimizing the design in terms of size and performance. It is recommended to operate at 500 kHz or higher.

This device provides precisely regulated output voltages from 0.5V to 0.875*PVin programmed via two external resistors or through the communication interfaces. They operate with an internal bias supply (LDO), typically 5.2V. This allows operation with a single supply. The output of this LDO is brought out at the Vcc pin and must be bypassed to the system power ground with a 10 uF decoupling capacitor. The Vcc pin may also be connected to the Vin pin, and an external Vcc supply between 4.5V and 5.5V may be used, allowing an extended operating bus voltage (PVin) range from 1.5V to 16V.

The device utilizes the on-resistance of the low side MOSFET (synchronous MOSFET) as current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

The IR38263 includes two low $R_{ds(on)}$ MOSFETs using Infineon's OptiMOS technology. These are specifically designed for low duty cycle, high efficiency applications.

DEVICE POWER-UP AND INITIALIZATION

During the power-up sequence, when Vin is brought up, the internal LDO converts it to a regulated 5.2V at Vcc. There is another LDO which further converts this down to 1.8V to supply the internal digital circuitry. An under-voltage lockout circuit monitors the voltage of VCC pin and the P1V8 pin, and holds the Power-on-reset (POR) low until these voltages exceed their thresholds and the internal 48 MHz oscillator is stable. When the device comes out of reset, it initializes a multiple times programmable (MTP) memory load cycle, where the contents of the MTP are loaded into the working registers. Once the registers are loaded from MTP, the designer can use PMBus commands to re-configure the various parameters to suit the specific VR design requirements if desired, irrespective of the status of Enable.

The typical default configuration utilizes the internal LDO to supply the VCC rail when PVin is brought up. For this configuration power conversion is enabled only when the Enable pin voltage exceeds it's under voltage threshold, the PVin bus voltage exceeds its under voltage threshold, the contents of the MTP have been fully loaded into the working registers and the device address has been read. The initialization sequence is shown in Figure 8. Another common default configuration uses an external power supply for the VCC rail. While in this configuration it is recommended to ensure the VCC rail reaches its target voltage prior the enable signal goes high.

Additional options are available to enable the device power conversion through software and these options may be configured to override the default by using the I2C interface or PMBus. For further details see the UN0075 IR3816x_IR3826x_IR3836x_PMBus commandset user note.

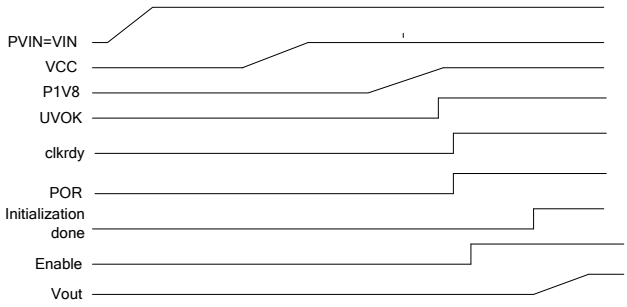


Figure 8: Initialization sequence showing PVin, Vin, Vcc, 1.8V, Enable and Vout signals as well as the internal logic signals

I2C AND PMBUS COMMUNICATION

The IR38263 have two 7-bit registers that are used to set the base I2C address and base PMBus address of the device, as shown below in Table 1.

Table 1: Registers used to set device base address

Register	Description
I2c_address[6:0]	The chip I2C address. An address of 0 will disable I2C communication. Note that disabling I2C does not disable PMBus.
Pmbus_address[6:0]	The chip PMBus address. An address of 0 will disable PMBus communication. Note that disabling PMBus does not disable I2C.

In addition, a resistor may be connected between the ADDR and LGND pins to set an offset from the default preconfigured I2C address (0x10) /PMBus address (0x40) in the MTP. Up to 16 different offsets can be set, allowing 16 devices with unique addresses in a single system. This offset, and hence, the device address, is read by the internal 10 bit ADC during the initialization sequence.

Table 2 below provides the resistor values needed to set the 16 offsets from the base address.

Table 2 : Address offset vs. External Resistor(R_{ADDR})

ADDR Resistor (Ohm)	Address Offset
499	+0
1050	+1
1540	+2
2050	+3
2610	+4
3240	+5
3830	+6
4530	+7
5230	+8
6040	+9
6980	+10
7870	+11
8870	+12
9760	+13
10700	+14
>11800	+15

The device will then respond to I2C/PMbus commands sent to this address. There is also a register bit *i2c_disable_addr_offset* that may be set in order to instruct the device to ignore the resistor offset for both i2c and PMBus. If this bit is set, the device will always respond to commands sent to the base address.

MODES FOR SETTING OUTPUT VOLTAGES

The IR38263 provides a configuration bit that allows the user to choose between PMBus and PVID mode. When this bit is set, the output voltage will ramp to the voltage set in the register selected by the VIDSEL0, VIDSEL1 and VIDSEL2 lines. These lines select a MTP register which contains a VID code that sets the output voltage. The VID tables can be configured for 5mV and 10mV VID steps are these are shown in the tables below. Note that the same VID value can result in different voltages depending on which VID table, 5mV or 10mV has been selected. When this bit is zero, the regulation is determined by the output voltage set by PMBus. It should be noted that irrespective of the mode used to set the output voltage, telemetry information always remains available on the i2c/PMBus. Table 3 shows how the VIDSELx lines are used to select the register containing the target value. It is worth noting that the VIDSEL lines may be driven with logic gates or with Open drain devices. When driven by open drain devices, a pullup resistor of 4.99K must be used. When driven by logic gates, a resistor of 4.99K is required in series with the pin.