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FEATURES

- Single 5V to 21V application
- Wide Input Voltage Range from 1V to 21V with external Vcc
- Output Voltage Range: 0.5V to 0.86*PVin
- Dual output, 4A/Phase
- Enhanced Line/Load Regulation with Feed-Forward
- Programmable Switching Frequency up to 1.5MHz
- Internal Digital Soft-Start
- Enable input with Voltage Monitoring Capability
- Thermally compensated current limit and Hiccup Mode Over Current Protection
- External synchronization with Smooth Clocking
- Precision Reference Voltage (0.5V +/-1%)
- Seq pin for Sequencing Applications
- Integrated MOSFETs, drivers and Bootstrap diode
- Thermal Shut Down
- Open Feedback Line Protection
- Over Voltage Protection
- Interleaved Phases to reduce Input Capacitors
- Monotonic Start-Up
- Operating Junction Temp: -40°C<Tj<125°C
- Small Size 5mm x 6mm PQFN
- Lead-free, Halogen-free, and RoHS Compliant

DESCRIPTION

The IR3891 Sup*IR*Buck® is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard PWM controller and MOSFETs make IR3891 a space-efficient solution, providing accurate power delivery for low output voltage.

IR3891 is a versatile regulator which offers programmability of switching frequency and a fixed current limit while operating in wide input and output voltage range.

The switching frequency is programmable from 300kHz to 1.5MHz for an optimum solution.

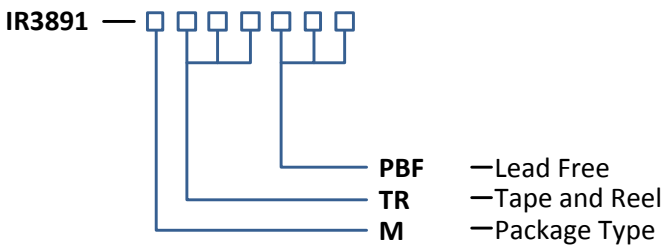
It also features important protection functions, such as Over Voltage Protection (OVP), Pre-Bias startup, hiccup current limit and thermal shutdown to give required system level security in the event of fault conditions.

APPLICATIONS

- Sever Applications
- Netcom Applications
- Set Top Box Applications
- Storage Applications
- Embedded telecom Systems
- Distributed Point of Load Power Architectures
- Computing Peripheral Voltage regulators
- General DC-DC Converters

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR3891	PQFN 5mm x 6mm	Tape and Reel	4000	IR3891MTRPBF



BASIC APPLICATION

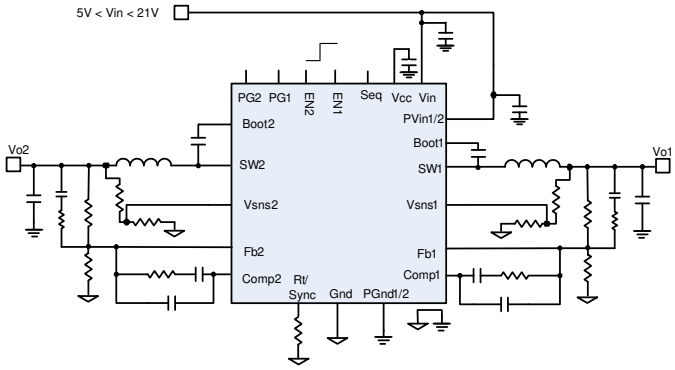


Figure 1: IR3891 Basic Application Circuit

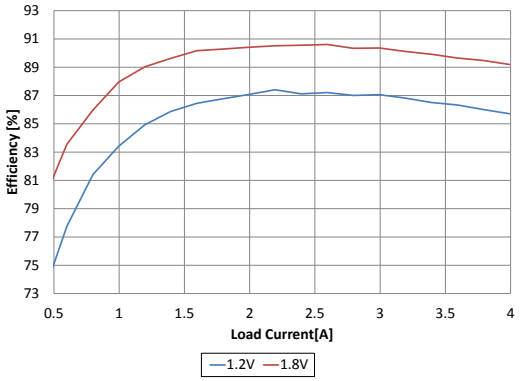
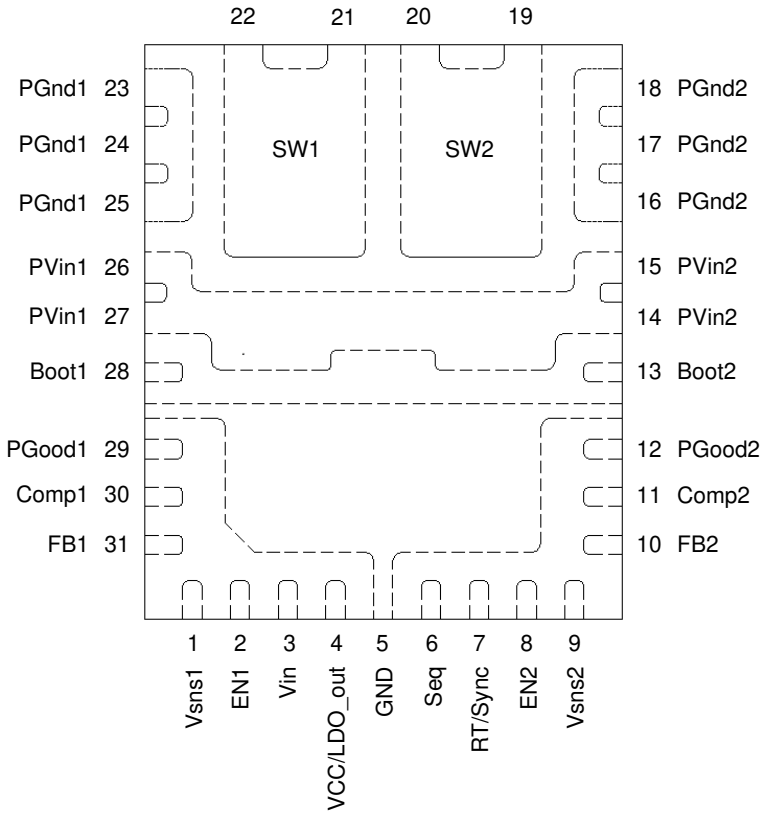


Figure 2: Efficiency [Vin=12V, Fsw=600kHz]

PIN DIAGRAM

5mm X 6mm POWER QFN
Top View



FUNCTIONAL BLOCK DIAGRAM

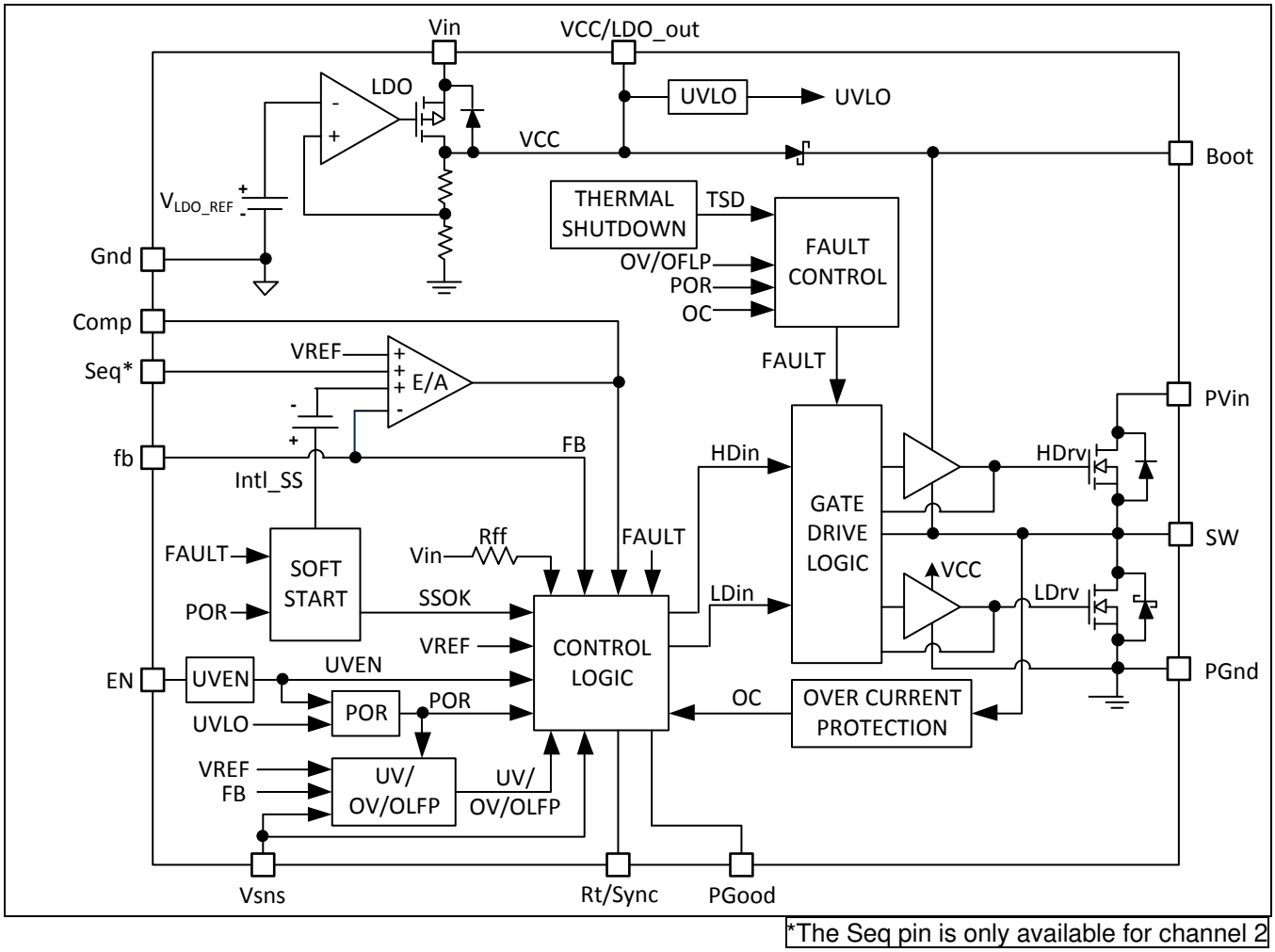


Figure 3: IR3891 Simplified Block Diagram (one phase)

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1, 9	Vsns 1/2	Sense pins for over-voltage protection and PGood. A resistor divider with the same ratio as the respective feedback resistor divider should be connected between each Vsns pin and its respective Vout.
2, 8	EN 1/2	Enable pins for turning on and off the regulator.
3	Vin	Input voltage for Internal LDO. A 1.0µF capacitor should be connected between this pin and PGnd. If external supply is connected to VCC pin, this pin should be shorted to VCC pin.
4	VCC/LDO_out	Input Bias Voltage, output of the internal LDO. Place a minimum 2.2µF cap from this pin to PGnd.
5	GND	Signal ground for internal reference and control circuitry.
6	Seq	Input to error amplifier for sequencing purposes. Can be left floating for non-sequencing applications. It is only connected to the Error-Amplifier of channel 2.
7	Rt/Sync	Multi-function pin to set switching frequency. Use an external resistor from this pin to Gnd to set the free-running switching frequency. Or use an external clock signal to connect to this pin through a diode, the device's switching frequency is synchronized with the external clock.
10, 31	FB 2/1	Inverting inputs to the error amplifiers. These pins are connected directly to the outputs of the regulator via resistor dividers to set the output voltages and provide feedback to the error amplifiers.
11, 30	Comp 2/1	Output of the error amplifiers. External resistor and capacitor networks are typically connected from these pins to its respective Fb pin to provide loop compensation.
12, 29	PGood 2/1	Power Good status pins are open drain outputs. The pins are typically connected to VCC via pull up resistors.
13, 28	Boot 2/1	Supply voltages for high side drivers, 100nF capacitors should be connected between these pins and their respective SW pin.
14, 15, 26, 27	PVin 2/1	Input voltage for power stage.
16, 17, 18, 23, 24, 25	PGnd 2/1	Power Ground. These pins serve as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
19, 20, 21, 22	SW 2/1	Switch nodes. These pins are connected to the output inductors.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin		-0.3V to 25V
Vin		-0.3V to 25V
VCC		-0.3V to 8V (Note 1)
SW		-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
BOOT		-0.3V to 33V
BOOT to SW		-0.3V to VCC + 0.3V (Note 2)
EN, PGood		-0.3V to VCC + 0.3V (Note 2)
Other Input/Output pins		-0.3V to 3.9V
PGnd to GND		-0.3V to + 0.3V
Junction Temperature Range		-40°C to 150°C
Storage Temperature Range		-55°C to 150°C
ESD	Machine Model	Class A
	Human Body Model	Class 1C
	Charged Device Model	Class III
Moisture Sensitivity level		JEDEC Level 2 @ 260°C
RoHS Compliant		Yes

Note:

1. VCC must not exceed 7.5V for Junction Temperature between -10°C and -40°C.
2. Must not exceed 8V.

THERMAL INFORMATION	
Thermal Resistance, Junction to Case Top (θ_{JC_TOP})	36 °C/W
Thermal Resistance, Junction to PCB (θ_{JB})	3.6 °C/W
Thermal Resistance, Junction to Ambient (θ_{JA}) (Note 3)	24.7 °C/W

Note:

3. Thermal resistance (θ_{JA}) is measured with components mounted on a high effective thermal conductivity test board in free air.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DEFINITION	MIN	MAX	UNIT
PVin	Input Bus Voltage *	1.0	21	V
Vin	Supply Voltage	5.0	21	
VCC	Supply Voltage **	4.5	7.5	
Boot to SW	Supply Voltage	4.5	7.5	
V_O	Output Voltage	0.5	0.86 * PVin	
I_O	Output Current	0	4	A / Phase
Fs	Switching Frequency	300	1500	kHz
T_J	Junction Temperature	-40	125	°C

* SW1/2 node must not exceed 25V

** When VCC is connected to an externally regulated supply, also connect Vin.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply over, 6.8V < Vin=PVin < 21V in 0°C < T_J < 125°C. Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Stage						
Power Losses	P_{LOSS}	Vin = 12V, $Vout_1$ = 1.8V, $Vout_2$ = 1.2V, I_O = 4A/phase, Fs = 600kHz, L1 =2.2uH, L2=1.5uH, Note 4		1.38		W
Top Switch	$R_{ds(on)\_Top}$	VBoot - Vsw= 5.3V, I_O = 4A, Tj = 25°C		27.5	36.4	mΩ
Bottom Switch	$R_{ds(on)\_Bot}$	Vcc = 5.3V, I_O = 4A, Tj = 25°C		19.5	24.2	
Bootstrap Diode Forward Voltage		I(Boot) = 10mA		300	450	mV
SW Leakage Current	I_{SW}	SW = 0V, Enable = 0V			1	µA
		SW = 0V, Enable = high, VSeq = 0V			2	µA
Dead Band Time	T_{db}	Note 4	10	20	30	ns
Supply Current						
VIN Supply Current (standby)	$I_{in(Standby)}$	EN = Low, No Switching		100	175	µA
VIN Supply Current (dynamic)	$I_{in(Dyn)}$	EN = High, Fs = 600kHz,		12.0	17	mA
VCC LDO Output						
Output Voltage	V_{cc}	Vin(min) = 6.8V, Io = 0-60mA, Cload = 2.2uF	5	5.3	5.6	V
VCC Dropout	V_{cc_drop}	Icc = 60mA, Cload = 2.2uF			0.75	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Short Circuit Current	Ishort			120		mA
Oscillator						
Rt Voltage	Vrt			1.0		V
Frequency Range	F_s	Rt = 80.6K	270	300	330	kHz
		Rt = 39.2K	540	600	660	
		Rt = 15K	1350	1500	1650	
Ramp Amplitude	Vramp	Vin = 6.8V, Vin slew rate max = 1V/µs, Note 4		1.02		Vp-p
		Vin = 12V, Vin slew rate max = 1V/µs, Note 4		1.80		
		Vin = 21V, Vin slew rate max = 1V/µs, Note 4		3.15		
		Vcc=Vin = 5V, For external Vcc operation, Note 4		0.75		
Min Pulse Width	Tmin(ctrl)	Note 4			60	ns
Max Duty Cycle	Dmax	Fs = 300kHz, Vin=Pvin=12V	86			%
Fixed Off Time	Toff	Note 4		200	250	ns
Sync Frequency Range	Fsync		270		1650	kHz
Sync Pulse Duration	Tsync		100	200		ns
Sync Level Threshold	High		3			V
	Low				0.6	
Error Amplifier						
Seq Input Offset Voltage	Vos_VSeq	VSeq – Vfb; VSeq=250mV	-3		+3	%
Input Bias Current	IFb(E/A)		-200		+200	nA
Seq Input impedance	Rin_Seq(E/A)	Internal Seq pull-up resistor		300		kΩ
Sink Current	Isink(E/A)		0.4	0.85	1.2	mA
Source Current	Isource(E/A)		3	4	7	mA
Slew Rate	SR	Note 4	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 4	20	30	40	MHz
DC Gain	Gain	Note 4	80	90	110	dB
Maximum Voltage	Vmax(E/A)		1.7	2	2.3	V
Minimum Voltage	Vmin(E/A)			120	220	mV
Vseq Common Mode Voltage			0		0.77	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reference Voltage						
Feedback Voltage	Vfb	VSeq=3.3V		0.5		V
Accuracy		0°C < Tj < 85°C	-1		+1	%
		-40°C < Tj < 125°C, Note 5	-1.5		+1.5	
Soft Start						
Soft Start Ramp Rate	Ramp (SS_start)		0.14	0.18	0.22	mV / µs
Fault Protection						
Current Limit	I_{CC}	Vcc=5.3V, Tj = 25°C	4.8	6.0	7.2	A / Phase
Hiccup blanking time	Tblk_Hiccup	Note 4		20.48		ms
OFLP Trip Threshold	OFLP(threshold)	Fb Falling	65	70	75	%Vref
OFLP Fault Prop Delay	OFLP(delay)		0.1	0.3	0.5	µs
OVP Trip Threshold	OVP(threshold)	Vsns Rising	115	120	125	%Vref
OVP Trip Threshold Hysteresis	OVP_Hys	Vsns falling from above 120% of Vref, Sync_FET turns off afterwards		25		mV
OVP Comparator Delay	OVP(delay)			2		µs
Thermal Shutdown		Note 4		140		°C
Thermal Hysteresis		Note 4		20		°C
V_{CC}-Start-Threshold	VCC_UVLO_Start	VCC Rising Trip Level	4.0	4.2	4.4	V
V_{CC}-Stop-Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	3.7	3.9	4.1	
Input / Output Signals						
Enable-Start-Threshold	EN_UVLO_Start	Supply ramping up	1.14	1.2	1.26	V
Enable-Stop-Threshold	EN_UVLO_Stop	Supply ramping down	0.95	1	1.05	
Enable leakage current	Ien	Enable=3.3V		3	4.5	µA
Power Good upper Threshold	VPG(upper)	Vsns Rising	80	85	90	%Vref
Power Good lower Threshold	VPG(lower)	Vsns Falling	75	80	85	%Vref
Lower Threshold Delay	VPG(lower)_Dly	Vsns Rising	1	1.3	1.6	ms
PGood Voltage Low	PG(voltage)	I_{Pgood}= -5mA			0.5	V

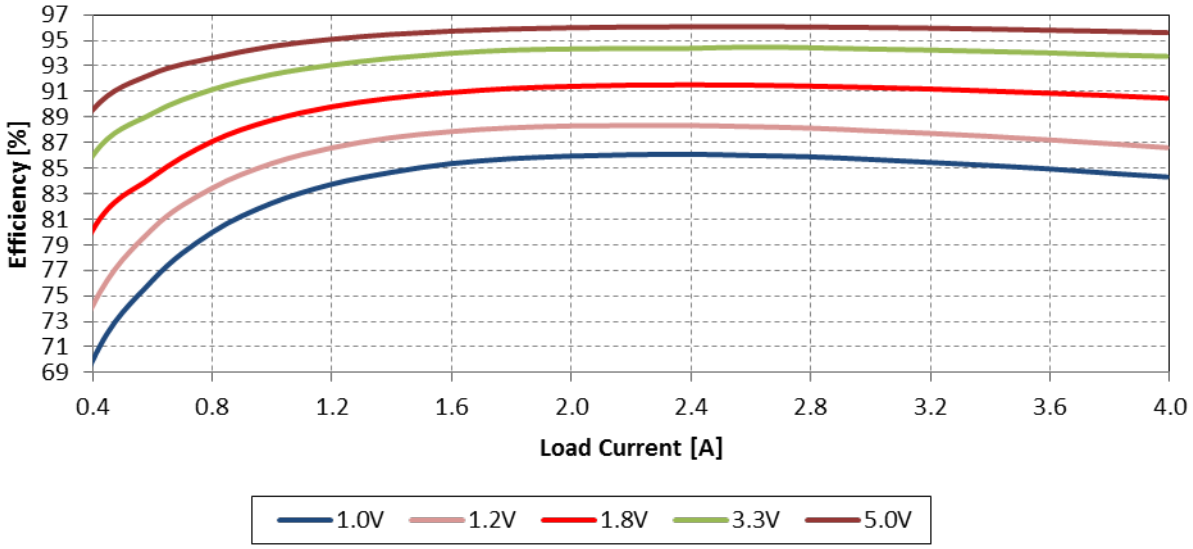
Note:

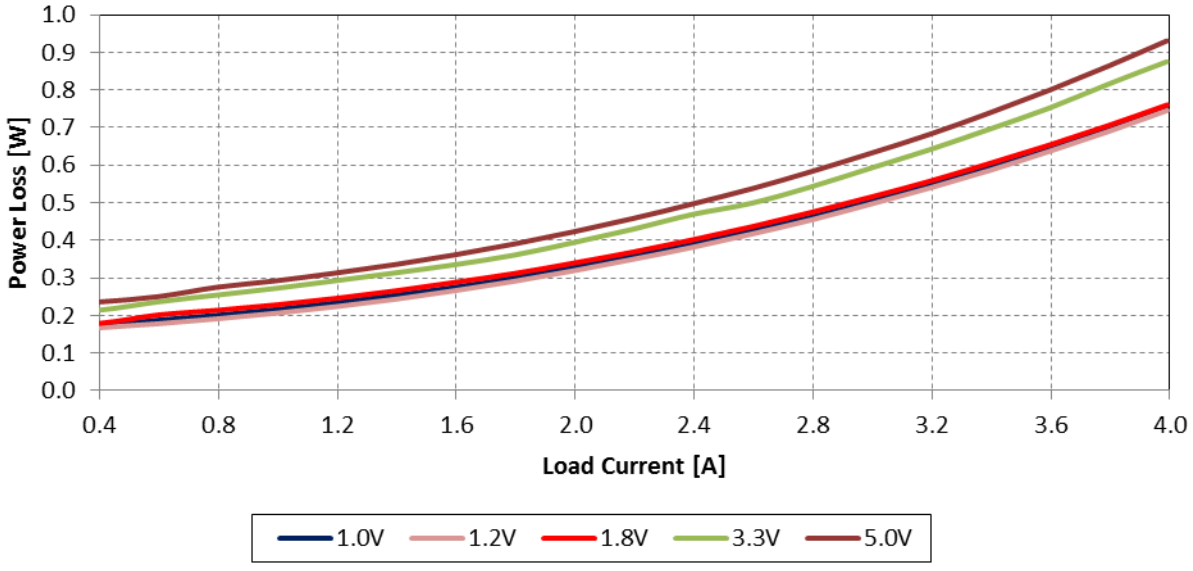
4. Guaranteed by design but not tested in production.
5. Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 12V, Vcc = Internal LDO, Io=0-4A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement while running a single channel and disabling the other.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
1.0	1.5	7443340150 (Wurth Elektronik)	4.4
1.2	1.5	7443340150 (Wurth Elektronik)	4.4
1.8	2.2	7443340220 (Wurth Elektronik)	4.4
3.3	3.3	7443340330 (Wurth Elektronik)	6.5
5.0	3.3	7443340330 (Wurth Elektronik)	6.5

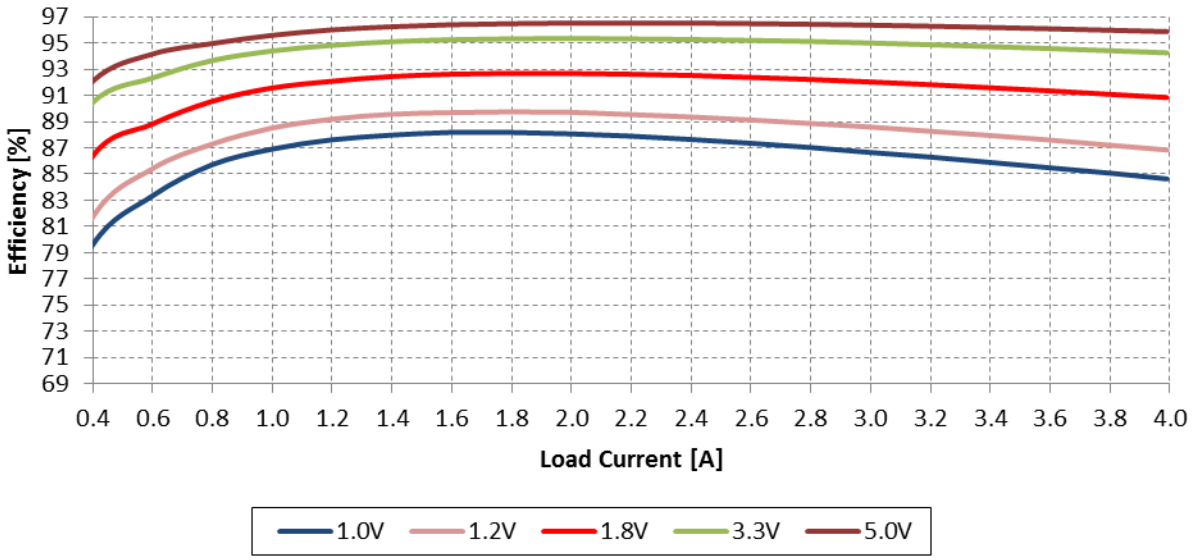


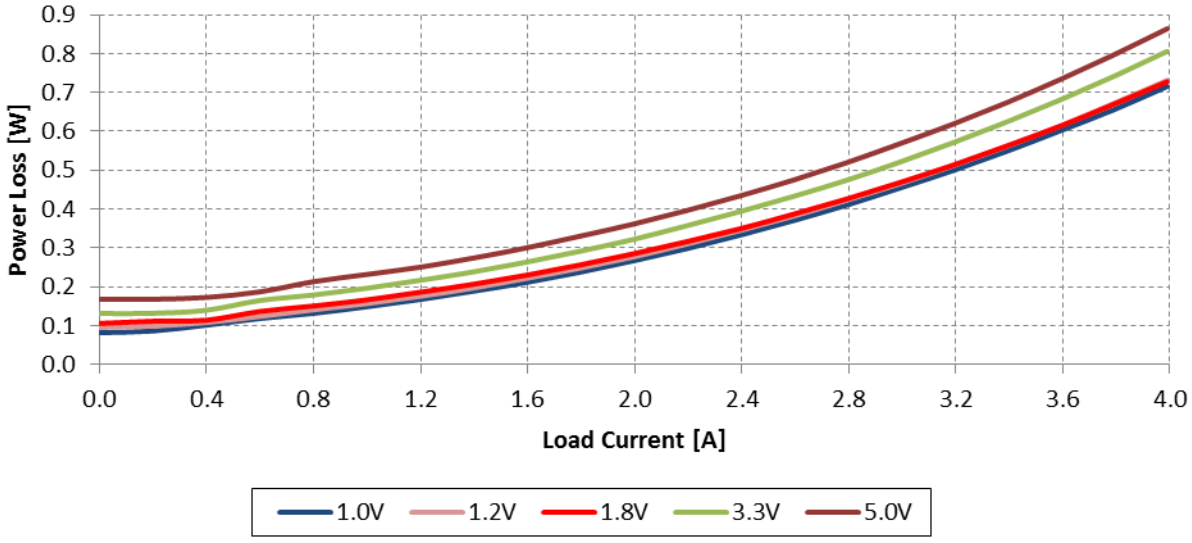


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 12V, Vin = Vcc = 5V, Io=0-4A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement while running a single channel and disabling the other.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
1.0	1.5	PCMB065T-1R5MS (Cyntec)	6.7
1.2	1.5	PCMB065T-1R5MS (Cyntec)	6.7
1.8	2.2	7443340220 (Wurth Elektronik)	4.4
3.3	3.3	7443340330 (Wurth Elektronik)	6.5
5.0	3.3	7443340330 (Wurth Elektronik)	6.5

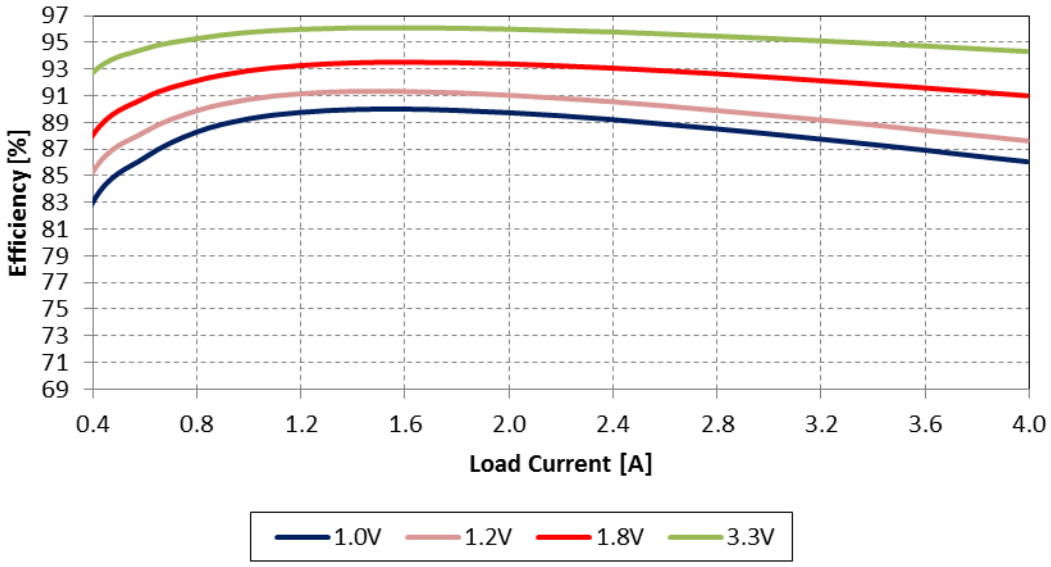


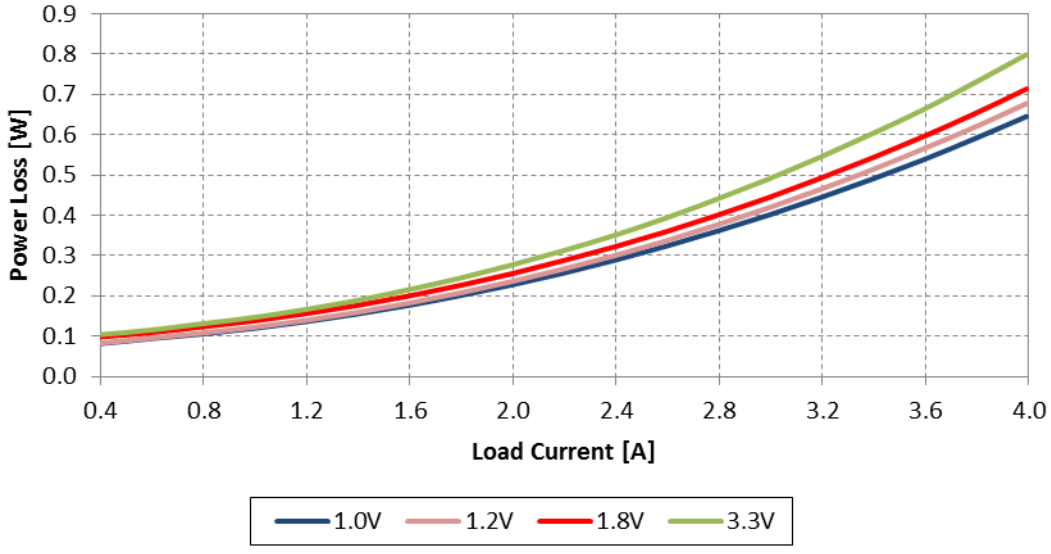


TYPICAL EFFICIENCY AND POWER LOSS CURVES

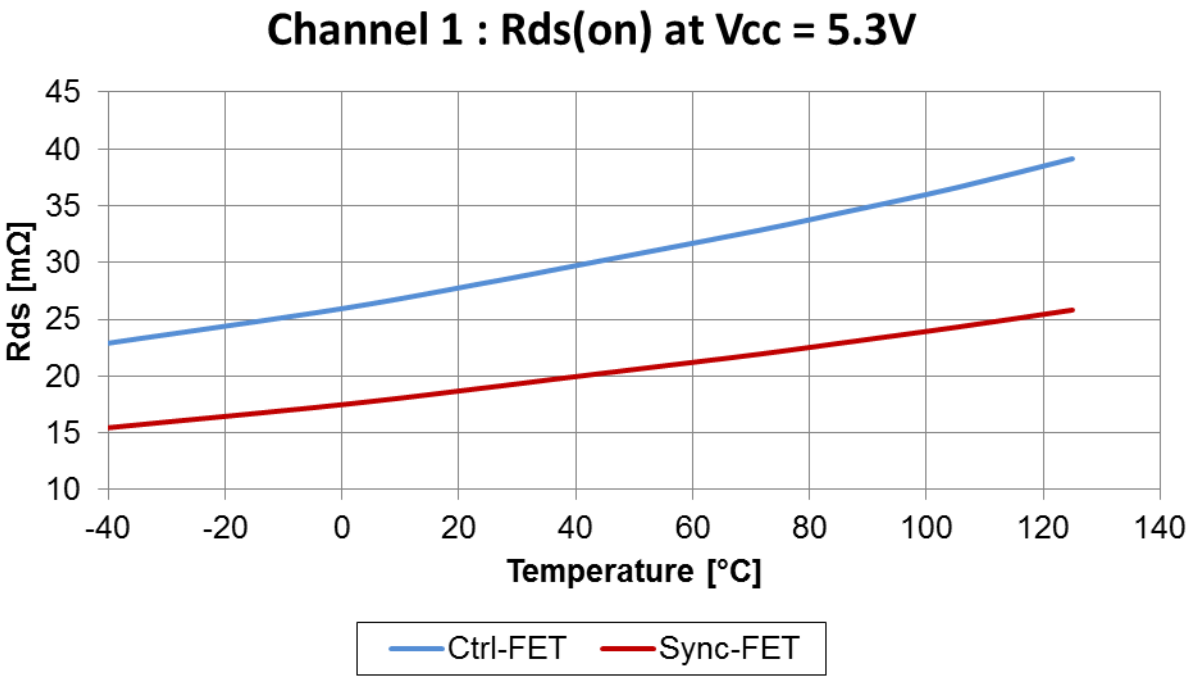
PVin = 5V, Vcc = 5V, Io=0-4A, Fs = 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement while running a single channel and disabling the other.

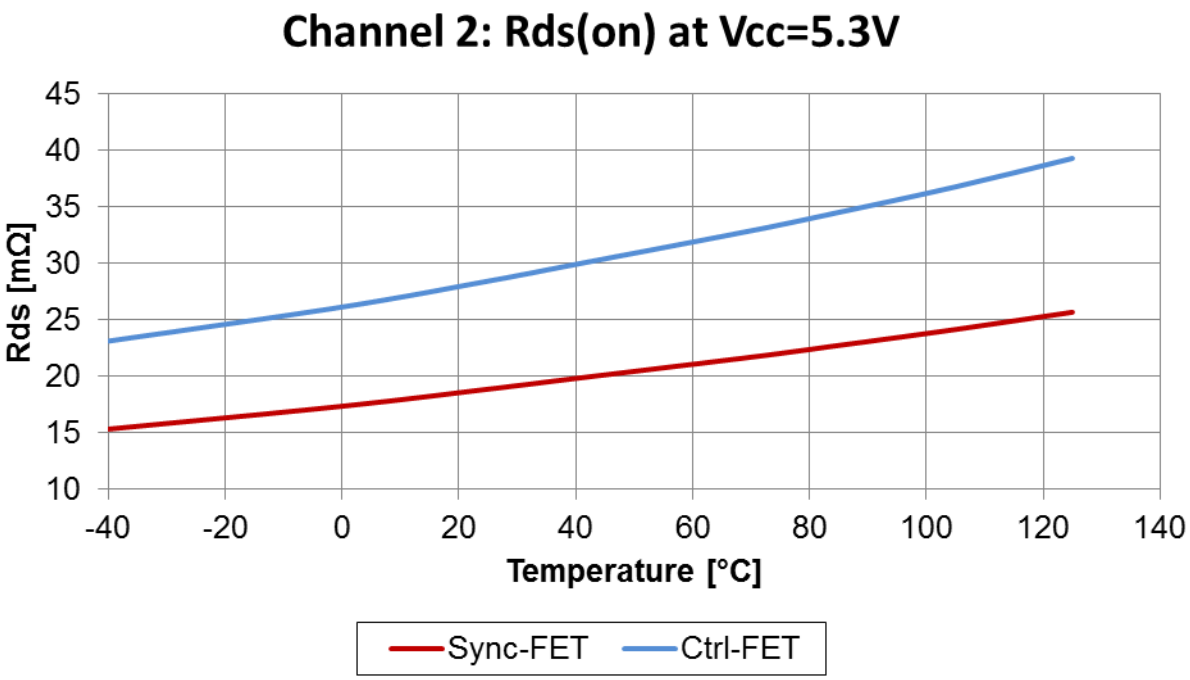
VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
1.0	1.0	PCMB065T-1R0MS (Cyntec)	5.6
1.2	1.5	PCMB065T-1R5MS (Cyntec)	6.7
1.8	1.5	PCMB065T-1R5MS (Cyntec)	6.7
3.3	1.5	PCMB065T-1R5MS (Cyntec)	6.7





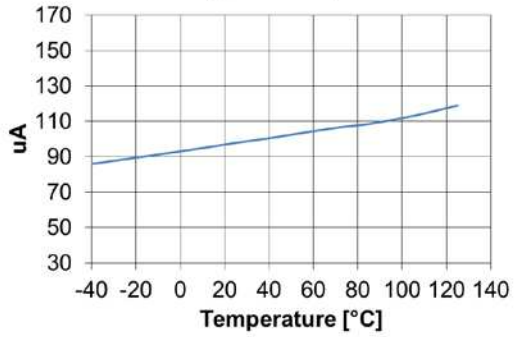
MOSFET RDSON VARIATION OVER TEMPERATURE



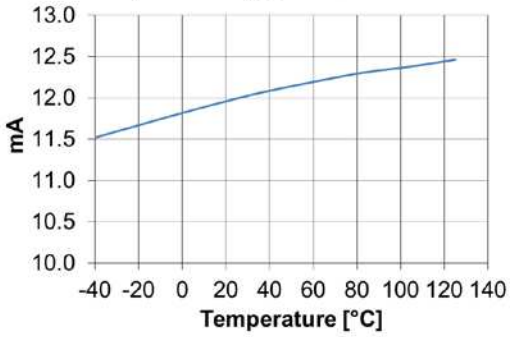


TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

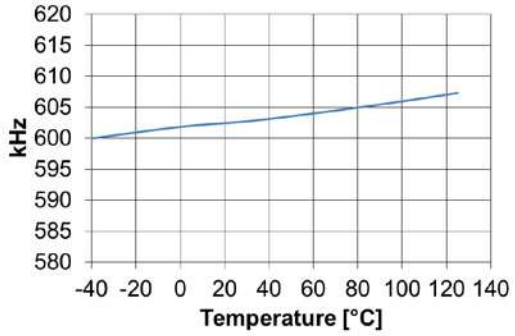
IIN (STANDBY)



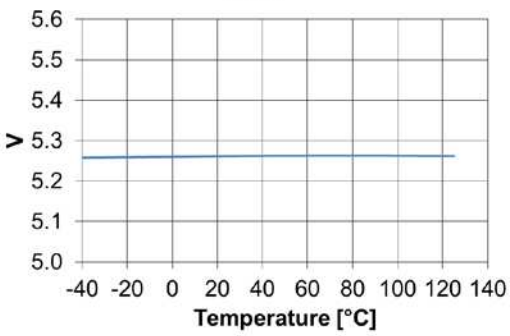
IIN(DYNAMIC) @ Fs=600kHz



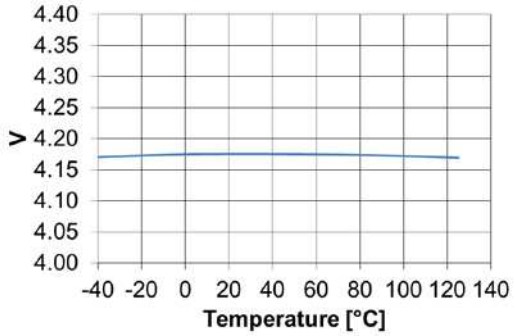
FREQUENCY [Rt=39.2kΩ]



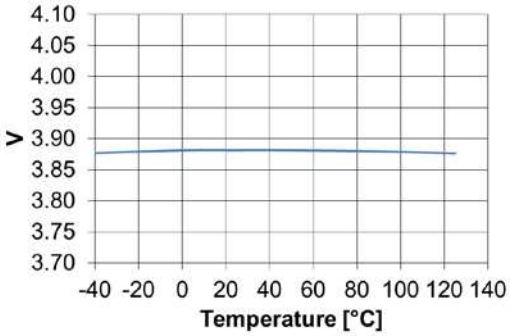
VCC



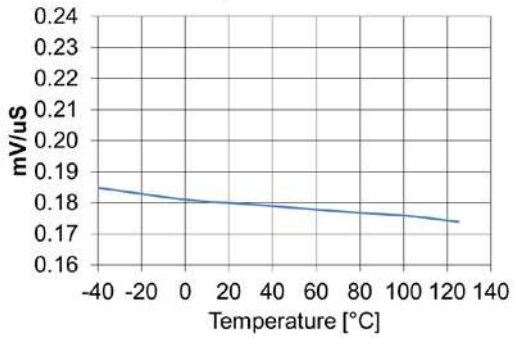
VCC_UVLO_START



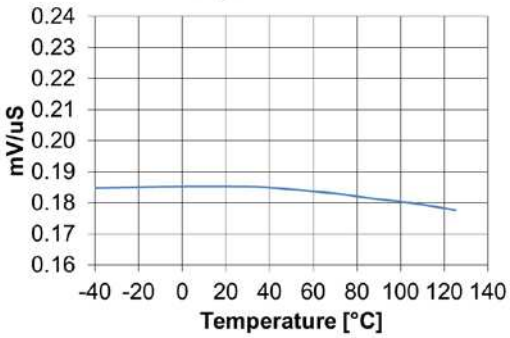
VCC_UVLO_STOP



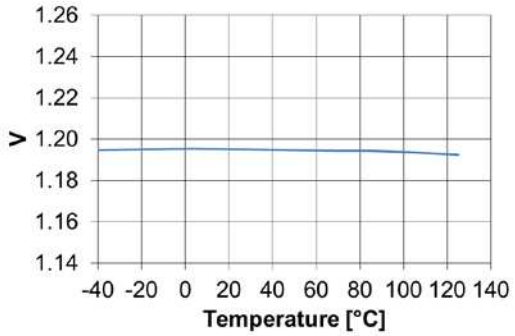
SS_START1



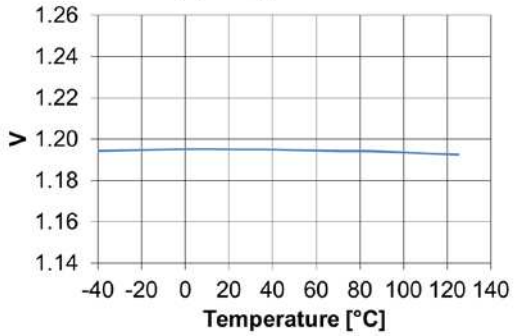
SS_START2



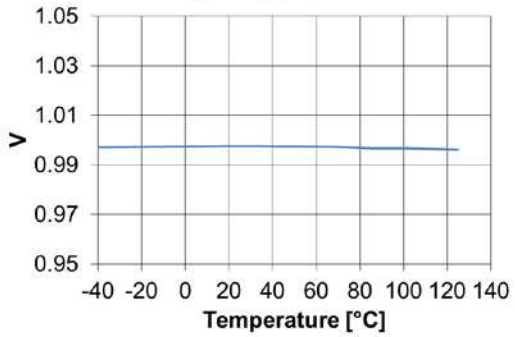
EN_UVLO_START1



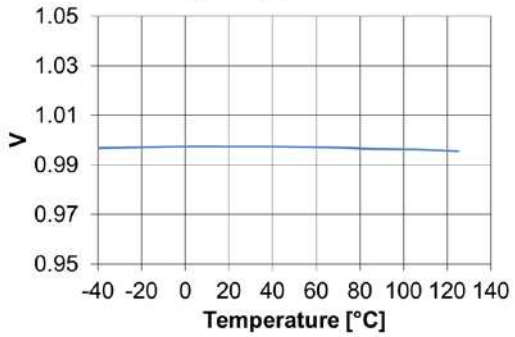
EN_UVLO_START2



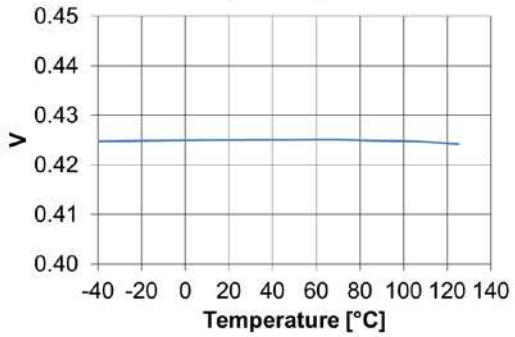
EN_UVLO_STOP1



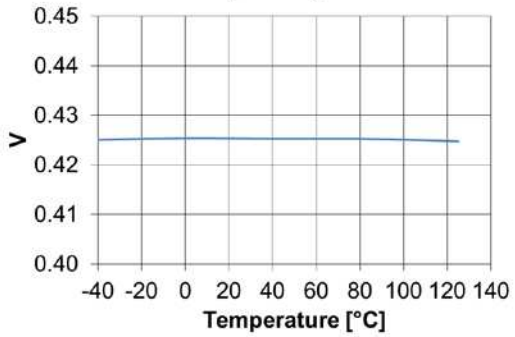
EN_UVLO_STOP2



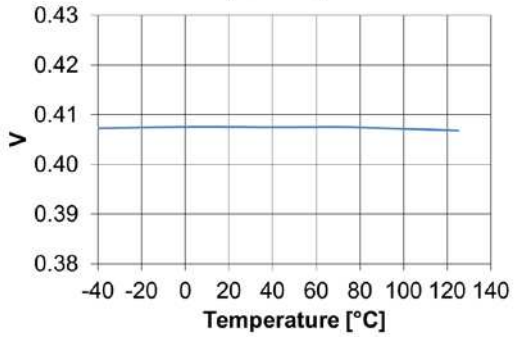
VPG (UPPER) 1



VPG (UPPER) 2



VPG (LOWER) 1



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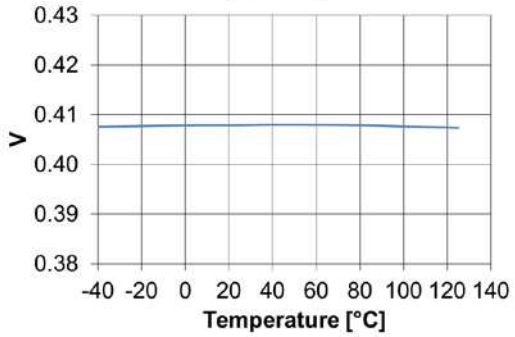

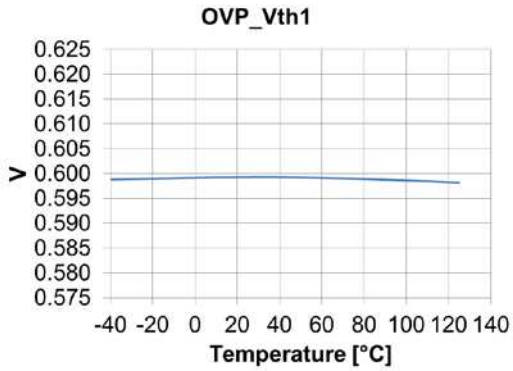

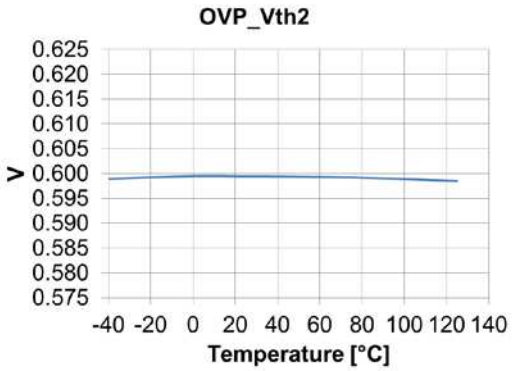

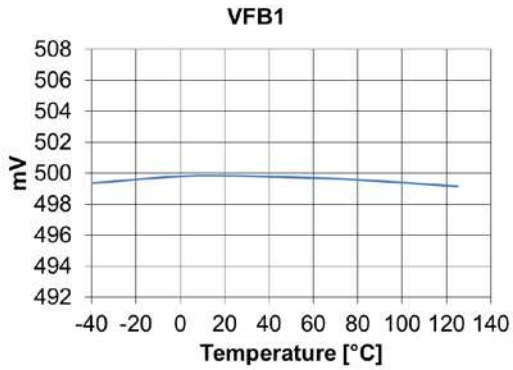

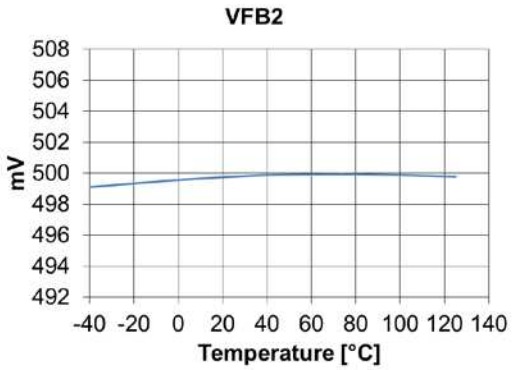

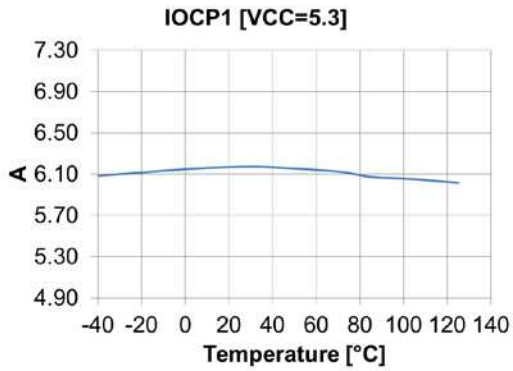

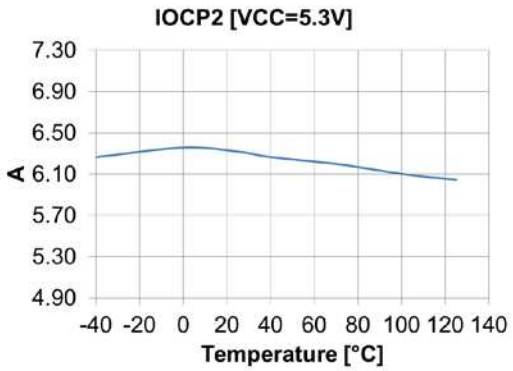

THEORY OF OPERATION

DESCRIPTION

The IR3891 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 300KHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR3891 provides precisely regulated output voltage programmed via two external resistors from 0.5V to 0.86*PVin.

The IR3891 operates with an internal low drop out regulator (LDO) which is connected to the VCC pin. This allows operation with a single supply. When using the internal LDO supply, the Vin pin should be connected the PVin pin. If an external bias is used, it should be connected to the VCC pin and the Vin pin should be shorted to the VCC pin.

The device utilizes the on-resistance of the low side MOSFET (sync FET) as a current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for an external current sense resistor.

IR3891 includes two low Rds(on) MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

UNDER-VOLTAGE LOCKOUT AND POR

The under-voltage lockout circuits monitor the voltage on the VCC pin and the EN1/2 pins. They ensure that the MOSFET driver outputs remain in the off state whenever either of these signals drops below the set thresholds. Normal operation resumes once VCC and EN rise above their thresholds.

The POR (Power On Ready) signal is high when all these signals reach the valid logic level (see system block diagram).

ENABLE

The EN pin offers another level of flexibility for startup. Each channel of the IR3891 is controlled by a separate EN pin. When the voltage at an EN pin voltage exceeds its precise threshold (EN_UVLO_START), the respective channel turns on. The precise threshold allows the user to implement an Under-Voltage Lockout (UVLO) function. By deriving the EN pin voltage from the bus voltage (PVin) through a suitable resistor divider, the user can set a PVin threshold voltage. The resistor divider scales the PVin voltage for the EN pin. Only after the bus voltage reaches or exceeds this level will the voltage at the Enable pin exceeds its threshold and enable the respective IR3891 channel. By connecting IR3891 in this configuration, the user can enable the part by applying PVin and ensures the IR3891 does not turn on until the bus voltage reaches the desired level (Figure 4). Therefore, in addition to being a logic input pin that enables channels on IR3891, the EN pin also offers UVLO functionality. UVLO functionality is particularly desirable for high output voltage applications, where it is beneficial to disable the IR3891 until PVin exceeds the desired output voltage level.

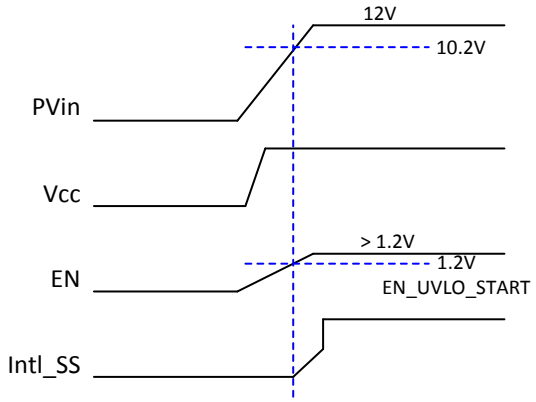

Figure 4: Normal Startup: IR3891 Channel starts when PVin reaches 10.2V by connecting EN to PVin using a resistor divider.

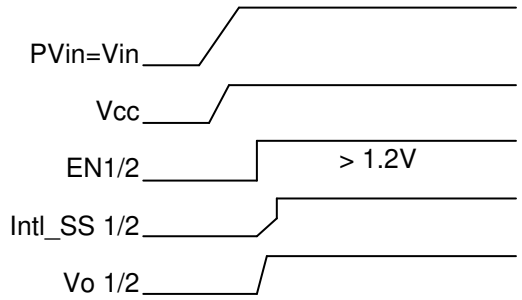

Figure 5: Recommended startup for Normal operation

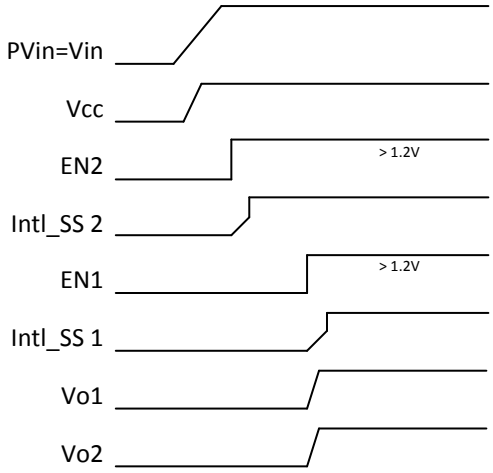

Figure 6: Recommended startup for sequencing operation (ratiometric or simultaneous)

Figure 5 shows the recommended start-up sequence for the normal (non-sequencing) operation of IR3891, when EN pins are used as a logic input. Figure 6 shows the recommended startup sequence for sequenced operation of IR3891.

PRE-BIAS STARTUP

IR3891 begins each start up by pre-charging the output to prevent oscillation and disturbances to the output voltage. The buck converter starts in an asynchronous fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. Figure 7 shows a typical pre-bias sequence. The sync FET always starts with a narrow pulse width (12.5% of the switching period). The pulse width increase after 16 pulses by 12.5% until the output reaches steady state value. There are 16 pulses for each step. Figure 8 shows the series of 16 x 8 startup pulses.

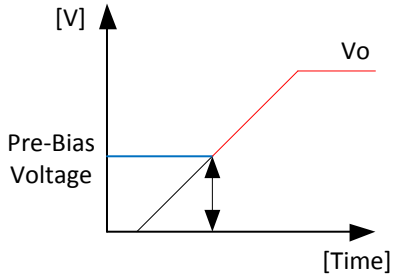

Figure 7: Pre-bias Start Up

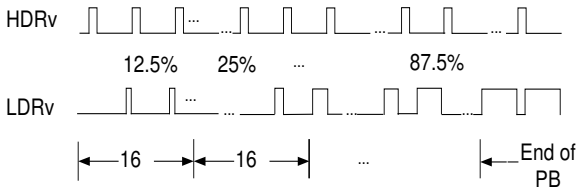

Figure 8: Pre-bias startup pulses

SOFT-START

IR3891 has an internal digital soft-start to control the output voltage rise and to limit the current surge during start-up. To ensure the correct start-up, the soft-start sequence initiates when the EN and VCC rise above their UVLO thresholds and generates Power On Ready (POR) signal. The internal soft-start rises with the typical rate of 0.2mV/µS from 0V to 1.5V. Figure 9 shows the waveforms during soft-start. The normal Vout start-up time is fixed, and is equal to:

$$Tstart = \frac{(0.65V - 0.15V)}{0.2mV / \mu S} = 2.5mS \qquad (1)$$

During the soft-start the over-current protection (OCP) and the over-voltage protection (OVP) is enabled to protect the device from short circuit or over voltage events.

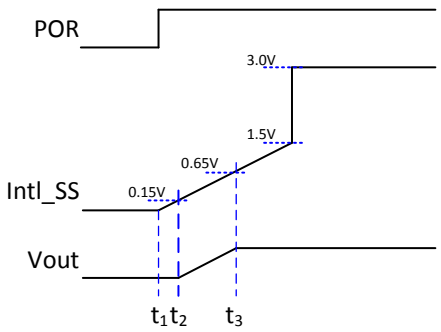

Figure 9: Theoretical operation waveforms during soft-start (non-sequencing)

OPERATING FREQUENCY

The switching frequency can be programmed between 300KHz-1.5MHz by connecting an external resistor from R_t/Sync pin to GND. Table 1 tabulates the oscillator frequency versus R_t.

Table 1: Switching Frequency (Fs) vs. External Resistor (R_t)

Rt (KΩ)	Freq (KHz)
80.6	300
60.4	400
48.7	500
39.2	600
34	700
29.4	800
26.1	900
23.2	1000
21	1100
19.1	1200
17.4	1300
16.2	1400
15	1500

EXTERNAL SYNCHRONIZATION

IR3891 incorporates an internal phase lock loop (PLL) circuit which enables synchronization of the internal oscillator to an external clock. This function is important to avoid sub-harmonic oscillations due to beat frequency for embedded systems when multiple point-of-load (POL) regulators are used. A multiple-function pin, Rt/Sync, is used to connect the external clock. If the external clock is present before the converter turns on, Rt/Sync pin can be connected to the external clock solely and no resistor is required. If the external clock is applied after the converter turns on, or the converter switching frequency needs to toggle between the external clock frequency and the internal free-running frequency, an external resistor from Rt/Sync pin to GND is required to set the free running frequency.

When an external clock is applied to Rt/Sync pin after the converter runs in steady state with its free-running frequency, a transition from the free-running frequency to the external clock frequency will happen. The switching frequency gradually synchronizes to the external clock frequency regardless of which one is faster. On the contrary, when the external clock signal is removed from Rt/Sync pin, the switching frequency gradually returns to the free-running frequency. In order to minimize the impact from these transitions to output voltage, a diode is recommended to add between the external clock and Rt/Sync pin. Figure 10 shows the timing diagram of these transitions.

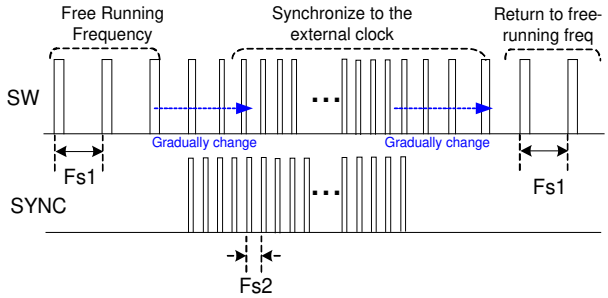

Figure 10: Timing diagram for synchronization to an external clock (Fs1>Fs2 or Fs1<Fs2)

An internal compensation circuit is used to change the PWM ramp slope according to the clock frequency applied on Rt/Sync pin. Thus, the effective amplitude of the PWM ramp (Vramp), which is used in compensation loop calculation, has minor impact from the variation of the external synchronization signal. Vin variation also affects the ramp amplitude, which is discussed separately in Feed-Forward section.

SHUTDOWN

IR3891 shutdown occurs when VCC drops below its threshold or a fault occurs. When VCC falls below VCC_UVLO_STOP, the part detects an UVLO event and the part turns off. Over-Voltage Protection, Over-Current Protection and Thermal Shutdown also cause the IR3891 shutdown. Faults are discussed in more detail below.

Each channel of the IR3891 can be shutdown separately by pulling the channel EN pin below its low threshold. Each EN pin controls only one channel to allow the user to operate each independently.

OVER CURRENT PROTECTION (CURRENT LIMIT AND HICCUP MODE)

The over-current protection is performed by sensing current through the $R_{DS(on)}$ of the Sync FET. This method enhances the converter's efficiency and reduces cost by eliminating a current sense resistor. The current limit is pre-set internally and compensated to maintain an almost constant limit over temperature.

IR3891 determines over-current events when the Synchronous FET is on. OCP circuit samples this current for 40 nsec typically after the rising edge of the PWM set pulse which has a width of 12.5% of the switching period. The PWM pulse starts at the falling edge of the PWM set pulse. This makes valley current sense more robust as current is sensed close to the bottom of the inductor downward slope where transient and switching noise are lower and helps to prevent false tripping due to noise and transient. An OC condition is detected if the load current exceeds the threshold, the converter enters into hiccup mode. PGood will go low and the internal soft start signal will be pulled low.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta i}{2} \qquad (2)$$

I_{OCP} = DC current limit hiccup point
I_{LIMIT} = Current Limit Valley Point
Δi = Inductor ripple current

Hiccup mode is when the converter stops and waits before restarting. The channel waits for Tblk_Hiccup, 2.48 ms typical, before the OC signal resets and restarts. In normal application, the converter restarts with a pre-bias sequence and soft-start. Figure 11 shows the timing diagram of the above OC protection. If another OC event is detected, the part repeats hiccup mode.

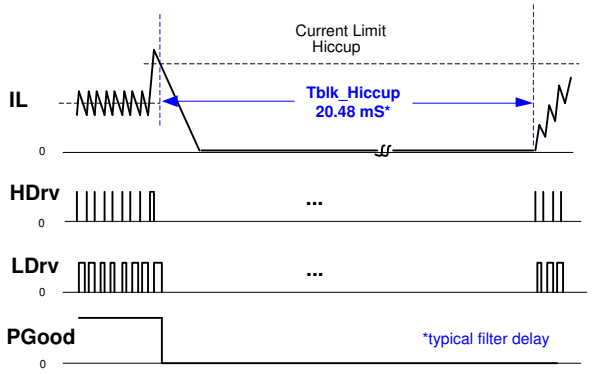

Figure 11: Timing diagram for pulse-by-pulse current limit and Hiccup mode

THERMAL SHUTDOWN

IR3891 provides thermal protection. A thermal fault is detected, when the temperature of the part reaches the Thermal Shutdown Threshold, 145°C typical. A thermal fault results in both channels turning off. The power MOSFETs are disabled during thermal shutdown. IR3891 automatically restarts when the temperature of the part drops back below the lower thermal limit, typically 20°C below the Thermal Shutdown Threshold.

FEED-FORWARD

Feed-Forward is an important feature which helps with stability and preserves load transient performance during PVin changes. In IR3891, Feed-Forward (F.F.) function is enabled when Vin pin is connected to PVin pin and Vin>5.0V. The PWM ramp amplitude (Vramp) is proportionally changed with respect to Vin to maintain PVin/Vramp ratio. The ratio is almost constant throughout the Vin range (as shown in Figure 12). By maintaining a constant PVin/Vramp, the control loop bandwidth and phase margin are more constant. F.F. function also helps minimize the effect of PVin changes on the output voltage.

Feed-Forward is based on the Vin voltage and needs to be accounted for when calculating IR3891 compensation. The PVin/Vramp ratio is not maintained when Vin and PVin are not equal. This is the case when an external bias voltage for VCC. When using an external VCC voltage, Vin pin should be connected to the VCC pin instead of the PVin pin. Compensation for the configuration should reflect the separation.

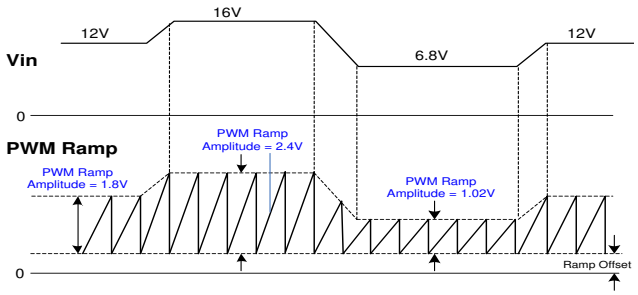

Figure 12: Timing diagram for Feed Forward (F.F.) Function

LOW DROPOUT REGULATOR (LDO)

IR3891 has an integrated low dropout (LDO) regulator which can provide gate drive voltage for both drivers. When using an internally biased configuration, the LDO draws from the Vin pin and provides a 5.3V (typ.), as shown in Figure 13. Vin and PVin can be connected together as shown in the internally biased single rail configuration, Figure 14.

An external bias configuration can provide gate drive voltage for the drivers instead of the internal LDO. To use an external bias, connected to Vin and VCC to the external bias, as shown in Figure 15. PVin can also be connected or a different rail can be used.

When using multiple rail configurations, calculate the compensation Vramp associated with Vin. Vramp is derived from Vin which can be different from PVin, refer to Feed-Forward section.

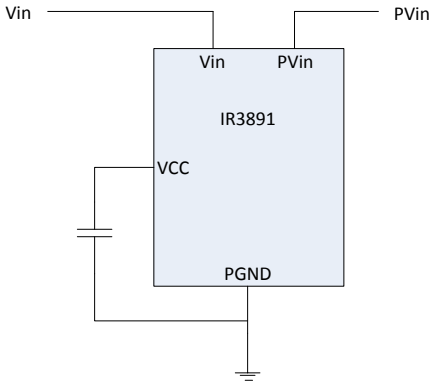

Figure 13: Internally Biased Configuration

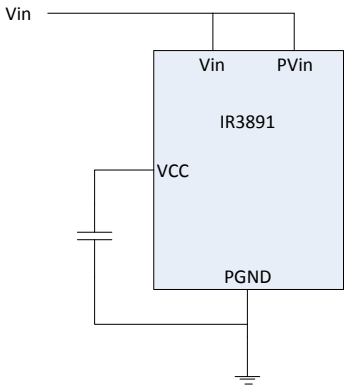

Figure 14: Internally Biased Single Rail Configuration

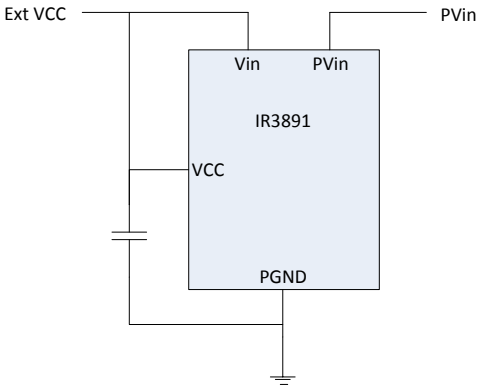

Figure 15: Externally Biased Configuration

OUTPUT VOLTAGE SEQUENCING

IR3891 can accommodate user sequencing options using Seq, EN1/2, and PGood1/2 pins. In the block diagram presented on page 3, the error-amplifier (E/A) has been depicted with three positive inputs. Ideally, the input with the lowest voltage is used for regulating the output voltage and the other two inputs are ignored. In practice the voltages of the other two inputs should be at least 200mV greater than the referenced voltage input so that their effects can completely be ignored.

In normal operating condition, the IR3891 channels initially follow their internal soft-starts (Intl_SS) and then references VREF. After Enable goes high, Intl_SS begins to ramp up from 0V. The FB pin follows the Intl_SS until it approaches VREF where the E/A starts to reference the VREF instead of the Intl_SS (refer to Figure 16). VREF and Seq are not referenced initially because they are higher than Intl_SS. VREF is 0.5V, typical. Seq is internally pulled

up to approximately 3.3V when left floating in normal operation and only used by channel 2.

In sequencing mode of operation, Vout2 is initially regulated with the Seq pin. Vout2 ramps up similar to the normal operation, but Intl_SS is replaced with Seq. Seq is kept to ground level until Intl_SS signal reaches its final value. FB2 follows Seq, until Seq approaches VREF where the E/A switches reference to the VREF. Vout2 is then regulated with respect to internal VREF (refer to Figure 17). The final Seq voltage should between 0.7V and 3.3V.

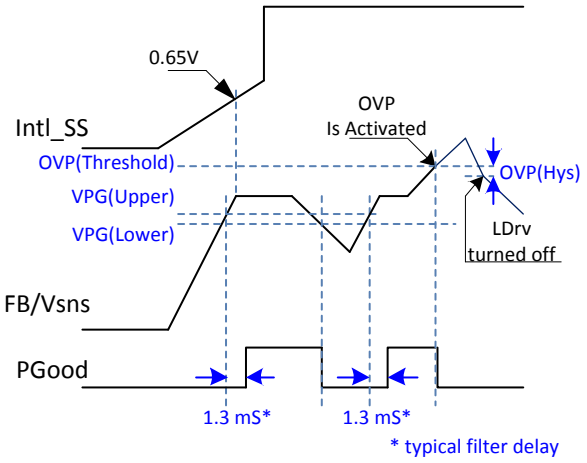

Figure 16: Timing Diagram for Output Sequence

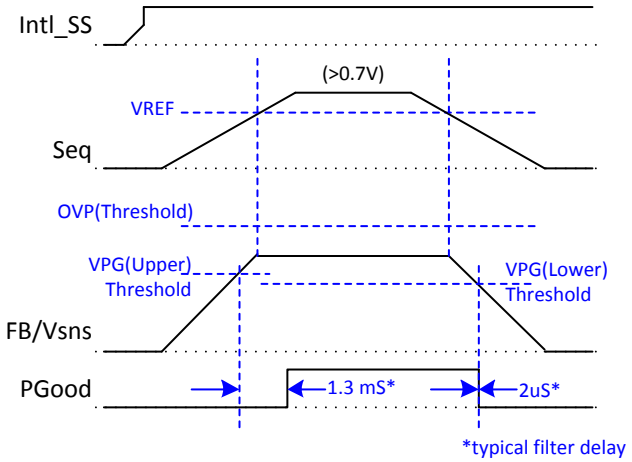

Figure 17: Timing Diagram for Sequence Startup (Seq ramping up/down)

IR3891 can perform simultaneous or ratiometric sequencing operations. Simultaneous sequencing is when the both outputs rise at the same rate. During Ratiometric sequencing, the ratio of the two outputs is held constant during power-up. Figure 19 shows examples of the two sequencing modes.

IR3891 uses a single configuration to implement both mode of sequencing operations. Figure 18 shows the typical circuit configuration for both modes of sequencing operation. The sequencing mode is determined by the R_A/R_B, R_E/R_F, and R_C/R_D ratios. If $R_E/R_F = R_C/R_D$, simultaneous startup is achieved. Vout2 follows Vout1 until the voltage at the Seq pin reaches VREF. After the voltage at the Seq pin exceeds VREF, VREF dictates Vout2. In ratiometric startup, Vout2 rises at a slower rate than Vout1. The resistor values are set up in the following way, $R_A/R_B > R_E/R_F > R_C/R_D$.

Table 2 summarizes the required conditions to achieve simultaneous or ratiometric sequencing operations.

Table 2: Required Conditions for Simultaneous / Ratiometric Tracking and Sequencing

Operating Mode	Seq	Required Condition
Normal (Non-sequencing, Non-tracking)	Floating	—
Simultaneous Sequencing	Ramp up from 0V	$R_A/R_B>R_E/R_F=R_C/R_D$
Ratiometric Sequencing	Ramp up from 0V	$R_A/R_B>R_E/R_F>R_C/R_D$

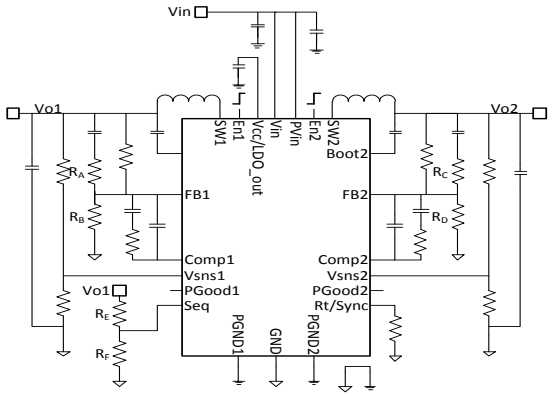

Figure 18: Application Circuit for Simultaneous and Ratiometric Sequencing

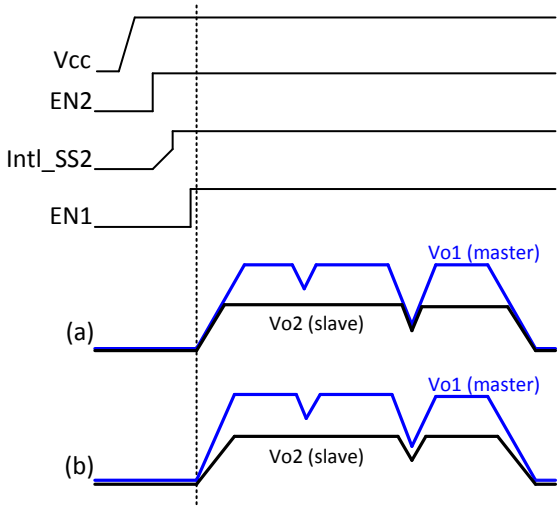

Figure 19: Typical waveforms for sequencing mode of operation: (a) simultaneous, (b) ratiometric

OVER-VOLTAGE PROTECTION (OVP)

Over-Voltage protection (OVP) disables the channel when the output voltage exceeds the over-voltage threshold. IR3891 achieves OVP by comparing Vsns pin to the internal over-voltage threshold set at OVP(threshold), 1.2*VREF typical. Vsns voltage is determined by an external voltage divider resistor network connected to the output in typical application. When Vsns exceeds the over-voltage threshold, an over-voltage is detected and OV signal asserts after OVP(delay). The high side drive signal HDrv is turned off immediately and PGood flags low. The low side drive signal is kept on until the Vsns voltage drops below the lower threshold. After that, HDrv is latched off until a reset is performed by cycling either VCC or the respective EN.

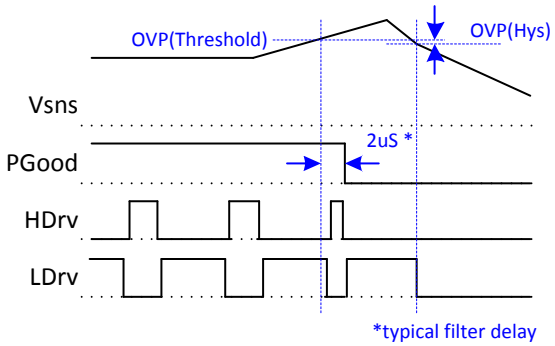

Figure 20: Timing diagram for OVP

OPEN FEEDBACK-LOOP PROTECTION

Open Feedback Loop protection (OFLP) is devised to shutdown the channel in case the feedback is broken. OFLP is activated when the Vsns is above the VPG(upper) threshold, 0.85*VREF typical, and remains active while Vsns is above the VPG(lower) threshold, 0.80*VREF. When FB drop below OFLP(threshold) threshold, 0.70*VREF, OFLP disables switching and pulls down on PGood. The part remains disabled until FB rises above OFLP(threshold) plus OFLP(Hys), 0.75*VREF. This function does not latch the part off nor does it require an EN or a VCC toggle to re-enable the part.

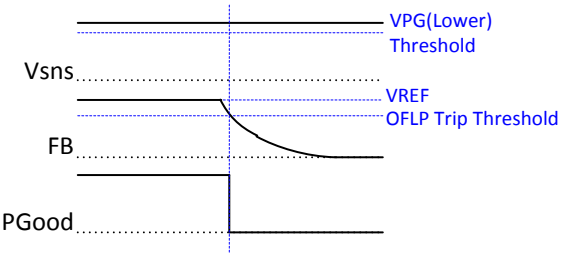

Figure 21: Timing Diagram for Open Feedback Line Protection (OFLP)

POWER GOOD OUTPUT

PGood is an open drain pin that monitors the UV, FAULT and the POR signals. PGood signal asserts approximately 1.3mS, after Vsns rises above VGP(Upper) threshold, 0.85*VREF typical, while FAULT is low and POR is high. It remains asserted while FAULT is low and POR is high and Vsns stays above VGP(Lower) threshold, 0.80*VREF typical. When Vsns falls below VGP(Lower) threshold there is a typical 2µS delay before PGood goes low. The two PGood signals are independent of each other and are set according to their respective channel.

SWITCH NODE PHASE SHIFT

The two converters on the IR3891 run interleaving phases by 180° to reduce input filter requirements. The two converters are synchronized to the user programmable oscillator. Channel 1 runs in phase with the oscillator while channel 2 runs out of phase. Staggering the switching cycles reduces the time the converters draw current from the supply simultaneously. The pulses of current drawn from the input induce voltage ripples across the input capacitor. The voltage ripple shapes are dependent on the different loading and output voltages of the two converters. By switching the converters at different times, the magnitude of voltage ripples reduces and input filter requirements become less stringent.

MINIMUM ON-TIME CONSIDERATIONS

The minimum on-time is the shortest amount of time which the Control FET may be reliably turned on. Internal delays and gate drive make up a large portion of the minimum on-time. IR3891 has a minimum on-time of 60nS.

Any design or application using IR3891 should operation with a pulse width greater than minimum on-time. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{PVin \times F_s} \quad (3)$$

In any application that uses IR3891, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on} \quad (4)$$

$$t_{on(\min)} \le \frac{V_{out}}{PV_{in} \times F_s} \quad (5)$$

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad (6)$$

The minimum output voltage is limited by the reference voltage and hence Vout(min) = 0.5V. For Vout(min) = 0.5V,

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad (7)$$

$$\therefore PV_{in} \times F_s \le \frac{0.5V}{60nS} = 8.33V/\mu S$$

Therefore, with an input voltage 16V and minimum output voltage, the converter should be designed for switching frequency not to exceed 520kHz. Conversely, the input voltage (PVin) should not exceed 5.55V for operation at the maximum recommended operating frequency (1.5MHz) and minimum output voltage (0.5V). Increasing the PVin greater than 5.55V will cause pulse skipping.

MAXIMUM DUTY RATIO

Maximum duty ratio is lower at higher frequencies and higher Vin voltages. A maximum off-time of 250nS is specified for IR3891. This provides an upper limit on the operating duty ratio at any given switching frequency. The off-time becomes a larger percentage of the switching period when high switching frequencies are used. Thus, a lower the maximum duty ratio can be achieved when frequencies increase.

Feed-Forward from the Vin voltage placed a limitation on the maximum duty cycle by saturating the compensation ramp. By maintaining a constant Vin/Vramp, the effective Vramp voltage is increased while the maximum range is remains the same. The ramp reaches the maximum limit before reaching the expected level. Reaching the maximum limit ends the switching cycle prematurely and results in a lower maximum duty cycle.

Maximum duty cycle is dependent on the Vin and switching frequency. Figure 22 is a theoretical plot of the maximum duty cycle vs. the switching frequency using typical parameter values. It shows how the maximum duty cycle is influenced by the Vin and the switching frequency.

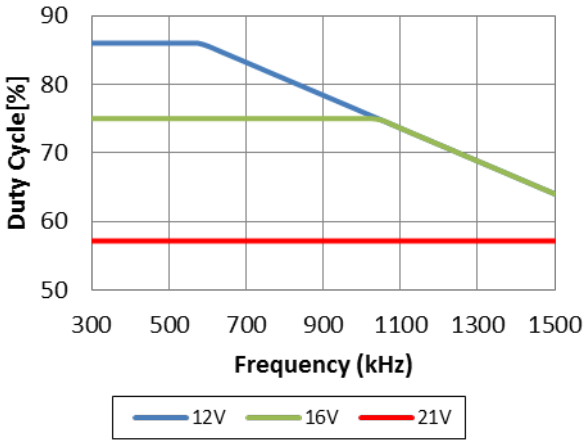

Figure 22: Maximum Duty Cycle vs. Switching Frequency

DESIGN EXAMPLE

The following example is a typical application for IR3891. The application circuit is shown in

V_{in} = PV_{in} = 12V (21V Max)
F_s = 600kHz

Channel 1:
V_o = 1.8V
I_o = 4A
Ripple Voltage = ± 1% * V_o
ΔV_o = ± 5% * Vo (for 50% load transient)

Channel 2:
V_o = 1.2V
I_o = 4A
Ripple Voltage = ± 1% * V_o
ΔV_o = ± 5% * Vo (for 50% load transient)

Enabling the IR3891

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage as shown in Figure 23.

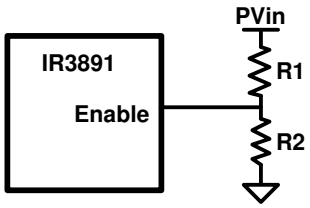

Figure 23: Using Enable pin for UVLO implementation

For a typical Enable threshold of V_{EN} = 1.2 V

$$PV_{in(\min)} \times \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2 \quad (8)$$

$$R_2 = R_1 \frac{V_{EN}}{PV_{in(\min)} - V_{EN}} \quad (9)$$

For $PV_{in\ (min)}$=9.2V, R_1=49.9K and R_2=7.5K ohm is a good choice.

Programming the frequency

For F_s = 600 kHz, select R_t = 39.2 KΩ, using Table 1.

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The FB pin is the inverting input of the error amplifier, which is internally referenced to VREF. The divider ratio is set to equal VREF at the FB pin when the output is at its desired value. When an external resistor divider is connected to the output as shown in Figure 24, the output voltage is defined by using the following equation:

$$V_o = V_{ref} \times \left(1 + \frac{R_5}{R_6}\right) \quad (10)$$

$$R_6 = R_5 \times \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad (11)$$

For the calculated values of R5 and R6, see feedback compensation section.

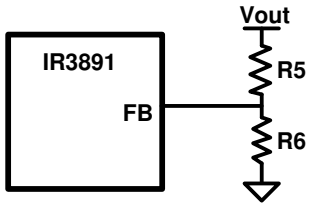

Figure 24: Typical application of the IR3891 for programming the output voltage

Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C1). The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode (Figure 25), which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C1 is approximately given as:

$$V_c \cong V_{cc} - V_D \quad (12)$$

When the control FET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage V_{in}. However, if the value of C1 is appropriately chosen, the voltage V_c across C1 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{Boot} \cong V_{in} + V_{cc} - V_D \quad (13)$$

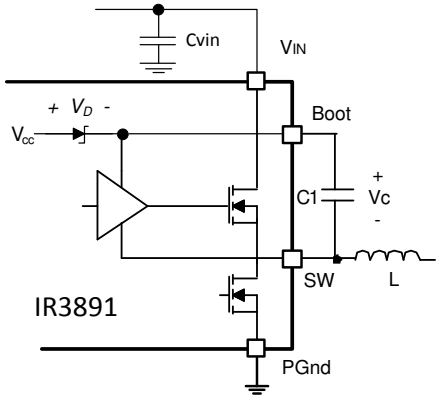

Figure 25: Bootstrap circuit to generate Vc voltage

A bootstrap capacitor of value 0.1uF is suitable for most applications.

Input Capacitor Selection

The ripple currents generated during the on time of the control FETs should be provided by the input capacitor. The RMS value of this ripple for each channel is expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1-D)} \quad (14)$$

$$D = \frac{V_o}{V_{in}} \quad (15)$$

Where:

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

For channel 1, I_o=4A and D = 0.15, the I_{RMS} = 1.43A.

For channel 2, I_o=4A and D = 0.1, the I_{RMS} = 1.2A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have 4x10uF, 25V ceramic capacitors, C3216X5R1E106K from TDK. In addition to these, although not mandatory, a 1x330uF, 25V SMD capacitor EEV-FK1E331P from Panasonic may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

Inductor Selection

Inductors are selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but may reduce efficiency and cause higher output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current. For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L \times \frac{\Delta i}{\Delta t}; \Delta t = D \times \frac{1}{F_s}$$

$$L = (V_{in} - V_o) \times \frac{V_o}{V_{in} \times \Delta i \times F_s} \quad (16)$$

Where:

V_{in} = Maximum input voltage
V_0 = Output Voltage
Δi = Inductor Peak-to-Peak Ripple Current
F_s = Switching Frequency
Δt = On time for Control FET
D = Duty Cycle

If $\Delta i \approx 20\% * I_o$, then the channel 1 output inductor is calculated to be 3.2µH. Select L=2.2µH, PCMB065T-2R2MS, from Cyntec which provides a compact, low profile inductor suitable for this application. For channel 2, the output inductor is calculated to be 2.25µH. Select L=1.5µH, PCMB065T-1R5MS, from Cyntec.

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors type and values. The criterion is normally based on the value of the

