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FEATURES

- Single 5V to 21V application
- Wide Input Voltage Range from 1.0V to 21V with external Vcc
- Output Voltage Range: 0.5V to 0.86×Vin
- Enhanced Line/Load Regulation with Feed-Forward
- Programmable Switching Frequency up to 1.5MHz
- Internal Digital Soft-Start/Soft-Stop
- Enable input with Voltage Monitoring Capability
- Thermally Compensated Current Limit with robust hiccup mode over current protection
- Smart internal LDO to improve light load and full load efficiency
- External Synchronization with Smooth Clocking
- Enhanced Pre-Bias Start-Up
- Precision Reference Voltage (0.5V+/-0.5%) with margining capability
- Vp for Tracking Applications (source/sink capability ±16A)
- Integrated MOSFET drivers and Bootstrap Diode
- Thermal Shut Down
- Programmable Power Good Output with tracking capability
- Monotonic Start-Up
- Operating temp: -40°C < Tj < 125°C
- Small Size: 5mm x 6mm PQFN
- Lead-free, Halogen-free and RoHS Compliant

DESCRIPTION

The IR3895 SupIRBuck™ is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard PWM controller and MOSFETs make IR3895 a space-efficient solution, providing accurate power delivery.

IR3895 is a versatile regulator which offers programmable of switching frequency and the fixed internal current limit while operates in wide input and output voltage range.

The switching frequency is programmable from 300kHz to 1.5MHz for an optimum solution.

It also features important protection functions, such as Pre-Bias startup, thermally compensated current limit, over voltage protection and thermal shutdown to give required system level security in the event of fault conditions.

APPLICATIONS

- Netcom Applications
- Embedded Telecom Systems
- Server Applications
- Storage Applications
- Distributed Point of Load Power Architectures

BASIC APPLICATION

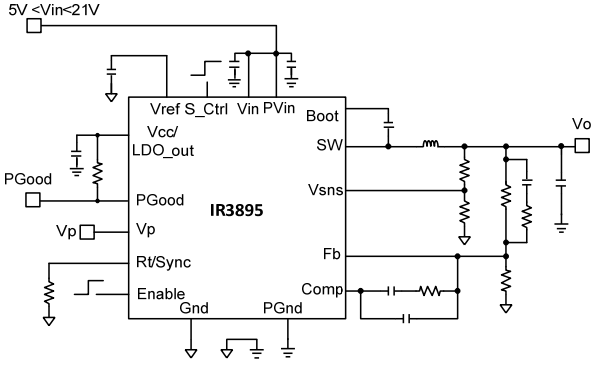


Figure 1: IR3895 Basic Application Circuit

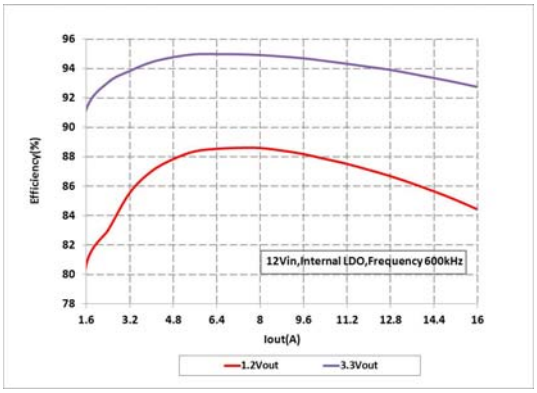
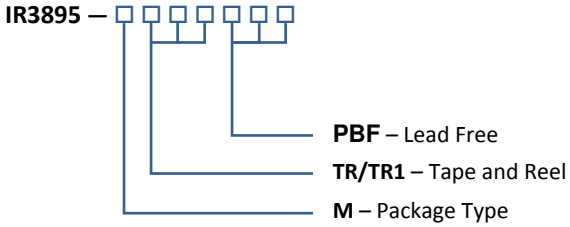


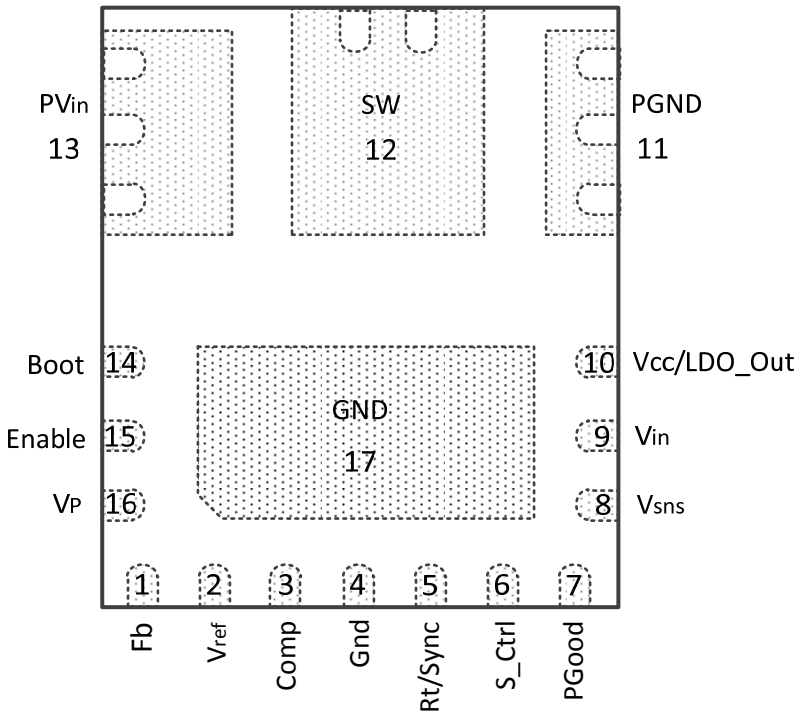
Figure 2:IR3895 Efficiency

ORDERING INFORMATION

Package	Tape & Reel Qty	Part Number
M	750	**IR3895MTR1PBF**
M	4000	**IR3895MTRPBF**



PIN DIAGRAM
5m x 6mm POWER QFN
(TOP VIEW)



$$\theta_{JA} = 30°C/W$$
$$\theta_{J\text{-}PCB} = 2°C/W$$

BLOCK DIAGRAM

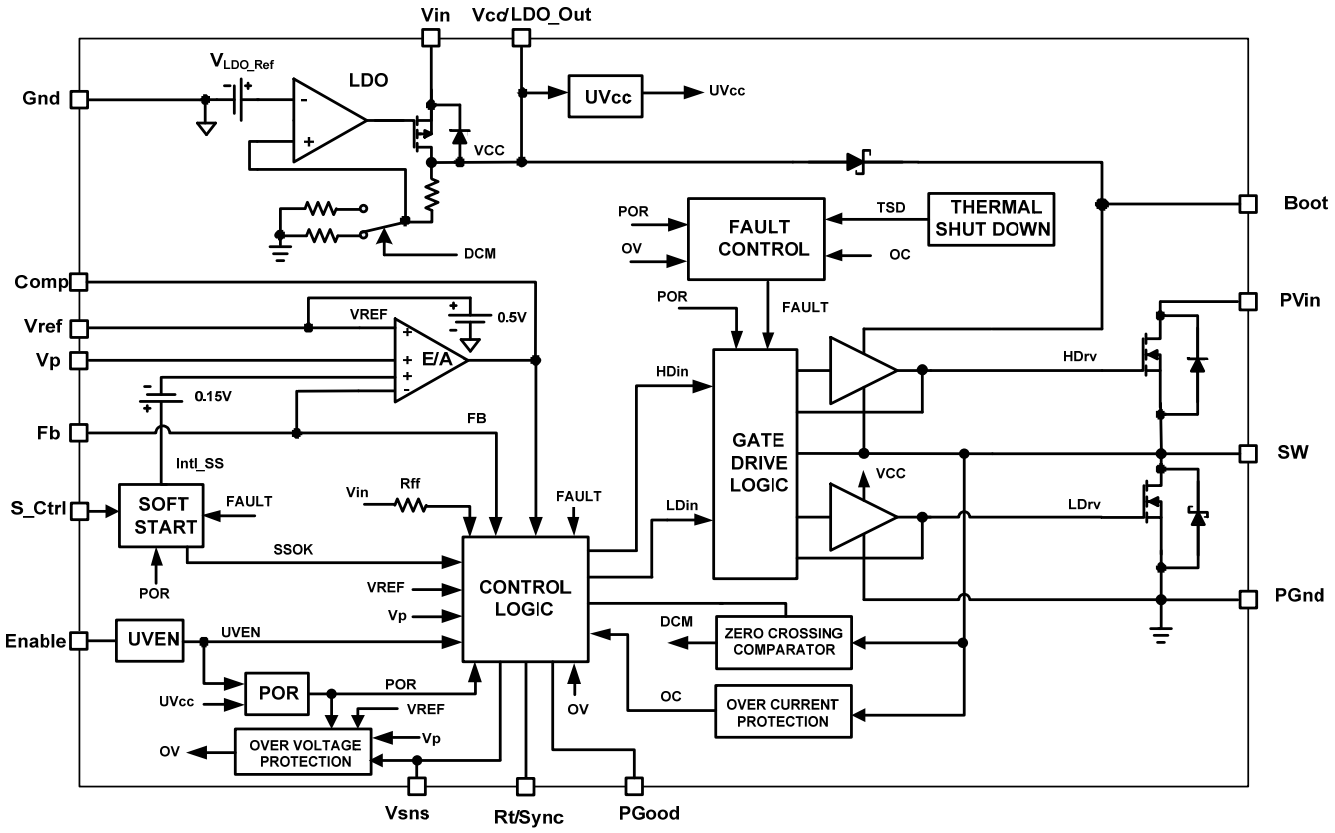


Figure 3: IR3895 Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	Vref	Internal reference voltage, it can be used for margining operation also. In normal and sequencing mode operation, a 100pF ceramic capacitor is recommended between this pin and Gnd. In tracking mode operation, Vref should be tied to Gnd.
3	Comp	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to Fb to provide loop compensation.
4	Gnd	Signal ground for internal reference and control circuitry.
5	Rt/Sync	Multi-function pin to set switching frequency. Use an external resistor from this pin to Gnd to set the free-running switching frequency. An external clock signal can be connected to this pin through a diode so that the device's switching frequency is synchronized with the external clock.
6	S_Ctrl	Soft start/stop control. A high logic input enables the device to go into the internal soft start; a low logic input enables the output soft discharged. Pull this pin to Vcc if this function is not used.
7	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to the voltage lower than or equal to the Vcc.
8	Vsns	Sense pin for over-voltage protection and PGood. It is optional to tie this pin to FB pin directly instead of using a resistor divider from Vout.
9	Vin	Input voltage for Internal LDO. A 1.0µF capacitor should be connected between this pin and PGnd. If external supply is connected to Vcc/LDO_out pin, this pin should be shorted to Vcc/LDO_out pin.
10	Vcc/LDO_Out	Input Bias for external Vcc Voltage/ output of internal LDO. Place a minimum 2.2µF cap from this pin to PGnd.
11	PGnd	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
12	SW	Switch node. This pin is connected to the output inductor.
13	PVin	Input voltage for power stage.
14	Boot	Supply voltage for high side driver, a 100nF capacitor should be connected between this pin and SW pin.
15	Enable	Enable pin to turn on and off the device, if this pin is connected to PVin pin through a resistor divider, input voltage UVLO can be implemented.
16	Vp	Input to error amplifier for tracking purposes. In the normal operation, it is left floating and no external capacitor is required. In the sequencing or the tracking mode operation, an external signal can be applied as the reference.
17	Gnd	Signal ground for internal reference and control circuitry.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin, Vin	-0.3V to 25V
Vcc/LDO_Out	-0.3V to 8V (Note 2)
Boot	-0.3V to 33V
SW	-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
Boot to SW	-0.3V to VCC + 0.3V (Note 1)
S_Ctrl, PGood	-0.3V to VCC + 0.3V (Note 1)
Other Input/Output Pins	-0.3V to +3.9V
PGnd to Gnd	-0.3V to +0.3V
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C (Note 2)
ESD Classification (HBM JESD22-A114)	2kV
Moisture Sensitivity Level	JEDEC Level 2@260°C

Note 1: Must not exceed 8V
Note 2: Vcc must not exceed 7.5V for Junction Temperature between -10°C and -40°C

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

	SYMBOL	MIN	MAX	UNITS
Input Voltage Range*	PVin	1.0	21	V
Input Voltage Range**	Vin	5	21	
Supply Voltage Range***	V_{CC}	4.5	7.5	
Supply Voltage Range	Boot to SW	4.5	7.5	
Output Voltage Range	V_O	0.5	0.86xVin	
Output Current Range	I_O	0	±16	A
Switching Frequency	F_S	300	1500	kHz
Operating Junction Temperature	T_J	-40	125	°C

*Maximum SW node voltage should not exceed 25V.

**For internally biased single rail operation. When Vin drops below 6.8V, the internal LDO enters dropout. Please refer to Smart LDO section and Over Current Protection for detailed application information.

*** Vcc/LDO_out can be connected to an external regulated supply. If so, the Vin input should be connected to Vcc/LDO_out pin.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply over, 6.8V < Vin = PVin < 21V, Vref = 0.5V in 0°C < T_J < 125°C. Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Stage						
Power Losses	P_{LOSS}	Vin = 12V, V_O = 1.2V, I_O = 16A, Fs = 600kHz, L = 0.4uH, Vcc = 6.4V (internal LDO), Note 4		3.4		W
Top Switch	$R_{ds(on)\_Top}$	VBoot - Vsw= 6.4V, I_O = 16A, T_j =25°C		9.6	13.5	mΩ
Bottom Switch	$R_{ds(on)\_Bot}$	Vcc = 6.4V, I_O = 16A, T_j =25°C		4.2	6.1	
Bootstrap Diode Forward Voltage		I(Boot) = 15mA	200	300	500	mV
SW Leakage Current	I_{SW}	SW = 0V, Enable = 0V			1	µA
		SW = 0V, Enable = high, Vp = 0V				
Dead Band Time	T_{db}	Note 4		20		ns
Supply Current						
Vin Supply Current (standby)	$I_{in(Standby)}$	EN = Low, No Switching			100	µA
Vin Supply Current (dynamic)	$I_{in(Dyn)}$	EN = High, Fs = 600kHz, Vin = PVin = 21V		20	23	mA
VCC LDO Output						
Output Voltage	V_{cc}	Vin(min) = 6.8V, Icc = 0-50mA, Cload = 2.2uF, DCM = 0	6.0	6.4	6.7	V
		Vin(min) = 6.8V, Icc = 0-50mA, Cload = 2.2uF, DCM = 1	4.0	4.4	4.85	
VCC Dropout	V_{cc_drop}	Icc=50mA,Cload=2.2uF			0.8	V
Short Circuit Current	Ishort			70		mA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Zero-crossing Comparator Delay	Tdly_zc	Note 4		256/Fs		s
Zero-crossing Comparator Offset	Vos_zc	Note 4	-4	0	4	mV
Oscillator						
Rt Voltage	Vrt			1.0		V
Frequency Range	F_s	Rt = 80.6K	270	300	330	kHz
		Rt = 39.2K	540	600	660	
		Rt = 15.0K	1350	1500	1650	
Ramp Amplitude	Vramp	Vin = 6.8V, Vin slew rate max = 1V/µs, Note 4		1.02		Vp-p
		Vin = 12V, Vin slew rate max = 1V/µs, Note 4		1.80		
		Vin = 21V, Vin slew rate max = 1V/µs, Note 4		3.15		
		Vcc=Vin=5V,For external Vcc operation, Note 4		0.75		
Ramp Offset	Ramp(os)	Note 4		0.16		V
Min Pulse Width	Tmin(ctrl)	Note 4			60	ns
Max Duty Cycle	Dmax	Fs = 300kHz, PVin = Vin = 12V	86			%
Fixed Off Time	Toff	Note 4		200	250	ns
Sync Frequency Range	Fsync		270		1650	kHz
Sync Pulse Duration	Tsync		100	200		ns
Sync Level Threshold	High		3			V
	Low				0.6	
Error Amplifier						
Input Offset Voltage	Vos_Vref	VFb – Vref, Vref = 0.5V	-1.5		+1.5	%
	Vos_Vp	VFb – Vp, Vp = 0.5V,Vref=0	-1.5		+1.5	
Input Bias Current	IFb(E/A)		-1		+1	µA
Input Bias Current	IVp(E/A)		0		+4	
Sink Current	Isink(E/A)		0.4	0.85	1.2	mA
Source Current	Isource(E/A)		4	7.5	11	mA
Slew Rate	SR	Note 4	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 4	20	30	40	MHz
DC Gain	Gain	Note 4	100	110	120	dB
Maximum output Voltage	Vmax(E/A)		1.7	2.0	2.3	V
Minimum output Voltage	Vmin(E/A)				100	mV
Common Mode input Voltage			0		1.2	V
Reference Voltage						
Feedback Voltage	Vfb	Vref and Vp pin floating		0.5		V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Accuracy		0°C < Tj < 70°C	-0.5		+0.5	%
		-40°C < Tj < 125°C, Note 3	-1.0		+1.0	
Vref Margining Voltage	Vref_marg		0.4		1.2	V
Sink Current	Isink_Vref	Vref = 0.6V	12.7	16.0	19.3	µA
Source Current	Isrc_Vref	Vref = 0.4V	12.7	16.0	19.3	
Vref Comparator Threshold	Vref_disable	Vref pin connected externally			0.15	V
	Vref_enable		0.4			
Soft Start/Stop						
Soft Start Ramp Rate	Ramp (SS_start)		0.16	0.2	0.24	mV/µs
Soft Start Ramp Rate	Ramp (SS_stop)		-0.24	-0.2	-0.16	
S_Ctrl Threshold	High		2.4			V
	Low				0.6	
Power Good						
PGood Turn on Threshold	VPG(on)	Vsns Rising, 0.4V < Vref < 1.2V	85	90	95	% Vref
		Vsns Rising, Vref < 0.1V	85	90	95	% Vp
PGood Lower Turn off Threshold	VPG(lower)	Vsns Falling, 0.4V < Vref < 1.2V	80	85	90	% Vref
		Vsns Falling, Vref < 0.1V	80	85	90	% Vp
PGood Turn on Delay	VPG(on)_Dly	Vsns Rising, see VPG(on)		1.28		ms
PGood Upper Turn off Threshold	VPG(upper)	Vsns Rising, 0.4V < Vref < 1.2V	115	120	125	% Vref
		Vsns Rising, Vref < 0.1V	115	120	125	% Vp
PGood Comparator Delay	VPG(comp)_ Dly	Vsns < VPG(lower) or Vsns > VPG(upper)	1	2	3.5	µs
PGood Voltage Low	PG(voltage)	IPgood = -5mA			0.5	V
Tracker Comparator Upper Threshold	VPG(tracker _upper)	Vp Rising, Vref < 0.1V		0.4		V
Tracker Comparator Lower Threshold	VPG(tracker _lower)	Vp Falling, Vref < 0.1V		0.3		
Tracker Comparator Delay	Tdelay(track er)	Vp Rising, Vref < 0.1V,see VPG(tracker_upper)		1.28		ms
Under-Voltage Lockout						
Vcc-Start Threshold	V_{CC}_UVLO_ Start	Vcc Rising Trip Level	4.0	4.2	4.4	V
Vcc-Stop Threshold	V_{CC}_UVLO_ Stop	Vcc Falling Trip Level	3.7	3.9	4.1	
Enable-Start-Threshold	Enable_UVL O_Start	Supply ramping up	1.14	1.2	1.26	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Enable-Stop-Threshold	Enable_UVLO_Stop	Supply ramping down	0.95	1	1.05	
Enable Leakage Current	Ien	Enable = 3.3V			1	µA
Over-Voltage Protection						
OVP Trip Threshold	OVP_Vth	Vsns Rising, 0.45V < Vref < 1.2V	115	120	125	% Vref
		Vsns Rising, Vref < 0.1V	115	120	125	% Vp
OVP Comparator Delay	OVP_Tdly		1	2	3.5	µs
Over-Current Protection						
Current Limit	I_{LIMIT}	Tj = 25°C, Vcc = 6.4V	18.0	20.5	24.4	A
Hiccup Blanking Time	Tblk_Hiccup			20.48		ms
Over-Temperature Protection						
Thermal Shutdown Threshold	Ttsd	Note 4		145		°C
Hysteresis	Ttsd_hys	Note 4		20		

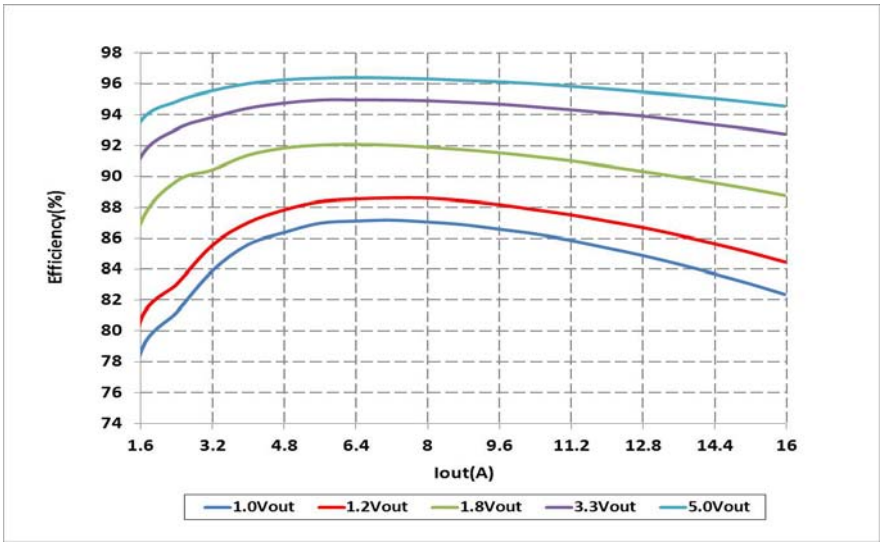
Note 3: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.
Note 4: Guaranteed by design but not tested in production.

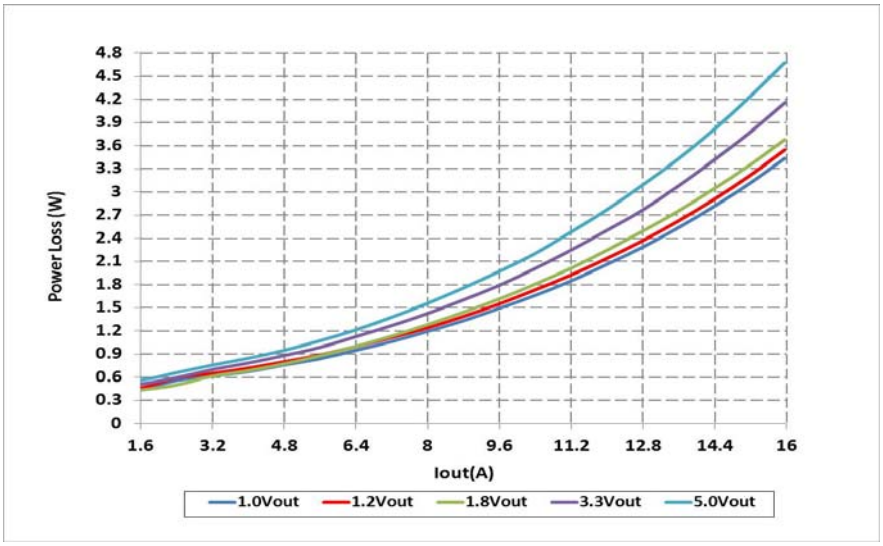
TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 12V, Vcc = Internal LDO (4.4V/6.4V), Io = 0A-16A, Fs = 600kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3895, the inductor losses and the losses of the input and output capacitors.

The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Vout(V)	Lout(µH)	P/N	DCR(mΩ)
1.0	0.4	59PR9875N (Vitec)	0.29
1.2	0.4	59PR9875N (Vitec)	0.29
1.8	0.47	7443330047(Wurth Elektronik)	0.8
3.3	0.88	MPC1040LR88C(NEC/Tokin)	2.3
5	1.0	7443330100(Wurth Elektronik)	1.35





TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 12V, Vcc = External 5V, Io = 0A-16A, Fs = 600kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3895, the inductor losses and the losses of the input and output capacitors.

The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Vout(V)	Lout(µH)	P/N	DCR(mΩ)
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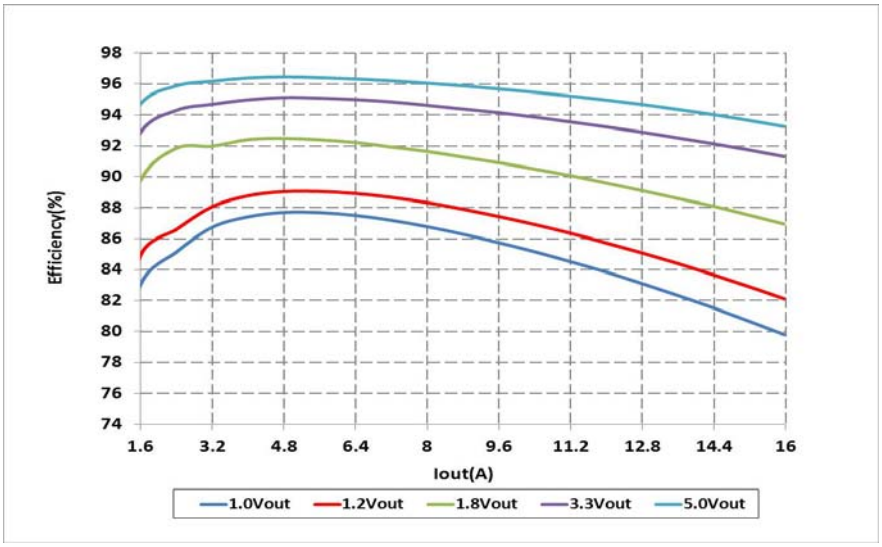
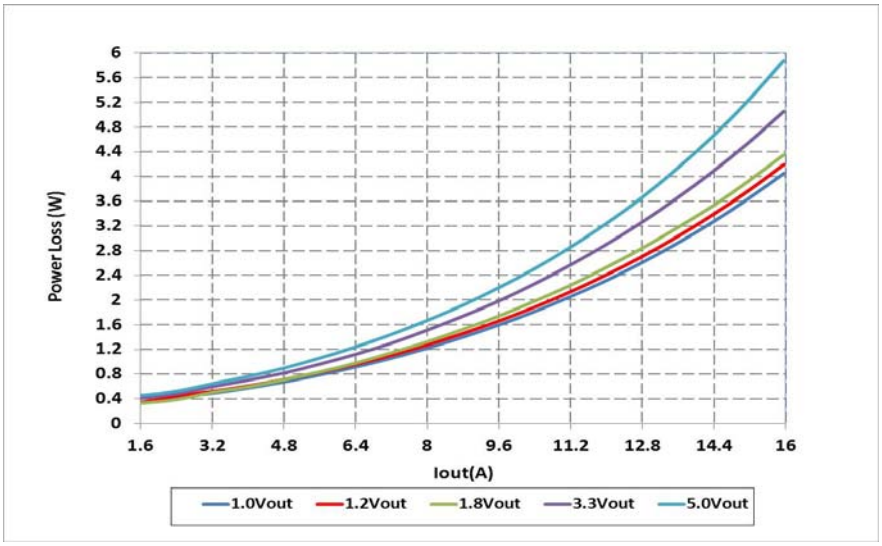
1.8	0.47	7443330047(Wurth Elektronik)	0.8
3.3	0.88	MPC1040LR88C(NEC/Tokin)	2.3
5	1.0	7443330100(Wurth Elektronik)	1.35



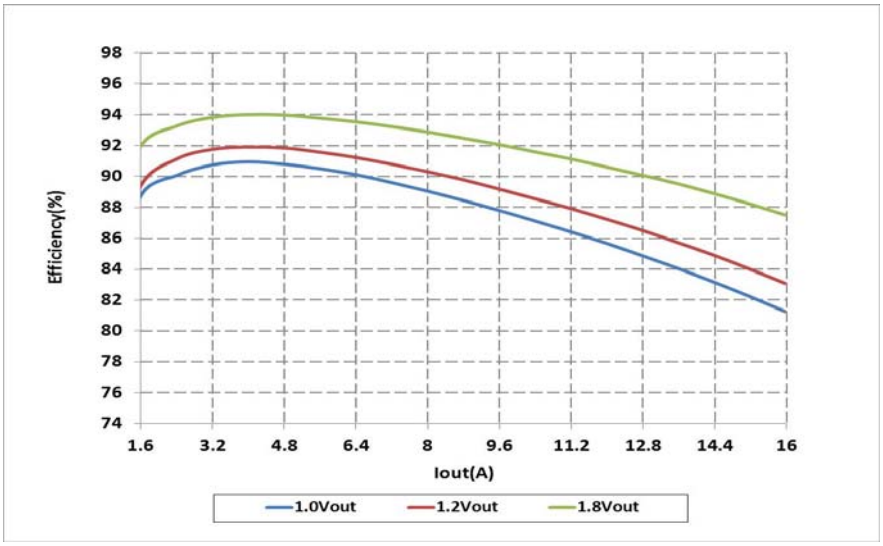


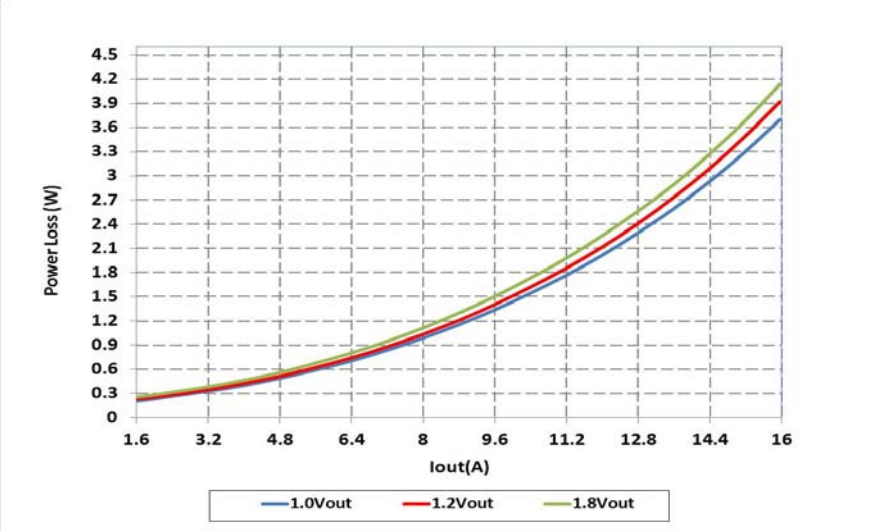
TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 5.0V, Vcc = 5.0V, Io = 0A-16A, Fs = 600kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3895, the inductor losses and the losses of the input and output capacitors.

The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Vout(V)	Lout(µH)	P/N	DCR(mΩ)
1.0	0.3	59PR9874N (Vitec)	0.29
1.2	0.3	59PR9874N (Vitec)	0.29
1.8	0.4	59PR9875N (Vitec)	0.29

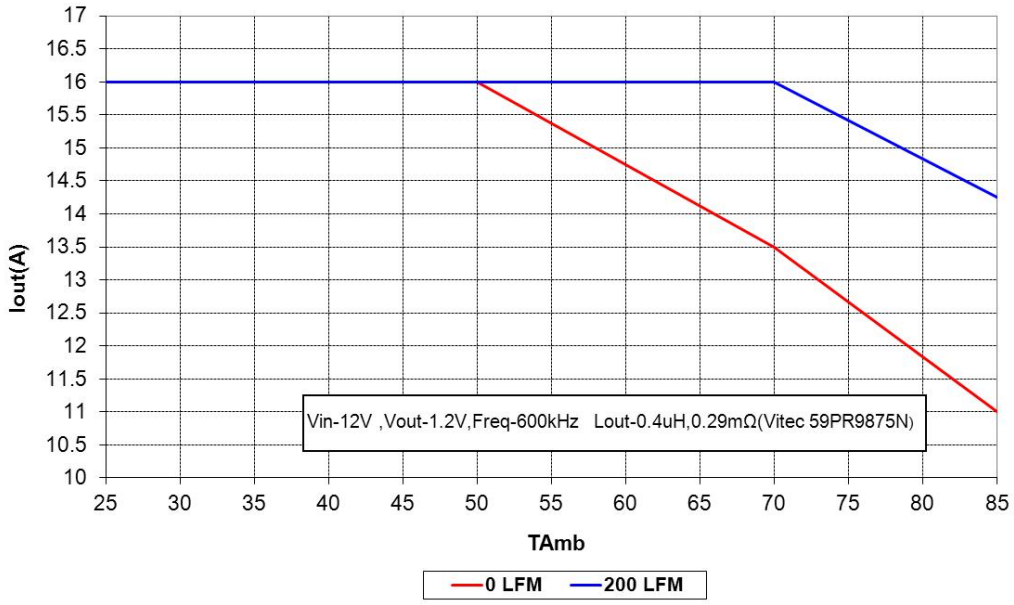




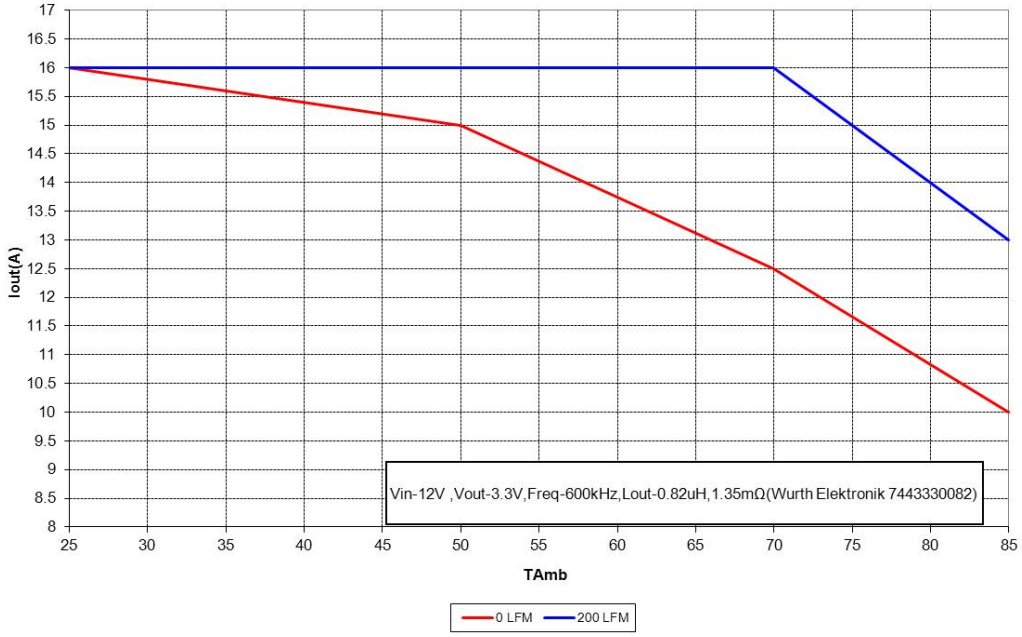
THERMAL DERATING CURVES

Measurement done on Evaluation board of IRDC3895.PCB is 4 layer board with 2 oz Copper, FR4 material, size 2.23"x2"

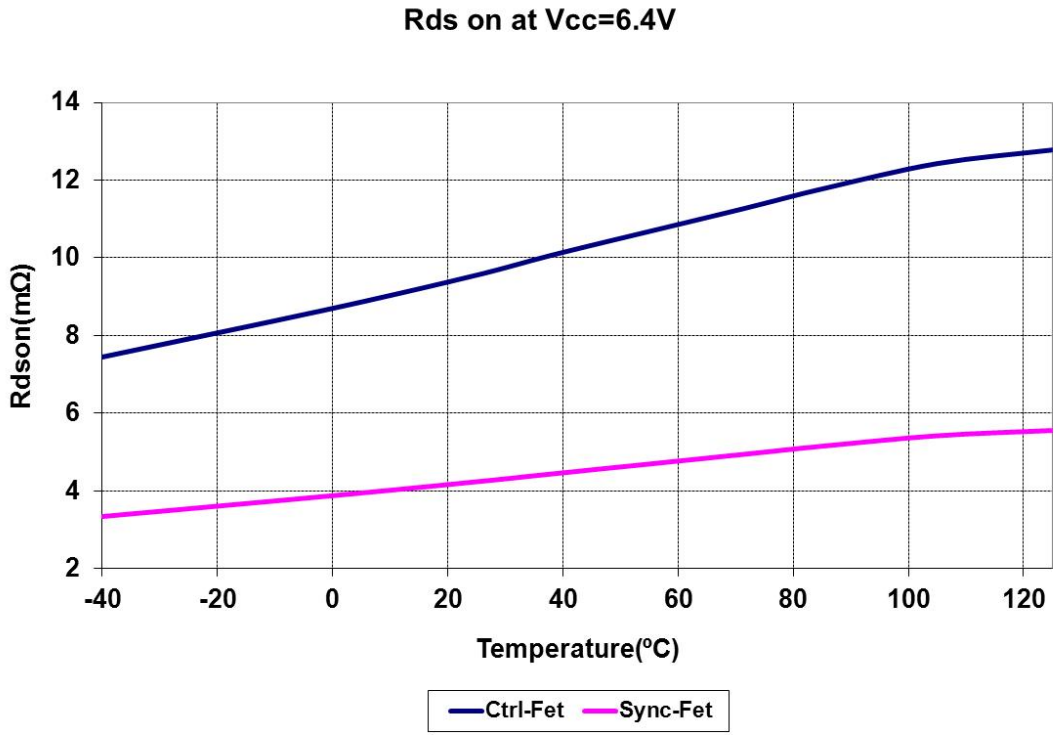
PVin = 12V, Vout=1.2V, Vcc = Internal LDO (6.4V), Fs = 600kHz



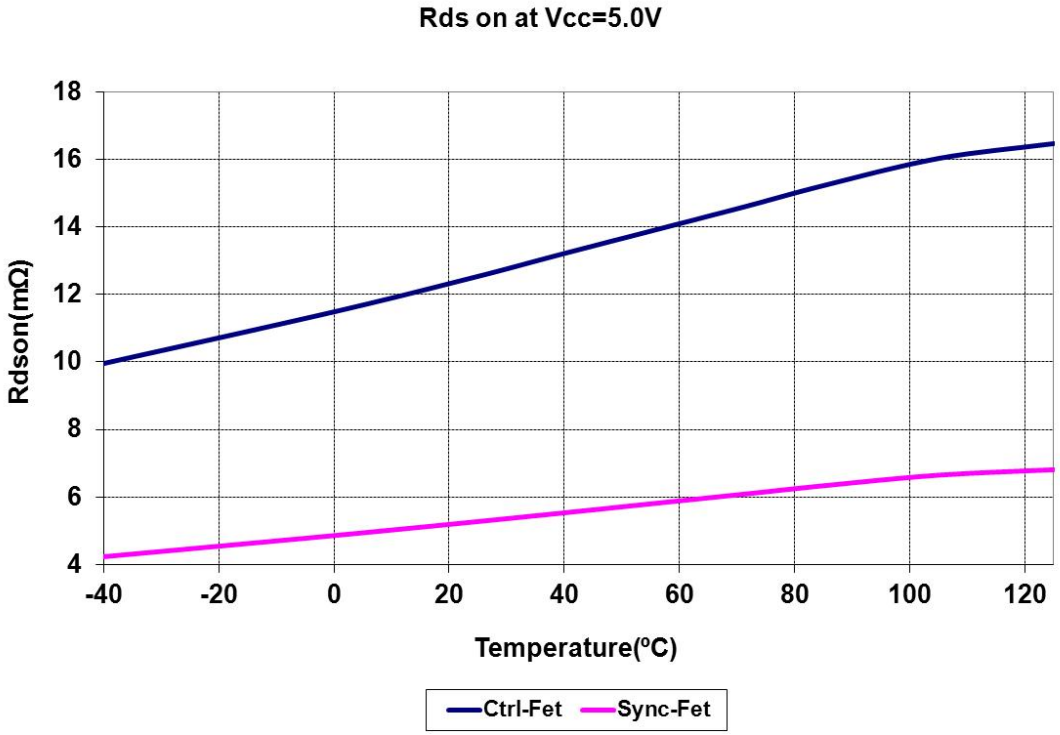
PVin = 12V, Vout=3.3V, Vcc = Internal LDO (6.4V), Fs = 600kHz



RDSON OF MOSFETS OVER TEMPERATURE AT V_{CC}=6.4V

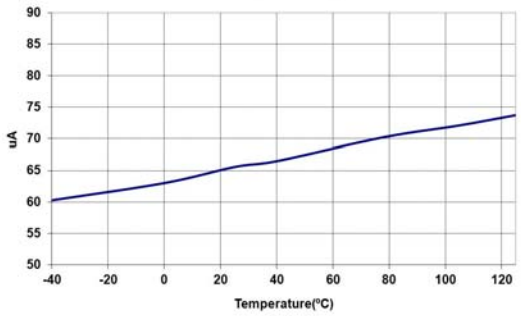


RDSON OF MOSFETS OVER TEMPERATURE AT Vcc=5.0V

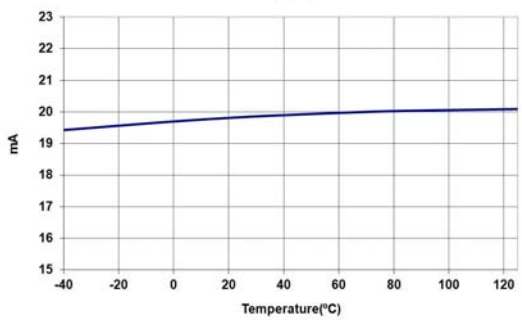


TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

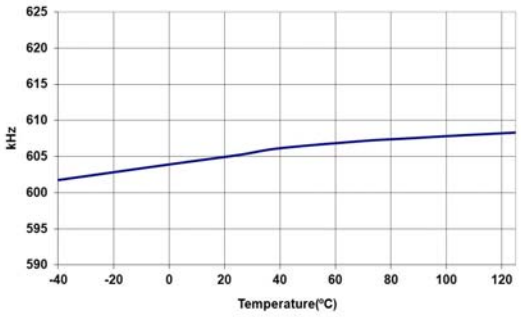
Iin (Stand by)



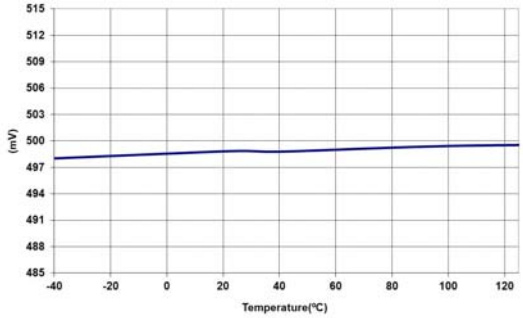
Iin (Dyn)



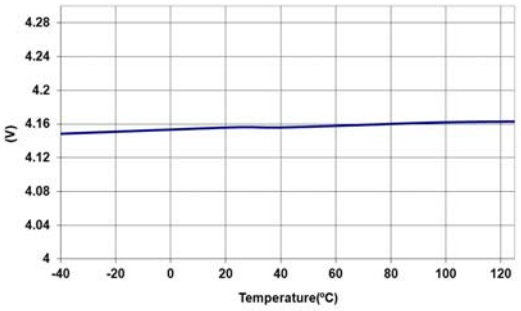
Frequency



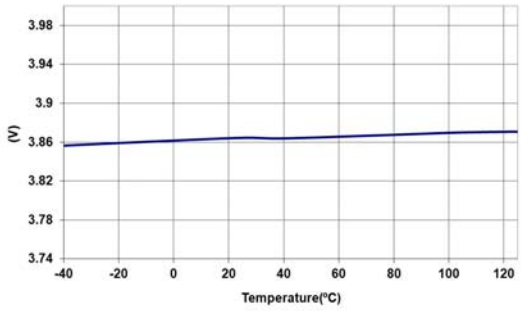
Vfb



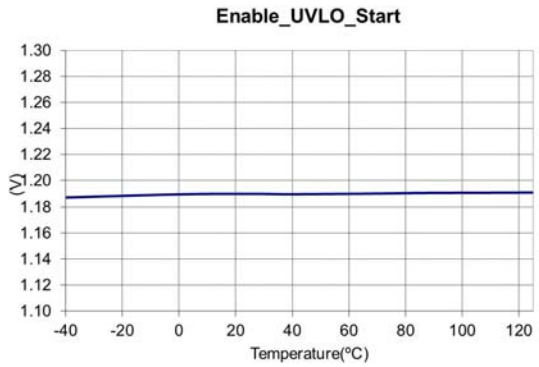
Vcc_UVLO_Start

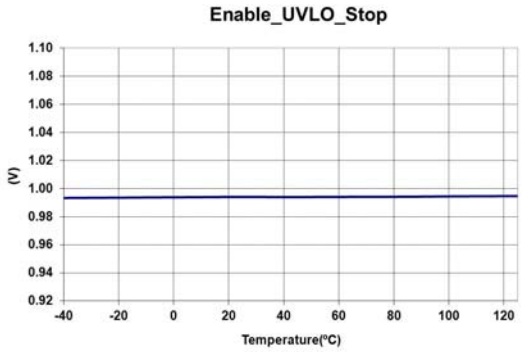


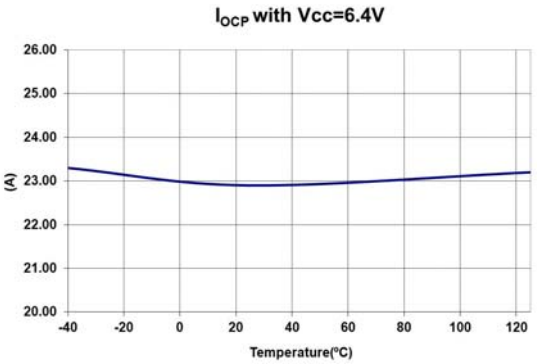
Vcc_UVLO_Stop



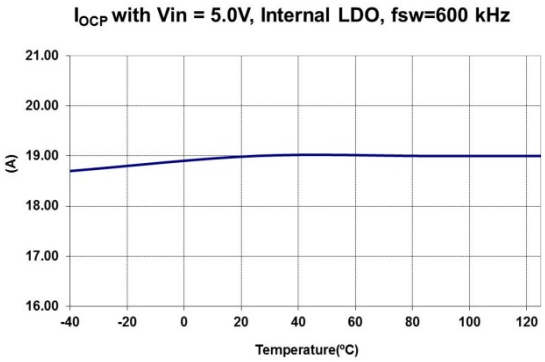
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)



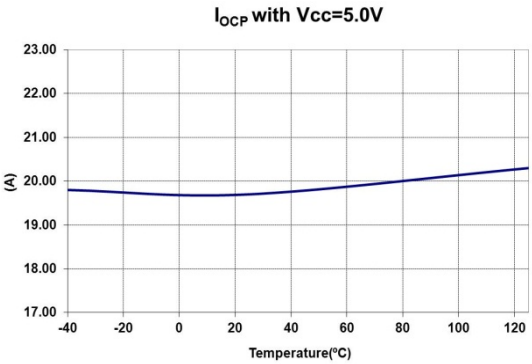




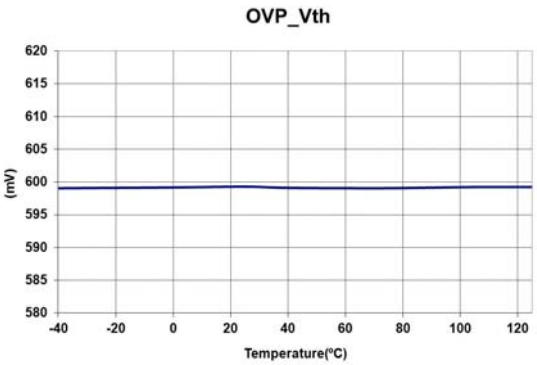
Internal LDO in regulation



Internal LDO in dropout mode

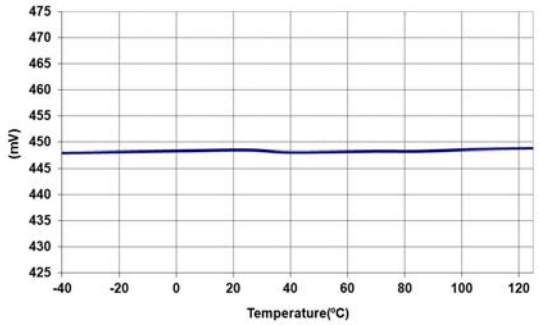


With an External 5V Vcc Voltage

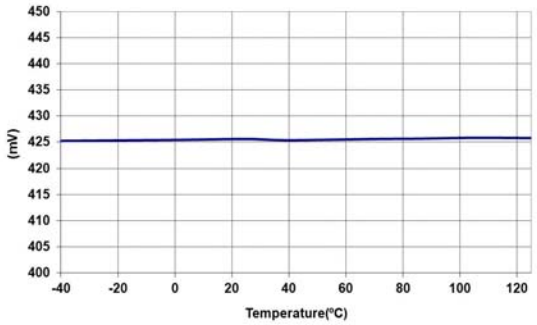


TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

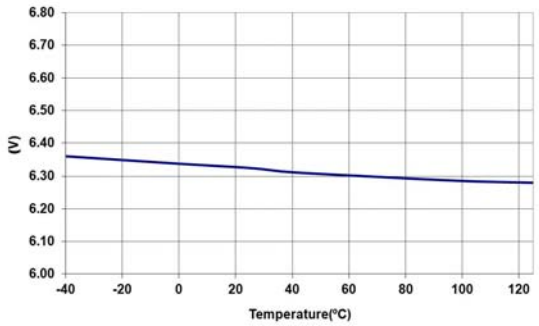
VPGon



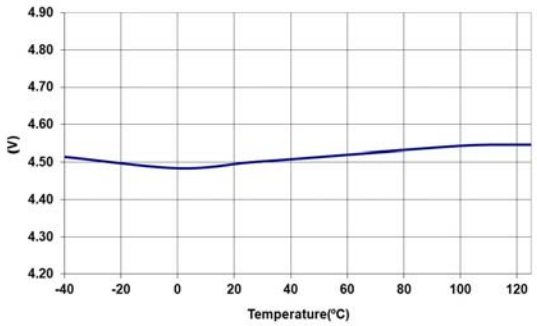
VPG(lower)



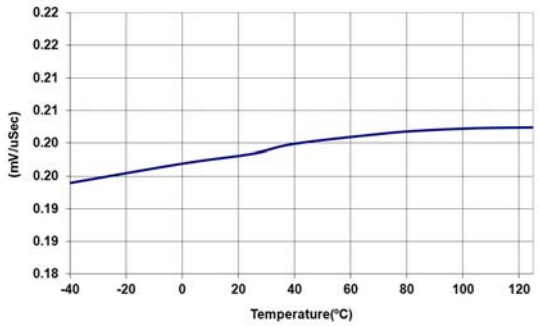
Vcc(DCM=0)



Vcc(DCM=1)



Ramp(SS_start)



THEORY OF OPERATION

DESCRIPTION

The IR3895 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 300 kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR3895 provides precisely regulated output voltage programmed via two external resistors from 0.5V to 0.86*Vin.

The IR3895 operates with an internal bias supply (LDO) which is connected to the Vcc/LDO_out pin. This allows operation with single supply. The bias voltage is variable according to load condition. If the output load current is less than half of the peak-to-peak inductor current, a lower bias voltage, 4.4V, is used as the internal gate drive voltage; otherwise, a higher voltage, 6.4V, is used. This feature helps the converter to reduce power losses. For internal biased single-rail operation, if the input voltage drops below 6.8V, the internal LDO starts to enter dropout mode.

The IC can also be operated with an external supply from 4.5 to 7.5V, allowing an extended operating input voltage (PVin) range from 1.0V to 21V. For using the internal LDO supply, the Vin pin should be connected to PVin pin. If an external supply is used, it should be connected to Vcc/LDO_Out pin and the Vin pin should be shorted to Vcc/LDO_Out pin.

The device utilizes the on-resistance of the low side MOSFET (sync FET) for over current protection. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

IR3895 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

UNDER-VOLTAGE LOCKOUT AND POR

The under-voltage lockout circuit monitors the voltage of Vcc/LDO_Out pin and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drop below the set thresholds. Normal operation resumes once Vcc/LDO_Out and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted the soft start sequence starts (see soft start section).

ENABLE

The Enable features another level of flexibility for start up. The Enable has precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3895 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3895 does not turn on until the bus voltage reaches the desired level (Fig. 4). Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold, IR3895 will be enabled. Therefore, in addition to being a logic input pin to enable the IR3895, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the IR3895 to be disabled at least until PVIN exceeds the desired output voltage level.

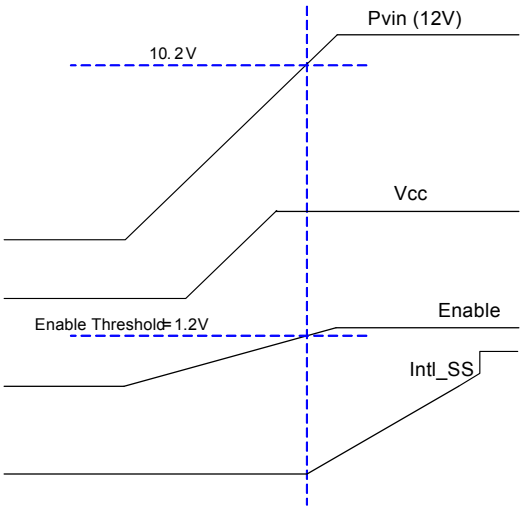


Figure 4: Normal Start up, device turns on when the bus voltage reaches 10.2V

A resistor divider is used at EN pin from PVin to turn on the device at 10.2V.

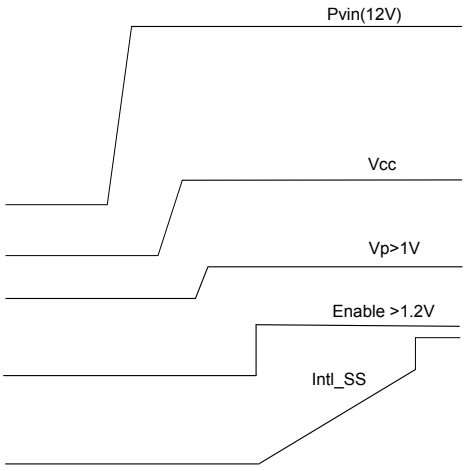


Figure 5a: Recommended startup for Normal operation

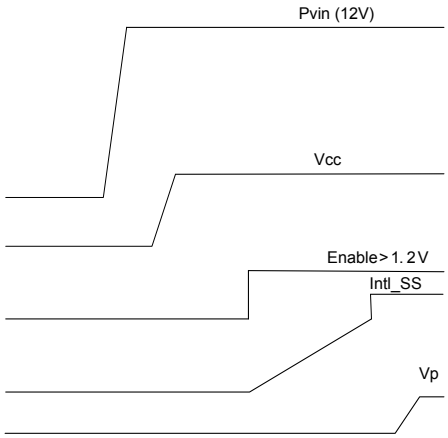


Figure 5b: Recommended startup for sequencing operation (ratiometric or simultaneous)

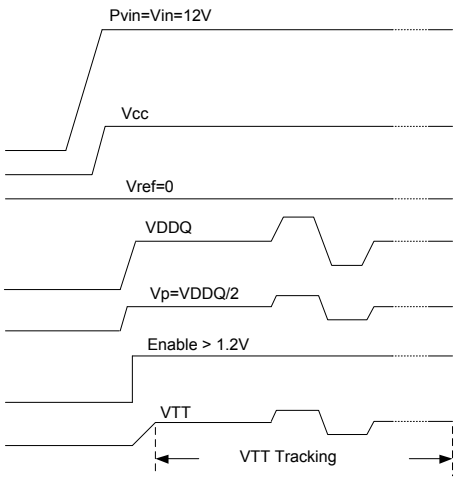


Figure 5c: Recommended startup for memory tracking operation (VTT-DDR4)

Figure 5a shows the recommended start-up sequence for the normal (non-tracking, non-sequencing) operation of IR3895, when Enable is used as a logic input. Figure 5b shows the recommended startup sequence for sequenced operation of IR3895 with Enable used as logic input. Figure 5c shows the recommended startup sequence for tracking operation of IR3895 with Enable used as logic input.

In normal and sequencing mode operation, Vref is left floating. A 100pF ceramic capacitor is recommended between this pin and Gnd. In tracking mode operation, Vref should be tied to Gnd.

It is recommended to apply the Enable signal after the VCC voltage has been established. If the Enable signal is present before VCC, a 50kΩ resistor can be used in series with the Enable pin to limit the current flowing into the Enable pin.

PRE-BIAS STARTUP

IR3895 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. Figure 6a shows a typical Pre-Bias condition at start up. The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5% until it reaches the steady state value. The number of these startup pulses for each step is 16 and it's internally programmed. Figure 6b shows the series of 16x8 startup pulses.

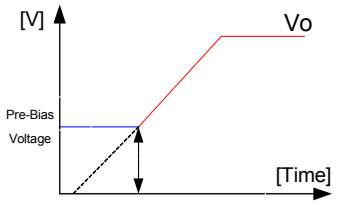


Figure 6a: Pre-Bias startup

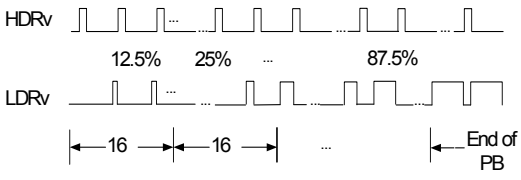


Figure 6b: Pre-Bias startup pulses

SOFT-START

IR3895 has an internal digital soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal soft-start (Intl_SS) signal linearly rises with the rate of 0.2mV/µs from 0V to 1.5V. Figure 7 shows the waveforms during soft start (also refer to Fig. 20). The normal Vout start up time is fixed, and is equal to:

$$T_{start} = \frac{(0.65\text{V}-0.15\text{V})}{0.2\text{mV}/\mu\text{s}} = 2.5\text{ms} \qquad (1)$$

During the soft start the over-current protection (OCP) and over-voltage protection (OVP) is enabled to protect the device for any short circuit or over voltage condition.

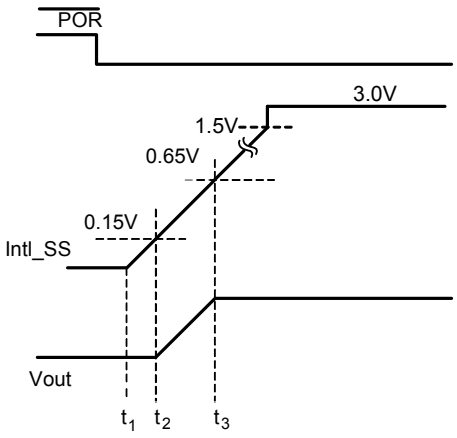


Figure 7: Theoretical operation waveforms during soft-start (non tracking / non sequencing)

OPERATING FREQUENCY

The switching frequency can be programmed between 300 kHz – 1500 kHz by connecting an external resistor from R_t pin to Gnd. Table 1 tabulates the oscillator frequency versus R_t.

SHUTDOWN

IR3895 can be shutdown by pulling the Enable pin below its 1.0V threshold. This will tri-state both the high side and the low side driver.

TABLE 1: SWITCHING FREQUENCY (FS) VS. EXTERNAL RESISTOR (R_T)

Rt (KΩ)	Freq (kHz)
80.6	300
60.4	400
48.7	500
39.2	600
34	700
29.4	800
26.1	900
23.2	1000
21	1100
19.1	1200
17.4	1300
16.2	1400
15	1500

OVER CURRENT PROTECTION

The over current (OC) protection is performed by sensing current through the $R_{DS(on)}$ of the Synchronous Mosfet. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any layout related noise issues. The current limit is pre-set internally and is compensated according to the IC temperature. So at different ambient temperature, the over-current trip threshold remains almost constant.

Note that the over current limit is a function of the Vcc voltage. Refer to the typical performance curves of the OCP current limit with the internal LDO and the external Vcc voltage. Detailed operation of OCP is explained as follows.

Over Current Protection circuit senses the inductor current flowing through the Synchronous Mosfet closer to the valley point. OCP circuit samples this current for 40nsec typically after the rising edge of the PWM set pulse which has a width of 12.5% of the switching period.The PWM pulse starts at the falling edge of the PWM set pulse. This makes valley current sense more robust as current is sensed close to the bottom of the inductor downward slope where transient and switching noise are lower and helps to prevent false tripping due to noise and transient. An OC condition is detected if the load current exceeds the threshold, the converter enters into hiccup mode. PGood will go low and the internal soft start signal will be pulled low. The converter goes into hiccup mode with a 20.48ms (typ.) delay as shown in Figure 8. The convertor stays in this mode until the over load or short circuit is removed. The actual DC output current limit point will be greater than the valley point by an amount equal to approximately

half of peak to peak inductor ripple current. The current limit point will be a function of the inductor value, input voltage, output voltage and the frequency of operation.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta I}{2} \quad (2)$$

I_{OCP}= DC current limit hiccup point
I_{LIMIT}= Current limit Valley Point
ΔI=Inductor ripple current

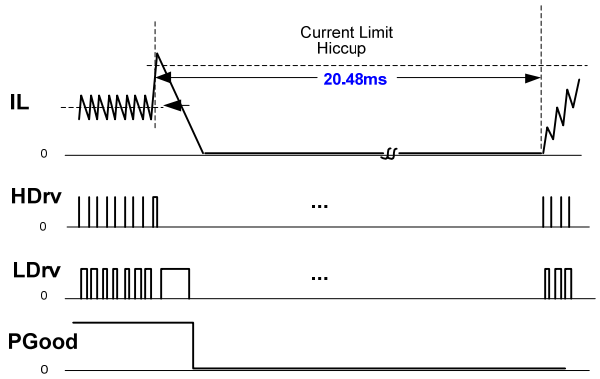


Figure 8: Timing Diagram for Current Limit Hiccup

THERMAL SHUTDOWN

Temperature sensing is provided inside IR3895. The trip threshold is typically set to 145°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and resets the internal soft start.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

EXTERNAL SYNCHRONIZATION

IR3895 incorporates an internal phase lock loop (PLL) circuit which enables synchronization of the internal oscillator to an external clock. This function is important to avoid sub-harmonic oscillations due to beat frequency for embedded systems when multiple point-of-load (POL) regulators are used. A multi-function pin, Rt/Sync, is used to connect the external clock. If the external clock is present before the converter turns on, Rt/Sync pin can be connected to the external clock signal solely and no other resistor is needed. If the external clock is applied after the converter turns on, or the converter switching frequency needs to toggle between the external clock frequency and the internal free-running frequency, an external resistor from Rt/Sync pin to Gnd is required to set the free-running frequency.

When an external clock is applied to Rt/Sync pin after the converter runs in steady state with its free-running frequency, a transition from the free-running frequency to the external clock frequency will happen. This transition is to gradually make the actual switching frequency equal to the external clock frequency, no matter which one is higher. On the contrary, when the external clock signal is removed from Rt/Sync pin, the switching frequency is also changed to free-running gradually. In order to minimize the impact from these transitions to output voltage, a diode is recommended to add between the external clock and Rt/Sync pin, as shown in Fig9a. Figure 9b shows the timing diagram of these transitions.

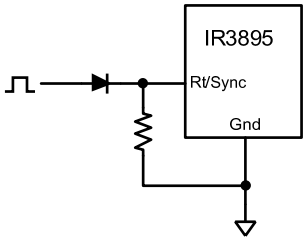


Figure 9a: Configuration of External Synchronization

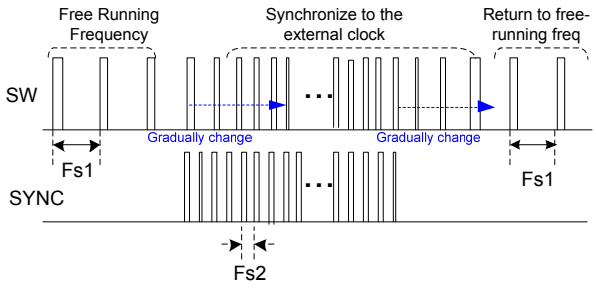


Figure 9: Timing Diagram for Synchronization to the external clock (Fs1>Fs2 or Fs1<Fs2)

An internal circuit is used to change the PWM ramp slope according to the clock frequency applied on Rt/Sync pin. Even though the frequency of the external synchronization clock can vary in a wide range, the PLL circuit will make sure that the ramp amplitude is kept constant, requiring no adjustment of the loop compensation. Vin variation also affects the ramp amplitude, which will be discussed separately in Feed-Forward section.

Feed-Forward

Feed-Forward (F.F.) is an important feature, because it can keep the converter stable and preserve its load transient performance when Vin varies in a large range. In IR3895, F.F. function is enabled when Vin pin is connected to PVin pin. In this case, the internal low dropout (LDO) regulator is used. The PWM ramp amplitude (Vramp) is proportionally changed with Vin to maintain Vin/Vramp almost constant throughout Vin variation range (as shown in Fig. 10). Thus, the control loop bandwidth and phase margin can be maintained constant. Feed-forward function can also minimize impact on output voltage from fast Vin change. The maximum Vin slew rate is within 1V/µs.

If an external bias voltage is used as Vcc, Vin pin should be connected to Vcc/LDO_out pin instead of PVin pin. Then the F.F. function is disabled. A re-calculation of control loop parameters is needed for re-compensation.

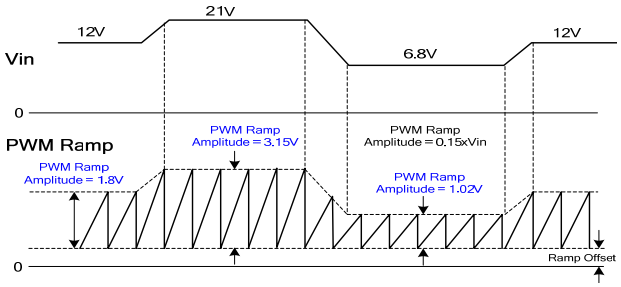


Figure 10: Timing Diagram for Feed-Forward (F.F.) Function

SMART LOW DROPOUT REGULATOR (LDO)

IR3895 has an integrated low dropout (LDO) regulator which can provide gate drive voltage for both drivers. In order to improve overall efficiency over the whole load range, LDO voltage is set to 6.4V (typical.) at mid- or heavy load condition to reduce Rds(on) and thus MOSFET conduction loss; and it is reduced to 4.4 (typical.) at light load condition to reduce gate drive loss.

The smart LDO can select its output voltage according to the load condition by sensing switch node (SW) voltage. At light load condition when part of the inductor current flows in the reverse direction (DCM=1), $V_{SW} > 0$ on LDrv falling edge in a switching cycle. If this case happens for consecutive 256 switching cycles, the smart LDO reduces its output to 4.4V. If in any one of the 256 cycles, Vsw < 0 on LDrv falling edge, the counter is reset and LDO voltage doesn't change. On the other hand, if Vsw < 0 on LDrv falling edge (DCM=0) , LDO output is increased to 6.4V. A hysteresis band is added to Vsw comparison to avoid chattering. Figure 11a shows the timing diagram. Whenever device turns on, LDO always starts with 6.4V, and then goes to 4.4V/6.4V depending upon the load condition. For internally biased single rail operation, Vin pin should be connected to PVin pin, as shown in Figure 11b. If external bias voltage is used, Vin pin should be connected to Vcc/LDO_Out pin, as shown in Figure 11c.

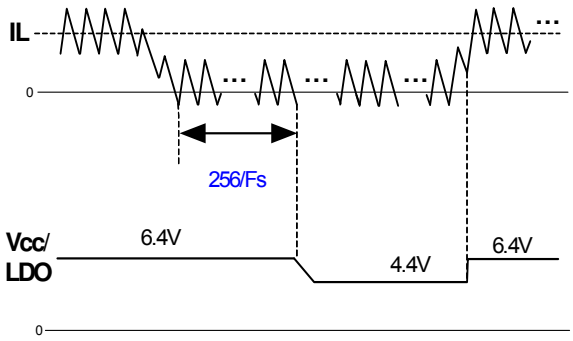


Figure 11a: Time Diagram for Smart LDO

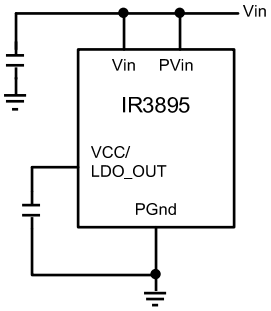


Figure 11b: Internally Biased Single Rail Operation

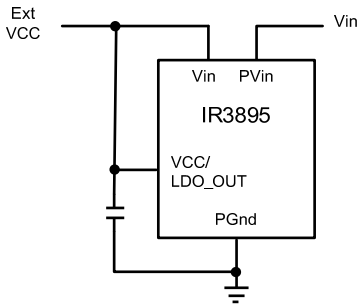


Figure 11c: Use External Bias Voltage

When the Vin voltage is below 6.8V, the internal LDO enters the dropout mode at medium and heavy load. The dropout voltage increases with the switching frequency. Figure 11d shows the LDO voltage for 600 kHz and 1000 kHz switching frequency respectively.

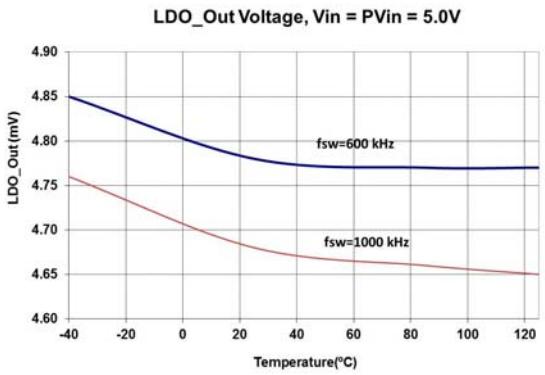


Figure 11d: LDO_Out Voltage in dropout mode

OUTPUT VOLTAGE TRACKING AND SEQUENCING

IR3895 can accommodate user programmable tracking and/or sequencing options using Vp, Vref, Enable, and Power Good pins. In the block diagram presented on page 3, the error-amplifier (E/A) has been depicted with three positive inputs. Ideally, the input with the lowest voltage is used for regulating the output voltage and the other two inputs are ignored. In practice the voltage of the other two inputs should be about 200mV greater than the low-voltage input so that their effects can completely be ignored. Vp is internally biased to 3.3V via a high impedance path. For normal operation, Vp and Vref is left floating (Vref should have a bypass capacitor).

Therefore, in normal operating condition, after Enable goes high, the internal soft-start (Intl_SS) ramps up the output voltage until Vfb (voltage of feedback/Fb pin) reaches about 0.5V. Then Vref takes over and the output voltage is regulated.

Tracking-mode operation is achieved by connecting Vref to GND. In tracking-mode, Vfb always follows Vp, which means Vout is always proportional to Vp voltage (typical for DDR/VTT rail applications). The effective Vp variation range is 0V~1.2V. Fig. 5c illustrates the start-up of VTT tracking for DDR4 application. Vp is proportional to VDDQ. After Vp is established, asserting Enable initiates the internal soft-start. VTT, which is the output of POL, starts to ramp up and tracks Vp.

In sequencing mode of operation (simultaneous or ratiometric), Vref is left floating and Vp is kept to ground level until Intl_SS signal reaches the final value. Then Vp is ramped up and Vfb follows Vp. When Vp>0.5V the error-amplifier switches to Vref and the output voltage is regulated with Vref.The final Vp voltage after sequencing startup should between 0.7V ~ 3.3V.

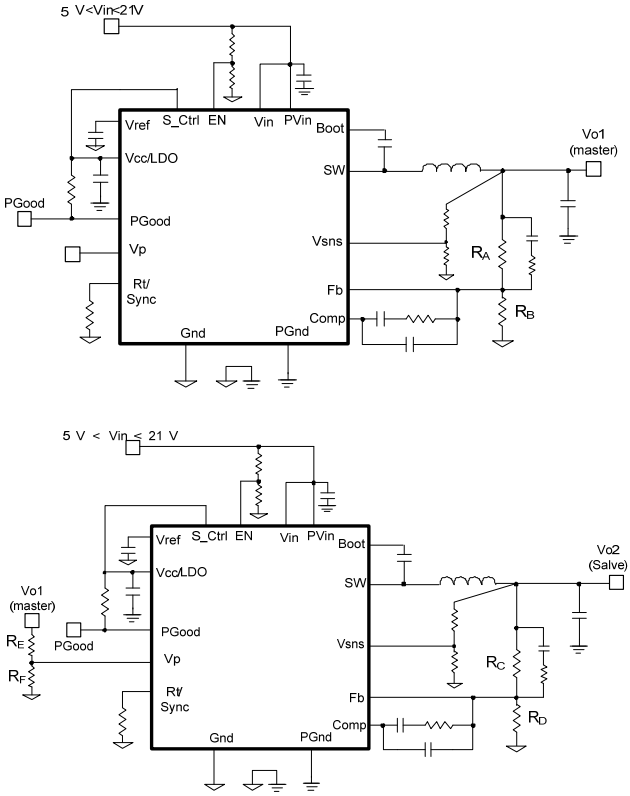


Figure 12: Application Circuit for Simultaneous and Ratiometric Sequencing

Tracking and sequencing operations can be implemented to be simultaneous or ratiometric (refer to Fig. 13 and 14). Figure 12 shows typical circuit configuration for sequencing operation. With this power-up configuration, the voltage at the Vp pin of the slave reaches 0.5V before the Fb pin of the master. If $\mathbf{R_E/R_F = R_C/R_D}$, simultaneous startup is achieved. That is, the output voltage of the slave follows that of the master until the voltage at the Vp pin of the slave reaches 0.5 V. After the voltage at the Vp pin of the slave exceeds 0.5V, the internal 0.5V reference of the slave dictates its output voltage. In reality the regulation gradually shifts from Vp to internal Vref. The circuit shown in Fig. 12 can also be used for simultaneous or ratiometric tracking operation if Vref of the slave is connected to GND. Table 2 summarizes the required conditions to achieve simultaneous/ratiometric tracking or sequencing operations.

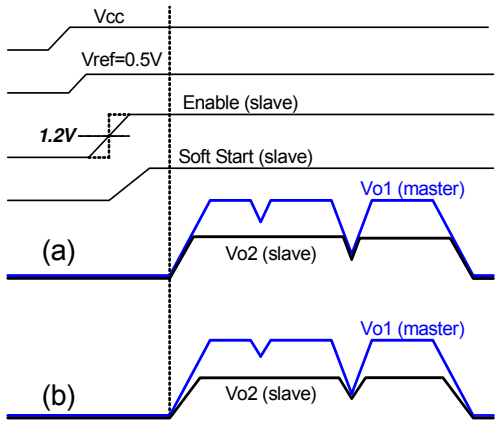


Figure 13: Typical waveforms for sequencing mode of operation: (a) simultaneous, (b) ratiometric

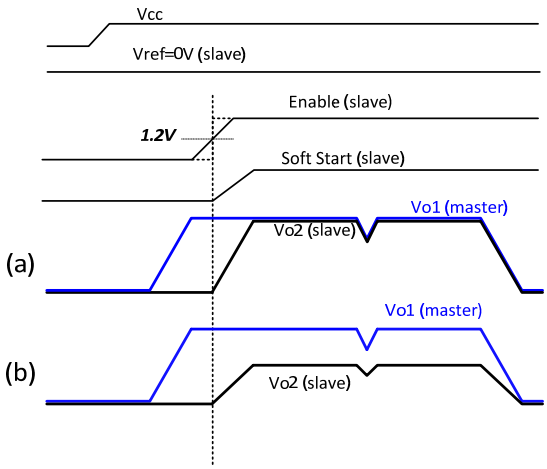


Figure 14: Typical waveforms in tracking mode of operation: (a) simultaneous, (b) ratiometric

TABLE 2: REQUIRED CONDITIONS FOR SIMULTANEOUS/RATIOMETRIC TRACKING AND SEQUENCING (FIG. 12)

Operating Mode	Vref (Slave)	Vp	Required Condition
Normal (Non-sequencing, Non-tracking)	0.5V (Floating)	Floating	—
Simultaneous Sequencing	0.5V	Ramp up from 0V	$R_A/R_B>R_E/R_F=R_C/R_D$
Ratiometric Sequencing	0.5V	Ramp up from 0V	$R_A/R_B>R_E/R_F>R_C/R_D$
Simultaneous Tracking	0V	Ramp up before En	$R_E/R_F=R_C/R_D$
Ratiometric Tracking	0V	Ramp up before En	$R_E/R_F>R_C/R_D$

VREF

This pin reflects the internal reference voltage which is used by the error amplifier to set the output voltage. In most operating conditions this pin is only connected to an external bypass capacitor and it is left floating. A 100pF ceramic capacitor is recommended for the bypass capacitor. To keep stand by current to minimum, Vref is not allowed come up until EN starts going high. In tracking mode this pin should be pulled to GND. For margining applications, an external voltage source is connected to Vref pin and overrides the internal reference voltage. The external voltage source should have a low internal resistance (<100Ω) and be able to source and sink more than 25µA.

POWER GOOD OUTPUT (TRACKING, SEQUENCING, VREF MARGINING)

IR3895 continually monitors the output voltage via the sense pin (Vsns) voltage. The Vsns voltage is an input to the window comparator with upper and lower threshold of 0.6V and 0.45V respectively. PGood signal is high whenever Vsns voltage is within the PGood comparator window thresholds. The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation.

The threshold is set differently at different operating modes and the results of the comparison sets the PGood signal. Figures 15, 16, and 17 show the timing diagram of the PGood signal at different operating modes. Vsns signal is also used by OVP comparator for detecting output over voltage condition.

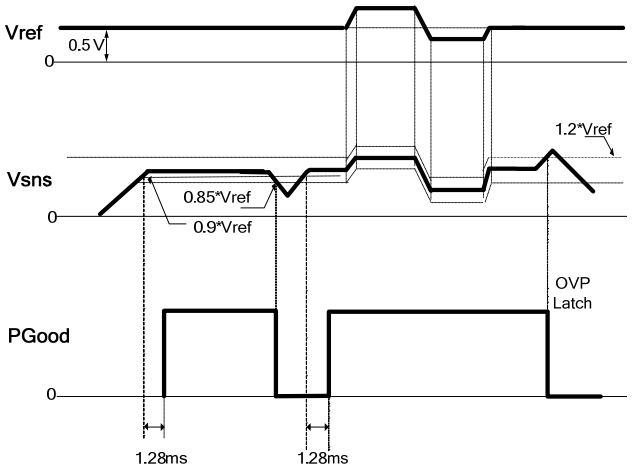


Figure 15: Non-sequence, Non-tracking Startup and Vref Margin (Vp pin floating)

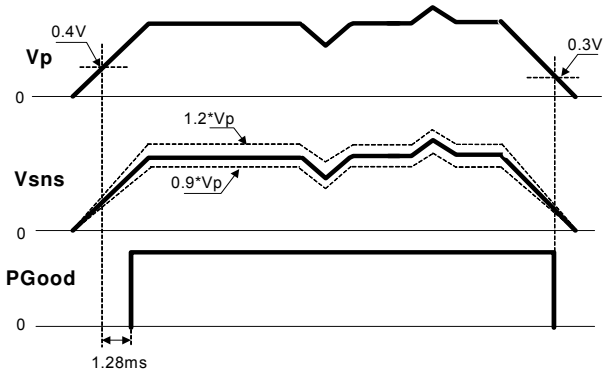


Figure 16: Vp Tracking (Vref =0V)

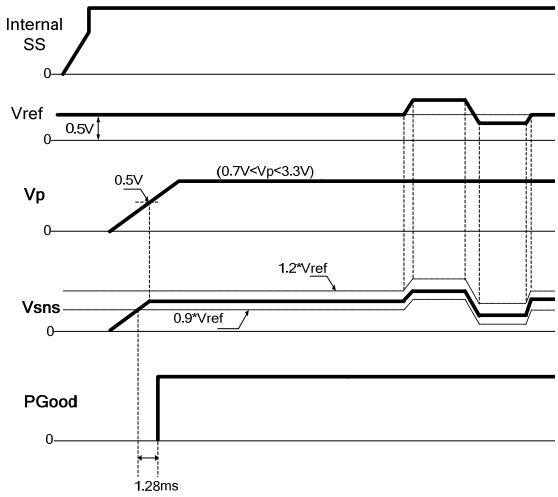


Figure 17: Vp Sequence and Vref Margin

OVER-VOLTAGE PROTECTION (OVP)

OVP is achieved by comparing Vsns voltage to an OVP threshold voltage. In non-tracking mode, OVP threshold voltage is 1.2×Vref; in tracking mode, it is set at 1.2×Vp. When Vsns exceeds the OVP threshold, an over voltage trip signal asserts after 2us (typ.) delay. Then the control FET is latched off immediately, PGood flags low. The sync FET remains on to discharge the output capacitor. When the Vsns voltage drops below the threshold, the sync FET turns off to prevent the complete depletion of the output capacitor. The control FET remains latched off until user cycle either Vcc or Enable.

OVP comparator becomes active only when the device is enabled. Furthermore, for OVP to be active Vref has to exceed 0.2V in non-tracking mode, or Vp has to exceed the threshold in tracking-mode, as illustrated in Fig 18a and Fig 18b. If either of the above conditions is not satisfied, OVP is disabled. Vsns voltage is set by the voltage divider connected to the output and it can be programmed externally. Figure 18c shows the timing diagram for OVP in non-tracking mode.

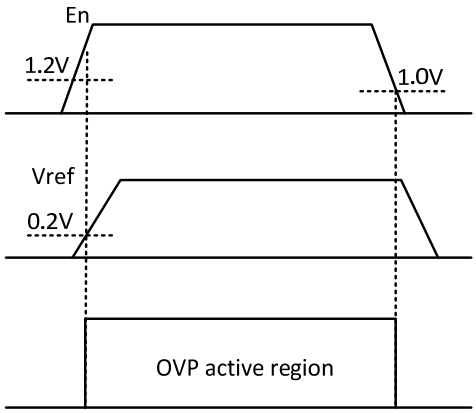


Figure 18a: Activation of OVP in non-tracking mode

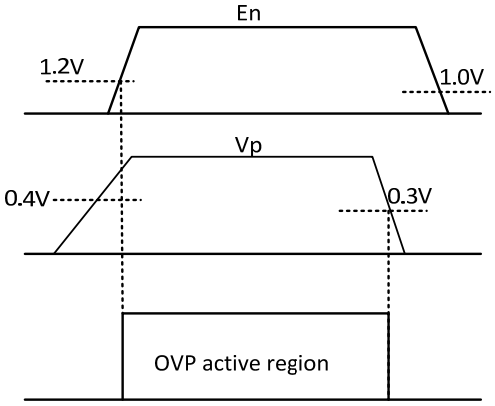


Figure 18b: Activation of OVP in tracking mode

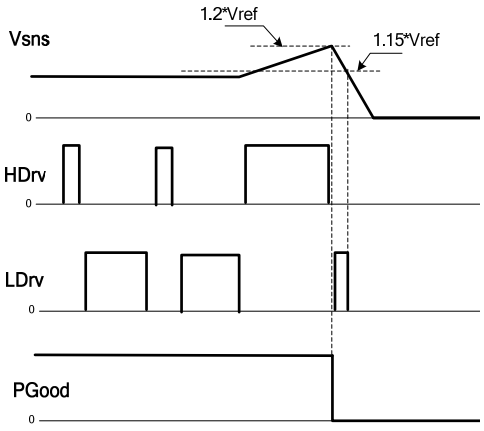


Figure 18: Timing Diagram for OVP in non-tracking mode