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IRAUDAMP11

120W x 3 Channel Class D Audio Power Amplifier Using the IRS2053M and IRF6665

By

Jun Honda, Liwei Zheng

CAUTION:

International Rectifier suggests the following guidelines for safe operation and handling of IRAUDAMP11 Demo board;

- **Always wear safety glasses whenever operating Demo Board**
- **Avoid personal contact with exposed metal surfaces when operating Demo Board**
- **Turn off Demo Board when placing or removing measurement probes**

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Introduction

The IRAUDAMP11 Demo board is a reference design which uses only one IC (IRS2053M) to derive appropriate input signals, amplify the audio input, and achieve a three-channel 120 W/ch (4Ω, THD+N=1%) half-bridge Class D audio power amplifier. The reference design demonstrates how to use the IRS2053M Class D audio controller and gate driver IC, implement protection circuits, and design an optimum PCB layout using IRF6665 DirectFET MOSFETs. The reference design contains all the required housekeeping power supplies for ease of use. The three-channel design is scalable, for power and number of channels.

Applications

- AV receivers
- Home theater systems
- Mini component stereos
- Powered speakers
- Sub-woofers
- Musical Instrument amplifiers
- Automotive after market amplifiers

Features

Output Power:	120W x 3 channels (4Ω, THD+N=1%) or 170W x 3 channels (4Ω, THD+N=10%)
Residual Noise:	220μV, IHF-A weighted, AES-17 filter
Distortion:	0.02% THD+N @ 60W, 4Ω
Efficiency:	90% @ 120W, 4Ω, single-channel driven, Class D stage
Multiple Protection Features:	Over-current protection (OCP), high side and low side Over-voltage protection (OVP), Under-voltage protection (UVP), high side and low side Over-temperature protection (OTP)
PWM Modulator:	Self-oscillating half-bridge topology with optional clock synchronization

Specifications

General Test Conditions (unless otherwise noted)		Notes / Conditions
Supply Voltages	±35V	
Load Impedance	4Ω	
Self-Oscillating Frequency	400kHz	No input signal, Adjustable
Gain Setting	28dB	1Vrms input yields rated power

Electrical Data	Typical	Notes / Conditions
IR Devices Used	IRS2053M Audio Controller and Gate-Driver, IRF6665 DirectFET MOSFETs	
Modulator	Self-oscillating, second order sigma-delta modulation, analog input	
Power Supply Range	± 25V to ±35V	Bipolar power supply
Output Power CH1-3: (1% THD+N)	120W	1kHz, ±35V
Output Power CH1-3: (10% THD+N)	170W	1kHz, ±35V

Rated Load Impedance	8-4Ω	Resistive load
Standby Supply Current	+75/-95mA	No input signal
Total Idle Power Consumption	6W	No input signal
Channel Efficiency	90%	Single-channel driven, 120W, Class D stage

.

Audio Performance	**Class D Output**	**Notes / Conditions**
THD+N, 1W	0.015%	1kHz, Single-channel driven
THD+N, 10W	0.01%	
THD+N, 60W	0.02%	
THD+N, 100W	0.03%	
Dynamic Range	101dB	A-weighted, AES-17 filter, Single-channel operation
Residual Noise, 22Hz - 20kHzAES17	220µV	Self-oscillating – 400kHz
Damping Factor	67	1kHz, relative to 4Ω load
Channel Separation	75dB	100Hz
	75dB	1kHz
	70dB	10kHz
Frequency Response : 20Hz-20kHz	±1dB	1W, 4Ω - 8Ω Load
: 20Hz-35kHz	±3dB	

Physical Specifications

Dimensions	3.94"(L) x 2.83"(W) x 0.85"(H) 100 mm (L) x 72 mm (W) x 21.5 mm(H)
Weight	0.130kgm

Connection Setup

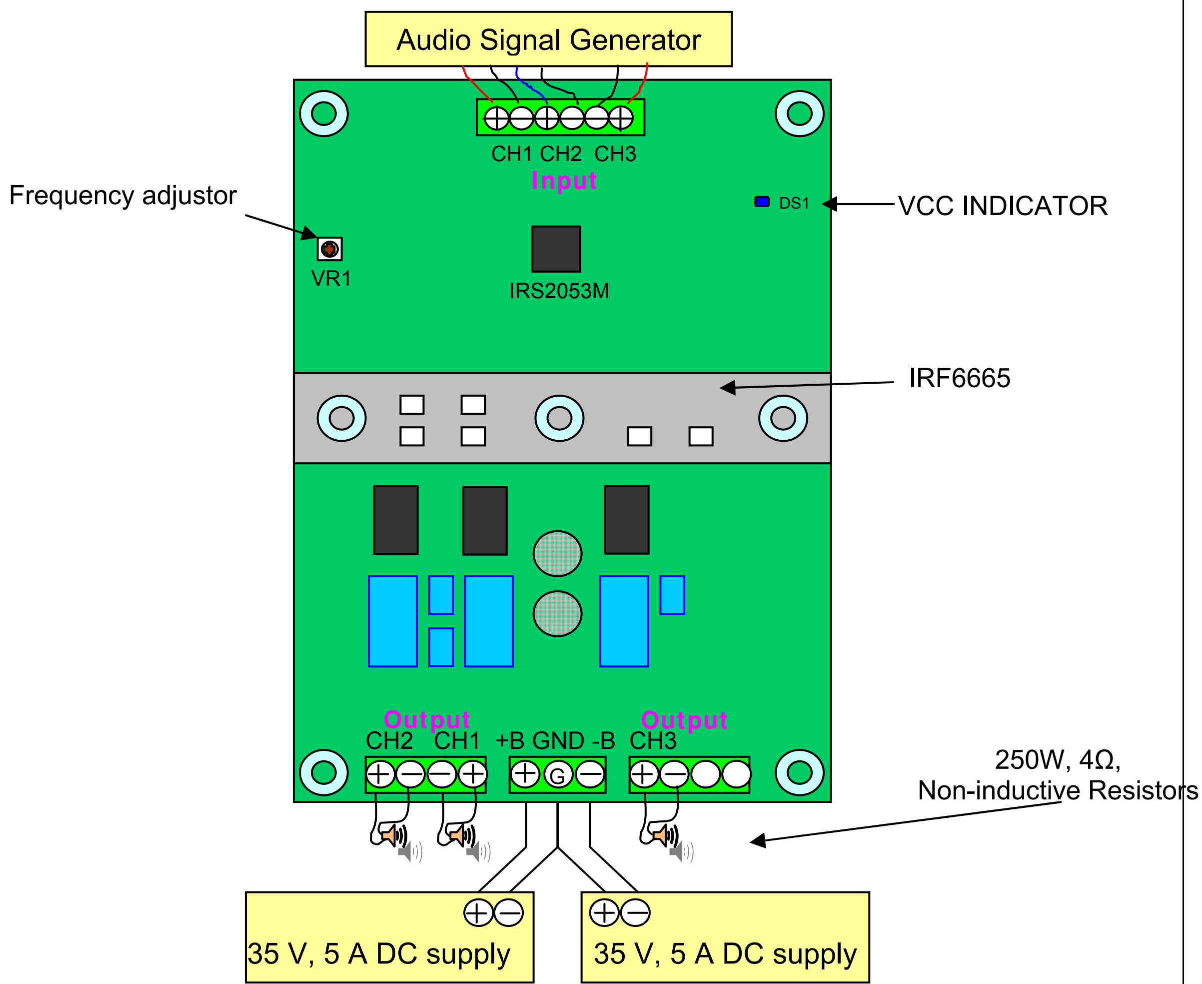


Fig 1 Typical Test Setup

Connector Description

CH1 IN	CN1	Analog input for CH1
CH2 IN	CN1	Analog input for CH2
CH3 IN	CN1	Analog input for CH3
SUPPLY	P1	Positive and negative supply (+B / -B)
CH1 OUT	P2	Output for CH1
CH2 OUT	P2	Output for CH2
CH3 OUT	P3	Output for CH3

Test Procedures

Test Setup:

1. Connect 4Ω-200 W dummy loads to 3 output connectors (P2 and P3 as shown on Fig 1) and an Audio Precision analyzer (AP).
2. Connect the Audio Signal Generator to CN1 for CH1~CH3 respectively (AP).
3. Set up the dual power supply with voltages of ±35V; current limit to 5A.
4. TURN OFF the dual power supply before connecting to On of the unit under test (UUT).
5. Connect the dual power supply to P1. as shown on Fig 1

Power up:

6. Turn ON the dual power supply. The ±B supplies must be applied and removed at the same time.
7. The Blue LED should turn ON immediately and stay ON
8. Quiescent current for the positive supply should be 75mA ±10mA at +35V.
9. Quiescent current for the negative supply should be 95mA ±10mA at –35V.

Switching Frequency test

10. With an Oscilloscope, monitor the switching waveform at test points VS1~VS3. Adjust VR1 to set the self oscillating frequency to 400 kHz ± 25 kHz when DUT in clock synchronize mode.

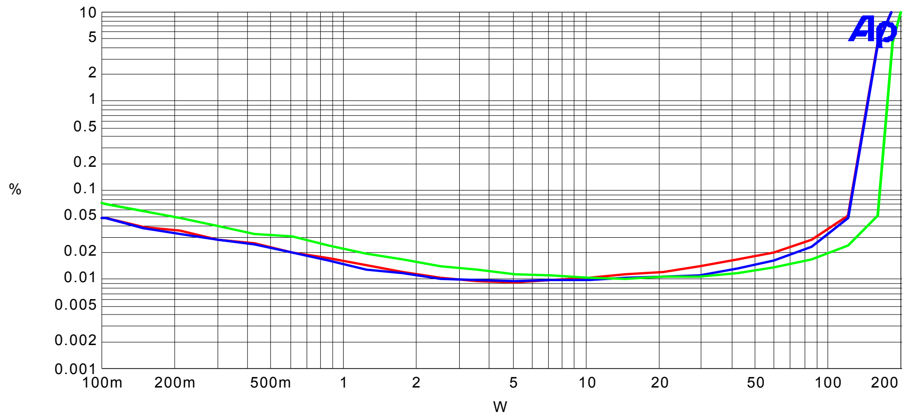
Functionality Audio Tests:

11. Set the signal generator to 1kHz, 20 mV_{RMS} output.
12. Connect the audio signal generator to CN1(Input of CH1,CH2,CH3)
13. Sweep the audio signal voltage from 15 mV_{RMS} to 1 V_{RMS}.
14. Monitor the output signals at P2/P3 with an oscilloscope. The waveform must be a non distorted sinusoidal signal.
15. Observe that a 1 V_{RMS} input generates an output voltage of 25.52 V_{RMS}(CH1/CH2). The ratio, R4x/(R3x) and R30x/(R31x), determines the voltage gain of IRAUDAMP11.

Test Setup using Audio Precision (Ap):

16. Use an unbalanced-floating signal from the generator outputs.
17. Use balanced inputs taken across output terminals, P2 and P3.
18. Connect Ap frame ground to GND at terminal P1.
19. Select the AES-17 filter(pull-down menu) for all the testing except frequency response.
20. Use a signal voltage sweep range from 15 mV_{RMS} to 1 V_{RMS}.
21. Run Ap test programs for all subsequent tests as shown in Fig 2- Fig 7below.

Performance and test graphs

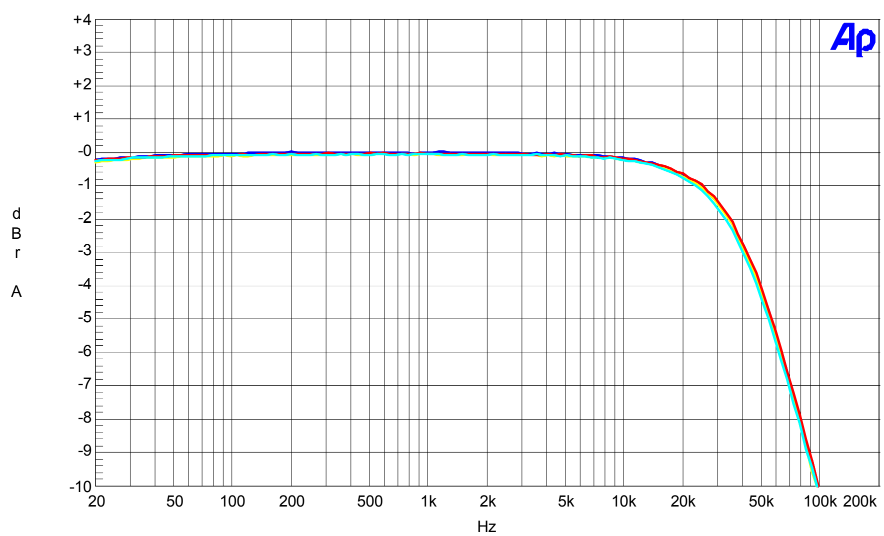


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ratio	Left	CH1
1	3	Blue	Solid	2	Anlr.THD+N Ratio	Left	CH2
2	3	Green	Solid	2	Anlr.THD+N Ratio	Left	

±B Supply = ±35V, 4 Ω Resistive Load

Fig 2 IRAUDAMP11, THD+N versus Power, Stereo, 4 Ω

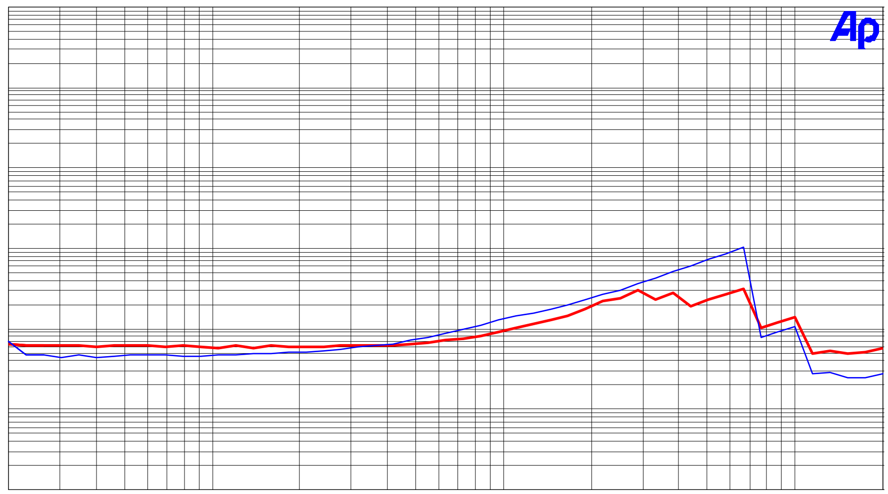
.



CH1-Blue; CH2-Yellow; CH3-Red

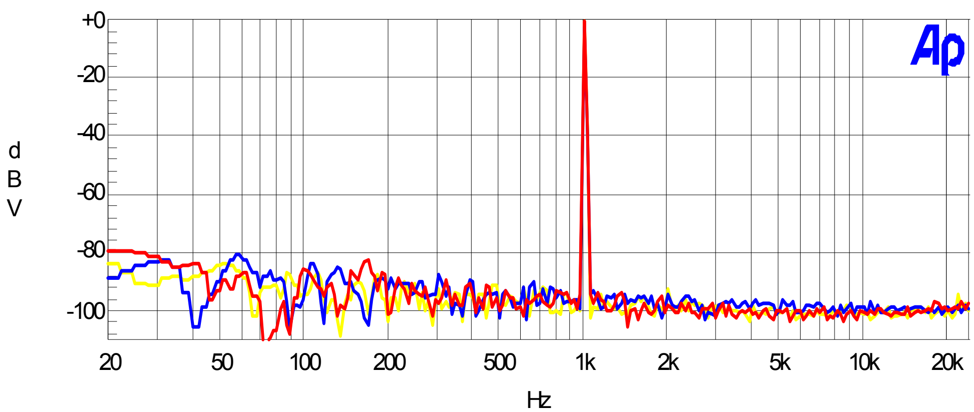
±B Supply = ±35V, 4 Ω Resistive Load

Fig 3 IRAUDAMP11, Frequency response



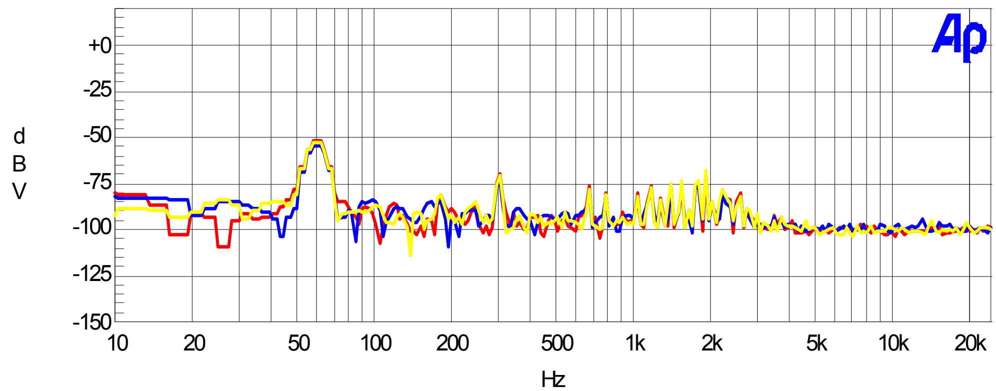
Red CH1, 10W Output
Blue CH1, 50W Output

Fig 4 THD+N Ratio vs. Frequency



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	2	Fft.Ch.1 Ampl	Left	CH2
1	2	Blue	Solid	2	Fft.Ch.2 Ampl	Left	CH3
2	1	Red	Solid	2	Fft.Ch.1 Ampl	Left	CH1

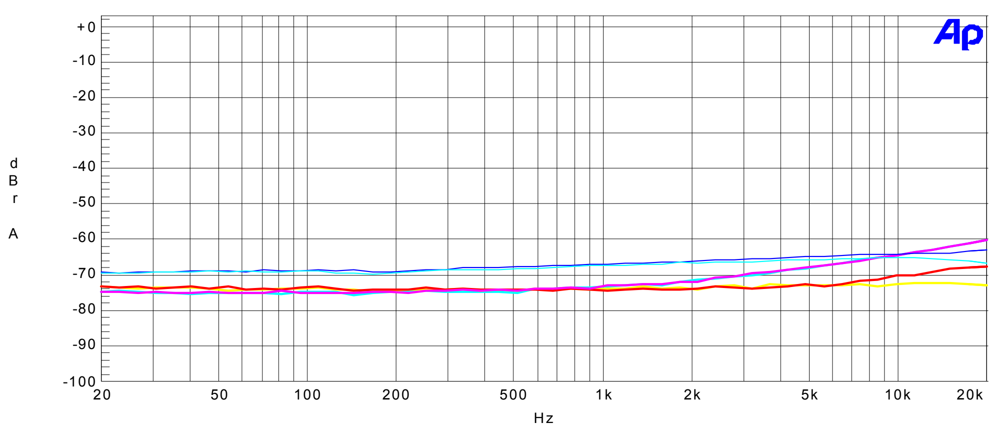
Fig 5, 1V output Frequency Spectrum



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Fft.Ch.1 Ampl	Left	CH1
1	2	Blue	Solid	2	Fft.Ch.2 Ampl	Left	CH3
2	1	Yellow	Solid	2	Fft.Ch.1 Ampl	Left	CH2

No signal, Self Oscillator @ 400kHz

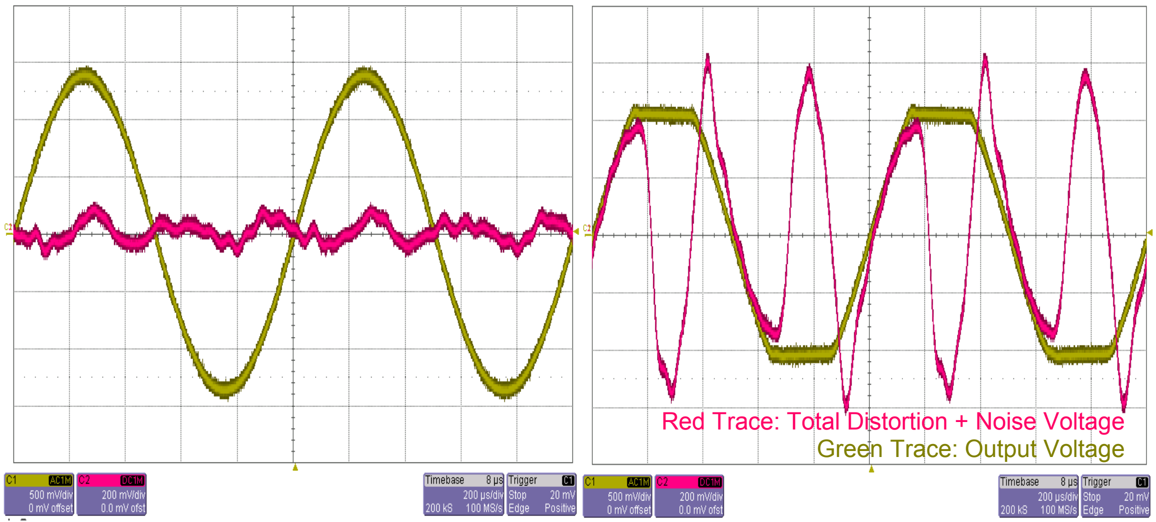
Fig 6, IRAUDAMP11 Noise Floor



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	Anlr.Ampl	Left	CH3_on;CH1_off
3	1	Yellow	Solid	2	Anlr.Ampl	Left	CH1_on;CH3_off
4	1	Red	Solid	2	Anlr.Ampl	Left	CH2_on;CH3_off
5	1	Magenta	Solid	2	Anlr.Ampl	Left	CH3_on;CH2_off
6	1	Blue	Solid	1	Anlr.Ampl	Left	CH2_on;CH1_off
7	1	Cyan	Solid	1	Anlr.Ampl	Left	Ch1_on;CH2_off

Fig 7, Channel separation vs. frequency

Clipping characteristics



60W / 4Ω, 1kHz, THD+N=0.02% **174W / 4Ω, 1kHz, THD+N=10%**

Measured Output and Distortion Waveforms(CH1/CH2)

Fig 8 Clipping Characteristics

Soft Clipping

IRS2053M has Clipping detection function, it monitors error voltage in COMP pin with a window comparator and pull an open drain nmos referenced to GND. Threshold to detect is at 10% and 90% of VAA-VSS. Each channel has independent CLIP outputs. Once IRS2053M detects Clipping, the CLIP pin will generate pulses to trigger soft clipping circuit as Fig 9, which limits output's maximum power.
Fig10 shows 20Hz and 20 kHz THD+N versus Power graph in CH3; it shows limitation of output's power with different frequency.

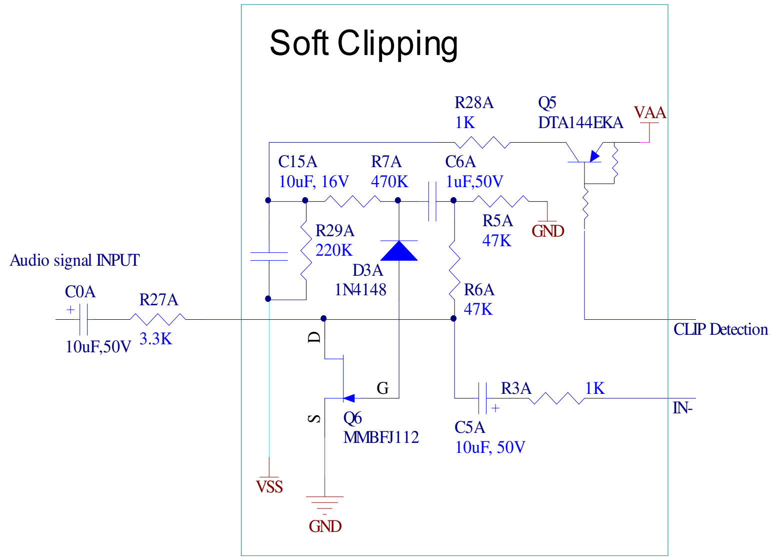
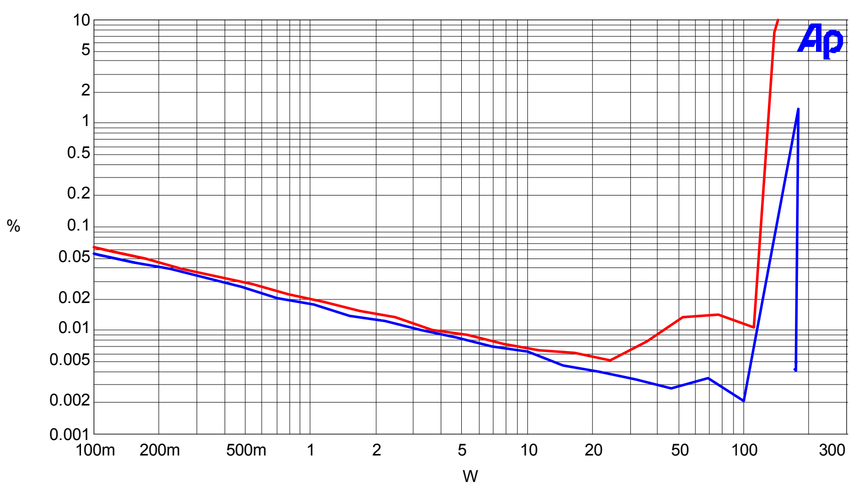


Fig 9 Soft Clipping Circuit



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ratio	Left	20Hz
2	1	Blue	Solid	2	Anlr.THD+N Ratio	Left	20kHz

±B Supply = ±35V, 4 Ω Resistive Load

Fig 10 IRAUDAMP11/CH3, THD+N versus Power, Stereo, 4 Ω

Efficiency

Fig 11 shows efficiency characteristics of the IRAUDAMP11. The high efficiency is achieved by following major factors:

1) Low conduction loss due to the DirectFETs offering low $R_{DS(ON)}$
2) Low switching loss due to the DirectFETs offering low input capacitance for fast rise and fall times

Secure dead-time provided by the IRS2053M, avoiding cross-conduction.

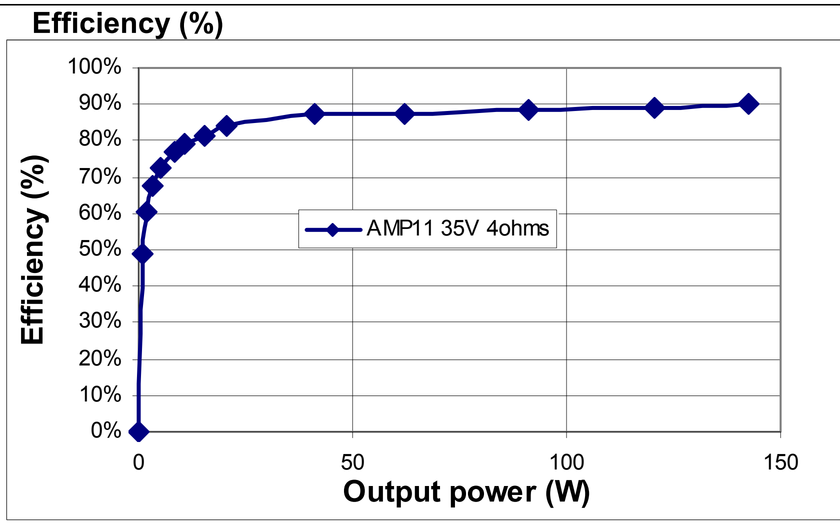


Fig 11, IRAUDAMP11 4 ohms load Stereo, ±B supply = ±35V

Thermal Considerations

With this high efficiency, the IRAUDAMP11 design can handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards, without additional heatsinks or forced air-cooling.

Thermal Interface Material's Pressure Control

The pressure between DirectFET & TIM (Thermal Interface Material) is controlled by depth of Heat Spreader's groove. Choose TIM which is recommended by IR. (Refer to AN-1035 for more details). TIM's manufacturer thickness, conductivity, & etc. determine pressure requirement. Below shows selection options recommended:

Common Thermal Interface Materials Cost Trades

Mfr.	Material	Type	Thickness (mils)	Pressure Required	Dispense/ Apply	Clips/ Screws	Can be applied to heat sink?	Mechanical Placement?
Dow Corning	1-4173	1 part heat-cured adhesive	#	Yes	Dispense	Clips	N	Y
Dow Corning	SE 4451	2 part heat-cured adhesive	#	Yes	Dispense	Clips	N	Y
Dow Corning	3-6652	2 part heat-cured adhesive	#	Yes	Dispense	Clips	N	Y
Dow Corning	TP-1500 Pad	Tacky - Phase Change at 52° C	10	>5psi, 20psi typ	Apply	Clips	Y	Y
Bergquist	Gap Pad 3000	conformable filled polymer sheet	15	>10psi	Apply	Clips/ Screws	N	Y
Bergquist	Gap Pad 2000	conformable filled polymer sheet	10	>10psi	Apply	Clips/ Screws	N	Y
Bergquist	Hi Flow 300	Phase Change at 55°C	2.4	>10psi	Apply	Clips	Y	*
Bergquist	Hi Flow 625	Phase Change at 65°C	5	>10psi	Apply	Clips	Y	*
Bergquist	Hi Flow 818	Phase Change at 65°C	5.5	>10psi	Apply	Clips	Y	*
Bergquist	Sil Pad 800	Conformable silicone elastomer	5	>10 higher better	Apply	Clips/ Screws	Y	*
Bergquist	Sil Pad 900	Conformable silicone elastomer	9	>10 higher better	Apply	Clips/ Screws	Y	*
Bergquist	Sil Pad A1500	Conformable silicone elastomer	10	10-50psi	Apply	Clips/ Screws	Y	*
Bergquist	Sil Pad A2000	Conformable silicone elastomer	10	10-50psi	Apply	Clips/ Screws	Y	*
Bergquist	Bond Ply 100	Pressure sensitive adhesive tape	5	>10psi	Apply	Clips	Y	Y
Bergquist	Bond Ply 100	Pressure sensitive adhesive tape	11	>10psi	Apply	Clips	Y	Y
Thermoset (Lord)	Gelease MG-120	Thermal grease/gel	#	5-7lbf	Dispense	Clips	N	Y
Shin Etsu	X-23-7783D	Thermal grease	##	-	Dispense	Clips	N	Y
Shin Etsu	X-23-7762	Thermal grease	##	-	Dispense	Clips	N	Y

Fig 12 TIM Information

Check the TIM's compression deflection with constant rate of strain (example as Fig.13) base on manufacturer's datasheet. According to the stress requirement, find strain range for the TIM. Then, calculate heat spreader groove depth as below:

Groove Depth=DirectFET's Height +TIM's Thickness*strain

**DirectFET's height should be measured from PCB to the top of DirectFET after reflow. The average height of IRF6665 is 0.6mm.

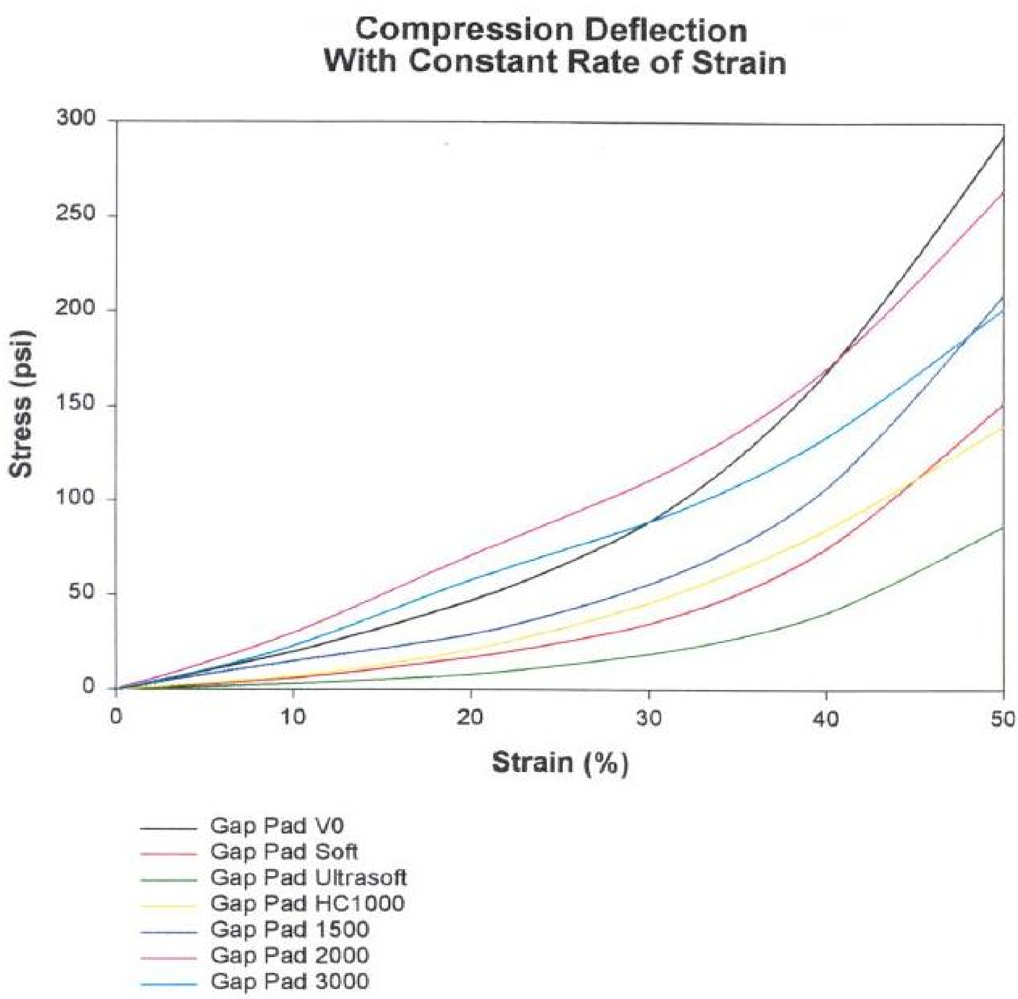
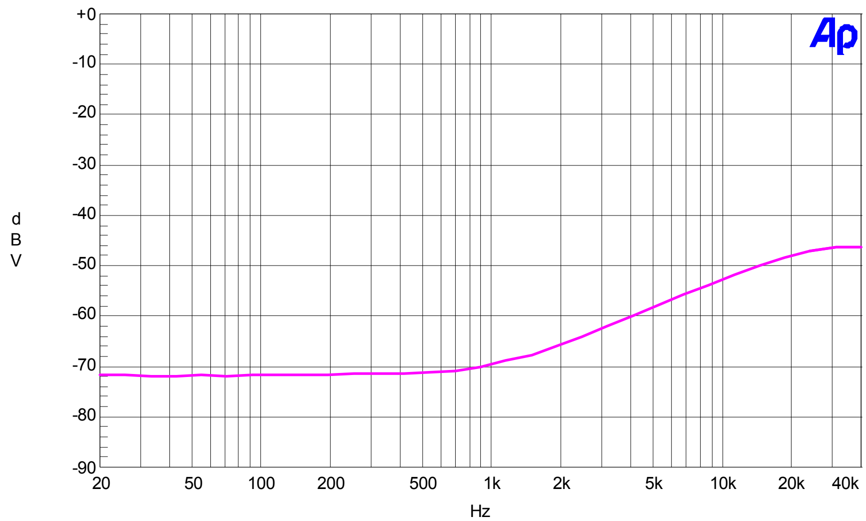


Fig 13 compression deflection with constant rate of strain

Power Supply Rejection Ratio (PSRR)

The IRAUDAMP11 obtains good power supply rejection ratio of -68 dB at 1kHz shown in Fig 14. With this high PSRR, IRAUDAMP11 accepts any power supply topology when the supply voltages fit between the min and max range.



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Magenta	Solid	2	Anlr.Ampl	Left	

Fig 14 Power Supply Rejection Ratio (PSRR)

Short Circuit Protection Response

Figs 15-16 show over current protection reaction time of the IRAUDAMP11 in a short circuit event. As soon as the IRS2053M detects an over current condition, it shuts down PWM. After one second, the IRS2053M tries to resume the PWM. If the short circuit persists, the IRS2053M repeats try and fail sequences until the short circuit is removed.

Short Circuit in Positive and Negative Load Current

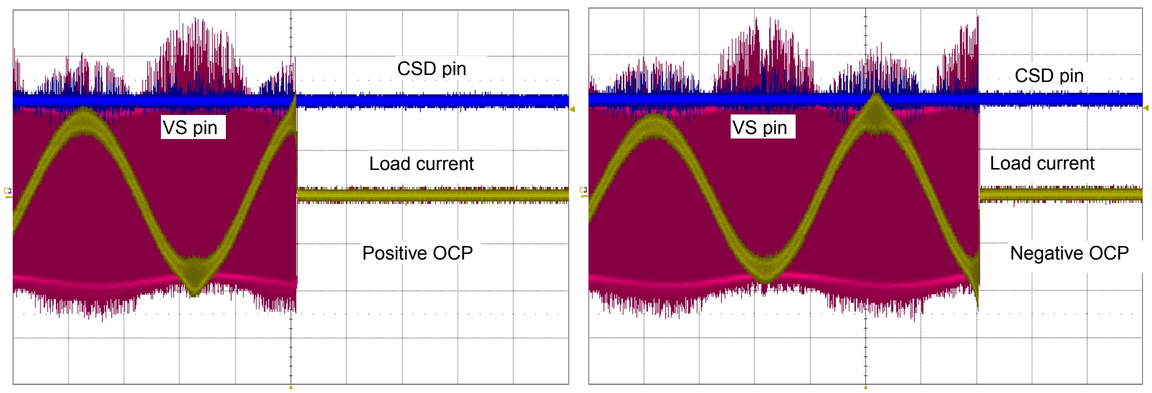


Fig 15 Positive and Negative OCP Waveforms

OCP Waveforms Showing CSD Trip and Hiccup

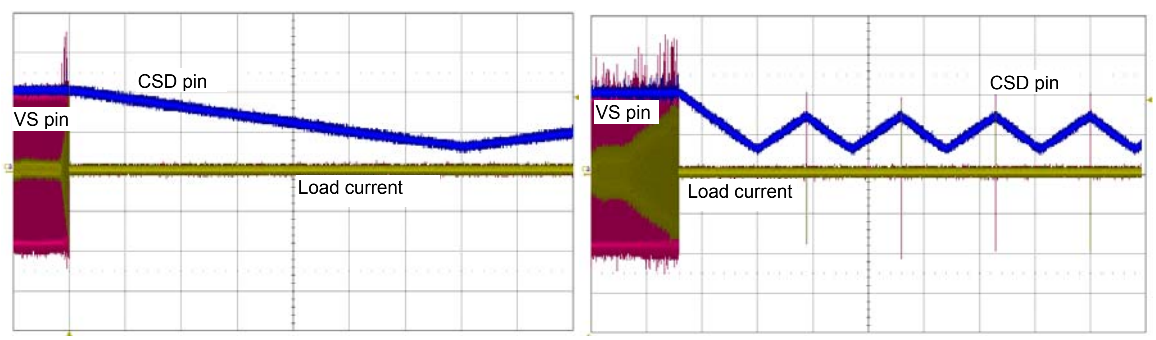


Fig 16 OCP Response with Continuous Short Circuit

IRAUDAMP11 Overview

The IRAUDAMP11 features a 3CH self-oscillating type PWM modulator for the smallest space, highest performance and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of error correction.

The IRAUDAMP11 self-oscillating topology consists of following essential functional blocks.

- Front-end integrator
- PWM comparator
- Level shifters
- Gate drivers and MOSFETs
- Output LPF

Integrator

Referring to Fig 17 below, the input operational amplifier of the IRS2053M forms a front-end second-order integrator with R3x, C2x, C3x, and R2x. The integrator that receives a rectangular feedback signal from the PWM output via R4x and audio input signal via R3x generates a quadratic carrier signal at the COMP pin. The analog input signal shifts the average value of the quadratic waveform such that the duty cycle varies according to the instantaneous voltage of the analog input signal.

PWM Comparator

The carrier signal at the COMP pin is converted to a PWM signal by an internal comparator that has a threshold at middle point between VAA and VSS. The comparator has no hysteresis in its input threshold.

Level Shifters

The internal input level-shifter transfers the PWM signal down to the low-side gate driver section. The gate driver section has another level-shifter that level shifts up the high-side gate signal to the high-side gate driver section.

Gate Drivers and DirectFETs

The received PWM signal is sent to the dead-time generation block where a programmable amount of dead time is added into the PWM signal between the two gate output signals of LO and HO to prevent potential cross conduction across the output power DirectFETs. The high-side level-shifter shifts up the high-side gate drive signal out of the dead-time block.

Each channel of the IRS2053M's drives two DirectFETs, high- and low-sides, in the power stage providing the amplified PWM waveform.

Output LPF

The amplified PWM output is reconstructed back to an analog signal by the output LC LPF. Demodulation LC low-pass filter (LPF) formed by L1 and C13, filters out the Class D switching carrier signal leaving the audio output at the speaker load. A single stage output filter can be used with switching frequencies of 400 kHz and greater; a design with a lower switching frequency may require an additional stage of LPF.

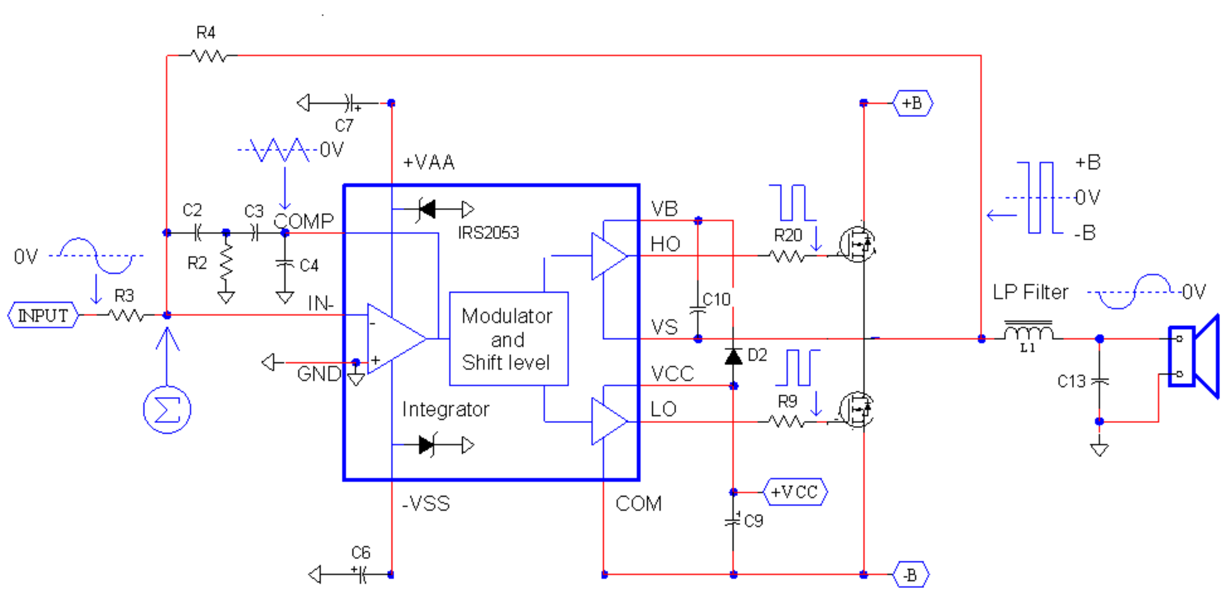


Fig 17 Simplified Block Diagram of IRAUDAMP11 Class D Amplifier

Functional Descriptions

IRS2053M Gate Driver IC

The IRAUDAMP11 uses the IRS2053M, a 3 Channel high-voltage (up to 200 V), high-speed power MOSFET driver with internal dead-time and protection functions specifically designed for Class D audio amplifier applications. These functions include OCP and UVP. The IRS2053M integrates bi-directional over current protection for both high-side and low-side MOSFETs. The dead-time can be selected for optimized performance according to the size of the MOSFET, minimizing dead-time while preventing shoot-through. As a result, there is no gate-timing adjustment required externally. Selectable dead-time through the DT pin voltage is an easy and reliable function which requires only two external resistors, R12 and R13 as shown on Fig 18 or Fig 24 below.

The IRS2053M offers the following functions.

- PWM modulator
- Dead-time insertion
- Over current protection
- Under voltage protection
- Level shifters

Refer to IRS2053M datasheet and AN-1158 for more details.

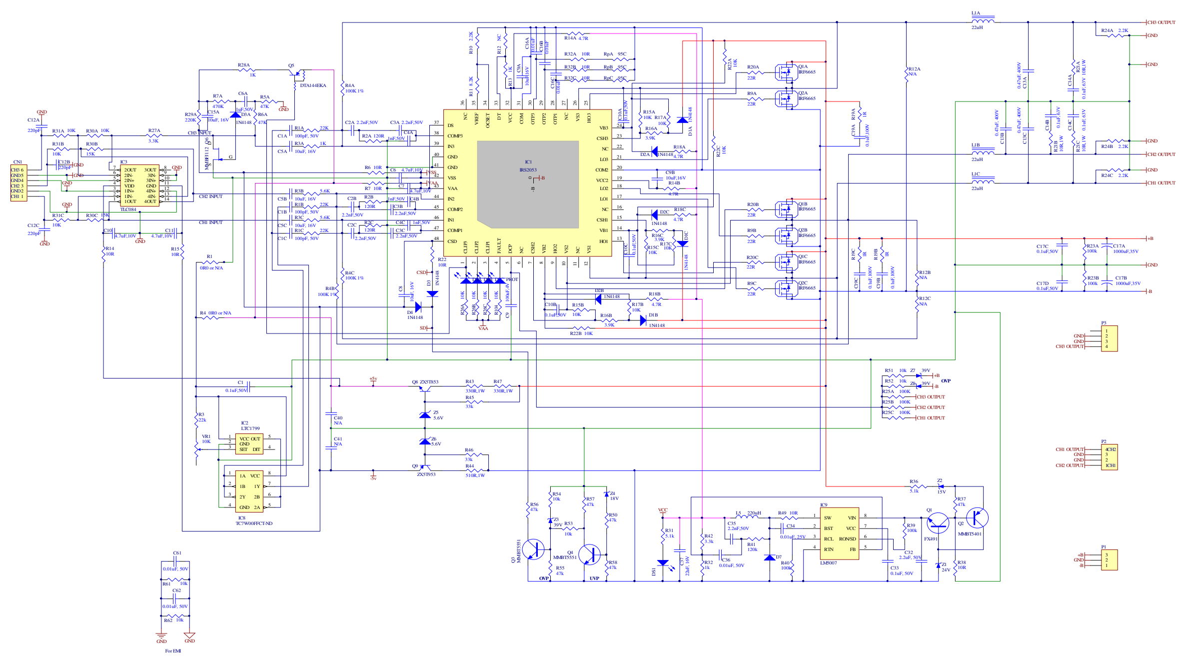


Fig 18 System-level View of IRAUDAMP11

Self-Oscillating Frequency

Self-oscillating frequency is determined by the total delay time along the control loop of the system; the propagation delay of the IRS2053M, the DirectFETs switching speed, the time-constant of front-end integrator (R2, R3, R4, C2, C3). Variations in +B and –B supply voltages also affect the self-oscillating frequency.

The self-oscillating frequency changes with the duty ratio. The frequency is highest at idling. It drops as duty cycle varies away from 50%.

Adjustments of Self-Oscillating Frequency

Use R2 to set different self-oscillating frequencies. The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute frequency and frequency relative to the other channels. In absolute terms, at higher frequencies, distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range.

Normally, when adjusting the self-oscillating frequency of the different channels, it is suggested to either match the frequencies accurately, or have them separated by at least 25kHz. Under the normal operating condition with no audio input signal, the switching-frequency is set around 400kHz in the IRAUDAMP11.

Selectable Dead-time

The dead-time of the IRS2053 is set based on the voltage applied to the DT pin. Fig 19 lists the suggested component value for each programmable dead-time between 45 and 105 ns.
All the IRAUDAMP11 models use DT1 (45ns) dead-time.

Dead-time Mode	R1	R2	DT/SD Voltage
DT1	<10k	Open	Vcc
DT2	5.6kΩ	4.7kΩ	0.46 x Vcc
DT3	8.2kΩ	3.3kΩ	0.29 x Vcc
DT4	Open	<10k	COM

Recommended Resistor Values for Dead Time Selection

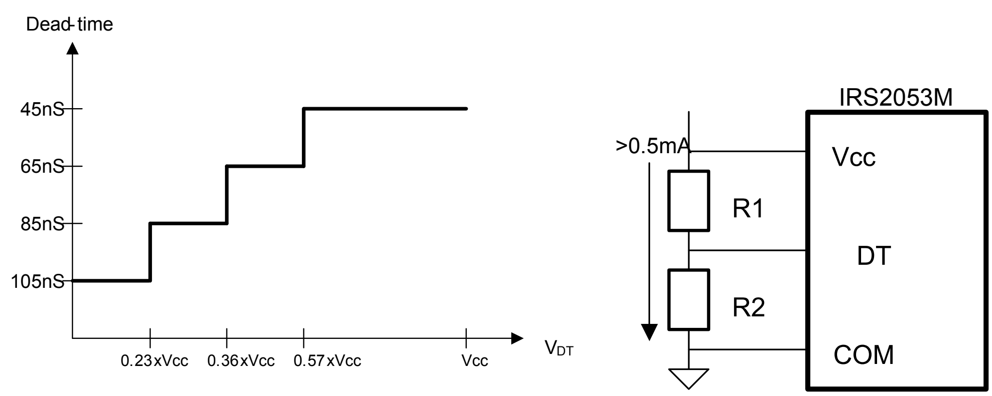


Fig 19 Dead-time Settings vs. V_{DT} Voltage

Protection System Overview

The IRS2053M integrates over current protection (OCP) inside the IC. The rest of the protections, such as over-voltage protection (OVP), under-voltage protection (UVP), and over temperature protection (OTP), are detected externally to the IRS2053M (Fig 20).

The external shutdown circuit will disable the output by pulling down CSD pins, (Fig 21). If the fault condition persists, the protection circuit stays in shutdown until the fault is removed.

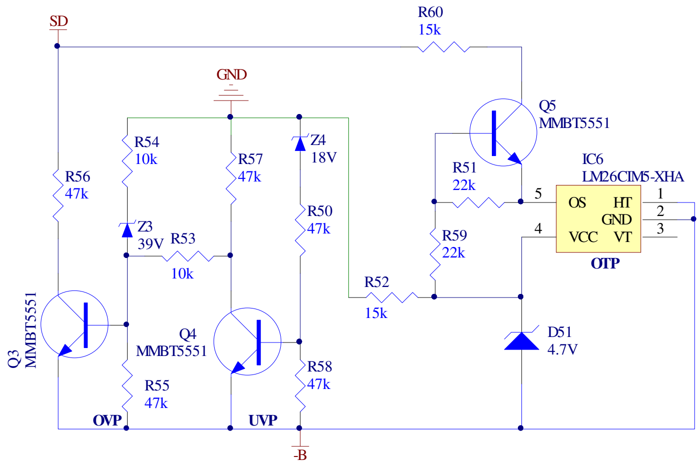


Fig 20 DCP, OTP, UVP and OVP Protection Circuits

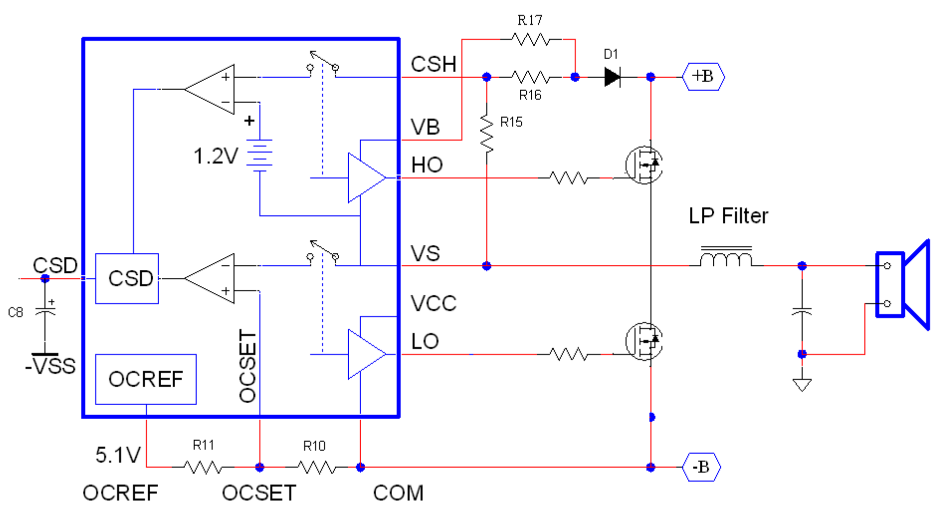


Fig 21 Simplified Functional Diagram of OCP

Over-Current Protection (OCP)

Low-Side Current Sensing

The low-side current sensing feature protects the low side DirectFET from an overload condition from negative load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. When the VS voltage becomes higher than the OCSET voltage during low-side conduction, the IRS2053 turns the outputs off and pulls CSD down to -VSS.

High-Side Current Sensing

The high-side current sensing protects the high side DirectFET from an overload condition from positive load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

High-side over-current sensing monitors drain-to-source voltage of the high-side DirectFET during the on state through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side DirectFET. In contrast to the low-side current sensing, the threshold of the CSH pin to trigger OC protection is internally fixed at 1.2V. An external resistive divider R15, R16 and R17 are used to program a threshold as shown in Fig 20. An external reverse blocking diode D1 is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D1, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source.

Over-Voltage Protection (OVP)

OVP is provided externally to the IRS2053M. OVP shuts down the amplifier if the bus voltage between GND and -B exceeds 39V. The threshold is determined by a Zener diode Z3. OVP protects the board from harmful excessive supply voltages, such as due to bus pumping at very low frequency-continuous output in stereo mode.

Under-Voltage Protection (UVP)

UVP is provided externally to the IRS2053M. UVP prevents unwanted audible noise output from unstable PWM operation during power up and down. UVP shuts down the amplifier if the bus voltage between GND and -B falls below a voltage set by Zener diode Z4.

Offset Null (DC Offset) Adjustment

The IRAUDAMP11 requires no output-offset adjustment. DC offsets are tested to be less than ±20 mV.

Over-Temperature Protection (OTP)

A Preset Thermostat IC, IC6 in Fig 19, is placed in close proximity to the heatsink which has 6 DirectFETs under it; and monitors heatsink temperature. If the heatsink temperature rises above 100 °C, the OTP shuts down all 3 channels by pulling down the CSD pins of the IRS2053M. OTP recovers once the temperature has cooled down.

Click and POP Noise Reduction

Thanks to the click and pop elimination function built into the IRS2053M, the IRAUDAMP11 does not require any additional components for this function.

Power Supply Requirements

For convenience, the IRAUDAMP11 has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies. Or use the IRAUDPS1 reference design which is a 12 volt systems Audio Power Supply for automotive applications designed to provide voltage rails (+B and –B) for Class D audio power amplifiers .

House Keeping Power Supply

The internally-generated housekeeping power supplies include ±5V for analog signal processing, and +12V supply (V_{CC}) referred to the negative supply rail -B for DirectFET gate drive. The gate driver section of the IRS2053M uses VCC to drive gates of the DirectFETs. V_{CC} is referenced to –B (negative power supply). D2, R18 and C10 form a bootstrap floating supply for the HO gate driver.

Bus Pumping

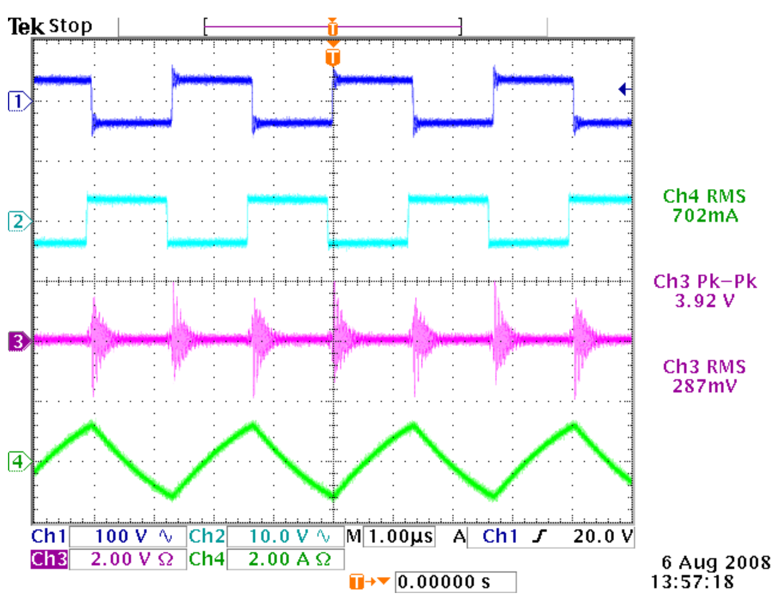
When the IRAUDAMP11 is running in stereo mode, the bus pumping effect takes place with low frequency, high output. Since the energy flowing in the Class D switching stage is bi-directional, there is a period where the Class D amplifier feeds energy back to the power supply. The majority of the energy flowing back to the supply is from the energy stored in the inductor in the output LPF.

Usually, the power supply has no way to absorb the energy coming back from the load. Consequently the bus voltage is pumped up, creating bus voltage fluctuations.

Following conditions make bus pumping worse:

1. Lower output frequencies (bus-pumping duration is longer per half cycle)
2. Higher power output voltage and/or lower load impedance (more energy transfers between supplies)
3. Smaller bus capacitance (the same energy will cause a larger voltage increase)

The OVP protects IRAUDAMP11 from failure in case of excessive bus pumping. One of the easiest counter measures of bus pumping is to drive both of the channels in a stereo configuration out-of-phase so that one channel consumes the energy flow from the other and does not return it to the power supply. Bus voltage detection monitors only +B supply, assuming the bus pumping on the supplies is symmetric in +B and -B supplies.



Blue: VS of CH3;Cyan: VS of CH2;Magenta: Voltage of +B;Green:Current of C13A
Fig 22 Auto-phase sync clock's BUS Pumping when idling