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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# IRAUDAMP5

## 120W x 2 Channel Class D Audio Power Amplifier Using the IRS2092S and IRF6645

*By*

Jun Honda, Manuel Rodríguez and Jorge Cerezo



Fig 1

**CAUTION:** International Rectifier suggests the following guidelines for safe operation and handling of IRAUDAMP5 Demo Board;

- Always wear safety glasses whenever operating Demo Board
- Avoid personal contact with exposed metal surfaces when operating Demo Board
- Turn off Demo Board when placing or removing measurement probes

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## Introduction

The IRAUDAMP5 reference design is a two-channel, 120W half-bridge Class D audio power amplifier. This reference design demonstrates how to use the IRS2092S Class D audio controller and gate driver IC, implement protection circuits, and design an optimum PCB layout using the IRF6645 DirectFET MOSFETs. The resulting design requires no heatsink for normal operation (one-eighth of continuous rated power). The reference design provides all the required housekeeping power supplies for ease of use. The two-channel design is scalable for power and the number of channels.

## Applications

AV receivers  
Home theater systems  
Mini component stereos  
Powered speakers  
Sub-woofers  
Musical Instrument amplifiers  
Automotive after market amplifiers

## Features

Output Power:	120W x 2 channels, Total Harmonic Distortion (THD+N) = 1%, 1 kHz
Residual Noise:	170 $\mu$ V, IHF-A weighted, AES-17 filter
Distortion:	0.005% THD+N @ 60W, 4 $\Omega$
Efficiency:	96% @ 120W, 4 $\Omega$ , single-channel driven, Class D stage
Multiple Protection Features:	Over-current protection (OCP), high side and low side Over-voltage protection (OVP), Under-voltage protection (UVP), high side and low side DC-protection (DCP), Over-temperature protection (OTP)
PWM Modulator:	Self-oscillating half-bridge topology with optional clock synchronization

## Specifications

General Test Conditions (unless otherwise noted)		Notes / Conditions
Supply Voltage	±35V	No input signal, Adjustable 1V <sub>rms</sub> input yields rated power
Load Impedance	8-4Ω	
Self-Oscillating Frequency	400kHz	
Gain Setting	26dB	

Electrical Data	Typical	Notes / Conditions
IR Devices Used	IRS2092S Audio Controller and Gate-Driver, IRF6645 DirectFET MOSFETs	
Modulator	Self-oscillating, second order sigma-delta modulation, analog input	
Power Supply Range	± 25V to ±35V	Bipolar power supply
Output Power CH1-2: (1% THD+N)	120W	1kHz
Output Power CH1-2: (10% THD+N)	170W	1kHz
Rated Load Impedance	8-4Ω	Resistive load
Standby Supply Current	±100mA	No input signal
Total Idle Power Consumption	7W	No input signal
Channel Efficiency	96%	Single-channel driven, 120W, Class D stage

Audio Performance	*Before Demodulator	Class D Output	Notes / Conditions
THD+N, 1W	0.009%	0.01%	1kHz, Single-channel driven
THD+N, 10W	0.003%	0.004%	
THD+N, 60W	0.003%	0.005%	
THD+N, 100W	0.008%	0.010%	
Dynamic Range	101dB	101dB	A-weighted, AES-17 filter, Single-channel operation
Residual Noise, 22Hz - 20kHzAES17	170μV	170μV	Self-oscillating – 400kHz
Damping Factor	2000	170	1kHz, relative to 4Ω load
Channel Separation	95dB	90dB	100Hz
	85dB	80dB	1kHz
	75dB	65dB	10kHz
Frequency Response : 20Hz-20kHz : 20Hz-35kHz	N/A	±1dB	1W, 4Ω - 8Ω Load
		±3dB	

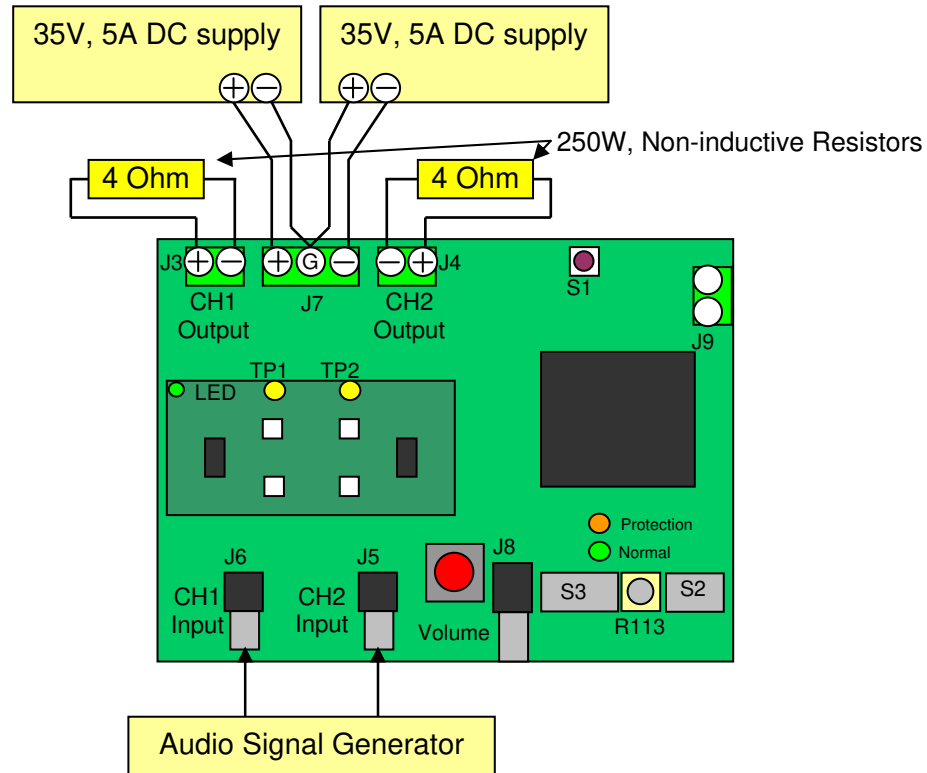
Thermal Performance	Typical	Notes / Conditions
Idling	T <sub>C</sub> =30°C T <sub>PCB</sub> =37°C	No signal input, T <sub>A</sub> =25°C
2ch x 15W (1/8 rated power)	T <sub>C</sub> =54°C T <sub>PCB</sub> =67°C	Continuous, T <sub>A</sub> =25°C
2ch x 120W (Rated power)	T <sub>C</sub> =80°C T <sub>PCB</sub> =106°C	At OTP shutdown @ 150 sec, T <sub>A</sub> =25°C

Physical Specifications	
Dimensions	5.8”(L) x 5.2”(W)

Note: Class D Specifications are typical

\*Before demodulator refers to audio performance measurements of the Class D output power stage only, with preamp and output filter bypassed this means performance measured before the low pass filter.

### Connection Setup



*Typical Test Setup*

**Fig 2**

### Connector Description

CH1 IN	J6	Analog input for CH1
CH2 IN	J5	Analog input for CH2
POWER	J7	Positive and negative supply (+B / -B)
CH1 OUT	J3	Output for CH1
CH2 OUT	J4	Output for CH2
EXT CLK	J8	External clock sync
DCP OUT	J9	DC protection relay output

## Test Procedures

1. Connect 4 $\Omega$ , 250W load to outputs connectors, J3 and J4 and Audio Precision analyzer (AP).
2. Connect Audio Signal Generator to J6 and J5 for CH1 and CH2 respectively (AP).
3. Connect a dual power supply to J7, pre-adjusted to  $\pm 35\text{V}$ , as shown in Figure 2 above.
4. Set switch S3 to middle position (self oscillating).
5. Set volume level knob R108 fully counter-clockwise (minimum volume).
6. Turn on the power supply. Note: always apply or remove the  $\pm 35\text{V}$  at the same time.
7. Orange LED (Protection) should turn on almost immediately and turn off after about 3s.
8. Green LED (Normal) then turns on after orange LED is extinguished and should stay on.
9. One second after the green LED turns on; the two blue LEDs on the Daughter Board should turn on and stay on for each channel, indicating that a PWM signal is present at LO
10. With an Oscilloscope, monitor switching waveform at test points TP1 and TP2 of CH1 and CH2 on Daughter Board.
11. If necessary, adjust the self-oscillating switching frequency of AUDAMP5 to 400KHz  $\pm 5\text{kHz}$  using potentiometer R29P. For IRAUDAMP5, the self-oscillating switching frequency is pre-calibrated to 400 KHz. To modify the AUDAMP5 frequency, change the values of potentiometers R21 and R22 for CH1 and CH2 respectively.
12. Quiescent current for the positive supply should be 70mA  $\pm 10\text{mA}$  at +35V.
13. Quiescent current for the negative supply should be 100mA  $\pm 10\text{mA}$  at -35V.
14. Push S1 switch, (Trip and Reset push-button) to restart the sequence of LEDs indicators, which should be the same as noted above in steps 6-9.

## Audio Tests:

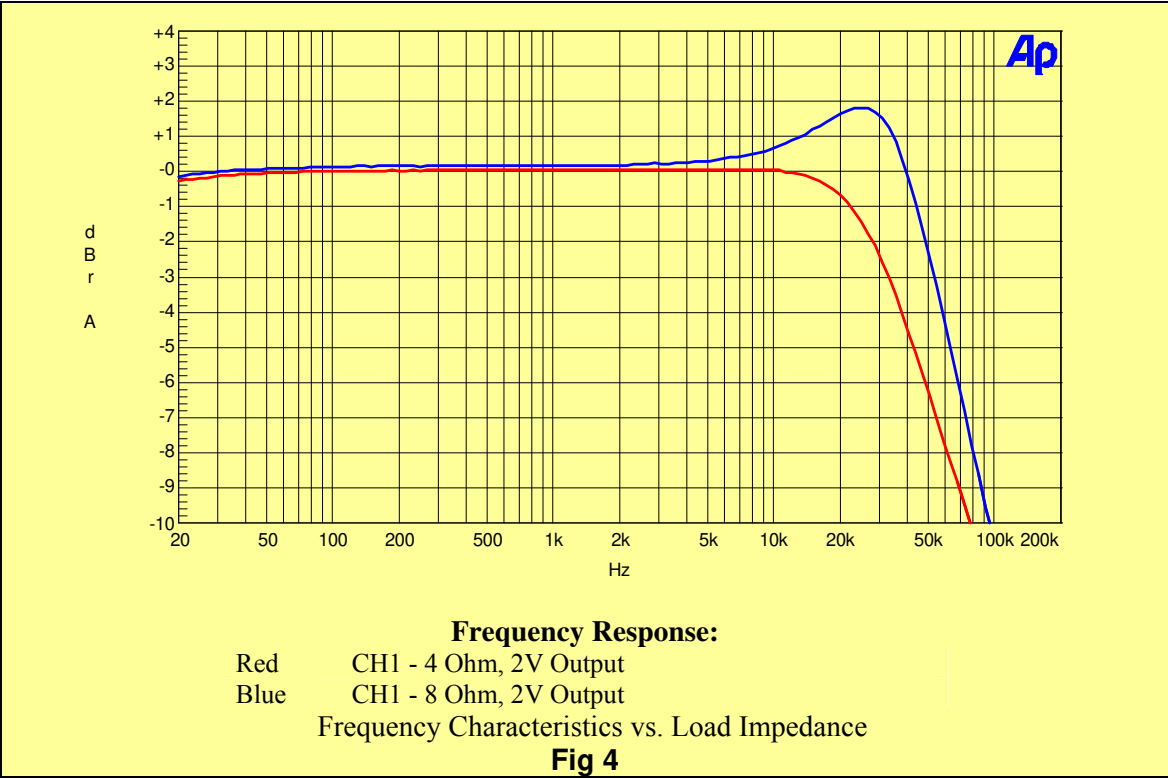
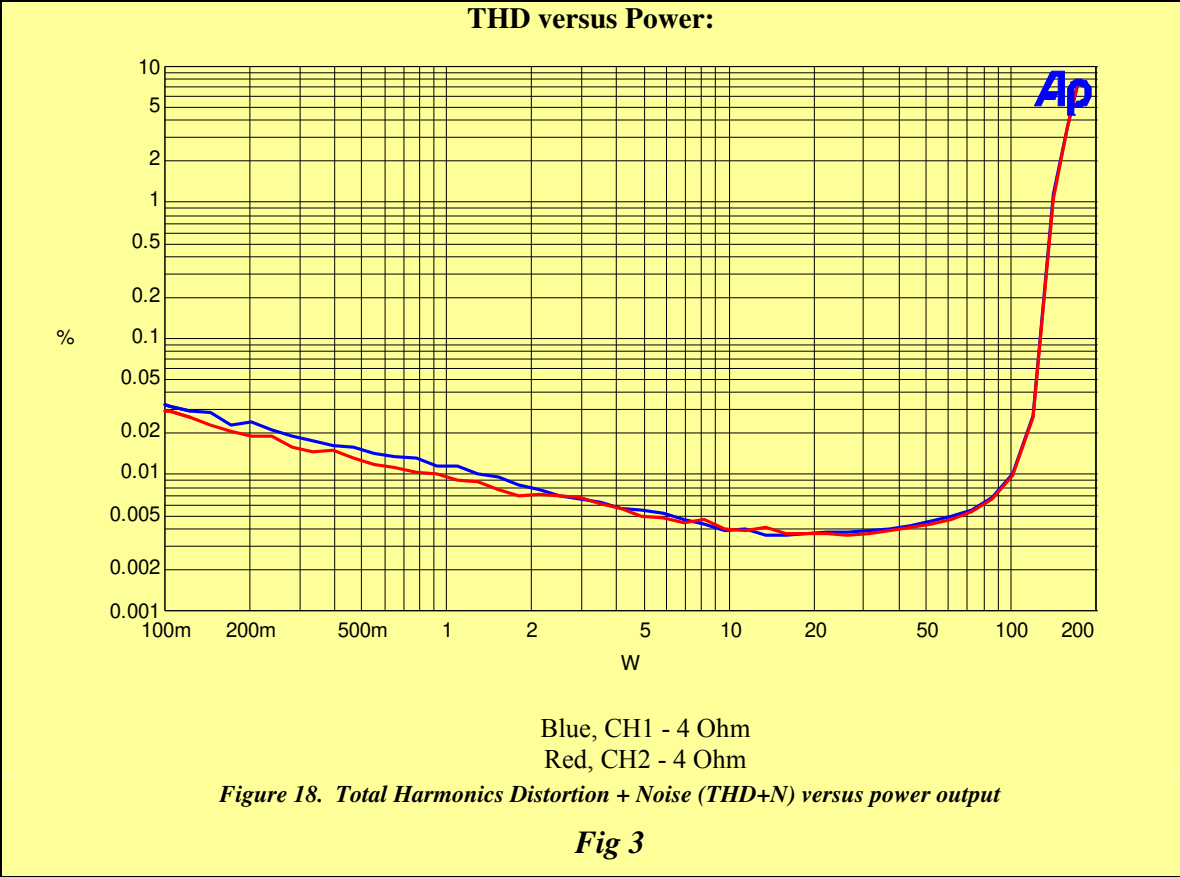
15. Apply 1 V RMS at 1KHz from the Audio Signal Generator
16. Turn control volume up (R108 clock-wise) to obtain an output reading of 100Watts for all subsequent tests as shown on the Audio Precision graphs below, where measurements are across J3 and J2 with an AES-17 Filter

## Typical Performance

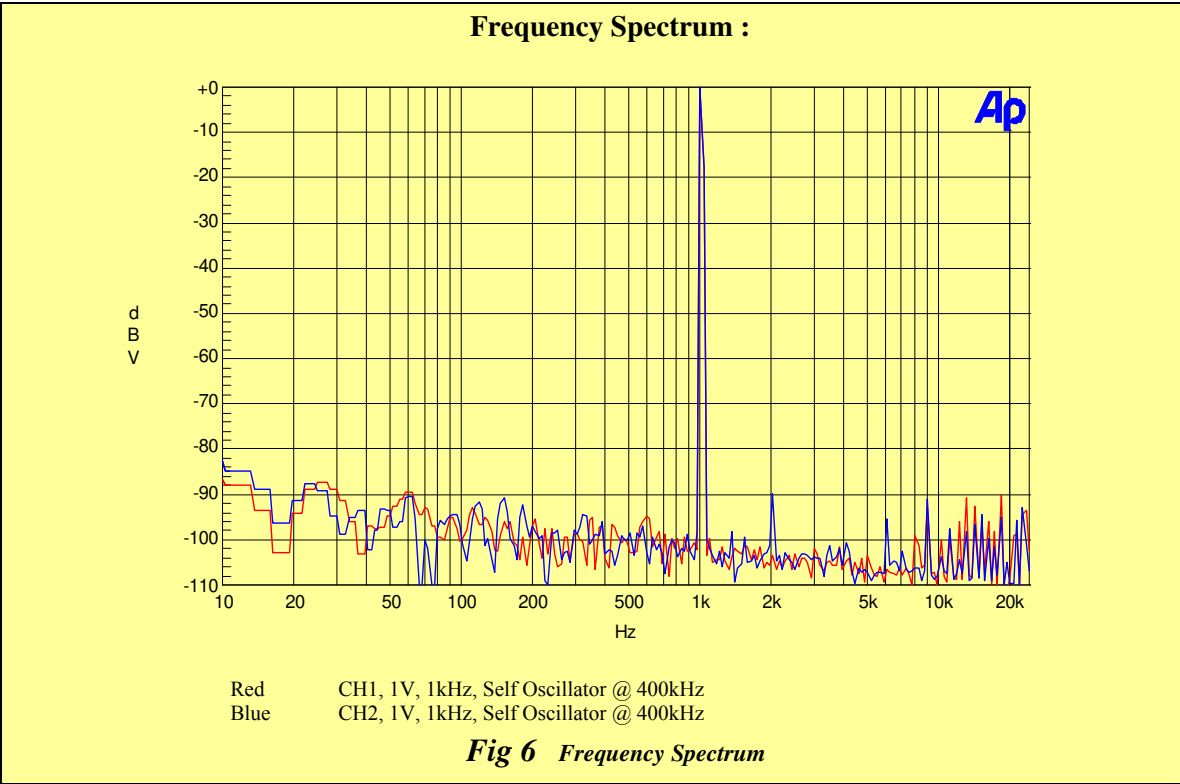
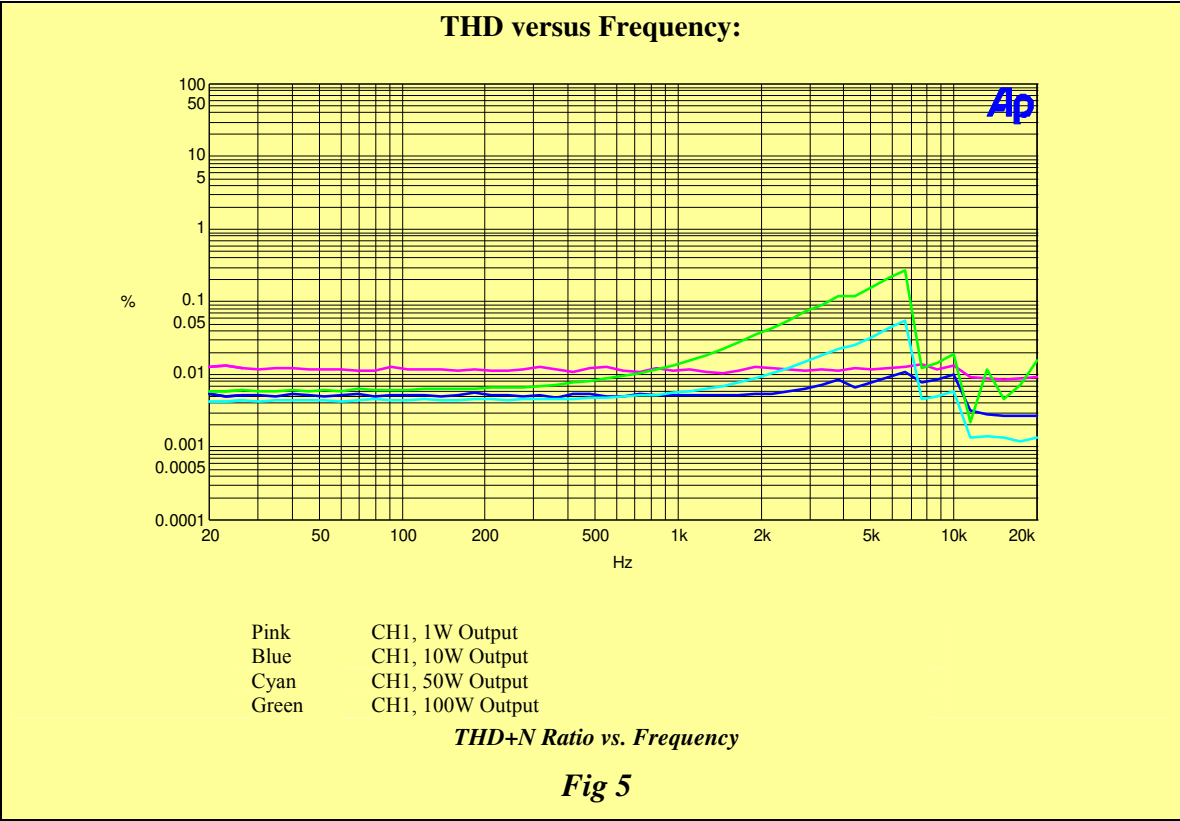
The tests below were performed under the following conditions:

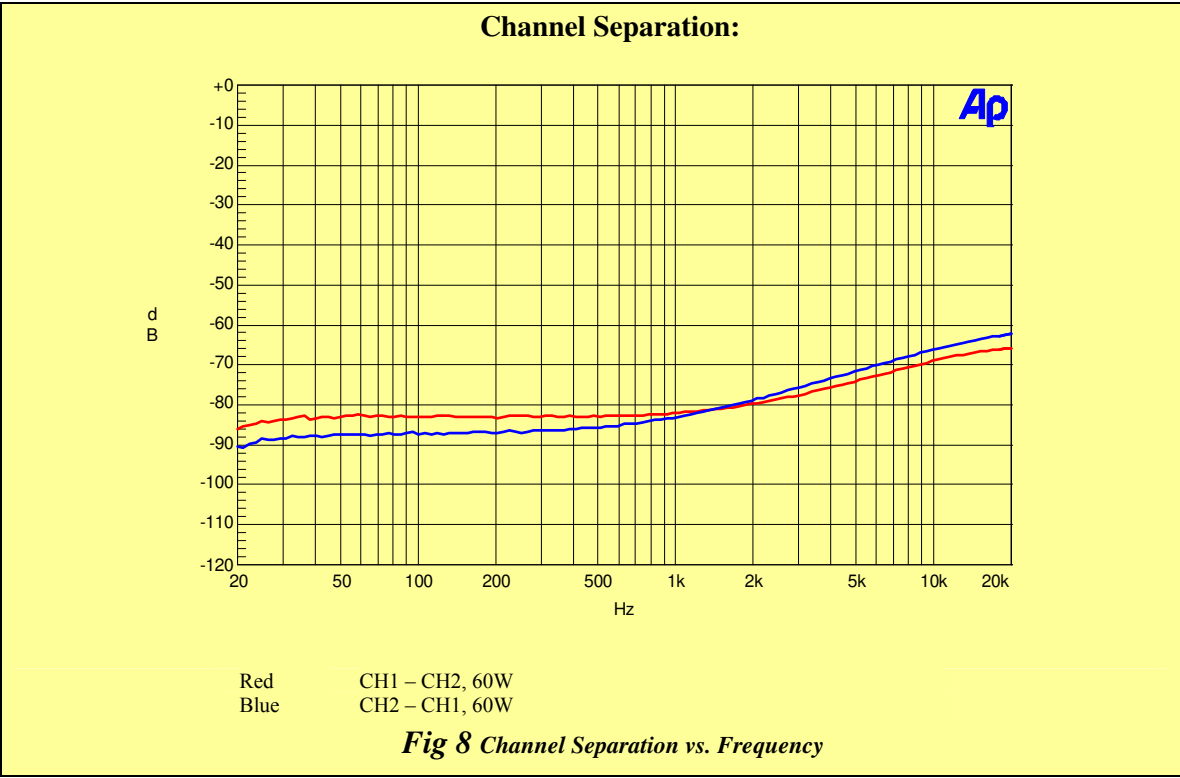
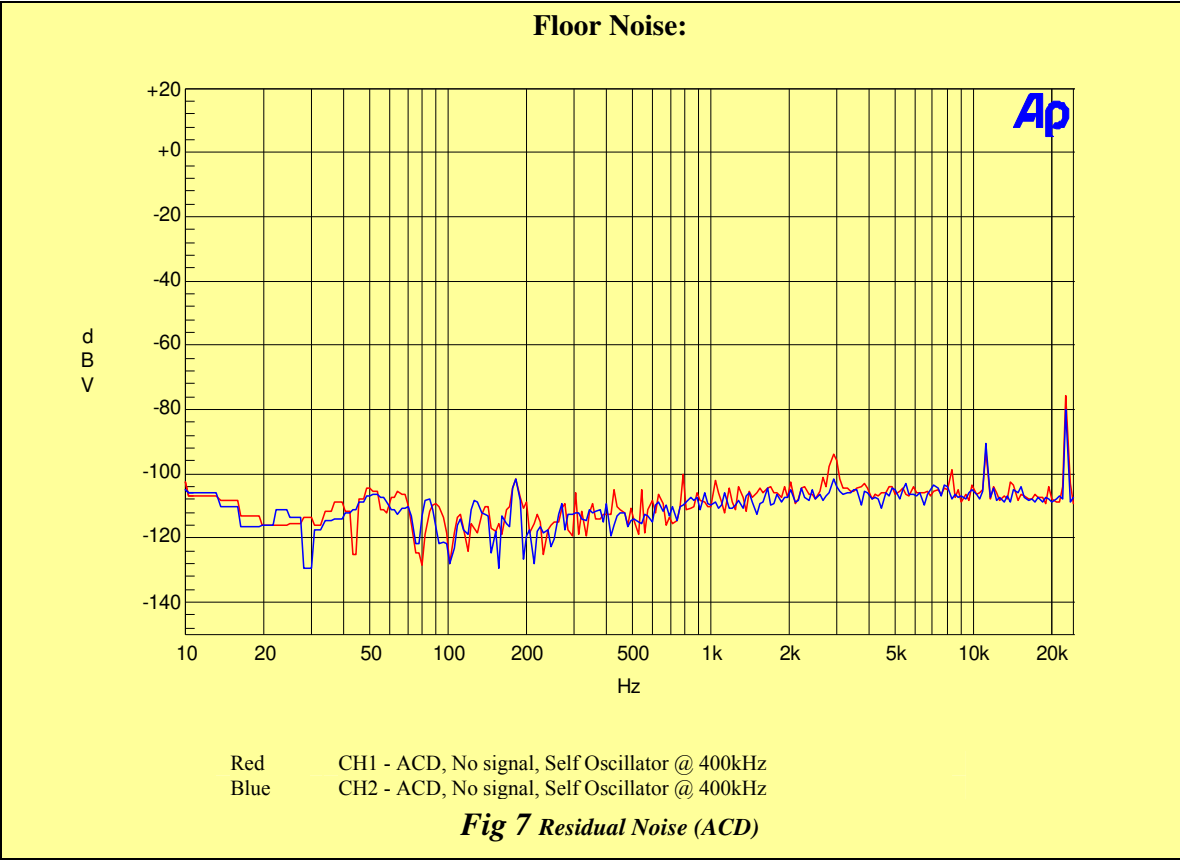
$\pm B$  supply =  $\pm 35\text{V}$ , load impedance = 4 $\Omega$  resistive load, 1kHz audio signal,

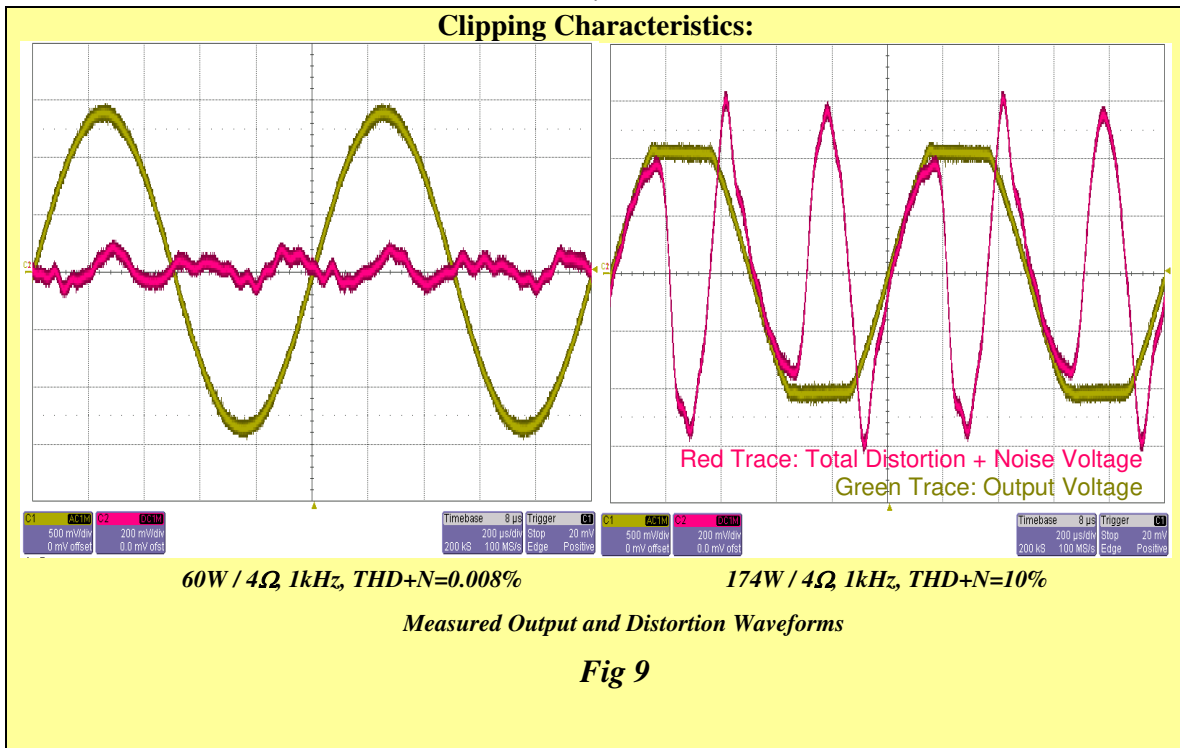
Self oscillator @ 400kHz and internal volume-control set to give required output with 1Vrms input signal, with AES-17 Filter, unless otherwise noted.











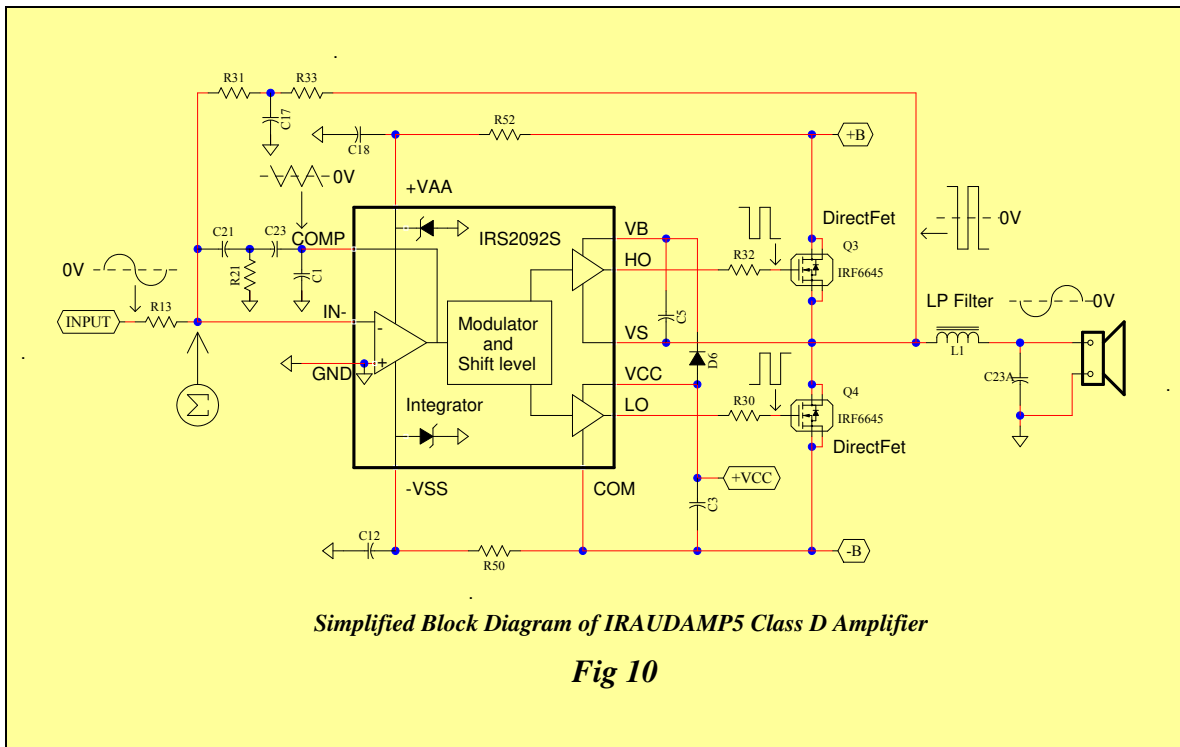
### IRAUDAMP5 Theory of Operation

Referring to Fig 10 below, the input error amplifier of the IRS2092S forms a front-end second-order integrator with C1, C21, C23 and R21. This integrator also receives a rectangular feedback waveform from R31, R33 and C17 into the summing node at IN- from the Class D power stage switching node (connection of DirectFET Q3 and DirectFET Q4). The quadratic oscillatory waveform of the switch node serves as a powered carrier signal from which the audio is recovered at the speaker load through a single-stage LC filter. The modulated signal is created by the fluctuations of the analog input signal at R13 that shifts the average value of this quadratic waveform through the gain relationship between R13 and R31 + R33 so that the duty cycle varies according to the instantaneous signal level of the analog input signal at R13.

R33 and C17 act to immunize the rectangular waveform from possible narrow noise spikes that may be created by parasitic impedances on the power output stage. The IRS2092S input integrator then processes the signal from the summing node to create the required triangle wave amplitude at the COMP output. The triangle wave then is converted to Pulse Width Modulation, or PWM, signals that are internally level-shifted Down and Up to the negative and positive supply rails. The level shifted PWM signals are called LO for low output, and HO for high output, and have opposite polarity. A programmable amount of dead time is added between the gate signals to avoid cross conduction between the power MOSFETs. The IRS2092S drives two IRF6645 DirectFET MOSFETs in the power stage to provide the amplified PWM waveform. The amplified analog output is reconstructed by demodulating the powered PWM at the switch node, called VS. (Show as VS on the schematic) This is done by means of the LC low-pass filter (LPF) formed by L1 and C23A, which filters out the Class D switching carrier signal, leaving the audio powered output at the speaker load. A single stage output filter can be used with switching

frequencies of 400 kHz and greater; lower switching frequencies may require additional filter components.

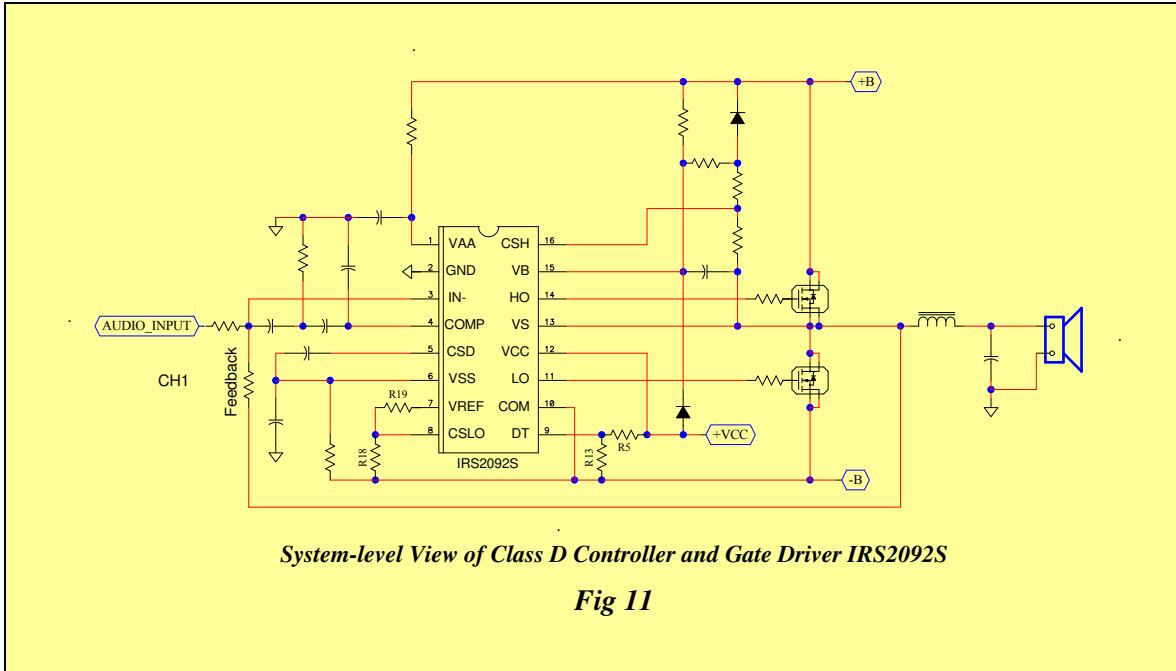
+VCC is referenced to -B and provides the supply voltage to the LO gate driver. D6 and C5 form a bootstrap supply that provides a floating voltage to the HO gate driver. The VAA and VSS input supplies are derived from +B and -B via R52 and C18, and R50 and C12, respectively. Thus, a fully functional Class D PWM amplifier plus driver circuit is realized in an SO16 package with just a few small components.



## System overview

### IRS2092S Gate Driver IC

The IRAUDAMP5 uses the IRS2092S, a high-voltage (up to 200V), high-speed power MOSFET PWM generator and gate driver with internal dead-time and protection functions specifically designed for Class D audio amplifier applications. These functions include OCP and UVP. Bi-directional current protection for both the high-side and low-side MOSFETs are internal to the IRS2092S, and the trip levels for both MOSFETs can be set independently. In this design, the dead time can be selected for optimized performance by minimizing dead time while preventing shoot-through. As a result, there is no gate-timing adjustment on the board. Selectable dead time through the DT pin voltage is an easy and reliable function which requires only two external resistors, R11 and R9 as shown on Fig11 below.

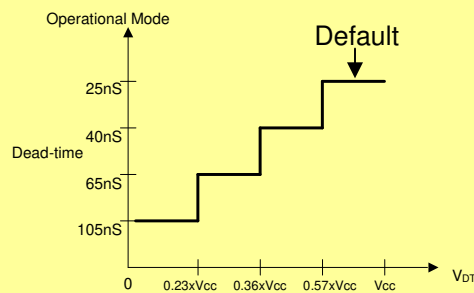


**Selectable Dead-Time**

The dead time of the IRS2092S is based on the voltage applied to the DT pin. (Fig 12) An internal comparator determines the programmed dead time by comparing the voltage at the DT pin with internal reference voltages. An internal resistive voltage divider based on different ratios of VCC negates the need for a precise reference voltage and sets threshold voltages for each of the four programmable settings. Shown in the table below are component values for programmable dead times between 25 and 105 ns. To avoid drift from the input bias current of the DT pin, a bias current of greater than 0.5mA is suggested for the external resistor divider circuit. Resistors with up to 5% tolerance can be used.

**Selectable Dead-Time**

Dead-time mode	Dead time	R5	R13	DT voltage	
DT1	~25ns	3.3k	8.2k	0.71 x Vcc	Default
DT2	~40ns	5.6k	4.7k	0.46 x Vcc	
DT3	~65ns	8.2k	3.3k	0.29 x Vcc	
DT4	~105ns	open	<10k	0 x Vcc	



**Fig 12 Dead-time Settings vs.  $V_{DT}$  Voltage**

**Over-Current Protection (OCP)**

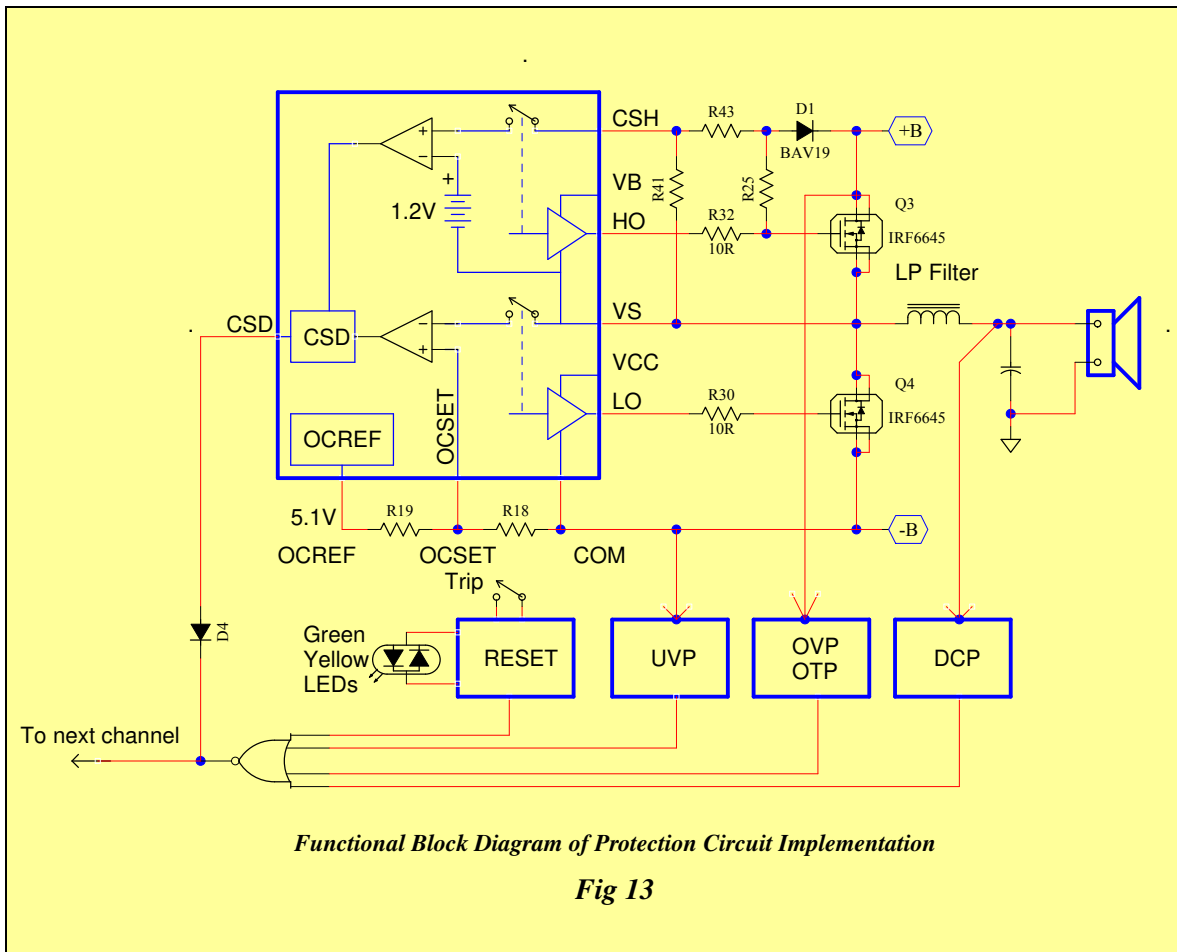
In the IRAUDAMP5, the IRS2092S gate driver accomplishes OCP internally, a feature discussed in greater detail in the “Protection” section.

**Offset Null (DC Offset)**

The IRAUDAMP5 is designed such that no output-offset nullification is required, thanks to closed loop operation. DC offsets are tested to be less than  $\pm 20\text{mV}$ .

**Protection**

The IRAUDAMP5 has a number of protection circuits to safeguard the system and speaker as shown in the figure 13 below, which fall into one of two categories – internal faults and external faults, distinguished by the manner in which a fault condition is treated. Internal faults are only relevant to the particular channel, while external faults affect the whole board. For internal faults, only the offending channel is stopped. The channel will hiccup until the fault is cleared. For external faults, the whole board is stopped using the shutdown sequencing described earlier. In this case, the system will also hiccup until the fault is cleared, at which time it will restart according to the startup sequencing described earlier.

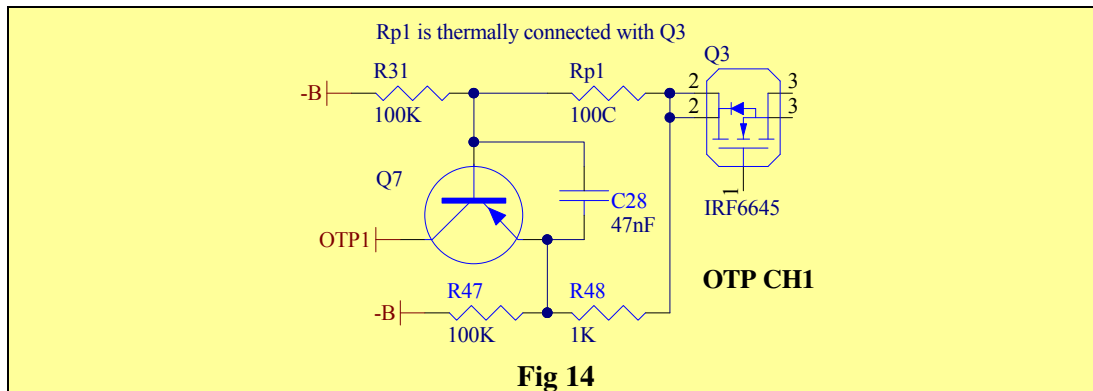


### Internal Faults

OCP and OTP are considered internal faults, which will only shutdown the particular channel by pulling low the relevant CSD pin. The channel will shutdown for about one-half a second and will hiccup until the fault is cleared.

### Over-Temperature Protection (OTP, Fig 14)

A separate PTC resistor is placed in close proximity to the high-side IRF6645 DirectFET MOSFET for each of the amplifier channels. If the resistor temperature rises above 100°C, the OTP is activated. The OTP protection will only shutdown the relevant channel by pulling the CSD pin low and will recover once the temperature at the PTC has dropped sufficiently. This temperature protection limit yields a PCB temperature at the MOSFET of about 100°C, which is limited by the PCB material and not by the operating range of the MOSFET.

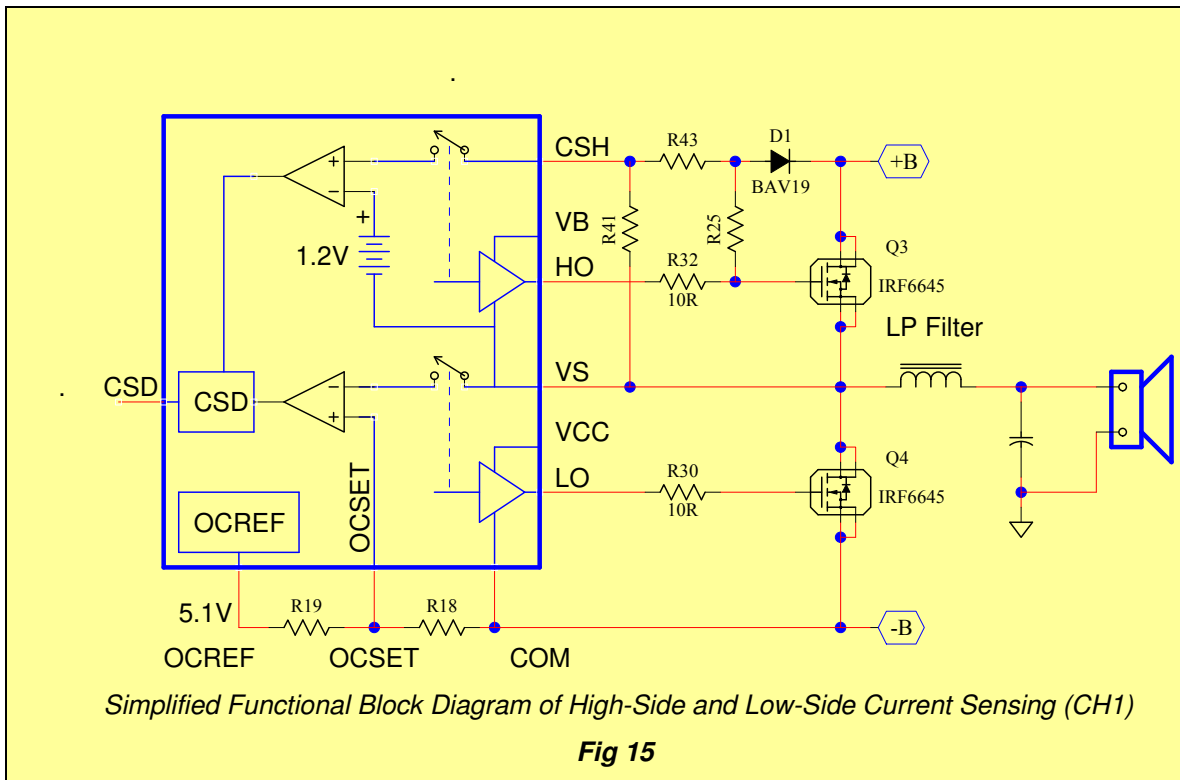


### Over-Current Protection (OCP)

The OCP internal to the IRS2092S shuts down the IC if an OCP is sensed in either of the output MOSFETs. For a complete description of the OCP circuitry, please refer to the IRS2092S datasheet. Here is a brief description:

### Low-Side Current Sensing

Fig 15 shows the low side MOSFET as is protected from an overload condition by measuring the low side MOSFET drain-to-source voltage during the low side MOSFET on state, and will shut down the switching operation if the load current exceeds a preset trip level. The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. Thus, if the VS voltage during low-side conduction is higher than the OCSET voltage, the IRS2092S will trip and CSD goes down. It is recommended to use VREF to supply a reference voltage to a resistive divider (R19 and R18 for CH1) to generate a voltage to OCSET; this gives better variability against VCC fluctuations. For IRAUDAMP5, the low-side over-current trip level is set to 0.65V. For IRF6645 DirectFET MOSFETs with a nominal  $R_{DS-ON}$  of 28mOhms at 25°C, this results in a ~23A maximum trip level. Since the  $R_{DS-ON}$  is a function of temperature, the trip level is reduced to ~15A at 100°C.



### High-Side Current Sensing (Fig15)

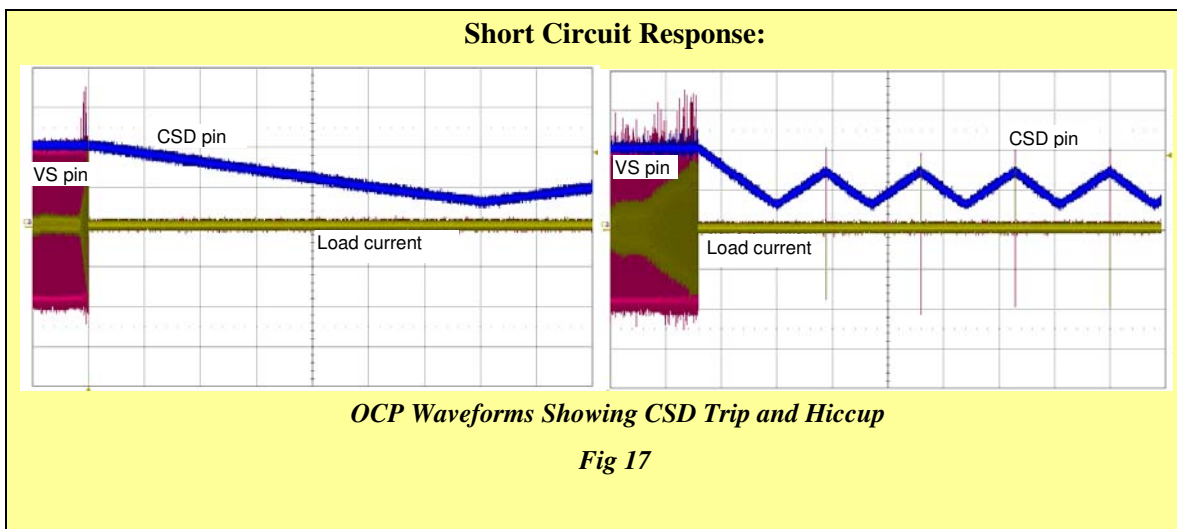
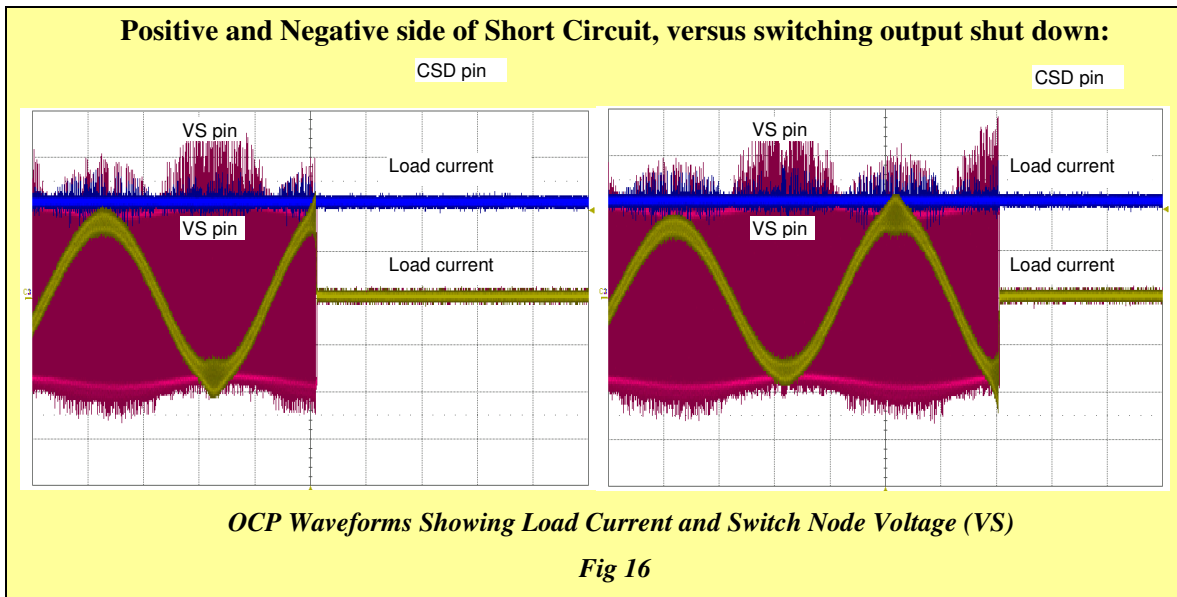
The high-side MOSFET is protected from an overload condition and will shutdown the switching operation if the load current exceeds a preset trip level. High-side over-current sensing monitors detect an overload condition by measuring the high side MOSFET's drain-to-source voltage ( $V_{DS}$ ) through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side MOSFET. In contrast to the low-side current sensing, the threshold of CSH pin to engage OC protection is internally fixed at 1.2V. An external resistive divider R43+R25 and R41 (for Ch1) can be used to program a higher threshold. An additional external reverse blocking diode (D1 for CH1) is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D1, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source. For IRAUDAMP5, the high-side over-current trip level is set to 0.6V across the high-side MOSFET. For the IRF6645 MOSFETs with a nominal  $R_{DS-ON}$  of 28 mOhms at 25°C, this results in a ~21A maximum trip level. Since the  $R_{DS-ON}$  is a function of temperature, the trip level is reduced to ~14A at 100°C.

For a complete description of calculating and designing the over-current trip limits, please refer to the IRS2092S datasheet.

### Positive and Negative Side of Short Circuit, versus switching output shut down:

The plots below show the speed that the IRS2092S responds to a short circuit condition. Notice that the envelope behind the sine wave output is actually the switching frequency ripple. Bus pumping naturally affects this topology.





**External Faults**

OVP, UVP and DCP are considered external faults. In the event that any external fault condition is detected, the shutdown circuit will disable the output for about three seconds, during which time the orange AUDAMP5 “Protection” LED will turn on. If the fault condition has not cleared, the protection circuit will hiccup until the fault is removed. Once the fault is cleared, the green “Normal” LED will turn on. There is no manual reset option.

**Over-Voltage Protection (OVP Fig 18)**

OVP will shut down the amplifier if the bus voltage between GND and -B exceeds 40V. The threshold is determined by the voltage sum of the Zener diode Z105, R140, and  $V_{BE}$  of Q109. As a result, it protects the board from hazardous bus pumping at very low audio signal frequencies by shutting down the amplifier. OVP will automatically reset after three seconds. Since the +B and -B supplies are assumed to be symmetrical (bus pumping, although asymmetrical in time,

will pump the bus symmetrically in voltage level over a complete audio frequency cycle), it is sufficient to sense only one of the two supply voltages for OVP. *It is therefore up to the user to ensure that the power supplies are symmetrical.*

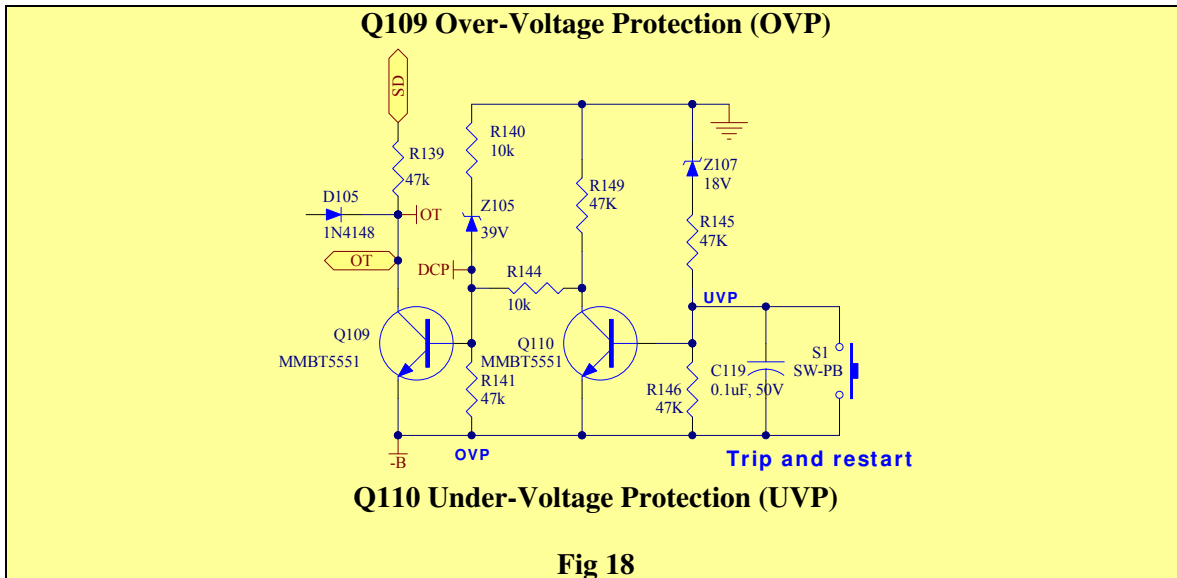


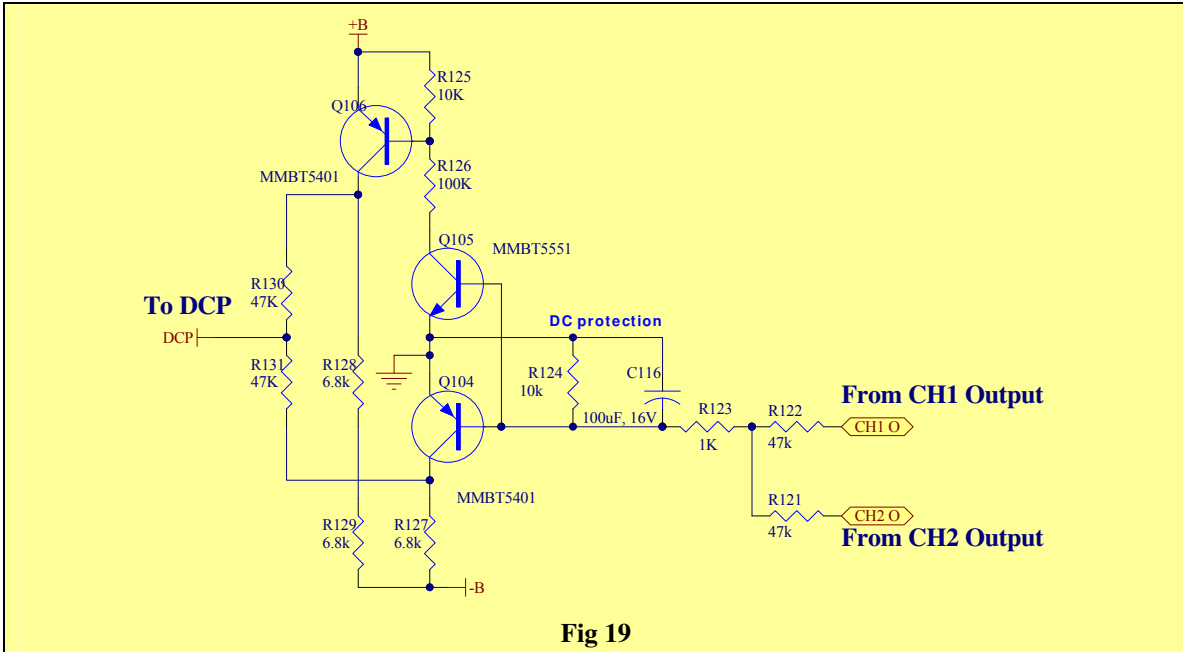
Fig 18

### Under-Voltage Protection (UVP, Fig18)

UVP will shutdown the amplifier if the bus voltage between GND and -B falls below 20V. The threshold is determined by the voltage sum of the Zener diode Z107, R145 and  $V_{BE}$  of Q110. As with OVP, UVP will automatically reset after three seconds, and only one of the two supply voltages needs to be monitored.

### Speaker DC-Voltage Protection (DCP, Fig 19)

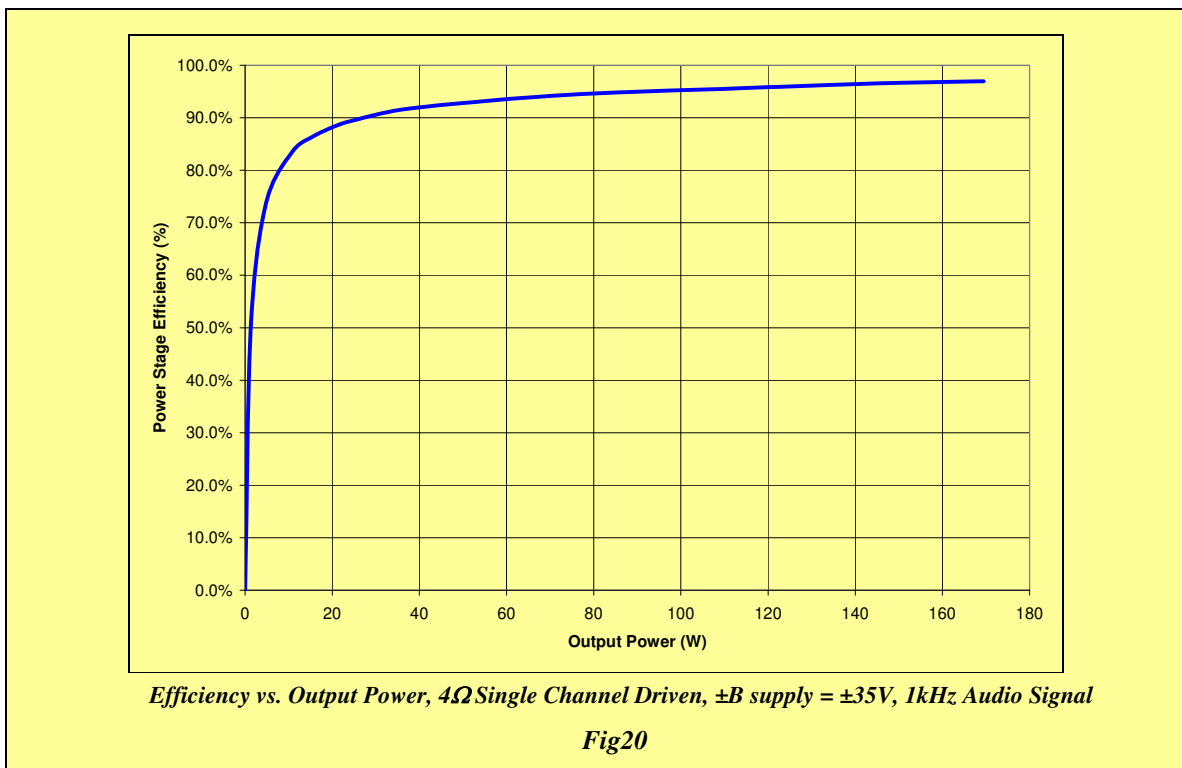
DCP is provided to protect against DC current flowing into the speakers. This abnormal condition is rare and is likely caused when the power amplifier fails and one of the high-side or low-side IRF6645 DirectFET MOSFETs remain in the ON state. DCP is activated if either of the outputs has more than  $\pm 4V$  DC offset (typical). Under this fault condition, it is normally required to shutdown the feeding power supplies. Since these are external to the reference design board, an isolated relay P1 is provided for further systematic evaluation of DC-voltage protection. This condition is transmitted to the power supply controller through connector J9, whose pins are shorted during a fault condition.



### Efficiency

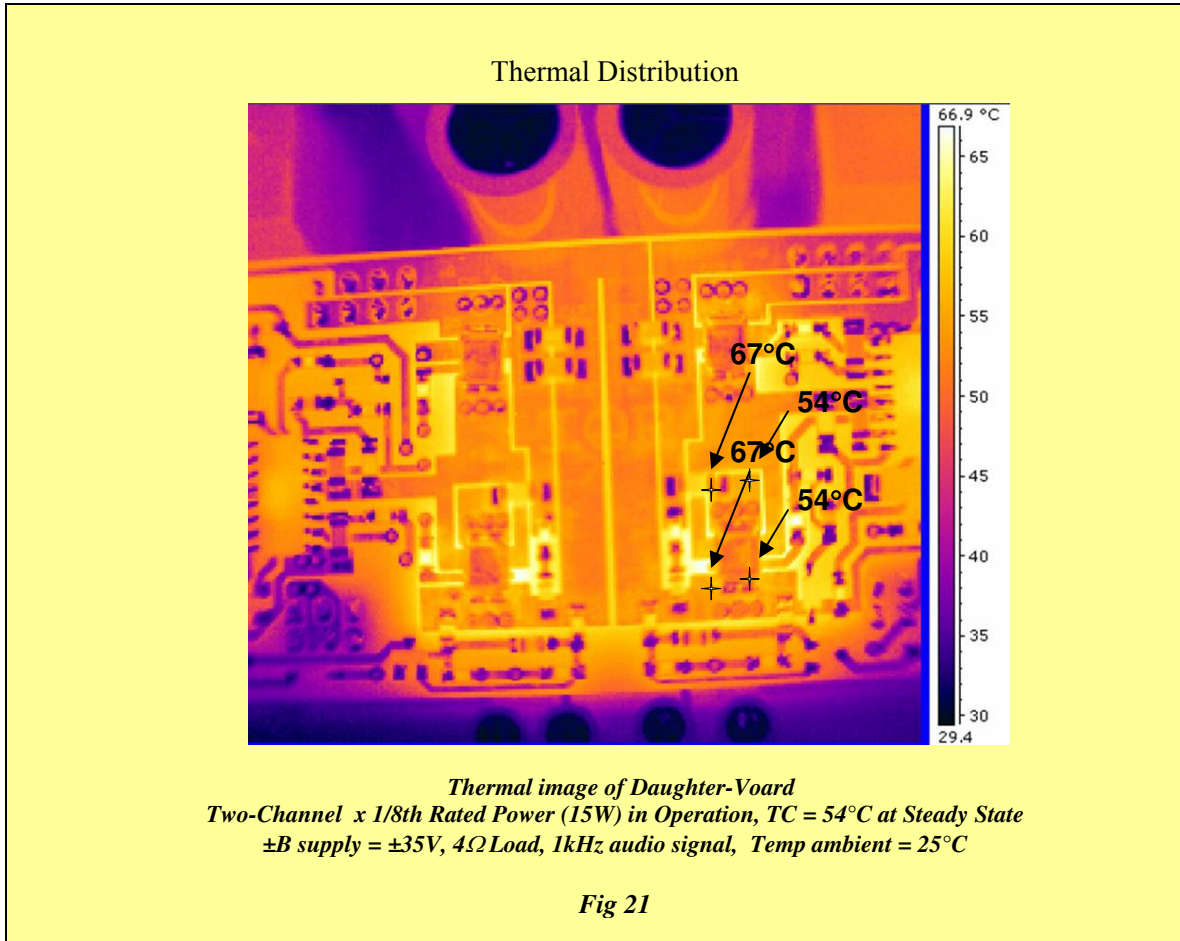
Figs 20 demonstrate that IRAUDAM5 is highly efficient, due to two main factors:

- a.) DirectFETs offer low  $R_{DS(ON)}$  and very low input capacitance, and b). The PWM operates as Pulse Density Modulation.



### Thermal Considerations

The daughter-board design can handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards. Without the addition of a heatsink or forced air-cooling, the daughter board cannot handle fully rated continuous power. A thermal image of the daughter board is as shown in Fig 21 below.



### Click and POP noise:

One of the most important aspects of any audio amplifier is the startup and shutdown procedures. Typically, transients occurring during these intervals can result in audible pop- or click-noise from the output speaker. Traditionally, these transients have been kept away from the speaker through the use of a series relay that connects the speaker to the audio amplifier only after the startup transients have passed and disconnects the speaker prior to shutting down the amplifier.

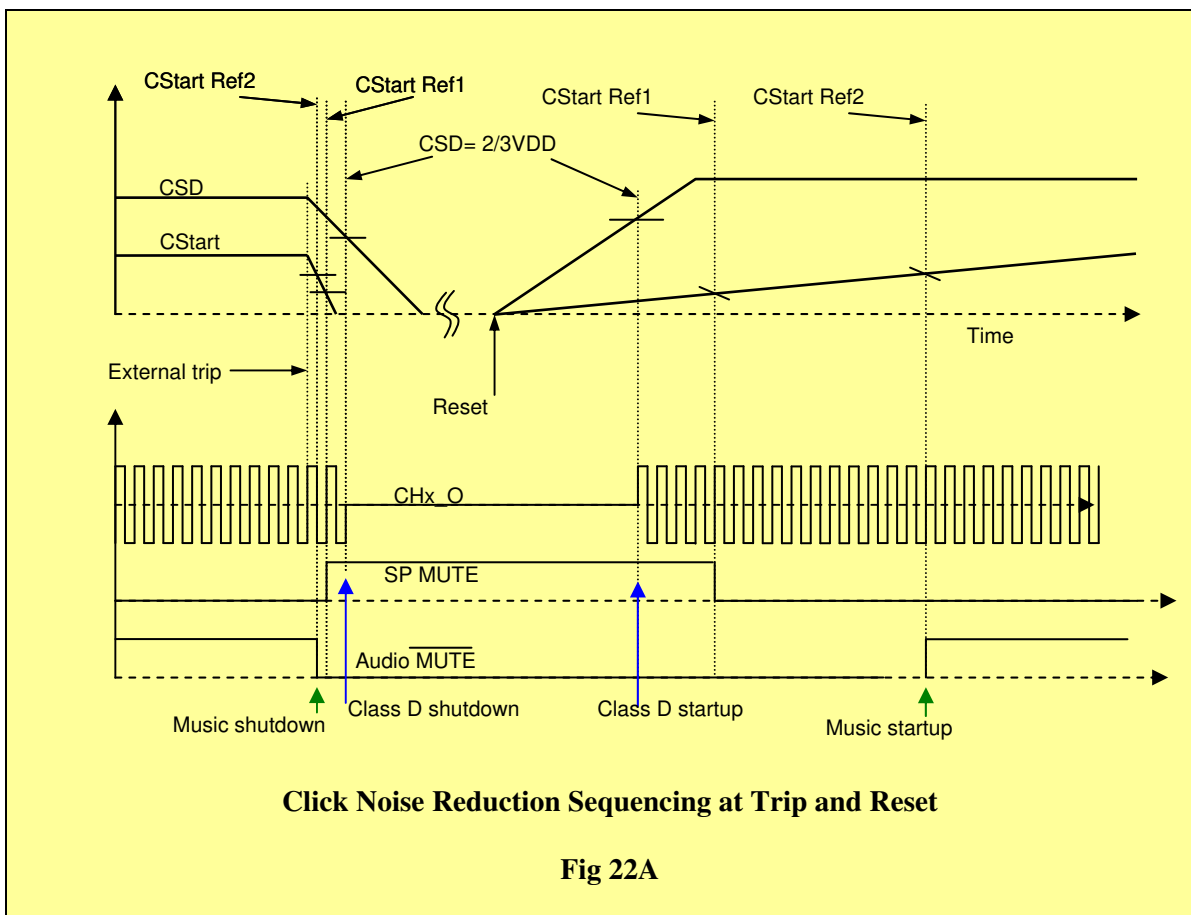
Thanks to the click and pop elimination function in the IRS2092S, IRAUDAMP5 does not use any series relay to disconnect the speaker from the audible transient noise.

### Click-Noise Reduction Circuit (Solid-State Shunt)

IRS2092S controller is relatively quiet with respect to class AB, but for additional click or POP noise reduction you may add a shunt circuit that further attenuates click or pop transients during turn on sequencing. The circuit is not populated on the present demo board; for implementation details, please refer to the IRAUDAMP4 user's manual at <http://www.irf.com/technical-info/refdesigns/audiokits.html>

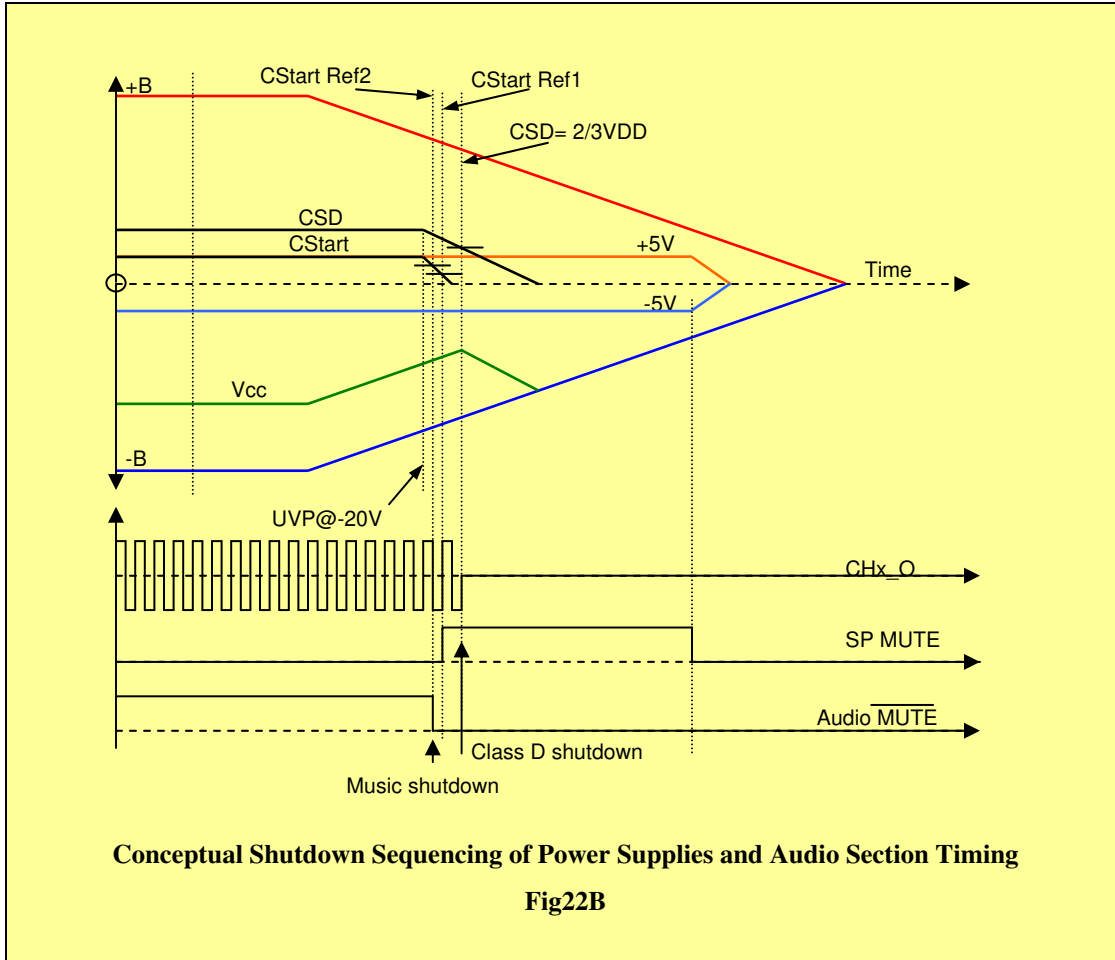
### Startup and Shutdown Sequencing (Fig 22)

The IRAUDAMP5 sequencing is achieved through the charging and discharging of the CStart capacitor C117. Along with the charging and discharging of the CSD voltage (C10 on daughter board for CH1) of the IRS2092S, this is all that is required for complete sequencing. The startup and shutdown timing diagrams are show in Figure 22A below:



For startup sequencing, the control power supplies start up at different intervals depending on the  $\pm B$  supplies. As the  $+/-B$  supplies reach +5 volts and -5 volts respectively, the  $+/-5V$  control supplies for the analog input start charging. Once +B reaches  $\sim 16V$ , VCC charges. Once -B reaches -20V, the UVP is released and CSD and CStart (C117) start charging. The Class D amplifier is now operational, but the preamp output remains muted until CStart reaches Ref2. At this point, normal operation begins. The entire process takes less than three seconds.

For Shutdown (Fig22B) sequencing is initiated once UVP is activated. As long as the supplies do not discharge too quickly, the shutdown sequence can be completed before the IRS2092S trips UVP. Once UVP is activated, CSD and CStart are discharged at different rates. In this case, threshold Ref2 is reached first and the preamp audio output is muted. It is then possible to shutdown the Class D stage (CSD reaches two-thirds VDD). This process takes less than 200ms.

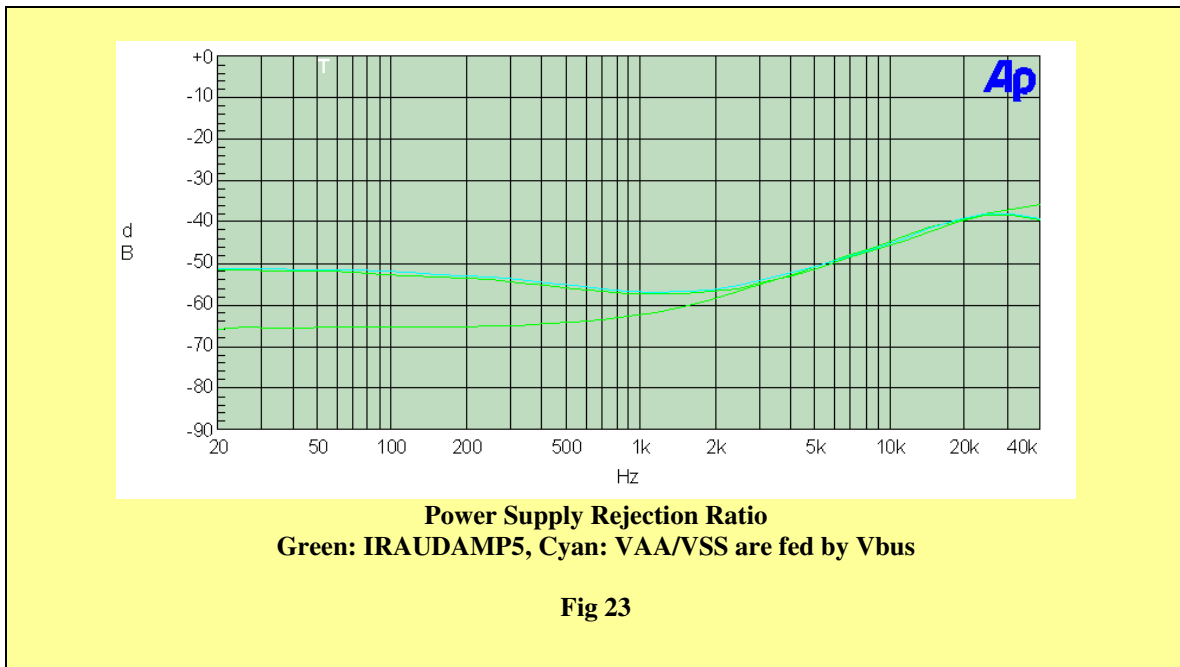


For any external fault condition (OTP, OVP, UVP or DCP – see “Protection”) that does not lead to power supply shutdown, the system will trip in a similar manner as described above. Once the fault is cleared, the system will reset (similar sequence as startup).

### Power Supplies

The IRAUDAMP5 has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies ranging from  $\pm 25V$  to  $\pm 35V$  (+B, GND, -B) for operation. The internally-generated housekeeping power supplies include a  $\pm 5V$  supply for analog signal processing (preamp etc.), while a +12V supply (VCC), referenced to -B, is included to supply the low and high side Class D gate-driver stages.

For the externally-applied power, a regulated power supply is preferable for performance measurements, but is not always necessary. The bus capacitors, C31 and C32 on the motherboard, along with high-frequency bypass-caps C14, C15; C32 and C33 on the daughter board, address the high-frequency ripple current that results from switching action. In designs involving unregulated power supplies, the designer should place a set of external bus capacitors having enough capacitance to handle the audio-ripple current. Overall regulation and output voltage ripple for the power supply design are not critical when using the IRAUDAMP5 Class D amplifier as the power supply rejection ratio (PSRR) of the IRAUDAMP5 is excellent, as shown on Figure 23 below.



### Bus Pumping (Fig24)

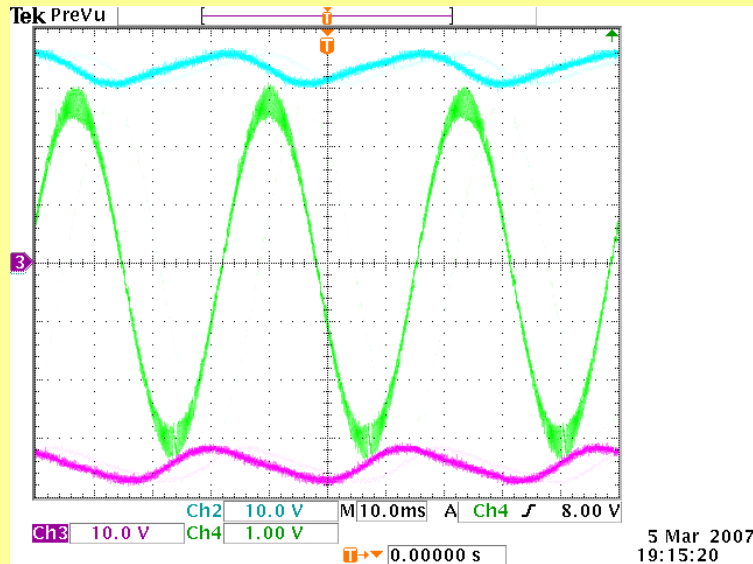
Since the IRAUDAMP5 is a half-bridge configuration, bus pumping does occur. Under normal operation during the first half of the cycle, energy flows from one supply through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage of the receiving power supply. In the second half of the cycle, this condition is reversed, resulting in bus pumping of the other supply.

These conditions worsen bus pumping:

1. Lower frequencies (bus-pumping duration is longer per half cycle)
2. Higher power output voltage and/or lower load impedance (more energy transfers between supplies)

3. Smaller bus capacitors (the same energy will cause a larger voltage increase)

The IRAUDAMP5 has protection features that will shut down the switching operation if the bus voltage becomes too high (>40V) or too low (<20V). One of the easiest countermeasures is to drive both of the channels in a stereo configuration out of phase so that one channel consumes the energy flow from the other and does not return it to the power supply. Bus voltage detection is only done on the -B supply, as the effect of the bus pumping on the supplies is assumed to be symmetrical in amplitude (although opposite in phase) with the +B supply.



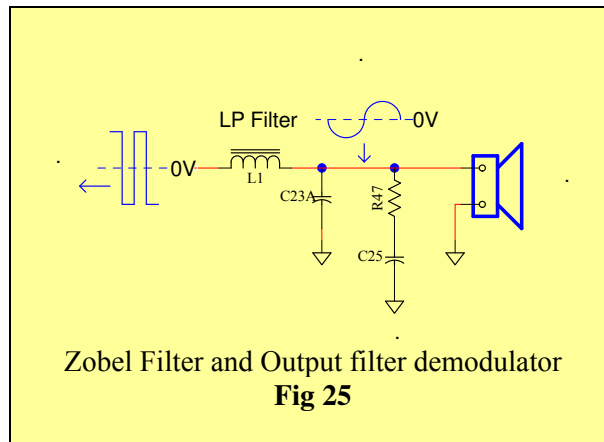
Bus Pumping Figure:  
Cyan = Positive Rail voltage (+B)  
Green = Speaker Output  
Pink = Negative Rail voltage (-B)

**Fig 24**

**Input Signal**

A proper input signal is an analog signal below 20 kHz, up to  $\pm 3.5V$  peak, having a source impedance of less than 600 ohms. A 30-60 kHz input signal can cause LC resonance in the output LPF, resulting in an abnormally large amount of reactive current flowing through the switching stage (especially at 8 ohms or higher impedance towards open load), and causing OCP activation. The IRAUDAMP5 has an RC network (Fig25), or Zobel network (R47 and C25 [CH1]), to dampen the resonance and protect the board in such an event, but is not thermally rated to handle continuous supersonic frequencies. *These supersonic input frequencies therefore should be avoided.* Separate mono RCA connectors provide input to each of the two channels. Although both channels share a common ground, it is necessary to connect each channel separately to limit noise and crosstalk between channels.



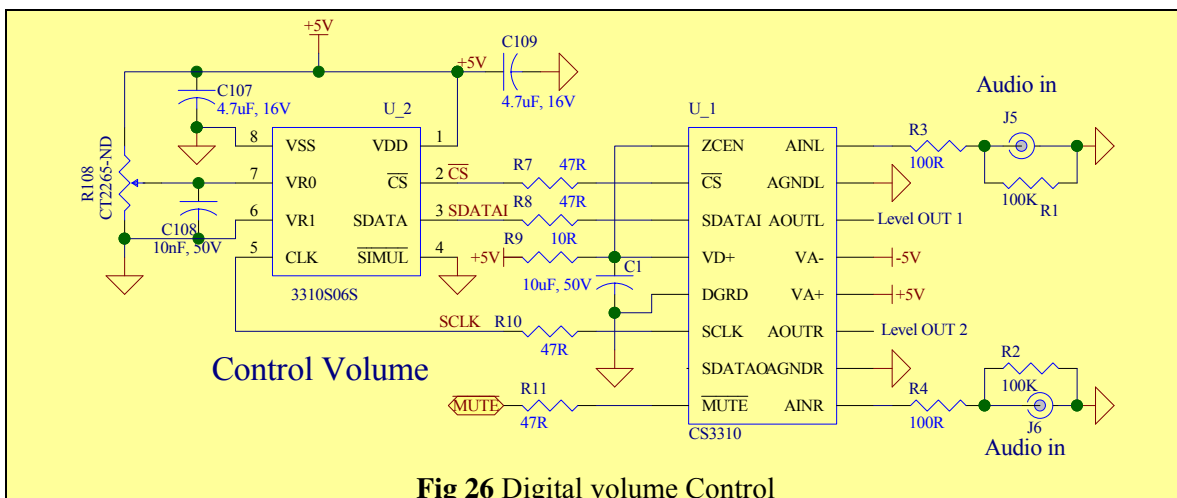


### Output

Both outputs for the IRAUDAMP5 are single-ended and therefore have terminals labeled (+) and (-), with the (-) terminal connected to power ground. Each channel is optimized for a 4-Ohm speaker load for a maximum output power (120W), but is capable of operating with higher load impedances (at reduced power), at which point the frequency response will have a small peak at the corner frequency of the output LC low pass filter. The IRAUDAMP5 is stable with capacitive-loading; however, it should be noted that the frequency response degrades with heavy capacitive loading of more than 0.1 $\mu$ F.

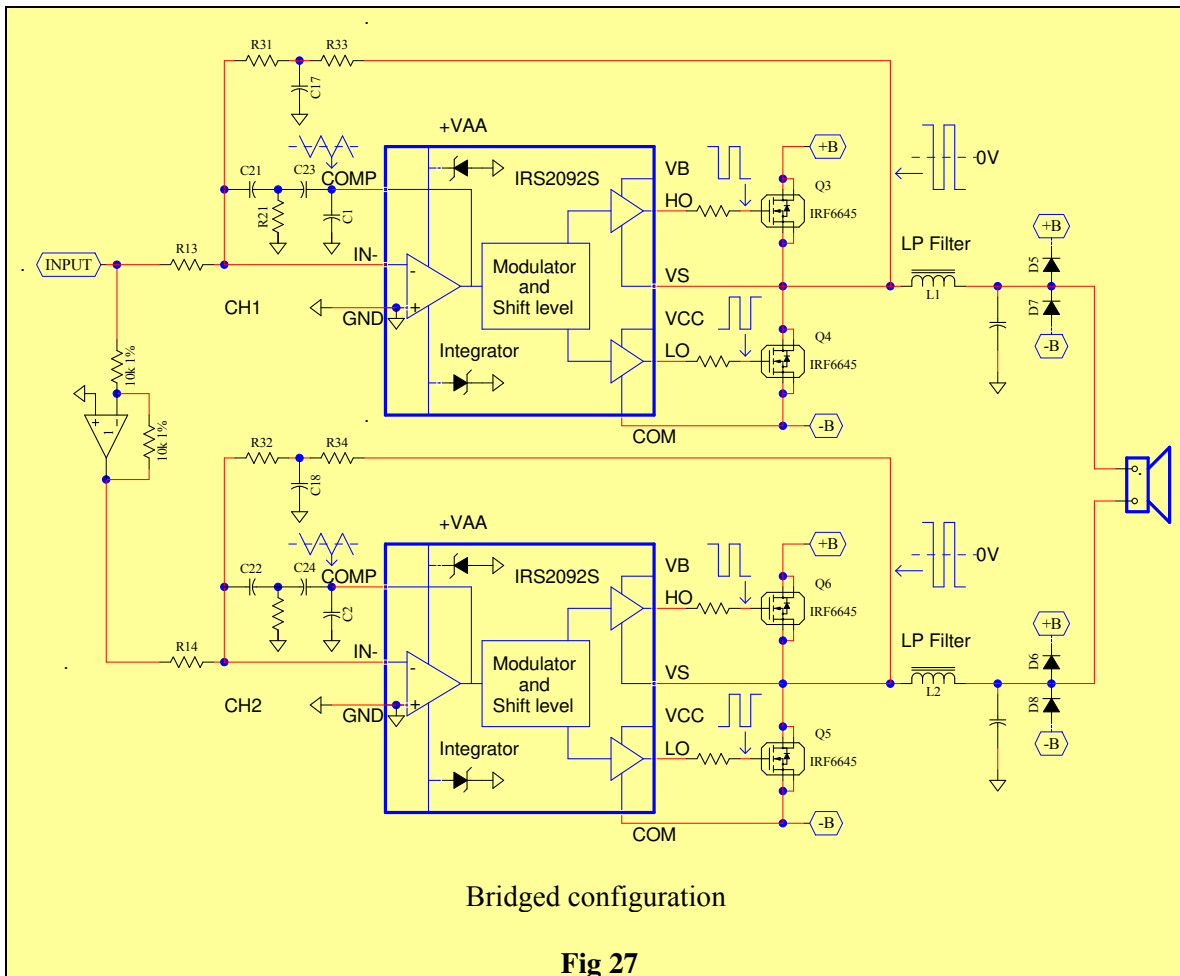
### Gain Setting / Volume Control

The IRAUDAMP5 has an internal volume control (potentiometer R108 labeled, "VOLUME", Fig 26) for gain adjustment. Gain settings for both channels are tracked and controlled by the volume control IC (U\_2), setting the gain from the microcontroller IC (U\_1). The maximum volume setting (clockwise rotation) corresponds to a total gain of +37.9dB (78.8V/V). The total gain is a product of the power-stage gain, which is constant (+23.2dB), and the input-stage gain that is directly-controlled by the volume adjustment. The volume range is about 100dB, with minimum volume setting to mute the system with an overall gain of less than -60dB. For best performance in testing, the internal volume control should be set to a gain of 21.9V/V, such that 1Vrms input will result in rated output power (120W into 4 $\Omega$ ), allowing for a >1 dB overdrive.



### Bridged Output

The IRAUDAMP5 is not intended for a bridge-tied-load, or BTL configuration. However, BTL operation can be achieved by feeding out-of-phase audio input signals to the two input channels as shown in the figure 27 below. In BTL operation, minimum load impedance is 8 Ohms and rated power is 240W non-clipping. The installed clamping diodes D5 – D8 are required for BTL operation, since reactive energy flowing from one output to the other during clipping can force the output voltage beyond the voltage supply rails if not clamped.



### Output Filter Design, Preamplifier and Performance

The audio performance of IRAUDAMP5 depends on a number of different factors. The section entitled, “Typical Performance” presents performance measurements based on the overall system, including the preamp and output filter. While the preamp and output filter are not part of the Class D power stage, they have a significant effect on the overall performance.

#### Output filter

Since the output filter is not included in the control loop of the IRAUDAMP5, the reference design cannot compensate for performance deterioration due to the output filter. Therefore, it is important to understand what characteristics are preferable when designing the output filter: