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International
IOR Rectifier

REFERENCE DESIGN

IRAUDAMP6

250W/8Ω x 2 Channel Class D Audio Power Amplifier Using the IRS20957S and IRF6785

By

Jun Honda, Jorge Cerezo and Liwei Zheng

CAUTION:

International Rectifier suggests the following guidelines for safe operation and handling of IRAUDAMP6 Demo board;

- **Always wear safety glasses whenever operating Demo Board**
- **Avoid physical contact with exposed metal surfaces when operating Demo Board**
- **Turn off Demo Board when placing or removing measurement probes**

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Introduction

The IRAUDAMP6 reference design is a two-channel, 250W/ch (8Ω) load half-bridge Class D audio power amplifier. This reference design demonstrates how to use the IRS20957S Class D audio controller and gate driver IC, implement protection circuits, and design an optimum PCB layout using the IRF6785 DirectFET MOSFETs. This reference design does not require increasing the size of the heatsink or require fan cooling for normal operation (one-eighth of continuous rated power).The reference design provides all the required housekeeping power supplies for ease of use. The two-channel design is scalable for power and the number of channels.

Applications

- AV receivers
- Home theater systems
- Mini component stereos
- Powered speakers
- Sub-woofers
- Musical Instrument amplifiers

Features

Output Power:	250W x 2 channels (8Ω load),
Residual Noise:	90μV, IHF-A weighted, AES-17 filter
Distortion:	0.005% THD+N @ 125W, 8Ω
Efficiency:	96% @ 250W, 8Ω, single-channel driven, Class D stage
Multiple Protection Features:	Over-current protection (OCP), high side and low side Over-voltage protection (OVP), Under-voltage protection (UVP), high side and low side DC-protection (DCP), Over-temperature protection (OTP)
PWM Modulator:	Self-oscillating half-bridge topology with optional clock synchronization

Specifications

General Test Conditions (unless otherwise noted)		Notes / Conditions
Supply Voltages	±73.5V	
Load Impedance	8-4Ω	
Self-Oscillating Frequency	400kHz	No input signal, Adjustable
Gain Setting	33dB	1Vrms input yields rated power

Electrical Data	Typical	Notes / Conditions
IR Devices Used	IRS20957S Audio Controller and Gate-Driver, IRF6785 DirectFET MOSFETs	
Modulator	Self-oscillating, second order sigma-delta modulation, analog input	
Power Supply Range	± 38V to ±75V	Bipolar power supply
Output Power CH1-2: (1% THD+N)	320W	1kHz
Output Power CH1-2: (10% THD+N)	410W	1kHz

Rated Load Impedance	8-4Ω	Resistive load
Idling Supply Current	±85mA	No input signal
Total Idle Power Consumption	11.9W	No input signal
Channel Efficiency	96%	Single-channel driven, 250W, Class D stage

.

Audio Performance	***Before Demodulator**	**Class D Output**	**Notes / Conditions**
THD+N, 1W THD+N, 10W THD+N, 60W THD+N, 100W THD+N, 200W	0.008% 0.003% 0.0015% 0.002% 0.009%	0.008% 0.004% 0.002% 0.004% 0.009%	1kHz, Single-channel driven
Dynamic Range	117dB	113dB	A-weighted, AES-17 filter, Single-channel operation
Residual Noise, 22Hz - 20kHzAES17	70μV	110μV	Self-oscillating – 400kHz
Damping Factor	2000	906	1kHz, relative to 8Ω load
Channel Separation	92dB 90dB 72dB	92dB 80dB 62dB	100Hz 1kHz 10kHz
Frequency Response : 20Hz-20kHz : 20Hz-35kHz	N/A	±0.25dB ±1dB	1W, 8Ω Load

Thermal Performance	**Typical**	**Notes / Conditions**
Idling	T_C =30°C T_{PCB}=36°C	No signal input, T_A=25°C
2ch x 31.25W (1/8 rated power)	T_C =54°C T_{PCB}=65°C	Continuous, T_A=25°C
2ch x 250W (Rated power)	T_C =80°C T_{PCB}=106°C	At OTP shutdown @ 150 sec, T_A=25°C

Physical Specifications

Dimensions	7.76”(L) x 5.86”(W) x 2.2”(H) 192 mm (L) x 149mm (W) x56mm(H)
Weight	0.54kgm

Connection Setup

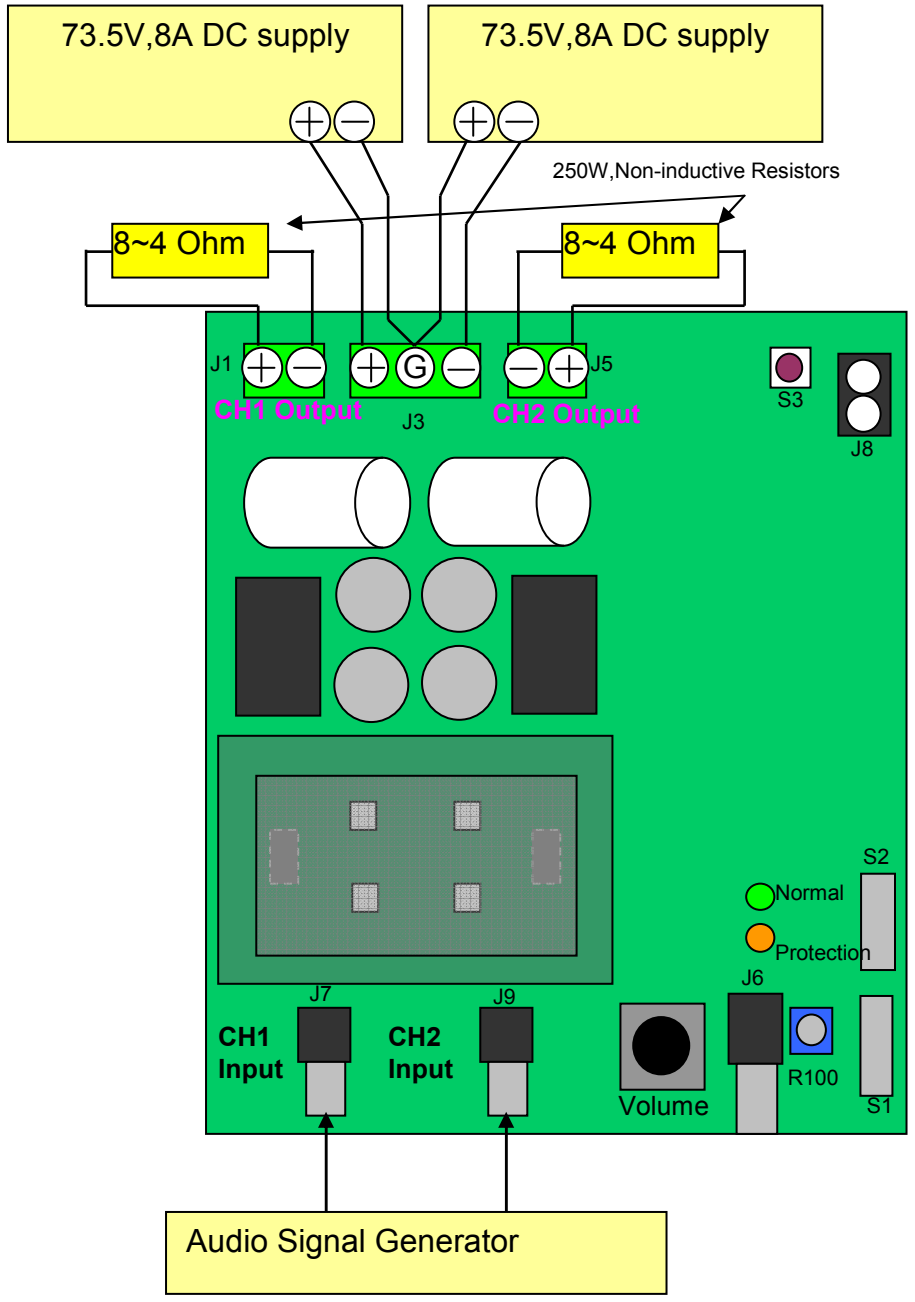


Fig 1 Typical Test Setup

Connector Description

CH1 IN	J7	Analog input for CH1
CH2 IN	J9	Analog input for CH2
POWER	J3	Positive and negative supply (+B / -B)
CH1 OUT	J1	Output for CH1
CH2 OUT	J5	Output for CH2
EXT CLK	J6	External clock sync
DCP OUT	J8	DC protection relay output

Test Procedures

Test Setup:

1. Connect 8Ω-250 W dummy loads to output connectors (J1 and J5 as shown on Fig 1) and parallel it with input of Audio Precision analyzer (AP).
2. Connect the Audio Signal Generator to J7 and J9 for CH1 and CH2 respectively (AP).
3. Set up the dual power supply with voltages of ±73.5V;set current limit to 8A.
4. TURN OFF the dual power supply before connecting to ON of the unit under test (UUT).
5. Set switch S1 to middle position (self oscillating).
6. Set volume level knob R130 fully counter-clockwise (minimum volume).
7. Connect the dual power supply to J3. as shown on Fig 1

Power up:

8. Turn ON the dual power supply. The ±B supplies must be applied and removed at the same time.
9. Red LED (Protection) should turn on almost immediately and turn off after about 3s.
10. Green LED (Normal) then turns on after red LED is extinguished and should stay on.
11. Quiescent current for the positive supply should be 84mA ±10mA at +73.5V.
12. Quiescent current for the negative supply should be 80mA ±10mA at –73.5V.
13. Push S3 switch(Trip and Reset push-buttom)to restart the sequence of LEDs indicators,which should be the same as noted above in steps 9-10.

Switching Frequency test

14. Monitor switching waveform at VS1/J4(pin9-12)of CH1 and VS2/J3(pin1-4)CH2 on Daughter Board using an Oscilloscope.
15. For IRAUDAMP6, the self-oscillating switching frequency is pre-calibrated to 400 KHz. To modify the IRAUDAMP6 frequency, change the values of potentiometers R49 and R74 for CH1 and CH2 respectively.

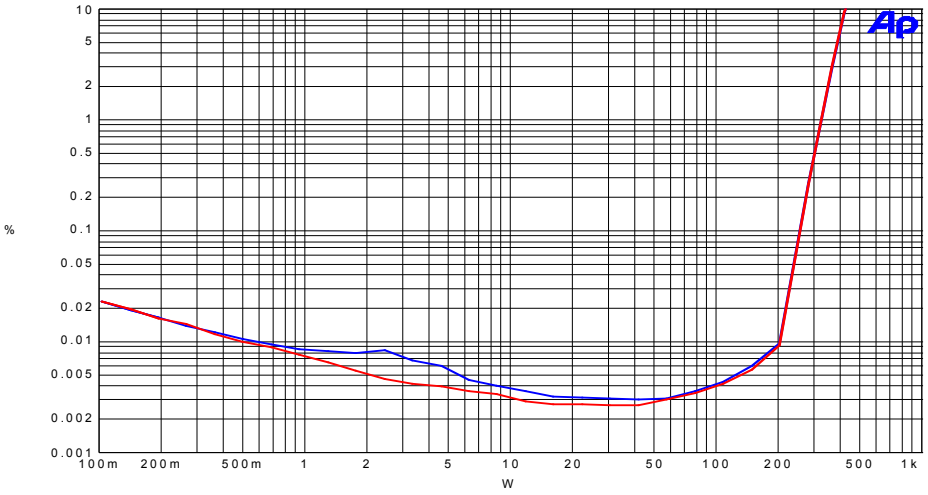
Functionality Audio Tests:

16. Apply 1V RMS at 1kHz sinusoidal signal from the Audio Signal Generator.
17. Turn control volume up (R130 clock-wise) to obtain an output reading of 250Watts.
18. For all subsequent tests as shown on the Audio Precision graphs below (Fig 2- Fig7), the measurements are taken across J1 and J5 with an AES-17 Filter. Observe that a 1 V_{RMS} input generates an output voltage of 44.7 V_{RMS}.
19. Sweep the audio signal voltage from 15 mV_{RMS} to 1 V_{RMS}.
20. Monitor the output signals at J1/J5 with an oscilloscope. The waveform must be a non distorted sinusoidal signal.

Test Setup using Audio Precision (Ap):

21. Use an unbalanced-floating signal from the generator outputs.
22. Use balanced inputs taken across output terminals, J1 and J5.
23. Connect Ap frame ground to GND at terminal J7/J9.
24. Select the AES-17 filter(pull-down menu) for all the testing except frequency response.
25. Sweep the input signal voltage from 15 mV_{RMS} to 1 V_{RMS}.
26. Run Ap test programs for all subsequent tests as shown in Fig 2- Fig 7below.

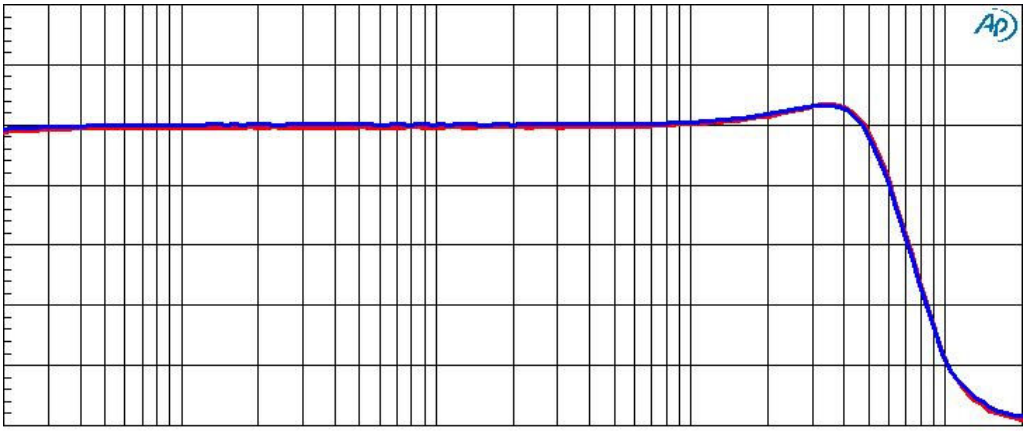
Performance and test graphs



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	2	Anlr.THD+N Ratio	Left	CH2
1	3	Red	Solid	2	Anlr.THD+N Ratio	Left	CH1

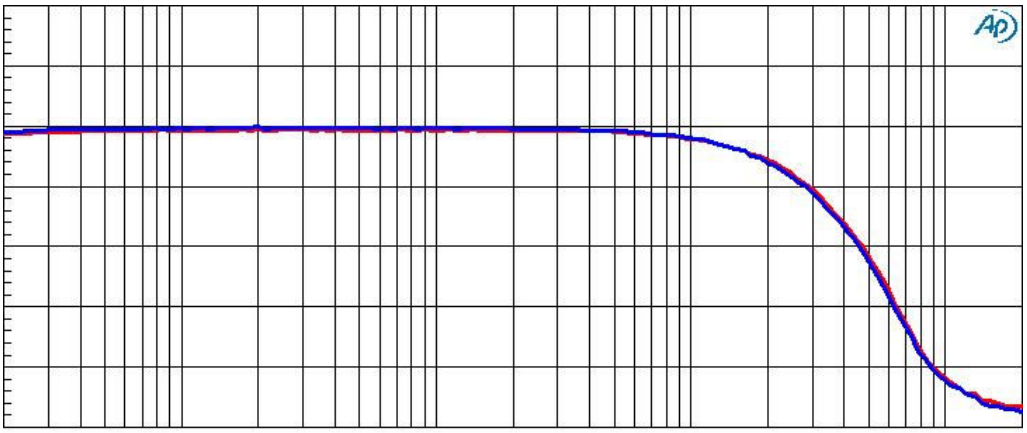
±B Supply = ±73.5V, 8 Ω Resistive Load

Fig 2 IRAUDAMP6, THD+N versus Power, Stereo, 8 Ω



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	2	Red	Solid	3	Anlr.Level B	Left	CH1_8Ohm
2	2	Blue	Solid	3	Anlr.Level B	Left	CH2_8Ohm

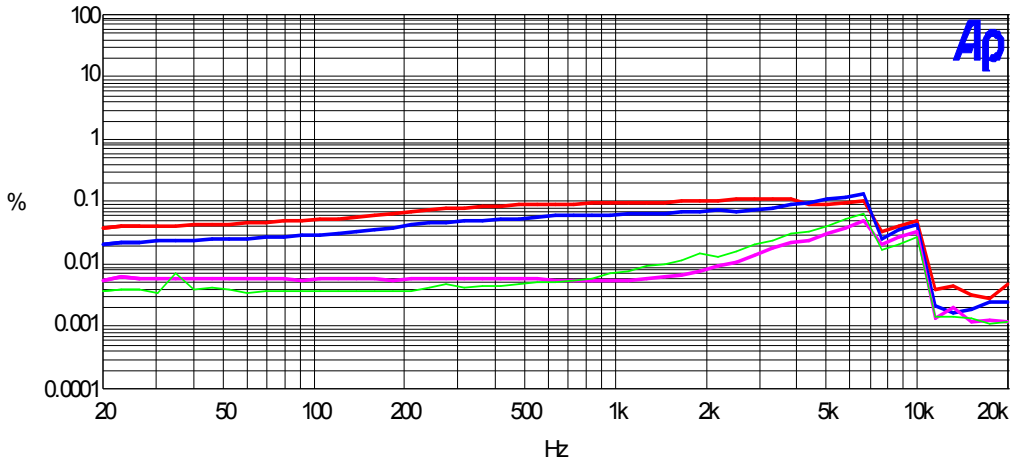
8 ohm load



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	2	Red	Solid	3	Anlr.Level B	Left	CH1_4Ohm
2	2	Blue	Solid	3	Anlr.Level B	Left	CH2_4Ohm

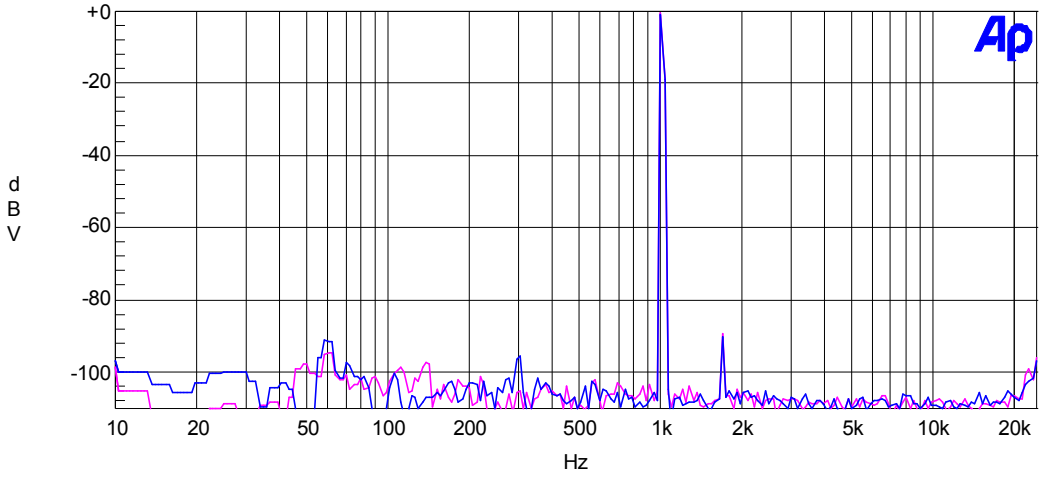
4 ohm load

Fig 3 IRAUDAMP6, Frequency response



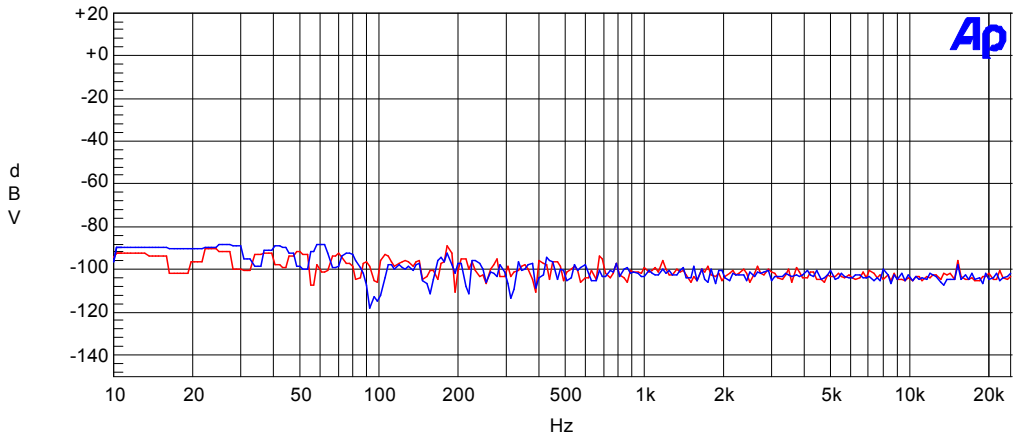
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ratio	Left	125W L
1	2	Blue	Solid	2	Anlr.THD+N Ratio	Left	125W R
2	1	Magenta	Solid	2	Anlr.THD+N Ratio	Left	25W L
2	2	Green	Solid	1	Anlr.THD+N Ratio	Left	25W R

Fig 4 THD+N Ratio vs. Frequency



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Magenta	Solid	1	Fft.Ch.1 Ampl	Left	
1	2	Blue	Solid	1	Fft.Ch.2 Ampl	Left	

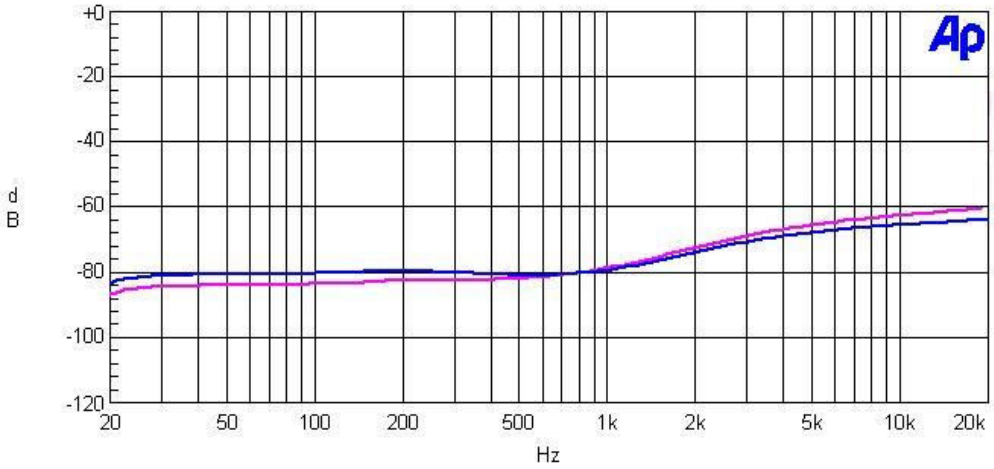
Fig 5, 1V output Frequency Spectrum



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	Fft.Ch.1 Ampl	Left	
1	2	Blue	Solid	1	Fft.Ch.2 Ampl	Left	

No signal, Self Oscillator @ 400kHz

Fig 6, IRAUDAMP6 Noise Floor



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Magenta	Solid	2	Anlr.Ratio	Left	CH1
1	2	Blue	Solid	2	Anlr.Ratio	Left	CH2

Fig 7, Channel separation vs. frequency

IRAUDAMP6 Overview

The IRAUDAMP6 features a 2CH self-oscillating type PWM modulator for the lowest component count, highest performance and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of error correction.

The IRAUDAMP6 self-oscillating topology consists of following essential functional blocks.

- Front-end integrator
- PWM comparator
- Level shifters
- Gate drivers and MOSFETs
- Output LPF

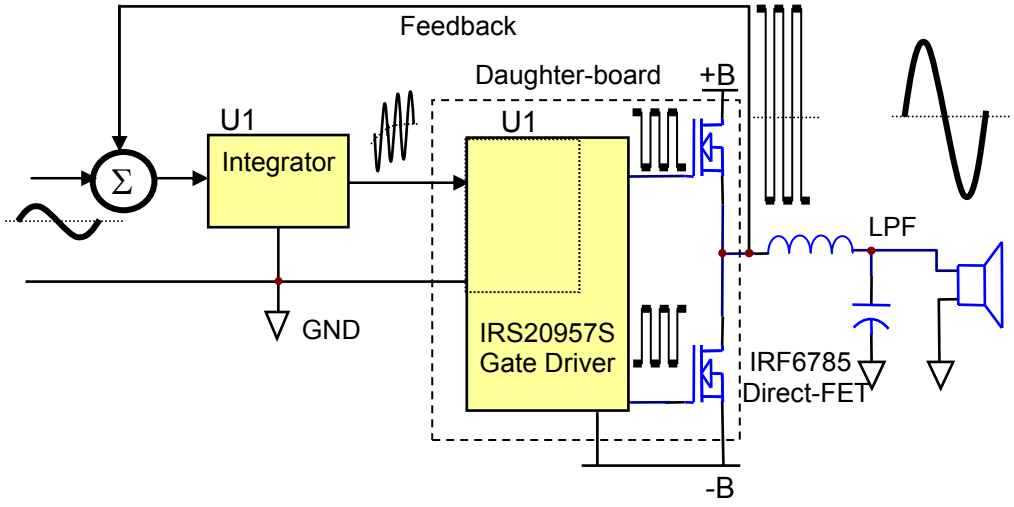


Fig 8, Simplified Block Diagram of Class D Amplifier

Functional Descriptions

Class D Operation

Referring to CH1 as an example, the op-amp U6 forms a front-end second-order integrator with C38, C42 & R50 + R49P. This integrator receives a rectangular feedback waveform from the Class D switching stage and outputs a quadratic oscillatory waveform as a carrier signal. To create the modulated PWM signal, the input signal shifts the average value of this quadratic waveform (through gain relationship between R40,AR154 and R38 + R39) so that the duty varies according to the instantaneous value of the analog input signal. The IRS20957 input comparator processes the signal to create the required PWM signal. This PWM signal is internally level-shifted down to the negative supply rail where this signal is split into two signals, with opposite polarity and added deadtime, for high-side and low-side MOSFET gate signals, respectively. The IRS20957 drives two IRF6785 DirectFET MOSFETs in the power stage to provide the amplified PWM waveform. The amplified analog output is re-created by demodulating the amplified PWM. This is done by means of the LC low-pass filter (LPF) formed by L4 and C34, which filters out the Class D switching carrier signal.

Power Supplies

The IRAUDAMP6 has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies ranging from ±38 V to ±82 V (+B, GND, -B) for operation. The internally-generated housekeeping power supplies include a ±5 V supply for analog signal processing (preamp, etc.), while a +12 V supply (V_{CC}), referenced to –B, is included to supply the Class D gate-driver stage.

For the externally-applied power, a regulated power supply is preferable for performance measurements, but not always necessary. The bus capacitors, C45 ~ C48 on the motherboard, along with high-frequency bypass-caps C19 ~ C26 on daughter board, address the high-frequency ripple current that result from switching action. In designs involving unregulated power supplies, the designer should place a set of bus capacitors, having enough capacitance to handle the audio-ripple current, externally. Overall regulation and output voltage ripple for the power supply design are not critical when using the IRAUDAMP6 Class D amplifier as the power supply rejection ratio (PSRR) of the IRAUDAMP6 is excellent (Fig 9).

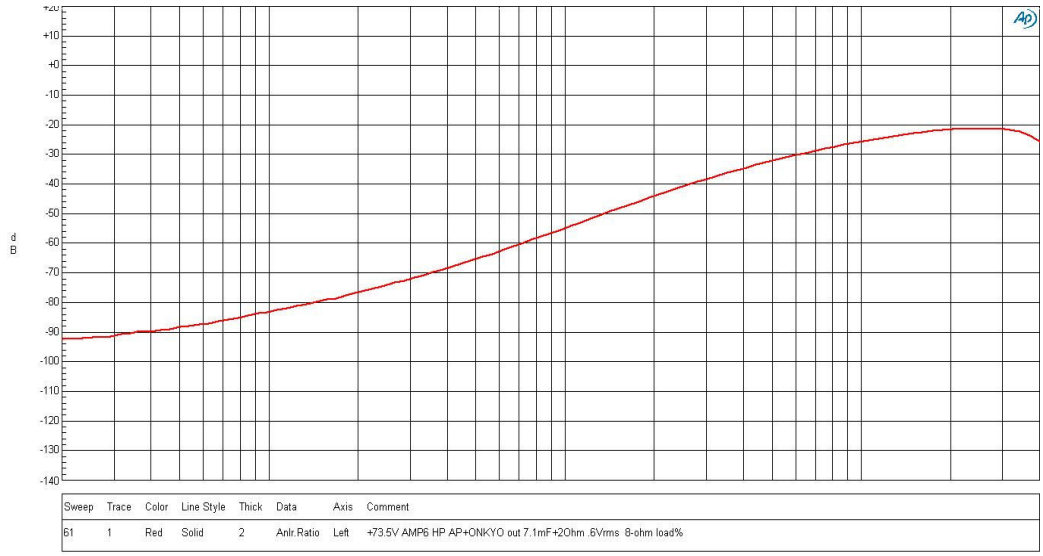


Fig 9, Amp6 Power Supply Rejection Ratio (PSRR)

Bus Pumping

Since the IRAUDAMP6 is a half-bridge configuration, bus pumping does occur. Under normal operation during the first half of the cycle, energy flows from one supply through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage of the receiving power supply. In the second half of the cycle, this condition is opposite, resulting in bus pumping of the other supply.

These conditions worsen bus pumping:

– Lower frequencies (bus-pumping duration is longer per half cycle)
– Higher power output voltage and/or lower load impedance (more energy transfers between supplies)
– Smaller bus capacitors (the same energy will cause a larger voltage increase)

The IRAUDAMP6 has protection features that will shutdown the switching operation if the bus voltage becomes too high (>82 V) or too low (<36 V). One of the easiest countermeasures is to drive both of the channels out of phase so that one channel consumes the energy flow from the other and does not return it to the power supply. Bus voltage detection is only done on the –B supply as the effect of the bus pumping on the supplies is assumed to be symmetrical in amplitude (although opposite in phase).

House Keeping Power Supply

The internally-generated housekeeping power supplies include ±5V for analog signal processing, and +12V supply (V_{CC}) referred to the negative supply rail -B for DirectFET gate drive. The gate driver section of the IRS20957 uses VCC to drive gates of the DirectFETs. V_{CC} is referenced to –B (negative power supply). D6, R4 and C15 form a bootstrap floating supply for the HO gate driver.

Input

A proper input signal is an analog signal ranging from 20Hz to 20kHz with up to 3 V_{RMS} amplitude with a source impedance of no more than 600 Ω. Input signal with frequencies from 30kHz to 60kHz may cause LC resonance in the output LPF, causing a large reactive current flowing through the switching stage, and the LC resonance can activate OCP.

The IRAUDAMP6 has an RC network called a Zobel network (R45 and C36) to damp the resonance and prevent peaking frequency response with light loading impedance. (Fig 10), but is not thermally rated to handle continuous supersonic frequencies. These supersonic input frequencies therefore should be avoided. Separate mono RCA connectors provide input to each of the two channels. Although both channels share a common ground, it is necessary to connect each channel separately to limit noise and crosstalk between channels.

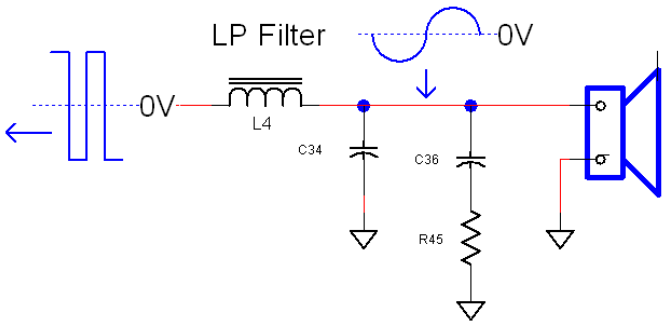


Fig 10 Output Low Pass Filter and Zobel Network

Output

Both outputs for the IRAUDAMP6 are single-ended and therefore have terminals labeled (+) and (-) with the (-) terminal connected to power ground. Each channel is optimized for a 8 Ω speaker load for a maximum output power of 250 W.

Load Impedance

Each channel is optimized for a 8 Ω speaker load in half bridge.

Gain Setting / Volume Control

The IRAUDAMP6 has an internal volume control (potentiometer R130 labeled, “VOLUME”) for gain adjustment. Gain settings for both channels are tracked and controlled by the volume control IC (U_2) setting the gain from the microcontroller IC (U_3). The total gain is a product of the power-stage gain, which is constant (+33 dB), and the input-stage gain that is directly-controlled by the volume adjustment. The volume range is about 100 dB with minimum volume setting to mute the system with an overall gain of less than -60 dB. For best performance in testing, the internal volume control should be set to 1 Vrms input will result in rated output power (250 W into 8 Ω).

Efficiency

Fig 11 shows efficiency characteristics of the IRAUDAMP6. The high efficiency is achieved by following major factors:

1) Low conduction loss due to the DirectFETs offering low $R_{DS(ON)}$
2) Low switching loss due to the DirectFETs offering low input capacitance for fast rise and fall times

Secure dead-time provided by the IRS20957, avoiding cross-conduction

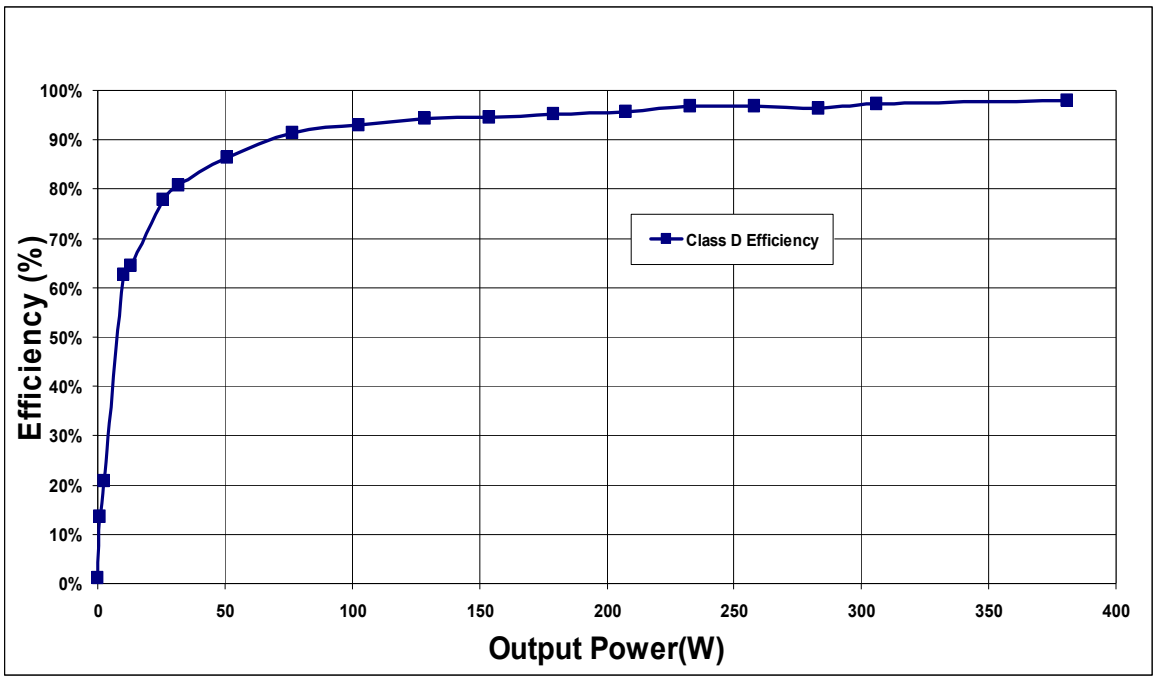


Fig 11, IRAUDAMP6 8 ohms load Stereo, ±B supply = ±73.5V

Output Filter Design and Preamplifier

The audio performance of the IRAUDAMP6 depends on a number of different factors. The section entitled, “Typical Performance” presents performance measurements based on the overall system, including the preamp and output filter. While the preamp and output filter are not part of the Class D power stage, they have a significant effect on the overall performance.

Output filter

The amplified PWM output is reconstructed back to an analog signal by the output LC LPF. Demodulation LC low-pass filter (LPF) formed by L4 and C34, filters out the Class D switching carrier signal leaving the audio output at the speaker load. A single stage output filter can be used with switching frequencies of 400 kHz and greater; a design with a lower switching frequency may require an additional stage of LPF.

Since the output filter is not included in the control loop of the IRAUDAMP6, the reference design cannot compensate for performance deterioration due to the output filter. Therefore, it is important to understand what characteristics are preferable when designing the output filter:

1) The DC resistance of the inductor should be minimal and be within 20 m_Ohm or less.
2) The linearity of the output inductor and capacitor should be high with respect to load current and voltage.

Preamplifier

The preamp allows partial gain of the input signal, and in the IRAUDAMP6, controls the volume. The preamp itself will add distortion and noise to the input signal, resulting in a gain through the Class D output stage and appearing at the output. Even a few micro-volts of noise can add significantly to the output noise of the overall amplifier. In fact, the output noise from the preamp contributes more than half of the overall noise to the system.

It is possible to evaluate the performance without the preamp and volume control, by moving resistors R154and R155 to R157 and R156, respectively. This effectively bypasses the preamp and connects the RCA inputs directly to the Class D power stage input. Improving the selection of preamp and/or output filter, will improve the overall system performance to approach that of the stand-alone Class D power stage.

Self-Oscillating PWM Modulator

The IRAUDAMP6 Class D audio power amplifier features a self-oscillating type PWM modulator for the lowest component count and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of correction.

The self-oscillating frequency is determined by the total delay time inside the control loop of the system. The delay of the logic circuits, the IRS20957 gate-driver propagation delay, the IRF6785 switching speed, the time-constant of front-end integrator (e.g. R50 + R49, C38 and C42 for CH1)

and variations in the supply voltages are critical factors of the self-oscillating frequency. Under normal conditions, the switching-frequency is around 400 kHz with no audio input signal and a +/- 73.5 V supply.

Adjustments of Self-Oscillating Frequency

The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute frequency and frequency relative to the other channels. In absolute terms, at higher frequencies, distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range. Normally when adjusting the self-oscillating frequency of the different channels, it is best to either match the frequencies accurately, or have them separated by at least 25 kHz.

Potentiometers for adjusting self-oscillating frequency	
R49	Switching frequency for CH1*
R74	Switching frequency for CH2*

*Adjustments have to be done at an idling condition with no signal input.

Switches and Indicators

There are two different indicators on the reference design:

- A Red LED, signifying a fault / shutdown condition when lit.
- A green LED on the motherboard, signifying conditions are normal and no fault condition is present.

There are three switches on the reference design:

- Switch S1 is an oscillator selector. This three-position switch is selectable for internal self-oscillator (middle position – “SELF”), or either internal (“INT”) or external (“EXT”) clock synchronization.
- Switch S2 is an internal clock-sync phase difference selector. This feature allows the designer to modify the clock-sync phase separation in order to avoid synchronized switching noise interference. With S2 is set to OFF, the sync-clock phase difference value is 180°.With S2 is set to INT, the clock-sync phase is set by potentiometer R100. With S2 is set to STG, one channel’s clock is quadrature-lagging
- Switch S3 is a trip and reset push-button. Pushing this button has the same effect of a fault condition. The circuit will restart about three seconds after the shutdown button is released.

Startup and Shutdown

One of the most important aspects of any audio amplifier is the startup and shutdown procedures. Typically, transients occurring during these intervals can result in audible pop- or click-noise on the output speaker. Traditionally, these transients have been kept away from the speaker through the use of a series relay that connects the speaker to the audio amplifier only after the startup transients have passed and disconnects the speaker prior to shutting down the amplifier. It is interesting to note that the audible noise of the relay opening and closing is not considered “click noise”, although in some cases, it can be louder than the click noise of non-relay-based solutions.

The IRAUDAMP6 does not use any series relay to disconnect the speaker from the audible transient noise, but rather a shunt-based click noise reduction circuit that yields audible noise levels that are far less that those generated by the relays they replace. This results in a more reliable, superior performance system.

For the startup and shutdown procedures, the activation (and deactivation) of the click-noise reduction circuit, the Class D power stage and the audio input (mute) controls have to be sequenced correctly to achieve the required click noise reduction. The overall startup sequencing, shutdown sequencing and shunt circuit operation are described below.

Click and POP Noise Reduction

To reduce the turn-on and turn-off click noise, a low impedance shunting circuit is used to minimize the voltage across the speaker during transients. For this purpose, the shunting circuit must include the following characteristics:

1) An impedance significantly lower than that of the speaker being shunted. In this case, the shunt impedance is ~100 mΩ, compared to the normal 8 Ω speaker impedance.
2) When deactivated, the shunting circuit must be able to block voltage in both directions due to the bi-directional nature of the audio output.
3) The shunt circuit requires some form of OCP. If one of the Class D output MOSFETs fails, or is conducting when the speaker mute (SP MUTE) is activated, the shunting circuit will effectively try to short one of the two supplies (+/-B).

The implemented click-noise reduction circuit is shown in Figure 12. Before startup or shutdown of the Class D power stage, the click-noise reduction circuit is activated through the SP MUTE control signal. With SP MUTE signal high, the speaker output is shorted through the back-to-back MOSFETs (U5 for Channel 1) with an equivalent on resistance of about 100 mΩ. The two transistors (U7 for Channel 1) are for the OCP circuit.

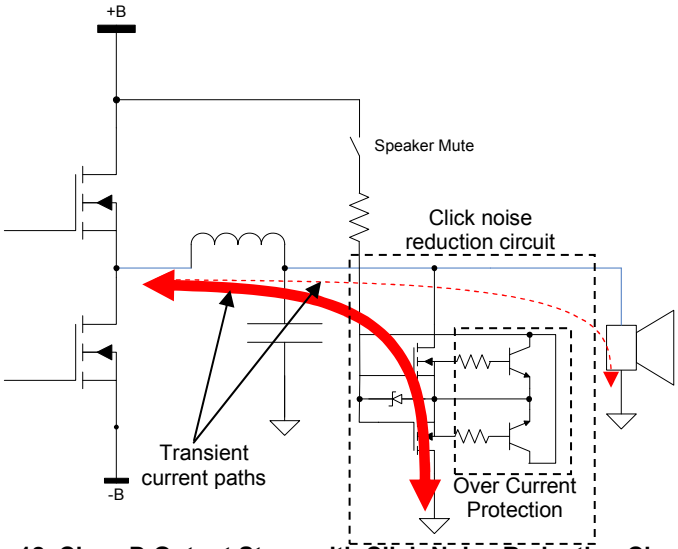


Fig 12, Class D Output Stage with Click-Noise Reduction Circuit

Startup and Shutdown Sequencing

The IRAUDAMP6 sequencing is achieved through the charging and discharging of the CStart capacitor C66. This, coupled to the charging and discharging of the voltage of CSD (C11 on daughter board for CH1) of the IRS20957, is all that is required for complete sequencing. The conceptual startup and shutdown timing diagrams are show in Figure 13.

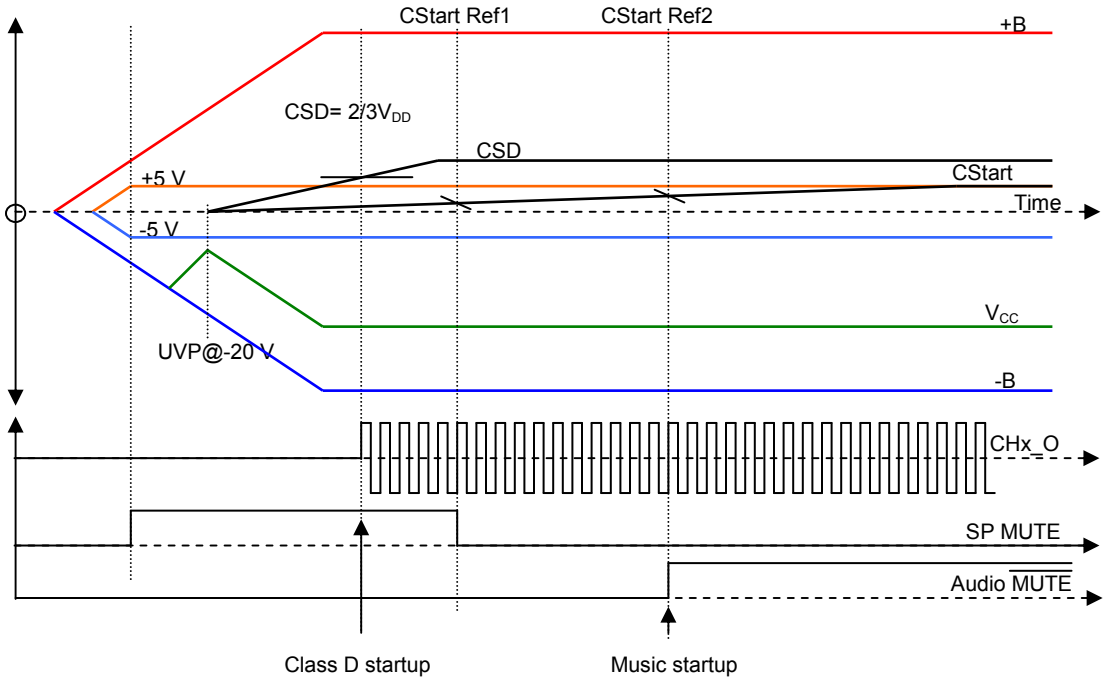


Fig 13, Conceptual Startup Sequencing of Power Supplies and Audio Section Timing

For startup sequencing, +/-B supplies startup at different intervals. As +/-B supplies reach +5 V and -5 V respectively, the analog supplies (+/-5 V) start charging and, once +B reaches ~16 V, V_{CC} charges. Once –B reaches -20 V, the UVP is released and CSD and CStart start charging. Once +/-5 V is established, the click-noise reduction circuit is activated through the SP MUTE control signal. As CSD reaches two-thirds V_{DD}, the Class D stage starts oscillating. Once the startup transient has passed, SP MUTE is released (CStart reaches Ref1). The Class D amplifier is now operational, but the preamp output remains muted until CStart reaches Ref2. At this point, normal operation begins. The entire process takes less than three seconds.

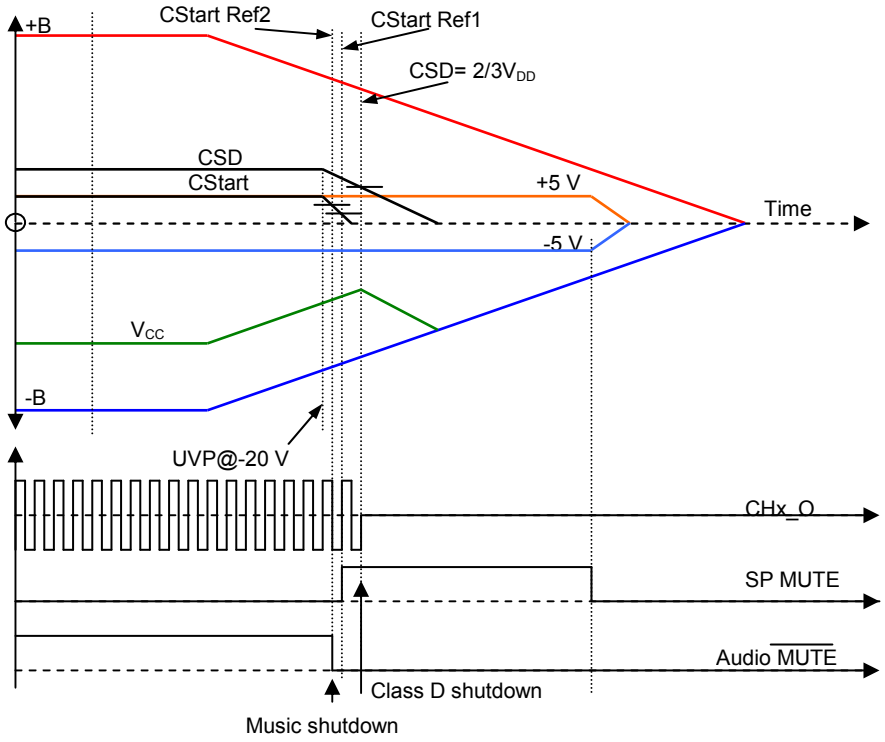


Fig 14, Conceptual Shutdown Sequencing of Power Supplies and Audio Section Timing

Shutdown sequencing is initiated once UVP is activated. As long as the supplies do not discharge too quickly, the shutdown sequence can be completed before the IRS20957 trips UVP. Once UVP is activated, CSD and CStart are discharged at different rates. In this case, threshold Ref2 is reached first and the preamp audio output is muted. Once CStart reaches threshold Ref1, the click-noise reduction circuit is activated (SP MUTE). It is then possible to shutdown the Class D stage (CSD reaches two-thirds V_{DD}). This process takes less than 200 ms.

For any external fault condition (OTP, OVP, UVP or DCP – see “Protection”) that does not lead to power supply shutdown, the system will trip in a similar manner as described above. Once the fault is cleared, the system will reset (similar sequence as startup).

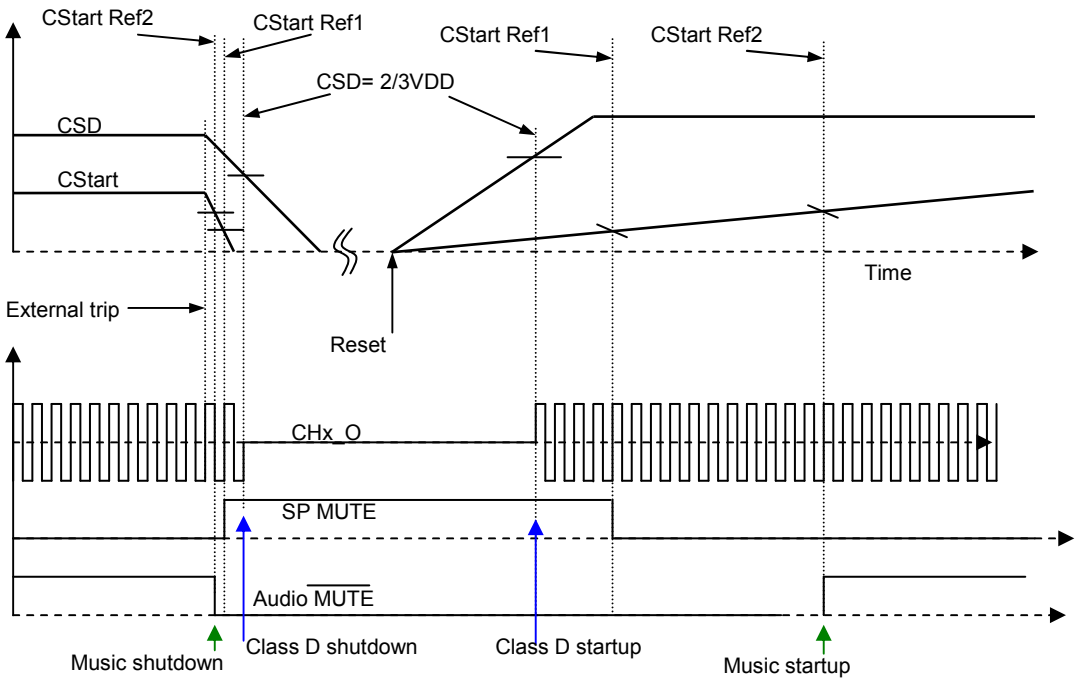


Fig 15, Conceptual Click Noise Reduction Sequencing at Trip and Reset

Selectable Dead-time

The IRS20957 determines its dead-time based on the voltage applied to the DT pin. An internal comparator translates which pre-determined dead-time is being used by comparing the DT voltage with internal reference voltages. A resistive voltage divider from V_{CC} sets threshold voltages for each setting, negating the need for a precise absolute voltage to set the mode. The threshold voltages between dead-time settings are set internally, based on different ratios of V_{CC} as indicated in the diagram below. In order to avoid drift from the input bias current of the DT pin, a bias current of greater than 0.5 mA is suggested for the external resistor divider circuit. Suggested values of resistance that are used to set a dead-time are given below. Resistors with up to 5% tolerance can be used.

Dead-time mode	Dead-time	R22	R19	DT Voltage
DT1	~15 ns	<10kΩ	Open	V_{CC}
DT2	~25 ns	5.6kΩ	4.7kΩ	0.46(V_{CC})
DT3	~35 ns	8.2kΩ	3.3kΩ	0.29(V_{CC})
DT4	~45 ns	Open	<10kΩ	COM

Recommended Resistor Values for Dead Time Selection

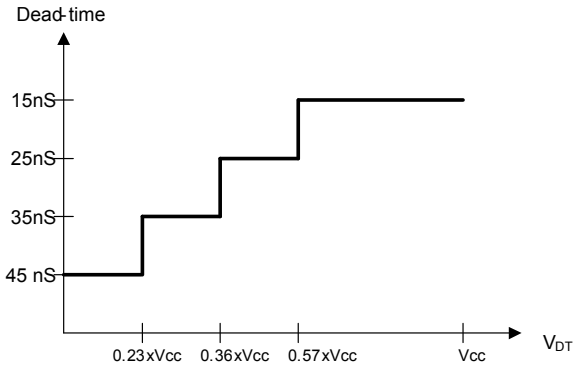


Fig 17 Dead-time Settings vs. V_{DT} Voltage

Level Shifters

The internal input level-shifter transfers the PWM signal down to the low-side gate driver section. The gate driver section has another level-shifter that level shifts up the high-side gate signal to the high-side gate driver section.

Protection System Overview

The IRS20957 integrates over current protection (OCP) inside the IC. The rest of the protections, such as over-voltage protection (OVP), under-voltage protection (UVP), and over temperature protection (OTP), are detected externally to the IRS20957.

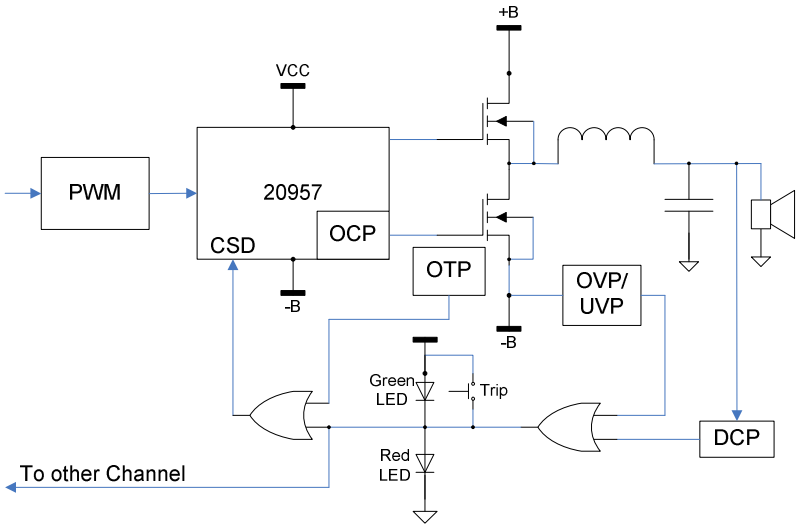


Fig 18, Functional Block Diagram of Protection Circuit Implementation

The external shutdown circuit will disable the output by pulling down CSD pins . If the fault condition persists, the protection circuit stays in shutdown until the fault is removed.

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Over-Current Protection (OCP)

The OCP internal to the IRS20957 shuts down the IC if an OCP is sensed in either of the output MOSFETs. For a complete description of the OCP circuitry, please refer to the IRS20957 datasheet. Here is a brief description:

Low-Side Current Sensing

The low-side current sensing feature protects the low side DirectFET from an overload condition from negative load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. When the VS voltage becomes higher than the OCSET voltage during low-side conduction, the IRS20957 turns the outputs off and pulls CSD down to -VSS.

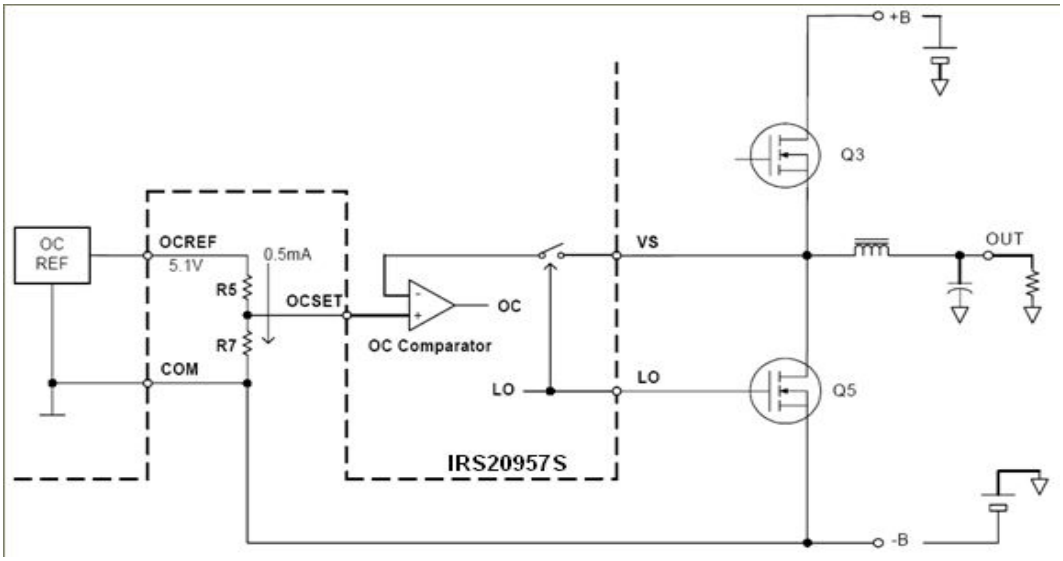

Fig 19 Simplified Functional Block Diagram of Low-Side Current Sensing

High-Side Current Sensing

The high-side current sensing protects the high side DirectFET from an overload condition from positive load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

High-side over-current sensing monitors drain-to-source voltage of the high-side DirectFET during the on state through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side DirectFET. In contrast to the low-side current sensing, the threshold of the CSH pin to trigger OC protection is internally fixed at 1.2V. An external resistive divider R30, R32 and R34 are used to program a threshold . An external reverse blocking diode D8 is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D8, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source.