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International
IOR Rectifier

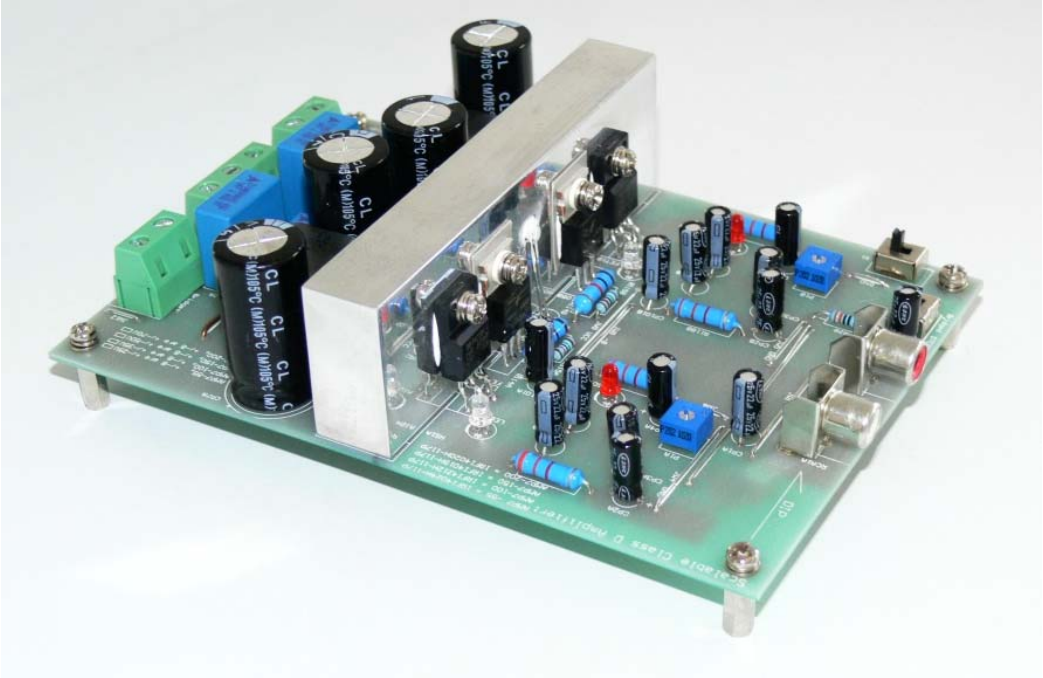
REFERENCE DESIGN

IRAUDAMP7S

25W-500W Scalable Output Power
Class D Audio Power Amplifier Reference Design
Using the IRS2092S Protected Digital Audio Driver

By

Jun Honda, Manuel Rodríguez, Liwei Zheng



CAUTION:

International Rectifier suggests the following guidelines for safe operation and handling of IRAUDAMP7S Demo Board:

- **Always wear safety glasses whenever operating Demo Board**
- **Avoid personal contact with exposed metal surfaces when operating Demo Board**
- **Turn off Demo Board when placing or removing measurement probes**

Item	Table of Contents	Page

Introduction

The IRAUDAMP7S reference design is a two-channel Class D audio power amplifier that features output power scalability. The IRAUDAMP7S offers selectable half-bridge (stereo) and full-bridge (bridged) modes.

This reference design demonstrates how to use the IRS2092 Class D audio driver IC, along with IR's digital audio dual MOSFETs, such as IRFI4024H-117P, IRFI4019H-117P, IRFI4212H-117P and IRFI4020H-117P, on a single layer PCB. The design shows how to implement peripheral circuits on an optimum PCB layout using a single sided board.

The resulting design requires a small heatsink for normal operation (one-eighth of continuous rated power). The reference design provides all the required housekeeping power supplies and protections.

Unless otherwise noted, this user's manual is based on 150V model, IRAUDAMP7S-150.

Other output power versions can be configured by replacing components given in the component selection of Table 5 on page 36

Applications

- AV receivers
- Home theater systems
- Mini component stereos
- Powered speakers
- Sub-woofers
- Musical Instrument amplifiers
- Automotive after market amplifiers

Features

Output Power:	Scalable output power from 25W- 500W (see Table 1)
Residual Noise:	200 μV, IHF-A weighted, AES-17 filter
Distortion:	0.007 % THD+N @ 60W, 4 Ω
Efficiency:	90 % @ 500W, 8 Ω, Class D stage
Multiple Protection Features:	Over-current protection (OCP), high side and low side MOSFET Over-voltage protection (OVP), Under-voltage protection (UVP), high side and low side MOSFET DC-protection (DCP), Over-temperature protection (OTP)
PWM topology:	Self-oscillating PWM, half-bridge or full-bridge topologies selectable

Table 1 IRAUDAMP7S Specification Table Series

Item		Model Name			
		AMP7S-55	**AMP7S-100**	**AMP7S-150**	**AMP7S-200**
IR Power MOSFET	FET1A, FET1B	IRFI4024H-117P	IRFI4212H-117P	IRFI4019H-117P	IRFI4020H-117P
Half Bridge	8 Ω	25W x 2	60W x 2	125W x 2	250W x 2
	4 Ω	50W x 2	120W x 2	250W x 2	Not Supported
Full Bridge	8 Ω	100W x 1	240W x 1	500W x 1	Not Supported
Nominal Supply Voltage	+B, -B	±25V	±35V	±50V	±70V
Min/Max Supply Voltage	+B, -B	±20V ~ ±28V	±28V ~ ±45V	±45V ~ ±60V	±60V ~ ±80V
Voltage Gain	Gv	20	30	36	40

Notes:

- **All the power ratings are at clipping power (THD+N = 1 %). To estimate power ratings at THD+N=10%, multiply them by 1.33**
- **See Table 5 on page 36 for the complete listing of components table.**

Specifications

General Test Conditions for IRAUDAMP7S-150 (unless otherwise noted)		**Notes / Conditions**
Power Supply Voltages		± 50V
Load Impedance		4 Ω
Self-Oscillating Frequency		400kHz
Voltage Gain		36

Electrical Data	**Typical**	**Notes / Conditions**
IR Devices Used	IRS2092, Protected digital audio driver IRFI4024H-117P, IRFI4019H-117P, IRFI4212H-117P, IRFI4020H-117P Digital audio MOSFETs	
PWM Modulator	Self-oscillating, second order sigma-delta modulation, analog input	
Power Supply Range	± 45V to ± 60V	Or see table 1 above
Output Power CH1-2: (1 % THD+N)	300W	1kHz
Output Power CH1-2: (10 % THD+N)	400W	1kHz
Rated Load Impedance	8 - 4 Ω	Resistive load
Standby Supply Current	+50 mA/-80 mA	No input signal
Total Idle Power Consumption	7W	No input signal
Channel Efficiency	90 %	Single-channel driven, 250W

.

Audio Performance

	Before Demodulator	Class D Output	Notes / Conditions
THD+N, 1W THD+N, 10W THD+N, 60W THD+N, 100W	0.01 % 0.005 % 0.005 % 0.007 %	0.02 % 0.007 % 0.007 % 0.008 %	1kHz, Single-channel driven
Dynamic Range	101 dB	101 dB	A-weighted, AES-17 filter, Single-channel operation
Residual Noise	200 µV	200 µV	22 Hz – 20kHz, AES17 filter Self-oscillating frequency 400kHz
Damping Factor	2000	120	1kHz, relative to 4 Ω load
Channel Separation	95 dB 85 dB 75 dB	90 dB 80 dB 65 dB	100Hz 1kHz 10kHz
Frequency Response : 20 Hz-20kHz	20 Hz-35kHz	±3 dB	1W, 4 Ω – 8 Ω Load

Thermal Performance (T_A=25 °C)

Condition	Typical	Notes / Conditions
Idling	T_C =30 °C T_{PCB}=37 °C	No signal input
2 ch x 31W (1/8 rated power)	T_C =54 °C T_{PCB}=67 °C	
2 ch x 250W (Rated power)	T_C =80 °C T_{PCB}=106 °C	OTP shutdown after 150 s

Physical Specifications

Dimensions	5.7”(L) x 4”(W) x 1.25”(H) 145 mm (L) x 100 mm (W) x 35 mm(H)
Weight	0.330kgm

Test Setup

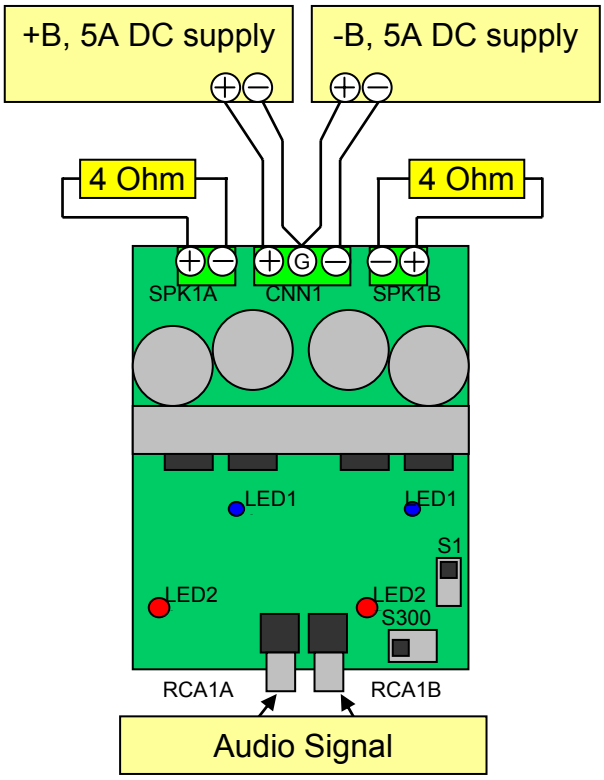


Fig 1 Typical Test Setup

Connector Description

CH1 IN	RCA1A	Analog input for CH1
CH2 IN	RCA1B	Analog input for CH2
SUPPLY	CNN1	Positive and negative supply (+B / -B)
CH1 OUT	SPK1A	Output for CH1
CH2 OUT	SPK1B	Output for CH2

Switches Descriptions

S1	Shutdown PWM
S300	Half bridge / Full bridge select

Indicator Description

LED1A, B	PWM (presence of low side gate signal)
LED2A,B	Protection

Test Procedures

Test Setup:

1. On the unit under test (UUT), set switch S1 to OFF and S300 to Stereo positions.
2. Connect 4 Ω-200 W dummy loads to output connectors, SPKR1A and SPKR1B, as shown on Fig 1.
3. Set up a dual power supply ±50V with 5A current limit
4. Turn OFF the dual power supply before connecting to UUT.
5. Connect the dual power supply to CNN1, as shown in Fig 1.

Power up:

6. Turn ON the dual power supply. The ±B supplies must be applied and removed at the same time.
7. The red LEDs (Protections) turn ON immediately and stay on as long as S1 is in OFF position. Blue LEDs stay OFF.
8. Quiescent current for the positive and negative supplies must be less than 50mA, while S1 is in OFF position. Under this condition, IRS2092 is in shutdown mode.
9. Slide S1 to ON position; after one second delay, the two blue LEDs turn ON and the red LEDs turns off. The two blue LEDs indicate that PWM oscillation is present. This transition delay time is controlled by CSD pin of IRS2092, capacitor CP3
10. Under the normal operating condition with no input signal applied, quiescent current for the positive supply must be less than 50 mA; the negative supply current must be less than 100 mA.

Switching Frequency Test:

11. With an oscilloscope, monitor switching waveform at test points VS1 & VS2 Adjust P1A & P1B to change self oscillating frequency to 400kHz ± 25kHz.
    Note: To change self-oscillating switching frequency, Adjust the potentiometer resistances of P11A and P11B for CH1 and CH2 respectively.

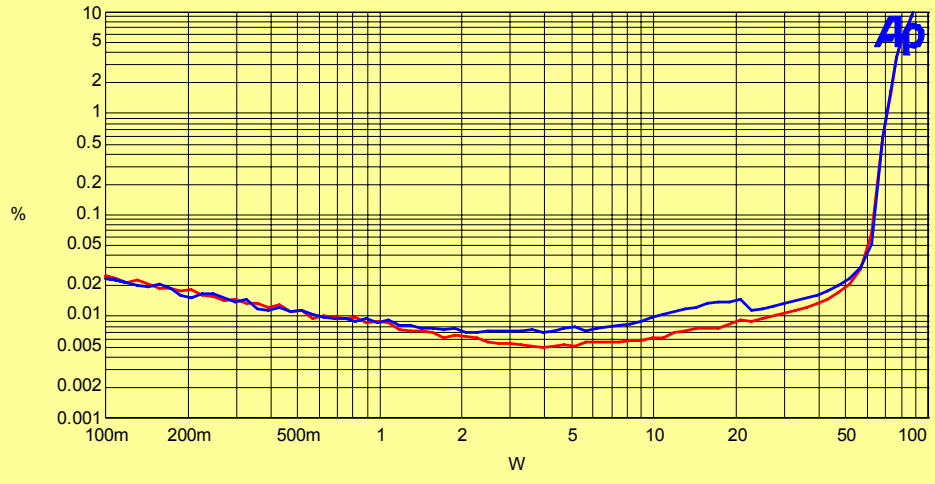
Audio Functionality Tests:

12. Set the signal generator to 1kHz, 20 mV_{RMS} output.
13. Connect audio signal generators to RCA1A and RCA1B.
14. Sweep the audio signal voltage from 15 mV_{RMS} to 1 V_{RMS}.
15. Monitor the output signals at SPK1A/B with an oscilloscope. Waveform must be a non distorted sinusoidal signal.
16. Observe 1 V_{RMS} input generates output voltage of 36 V_{RMS}. The ratio, R8/(R7+R2), determines the voltage gain of IRAUDAMP7S.
17. Set switch S300 to Bridged position.
18. Observe that voltage gain doubles.

Test Setup using Audio Precision (Ap):

19. Use unbalance-floating signal generator outputs.
20. Use balanced inputs taken across output terminals, SPKR1A and SPKR1B.
21. Connect Ap frame ground to GND in terminal CNN1.
22. Place AES-17 filter for all the testing except frequency response.
23. Use signal voltage sweep range from 15 mV_{RMS} to 1 V_{RMS}.
24. Run Ap test programs for all subsequent tests as shown in Fig 2- Fig 13 below.

Test Results



Red = CH1, Blue = CH2

±B Supply = ±25V, 4 Ω Resistive Load

Fig 2 IRAUDAMP7S-55, THD+N versus Power, Stereo, 4 Ω

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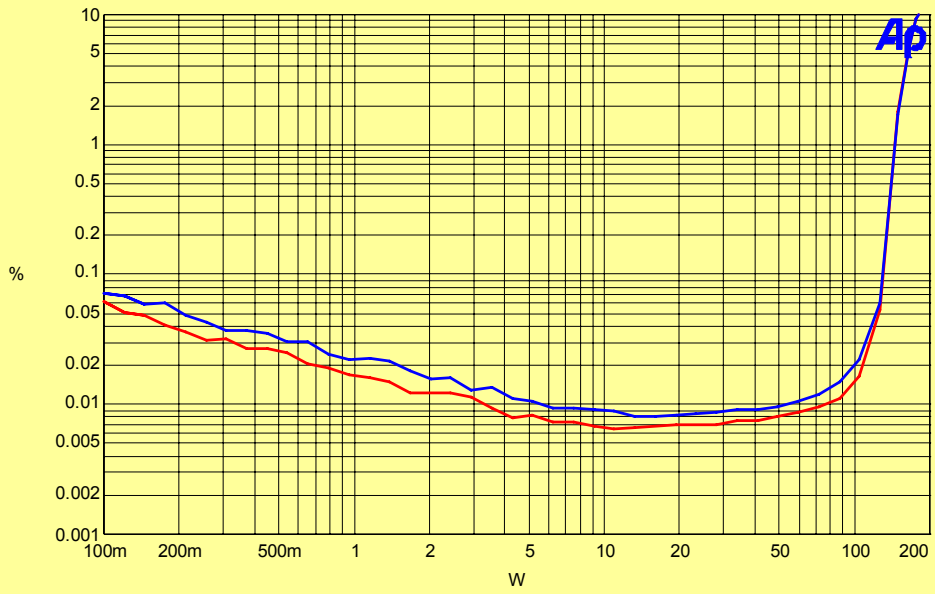

Red = CH1, Blue = CH2

±B Supply = ±35V, 4 Ω Resistive Load

Fig 3 IRAUDAMP7S-100, THD+N versus Power, Stereo, 4 Ω

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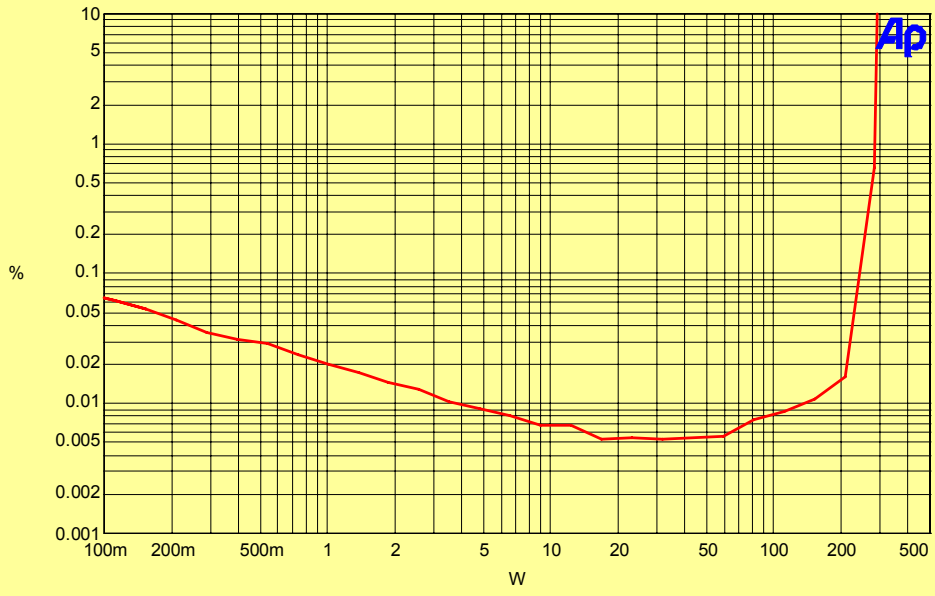

±B Supply = ±35V, 8 Ω Resistive Load, Bridged

Fig 4 IRAUDAMP7S-100, THD+N versus Power, Bridged, 8 Ω

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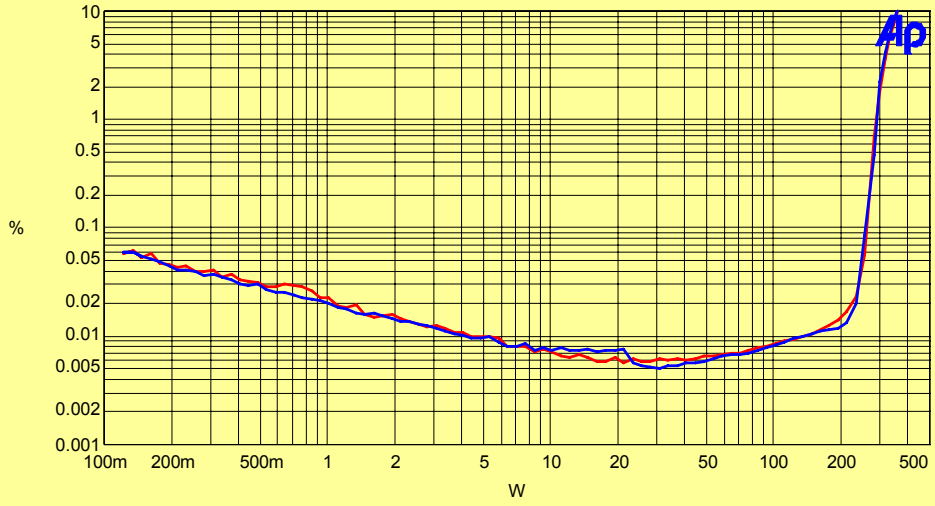

Red = CH1, Blue = CH2

±B Supply = ±50V, 4 Ω Resistive Load

Fig 5 IRAUDAMP7S-150, THD+N versus Power, Stereo, 4 Ω

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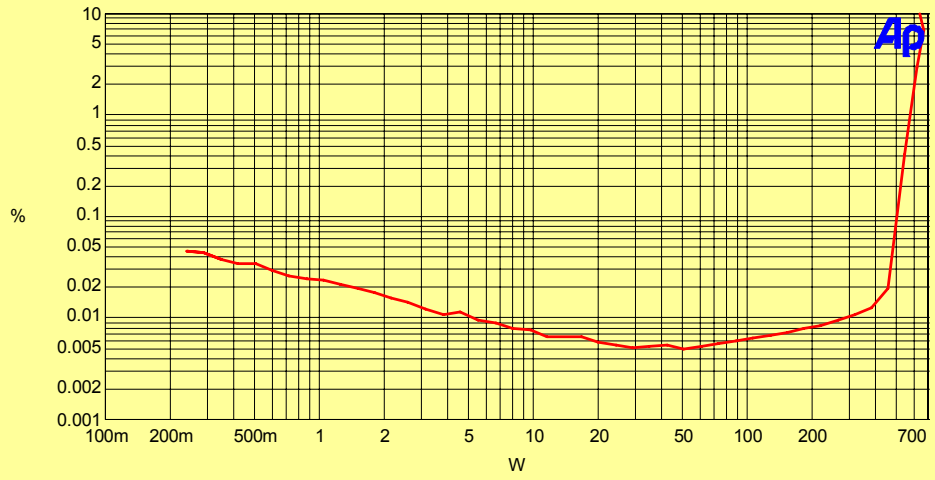

±B Supply = ±50V, 8 Ω Resistive Load

Fig 6 IRAUDAMP7S-150, THD+N versus Power, Bridged 8 Ω

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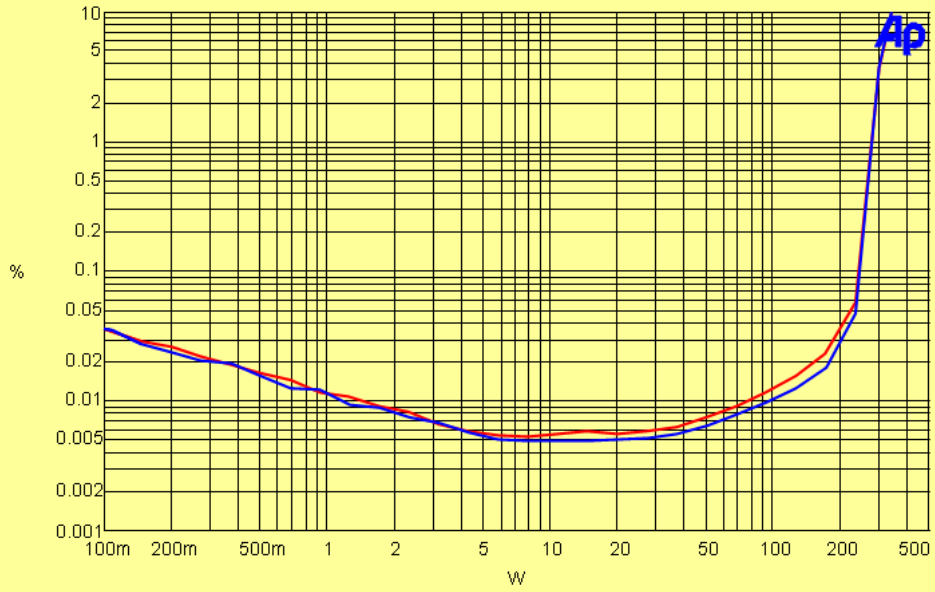
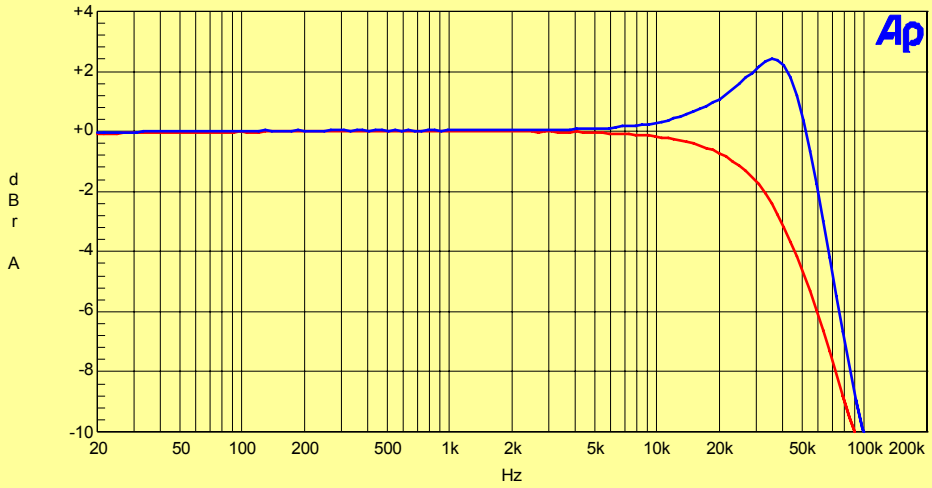


Red = CH1, Blue = CH2

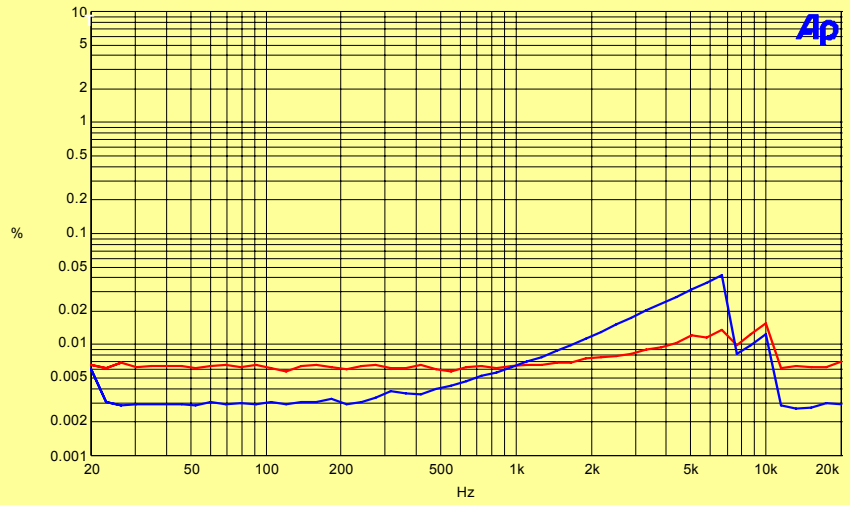
±B Supply = ±70V, 8 Ω Resistive Load

Fig 7 IRAUDAMP7S-200, THD+N versus Power, Stereo 8 Ω



Red	CH1 - 4 Ω, 2 V Output referenced
Blue	CH1 - 8 Ω, 2 V Output referenced

Fig 8 Frequency Response (All Models)



Red	CH1, 10W Output
Blue	CH1, 50W Output

Fig 9 IRAUDAMP7S-150, THD+N versus Frequency, *4Ω*

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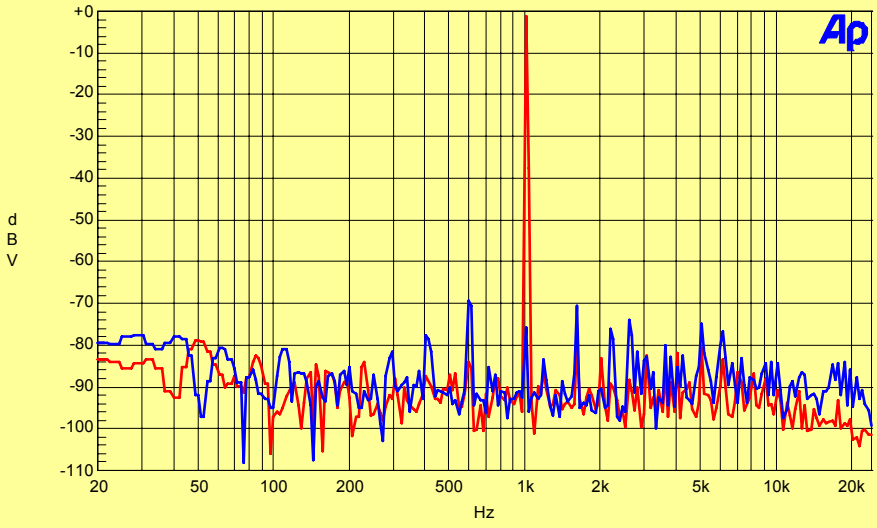

Red = CH1, Blue = CH2

1V Output

Fig 10 IRAUDAMP7S-150, 1 kHz – 1 V Output Spectrum, Stereo

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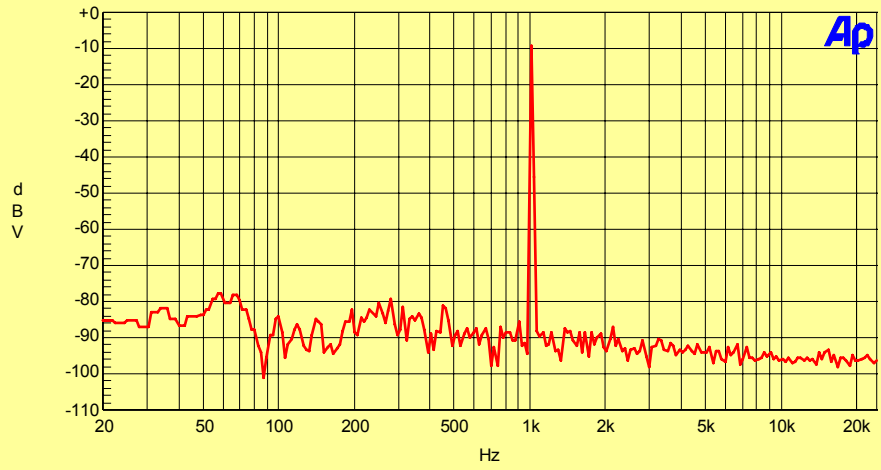

1V Output

Fig 11 IRAUDAMP7S-150, 1 kHz - 1V Output Spectrum, Bridged

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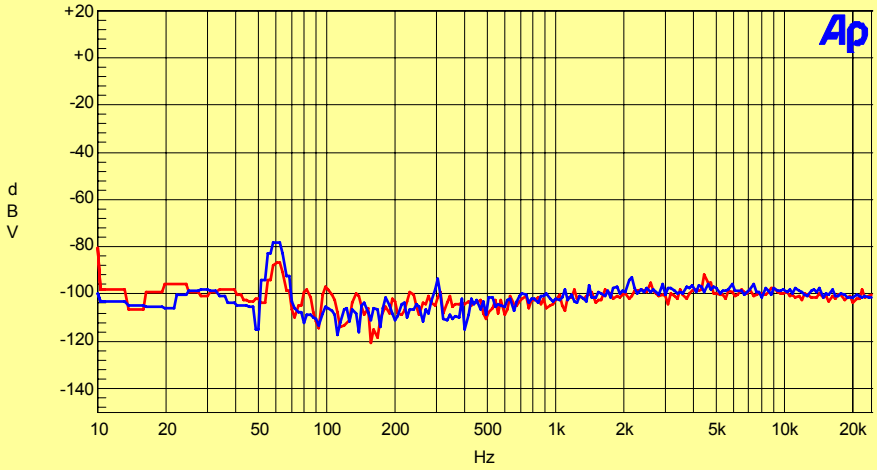


Red	CH1 - ACD, No signal, Self Oscillator @ 400kHz
Blue	CH2 - ACD, No signal, Self Oscillator @ 400kHz

Fig 12 IRAUDAMP7S-150 Noise Floor

.

Clipping characteristics

210 W / 4 Ω, 1 kHz, THD+N = 0.02 % **310 W / 4 Ω, 1 kHz, THD+N = 10 %**

Measured Output and Distortion Waveforms

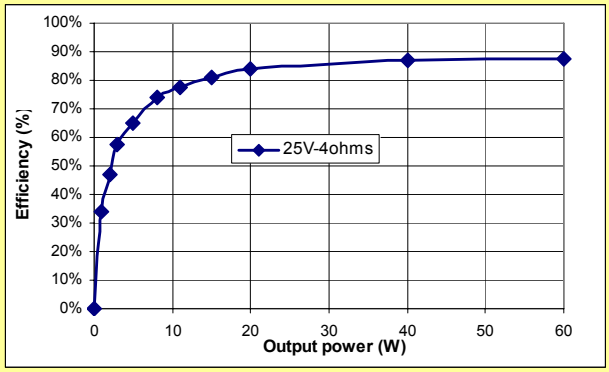
Fig 13 Clipping Characteristics

.

Efficiency

Figs 14-19 show efficiency characteristics of the IRAUDAMP7S. The high efficiency is achieved by following major factors:

1) Low conduction loss due to the dual FETs offering low $R_{DS(ON)}$
2) Low switching loss due to the dual FETs offering low input capacitance for fast rise and fall times
3) Secure dead-time provided by the IRS2092, avoiding cross-conduction



±B Supply = ±25 V

Fig 14 Efficiency versus Output Power, IRAUDAMP7S-55, 4 Ω, Stereo

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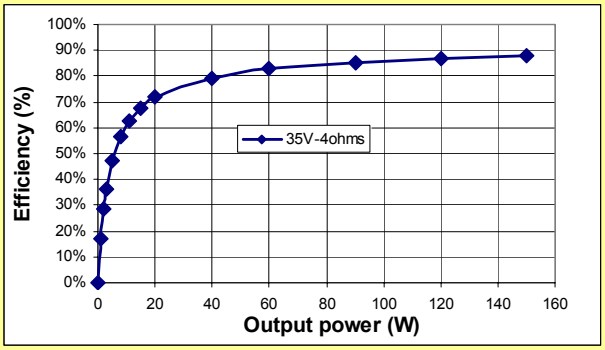

±B Supply = ±35 V

Fig 15 Efficiency versus Output Power, IRAUDAMP7S-100, 4 Ω, Stereo

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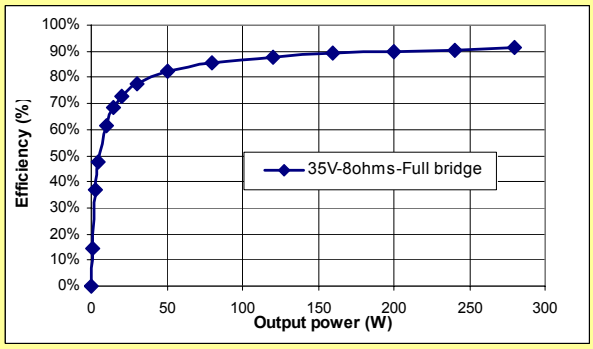

±B Supply = ±35V

Fig 16 Efficiency versus Output Power, IRAUDAMP7S-100, 8 Ω, Bridged

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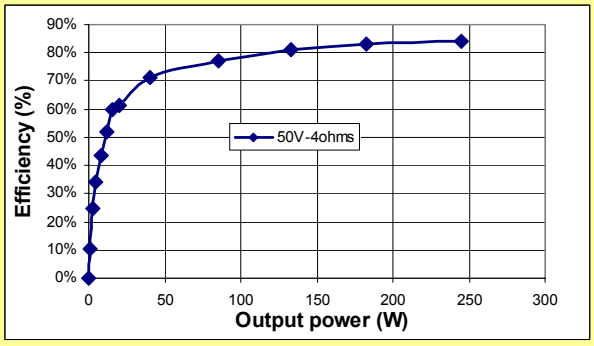
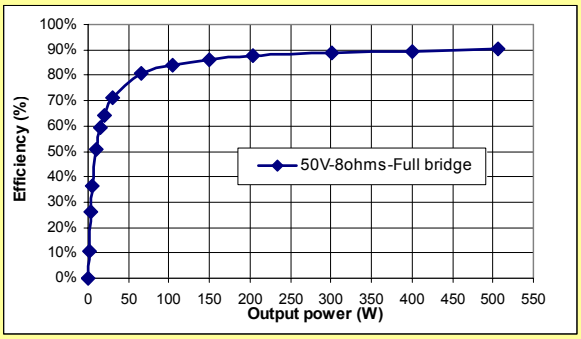


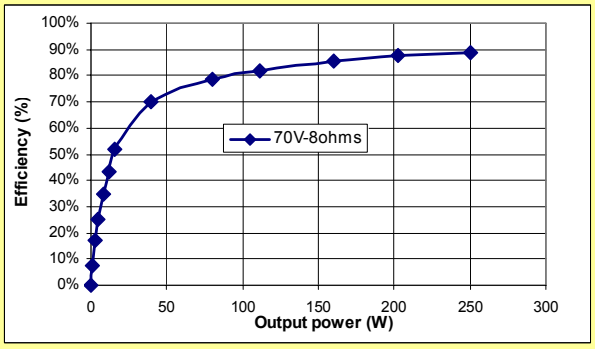
±B Supply = ±50V

Fig 17 Efficiency versus Output Power, IRAUDAMP7S-150, 4 Ω, Stereo



±B Supply = ±50V

Fig 18 Efficiency versus Output Power, IRAUDAMP7S-150, 8 Ω, Bridged



±B supply = ±70V

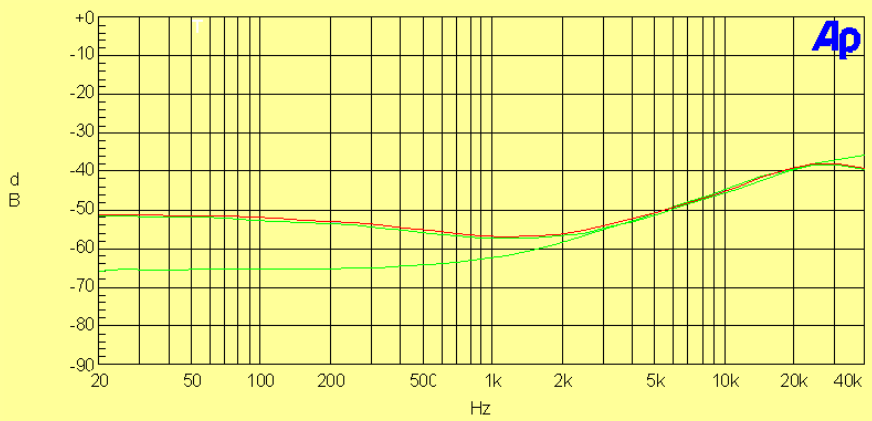
Fig 19 Efficiency versus Output Power, IRAUDAMP7S-200, 8 Ω, Stereo

Thermal Considerations

With this high efficiency, the IRAUDAMP7S design can handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards, without additional heatsink or forced air-cooling.

Power Supply Rejection Ratio (PSRR)

The IRAUDAMP7S obtains good power supply rejection ratio of -65 dB at 1kHz shown in Fig 20. With this high PSRR, IRAUDAMP7S accepts any power supply topology as far as the supply voltages fit in the min and max range.



Red: VAA & VSS are fed by +/-B bus
Green: VAA & VSS are fed by external +/-5 V regulated power supplies.

Fig 20 IRAUDAMP7S Power Supply Rejection Ratio

Short Circuit Protection Response

Figs 21-23 show over current protection reaction time of the IRAUDAMP7S in a short circuit event. As soon as the IRS2092 detects over current condition, it shuts down PWM. After one second, the IRS2092 tries to resume the PWM. If the short circuit persists, the IRS2092 repeats try and fail sequences until the short circuit is removed.

Short Circuit in Positive and Negative Load Current

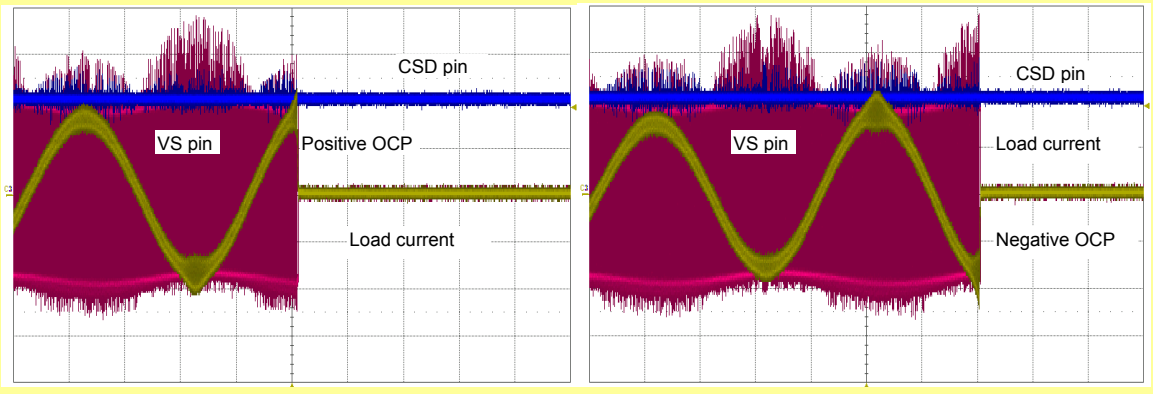


Fig 21 Positive and Negative OCP Waveforms

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OCP Waveforms Showing CSD Trip and Hiccup

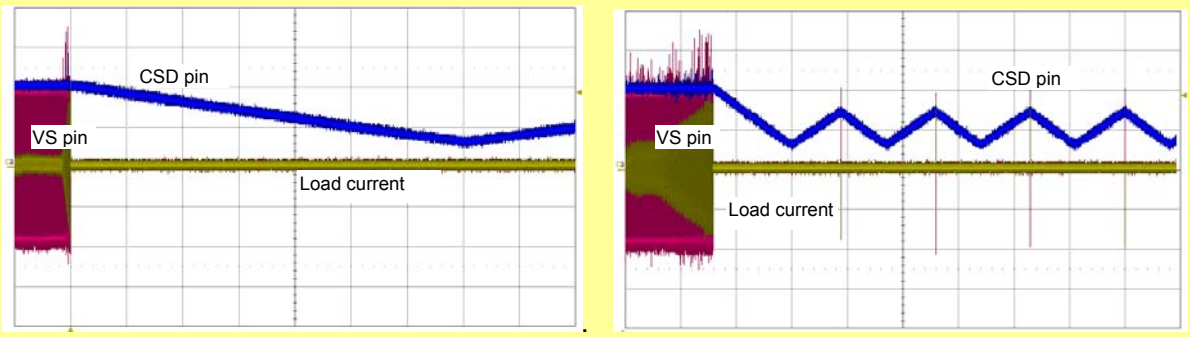

Fig 22 OCP Response with Continuous Short Circuit

Actual Reaction Time

OCP Waveforms Showing actual reaction time

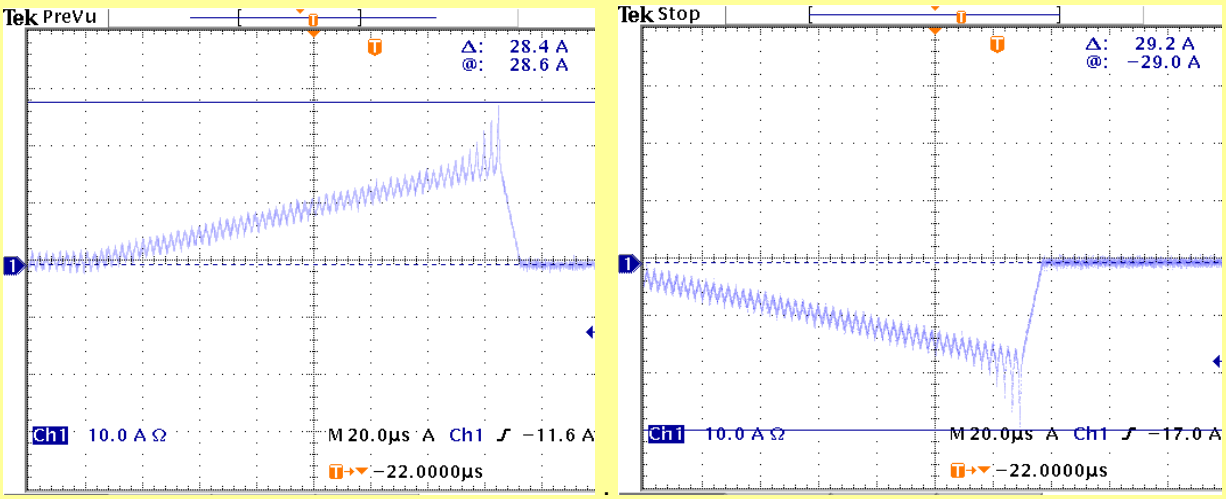

Fig. 23 High and Low Side OCP current waveform reaction time

IRAUDAMP7S Overview

The IRAUDAMP7S features a self-oscillating type PWM modulator for the lowest component count, highest performance and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The

benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of error correction.

The IRAUDAMP7S self-oscillating topology consists of following essential functional blocks.

- Front-end integrator
- PWM comparator
- Level shifters
- Gate drivers and MOSFETs
- Output LPF

Integrator

Referring to Fig 24 below, the input operational amplifier of the IRS2092 forms a front-end second-order integrator with R7, C4, C6, P1, and R11. The integrator that receives a rectangular feedback signal from the PWM output via R8 and audio input signal via R7 generates quadratic carrier signal in COMP pin. The analog input signal shifts the average value of the quadratic waveform such that the duty cycle varies according to the instantaneous voltage of the analog input signal.

PWM Comparator

The carrier signal in COMP pin is converted to PWM signal by an internal comparator that has threshold at middle point between VAA and VSS. The comparator has no hysteresis in its input threshold.

Level Shifters

The internal input level-shifter transfers the PWM signal down to the low-side gate driver section. The gate driver section has another level-shifter that level shifts up the high-side gate signal to the high-side gate driver section.

Gate Drivers and MOSFETs

The received PWM signal is sent to the dead-time generation block where a programmable amount of dead time is added into the PWM signal between the two gate output signals of LO and HO to prevent potential cross conduction across the output power MOSFETs. The high-side level-shifter shifts up the high-side gate drive signal out of the dead-time block.
The IRS2092 drives two MOSFETs, high- and low-sides, in the power stage providing the amplified PWM waveform.

Output LPF

The amplified PWM output is reconstructed back to analog signal by the output LC LPF. Demodulation LC low-pass filter (LPF) formed by L1 and C12, filters out the Class D switching carrier signal leaving the audio output at the speaker load. A single stage output filter can be used with switching frequencies of 400 kHz and greater; a design with a lower switching frequency may require an additional stage of LPF.

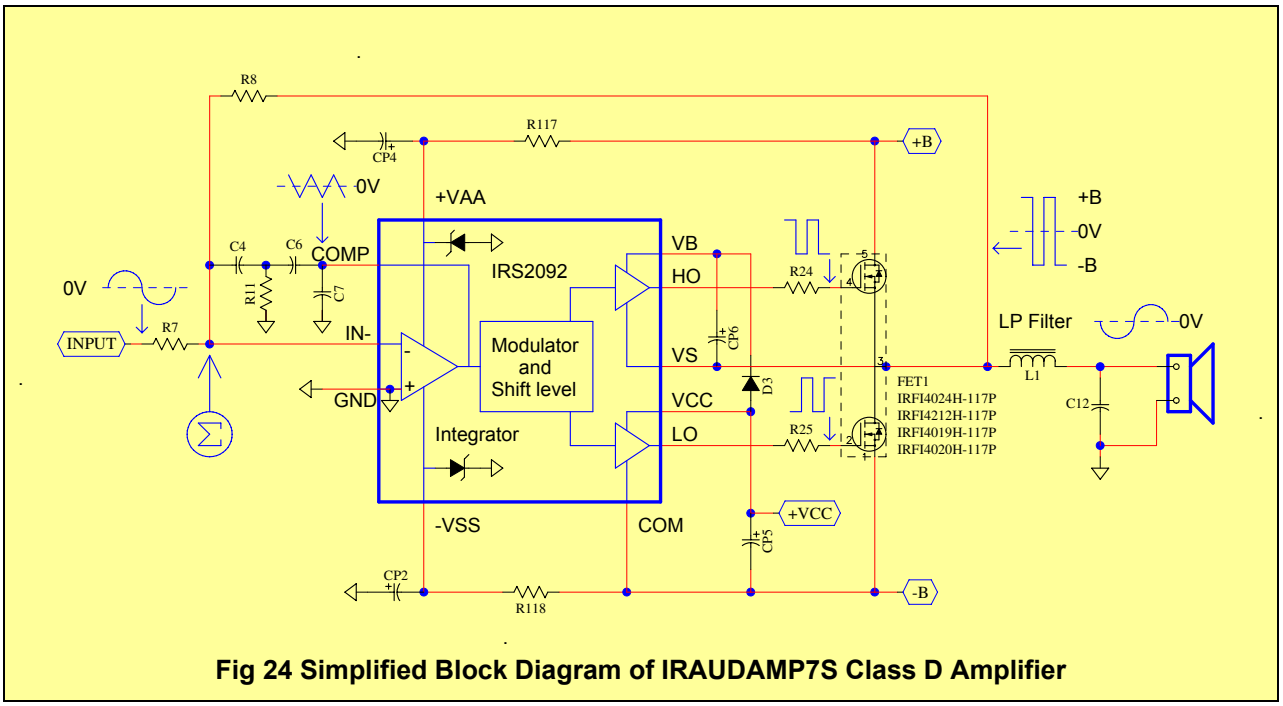

Fig 24 Simplified Block Diagram of IRAUDAMP7S Class D Amplifier

Functional Descriptions

IRS2092 Gate Driver IC

The IRAUDAMP7S uses IRS2092, a high-voltage (up to 200 V), high-speed power MOSFET driver with internal dead-time and protection functions specifically designed for Class D audio amplifier applications. These functions include OCP and UVP. The IRS2092 integrates bi-directional over current protection for both high-side and low-side MOSFETs. The dead-time can be selected for optimized performance according to the size of the MOSFET, minimizing dead-time while preventing shoot-through. As a result, there is no gate-timing adjustment required externally. Selectable dead-time through the DT pin voltage is an easy and reliable function which requires only two external resistors, R26 and R27 as shown on Fig 25 below.

The IRS2092 offers the following functions.

- PWM modulator
- Dead-time insertion
- Over current protection
- Under voltage protection
- Level shifters

Refer to IRS2092 datasheet and AN-1138 for more details.

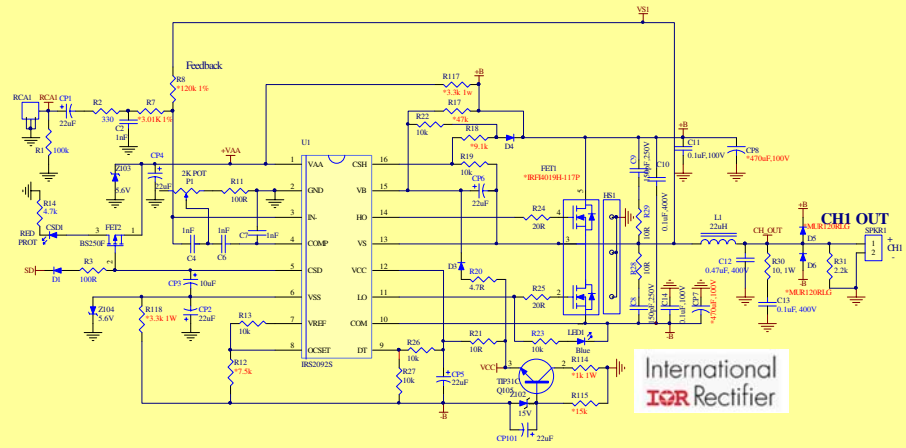

Fig 25 System-level View of IRAUDAMP7S

Self-Oscillating Frequency

Self-oscillating frequency is determined by the total delay time along the control loop of the system; the propagation delay of the IRS2092, the MOSFETs switching speed, the time-constant of front-end integrator (P1, R7, R11 R8, C4, C6, C7). Variations in +B and –B supply voltages also affect the self-oscillating frequency.

The self-oscillating frequency changes with the duty ratio. The frequency is highest at idling. It drops as duty cycle varies away from 50%.

Adjustments of Self-Oscillating Frequency

Use P1 & R11 to set different self-oscillating frequencies. The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute frequency and frequency relative to the other channels. In the absolute terms, at higher frequencies distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range.

Normally, when adjusting the self-oscillating frequency of the different channels, it is suggested to either match the frequencies accurately, or have them separated by at least 25kHz. Under the normal operating condition with no audio input signal, the switching-frequency is set around 400kHz in the IRAUDAMP7S.

Selectable Dead-time

The dead-time of the IRS2092 is set based on the voltage applied to the DT pin. Fig 26 lists the suggested component value for each programmable dead-time between 25 and 105 ns.
All the IRAUDAMP7S models use DT2 (45ns) dead-time.

Dead-time Mode	R1	R2	DT/SD Voltage
DT1	<10k	Open	Vcc
DT2	5.6kΩ	4.7kΩ	0.46 x Vcc
DT3	8.2kΩ	3.3kΩ	0.29 x Vcc
DT4	Open	<10k	COM

Recommended Resistor Values for Dead Time Selection

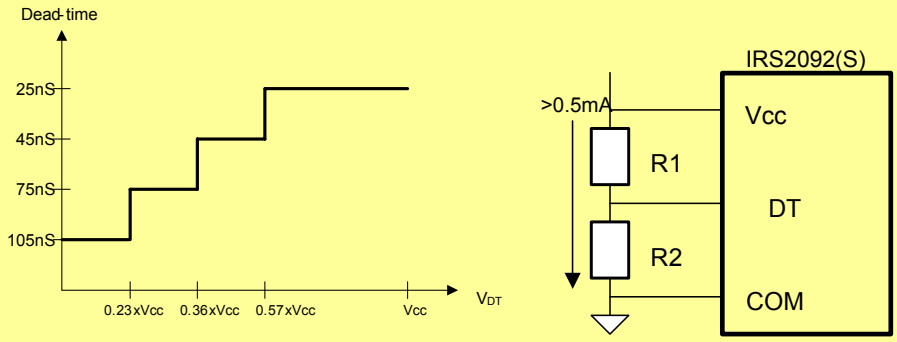

Fig 26 Dead-time Settings vs. V_{DT} Voltage

Protection System Overview

The IRS2092 integrates over current protection (OCP) inside the IC. The rest of the protections, such as over-voltage protection (OVP), under-voltage protection (UVP), speaker DC offset protection (DCP) and over temperature protection (OTP), are realized externally to the IRS2092 (Fig 27).

In the event that any of these external fault conditions are detected, the external shutdown circuit will disable the output by pulling down CSD pins, turning on red LEDs, and turning off blue LEDs (Fig 28). If the fault condition persists, the protection circuit stays in shutdown until the fault is removed. Once the fault is cleared, the blue LEDs turn on and red LEDs turn off.

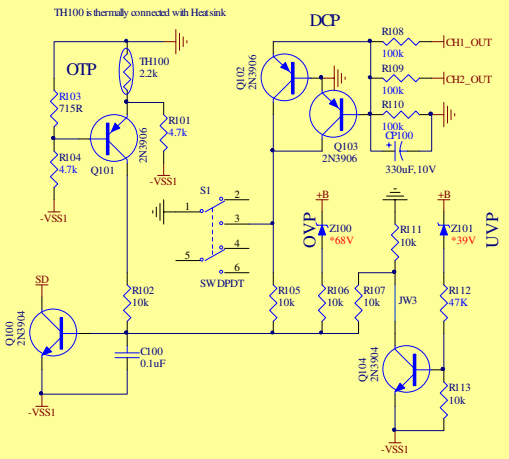

Fig 27 DCP, OTP, UVP and OVP Protection Circuits

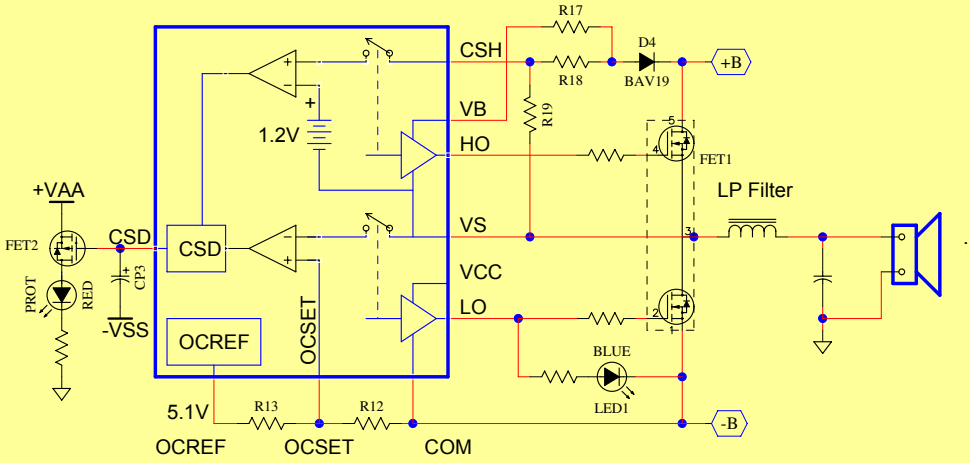

Fig 28 Simplified Functional Diagram of OCP and Associated LED Indicators

Over-Current Protection (OCP)

Low-Side Current Sensing

The low-side current sensing feature protects the low side MOSFET from an overload condition in negative load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. When the VS voltage during low-side conduction gets higher than the OCSET voltage, the IRS2092 turns off outputs and pulls CSD down to -VSS.

High-Side Current Sensing

The high-side current sensing protects the high side MOSFET from an overload condition in positive load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

High-side over-current sensing monitors drain-to-source voltage of the high-side MOSFET while it is in the on state through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side MOSFET. In contrast to the low-side current sensing, the threshold of CSH pin to trigger OC protection is internally fixed at 1.2V. An external resistive divider R19, R18 and R17 are used to program a threshold as shown in Fig 26. An external reverse blocking diode D4 is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D4, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source.

Table 2 Actual OCP table setting thresholds

Function	Device	Amp7-55	Amp7-100	Amp7-150	Amp7-200
OCSET	R12A R12B	1.3K	3.9K	7.5K	5.1K
Tested OCP current 25°C			23A	30A	23A
CSH	R18A R18B	0.0	4.7K	9.1K	8.2K
Tested OCP current 25°C			23A	29A	23A
Peak load current at rated power		6.0A	8.7A	12.2A	8.9A

Over-Voltage Protection (OVP)

OVP is provided externally to the IRS2092. OVP shuts down the amplifier if the bus voltage between GND and +B exceeds 75V. The threshold is determined by a Zener diode Z100. OVP

protects the board from harmful excessive supply voltages, such as due to bus pumping at very low frequency continuous output in stereo mode.

Under-Voltage Protection (UVP)

UVP is provided externally to the IRS2092. UVP prevents unwanted audible noise output from unstable PWM operation during power up and down. UVP shuts down the amplifier if the bus voltage between GND and +B falls below a voltage set by Zener diode Z101.

Speaker DC-Voltage Protection (DCP)

DCP protects speakers against DC output current feeding to its voice coil. DC offset detection detects abnormal DC offset and shuts down PWM. If this abnormal condition is caused by a MOSFET failure because one of the high-side or low-side MOSFETs short circuited and remained in the on state, the power supply needs to be cut off in order to protect the speakers. Output DC offset greater than ±4V triggers DCP.

Offset Null (DC Offset) Adjustment

The IRAUDAMP7S requires no output-offset adjustment. DC offsets are tested to be less than ±20 mV.

Over-Temperature Protection (OTP)

A NTC resistor, TH100 in Fig 25, is placed in close proximity to two dual MOSFETs on a heatsink to monitor heatsink temperature. If the heatsink temperature rises above 100 °C, the OTP shuts down both channels by pulling down CSD pins of the IRS2092. OTP recovers once the temperature has cooled down.

ON-OFF Switch

OFF position of S1 forces the IRAUDAMP7S to stay in shutdown mode by pulling down the CSD pin. During the shutdown mode the output MOSFETs are kept off.

Click and POP Noise Reduction

Thanks to the click and pop elimination function built into the IRS2092, IRAUDAMP7S does not use any additional components for this function.