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International
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REFERENCE DESIGN

# IRAUDAMP9

## 1.7 kW / 2-Ω Single Channel Class D Audio Power Amplifier Using the IRS2092S and IRFB4227

By

Israel Serrano and Jun Honda

**CAUTION:**

**International Rectifier recommends the following guidelines for safe operation and handling of IRAUDAMP9 demo board:**

- **Always wear safety glasses when operating demo board**
- **Avoid physical contact with exposed metal surfaces when operating the demo board**
- **Turn off demo board when placing or removing measurement probes**

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## Introduction

The IRAUDAMP9 reference design is a single-channel 1.7-kW ( @ 2Ω load) half-bridge Class D audio power amplifier. This reference design demonstrates how to use the IRS2092S Class D audio controller and external gate buffer, to implement protection circuits, and design an optimum PCB layout using the IRFB4227 (x 2 Pairs) TO-220 MOSFETs. This reference design may require additional heatsink or fan for normal operation (one-eighth of continuous rated power). The reference design provides all the required housekeeping power supplies for ease of use. The 1-channel design is capable of delivering higher than its rated power with provision of larger heat sink ( Rth <2° C / W).

### Applications

- Pro-Audio amplifiers
- Powered speakers
- Active Sub-woofers
- P.A. Systems
- Car audio amplifier
- Musical Instrument Amplifier

### Features

| | |
|---|---|
| Output Power: | 1.7 kW Single channel (2 Ω load, 1kHz, THD+N=10%), |
| Residual Noise: | 290μV, IHF-A weighted, AES-17 filter |
| Distortion: | 0.07% THD+N @ 600W, 2Ω |
| Efficiency: | 97% @ 1.7 kW, 2Ω |
| Multiple Protection Features: | Output Over-current protection (OCP), high side and low side<br>Input Over-voltage protection (OVP),<br>Input Under-voltage protection (UVP),<br>Output DC-offset protection (DCP),<br>Over-temperature protection (OTP) |
| PWM Modulator: | Self-oscillating half-bridge topology with optional clock synchronization |

## Specifications

| **General Test Conditions (unless otherwise noted)** | | **Notes / Conditions** |
|---|---|---|
| Supply Voltages | ±75V | |
| Load Impedance | 2Ω | |
| Self-Oscillating Frequency | 300kHz | No input signal, Adjustable |
| Gain Setting | 33dB | 1Vrms input yields 1-kW sinusoidal output power |

| **Electrical Data** | **Typical** | **Notes / Conditions** |
|---|---|---|
| IR Devices Used | IRS2092S Audio Controller and Gate-Driver,<br>IRFB4227 (x 2 Pairs) TO-220 MOSFETs | |
| Modulator | Self-oscillating, second order sigma-delta modulation, analog input | |
| Power Supply Range | ± 48V to ±80V | Bipolar power supply |
| Output Power CH1: (1% THD+N) | 1200W | 1kHz Sinewave |
| Output Power CH1: (10% THD+N) | 1700W | 1kHz Sinewave |
| Rated Load Impedance | 2 Ω | Non-inductive Resistive load |
| Idling Supply Current | +67mA , -105mA | No input signal |
| Total Idle Power Consumption | 13.2 W | No input signal |
| System Efficiency | 97%<br>94%<br>74 % | @ +/- 75V 1.7 kW, 2Ω<br>@ +/- 75V 1.2 kW, 2Ω<br>@ +/- 75V 125 W (1/8 Po-rated), 2Ω |

| Audio Performance | Class D Output | Notes / Conditions |
|---|---|---|
| THD+N, @ 1W<br>THD+N, @ 125W<br>THD+N, @ 250W<br>THD+N, @ 500W<br>THD+N, @ 1250W<br>THD+N, @ 1700W | 0.024%<br>0.025%<br>0.025%<br>0.049%<br>1.0 %<br>10.0% | 1kHz, +/-75Vbus,<br>2-ohm load |
| Dynamic Range | 99.4 dB | A-weighted, AES-17 filter,<br>Single-channel operation |
| Residual Noise, 22Hz - 20kHz AES17 | 290μV | Self-oscillating – 300kHz<br>AP BW:<10Hz- 20kHz AES17<br>IHF-A weighted |
| Damping Factor | 81.9 | 1kHz, relative to 2Ω load |
| Frequency Response : 20Hz-20kHz | ±1dB | 1W, 2Ω Load |

| Thermal Performance | Typical | Notes / Conditions |
|---|---|---|
| Idling | $T_C$ = 56°C | No signal input, $T_A$=25°C, after 5 min |
| 125W (1/8 rated power) | $T_C$ = 104°C | Continuous @ $T_A$=25°C<br>*requires larger heatsink design for continuous operation |
| 1.2 kW | $T_C$ = 118°C | At OTP shutdown after 130 sec, $T_A$=25°C |

**Physical Specifications**

| | |
|---|---|
| Dimensions | 7.76”(L) x 5.86”(W) x 2.2”(H)<br>192 mm (L) x 149mm (W) x 56mm(H) |
| Weight | 0.54kgm |

## Connection Setup

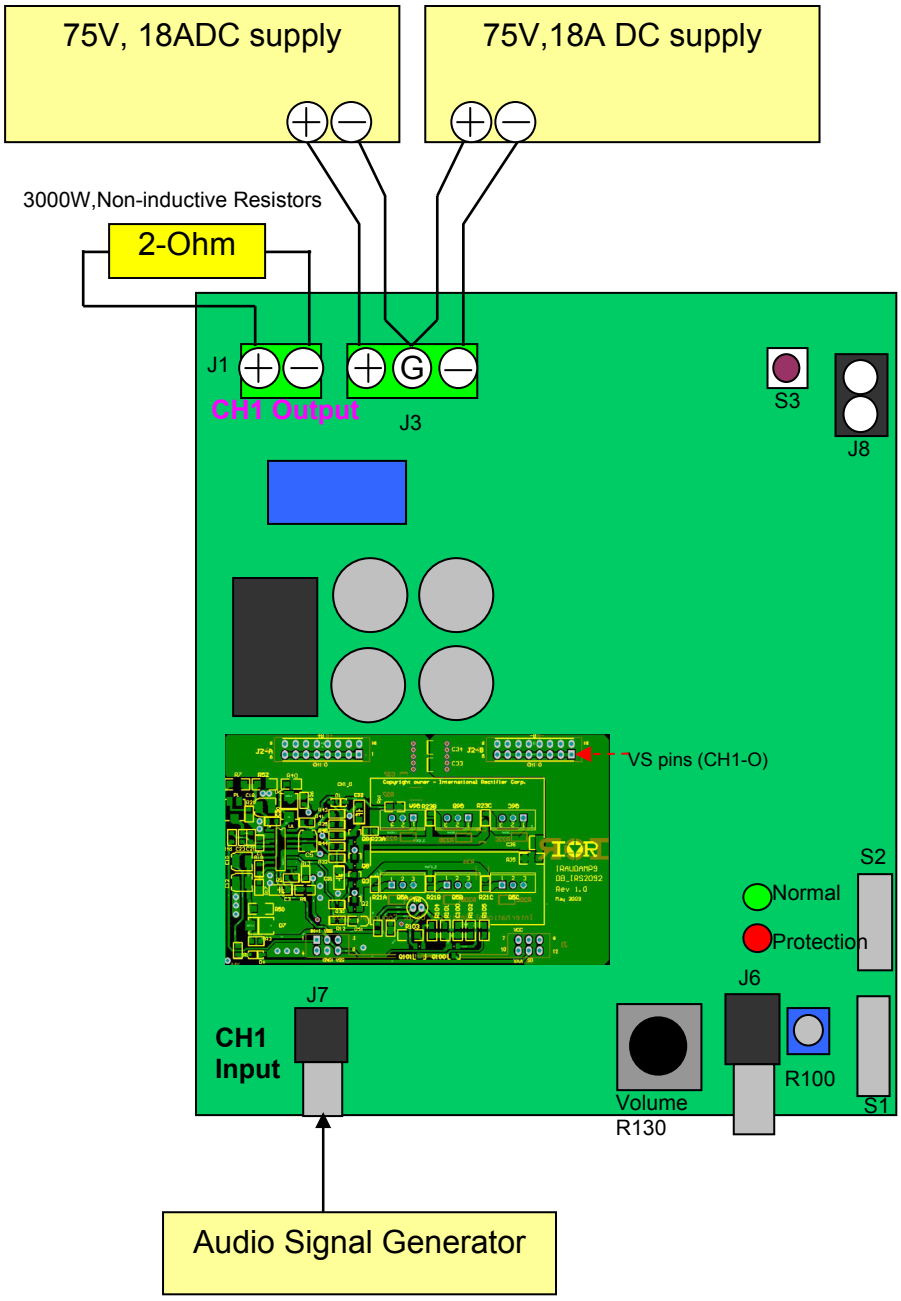



**Figure 1 Typical Test Setup**

### Connector Description

| | | |
|---|---|---|
| CH1 IN | J7 | Analog input for CH1 |
| POWER | J3 | Positive and negative supply (+B / -B) |
| CH1 OUT | J1 | Output for CH1 |
| EXT CLK | J6 | External clock sync |
| DCP OUT | J8 | DC protection relay output |

## Test Procedures

### Test Setup:

1. Connect 2Ω - 3000 W dummy loads to the output connectors (J1 as shown on Figure 1).
2. Connect the Audio Precision Analyzer (AP) signal Generator output to J7.
3. Initially set the voltages of the dual power supplies to ±75V with current limits to 0.5 A.
4. Make sure to TURN OFF the dual power supplies before connecting to the unit under test (UUT).
5. Set switch S1 to middle position (self oscillating).
6. Set volume level knob R130 fully counter-clockwise (minimum volume).
7. Connect the dual power supply to J3 as shown in Figure 1.

### Power up:

8. Turn ON the dual power supply. The ±B supplies must be applied and removed at the same time.
9. Red LED (Protection) should turn on almost immediately and turn off after about 3s.
10. Green LED (Normal) then turns on after the red LED is extinguished and should stay ON.
11. Note the quiescent current for the positive supply should be 67mA ±10mA at +75V.
12. Quiescent current for the negative supply should be 105mA ±15mA at –75V.
13. Push switch S3 (Trip and Reset push-button) to restart the LEDs sequence, which should be the same as noted above in steps 9 and 10.

### Switching Frequency test

14. Monitor switching waveform at VS1/J4 (pins 9-12) of CH1 on Daughter Board using an oscilloscope.
15. For IRAUDAMP9, the self-oscillating switching frequency is pre-calibrated to 300 kHz. To modify the IRAUDAMP9 frequency, adjust the potentiometer P1 for CH1.

### Audio Functional Tests:

16. Set the current limit of the dual power supplies to ~18A. Make sure the volume control potentiometer is turned to full counterclockwise position. Apply 1V rms @ 1 kHz from the Audio Signal Generator to the audio input connector J7.
17. Turn control volume, R130 clock-wise to obtain an output reading of 1.0 kW. For all the subsequent tests as shown on the Audio Precision graphs below, measurements are taken across J1 with an AES-17 Filter. Observe that a 1 $V_{RMS}$ input generates an output voltage of ~44.8 $V_{RMS}$. Alternatively, a 100-mVrms input would give an output of ~ 10.03W that corresponds to 4.48Vrms across a 2-ohm load.
18. Using an oscilloscope monitor the output signals at J1 while sweeping the audio input signal from 10 $mV_{RMS}$ to 2 $V_{RMS}$. The waveform must be a non distorted sinusoidal signal.

### Test Setup using Audio Precision Analyzer (Ap):

19. Use an unbalanced-floating signal from the generator outputs.
20. Use balanced inputs taken across output terminal J1.
21. Connect Ap chasis ground to GND at terminal J7.
22. Select the AES-17 filter (pull-down menu) for all the testing except frequency response.
23. Use input signal ranging from 15 $mV_{RMS}$ to 1 $V_{RMS}$.
24. Run Ap test programs for all subsequent tests as shown in Figure 2 below.

## Performance and test graphs

**±B Supply = ± 75V, 2 Ω Load**

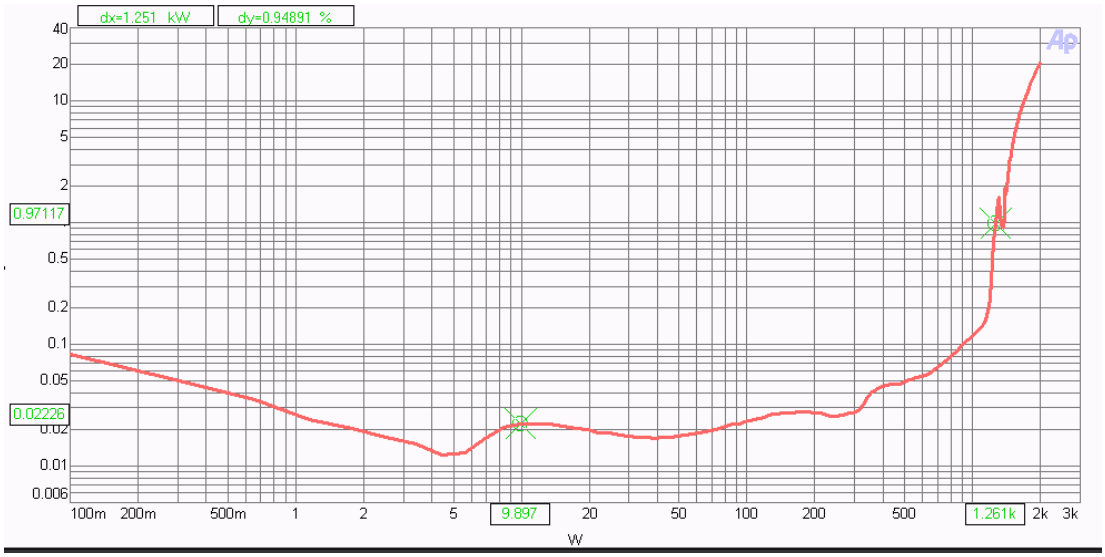



**Figure 2 THD+N vs. Power**

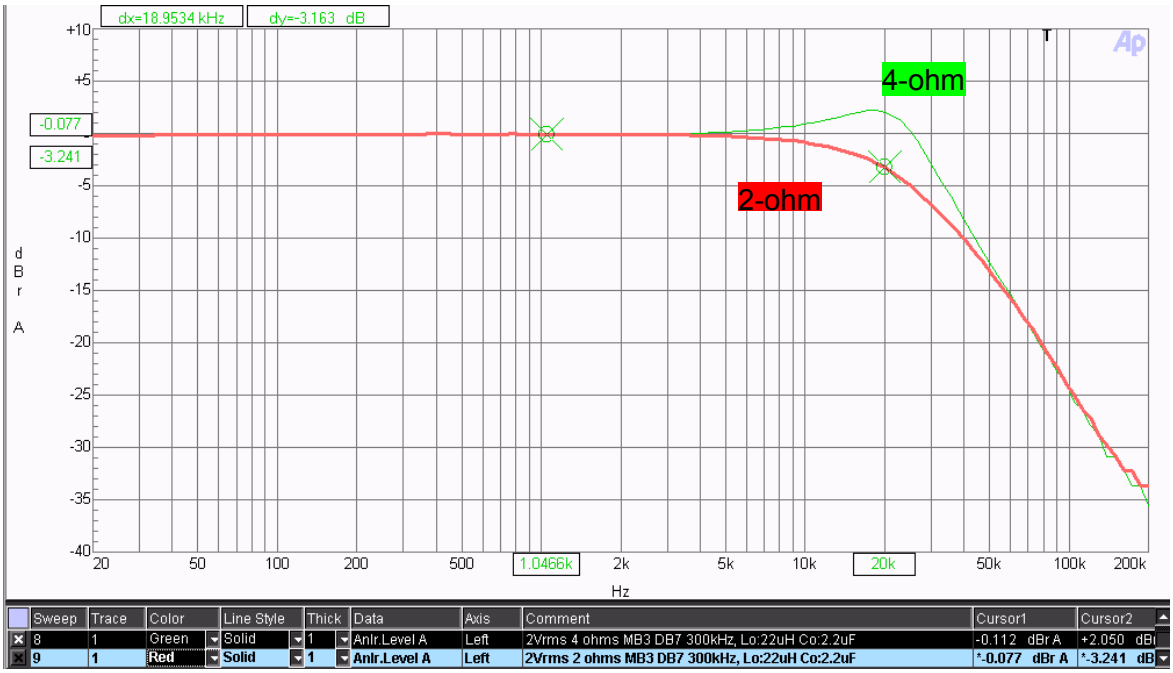



**Figure 3 Frequency response**

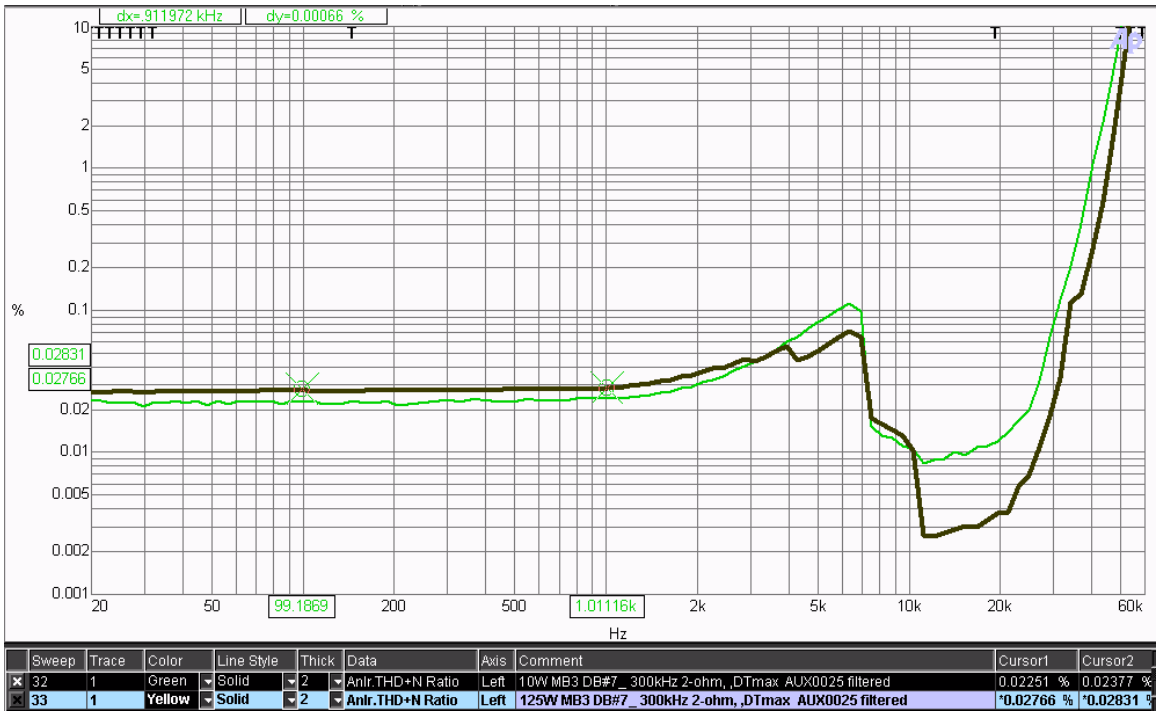
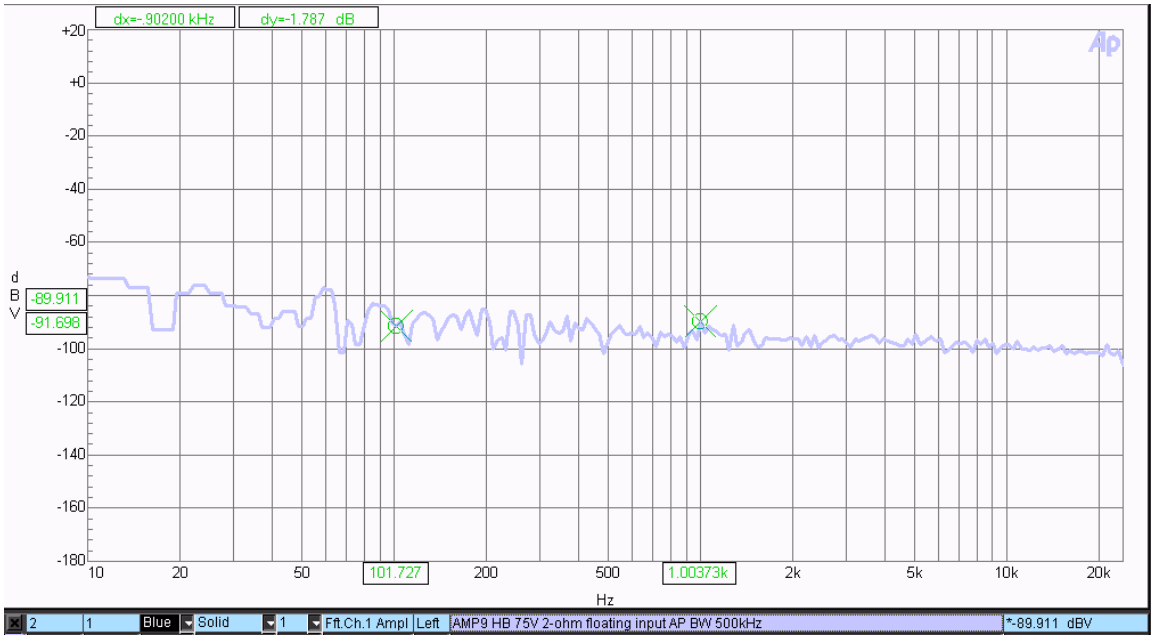



**Figure 4 THD+N vs. Frequency at 10W and 125W**




No signal, Self Oscillator @ 300kHz

**Figure 5 Noise Floor**

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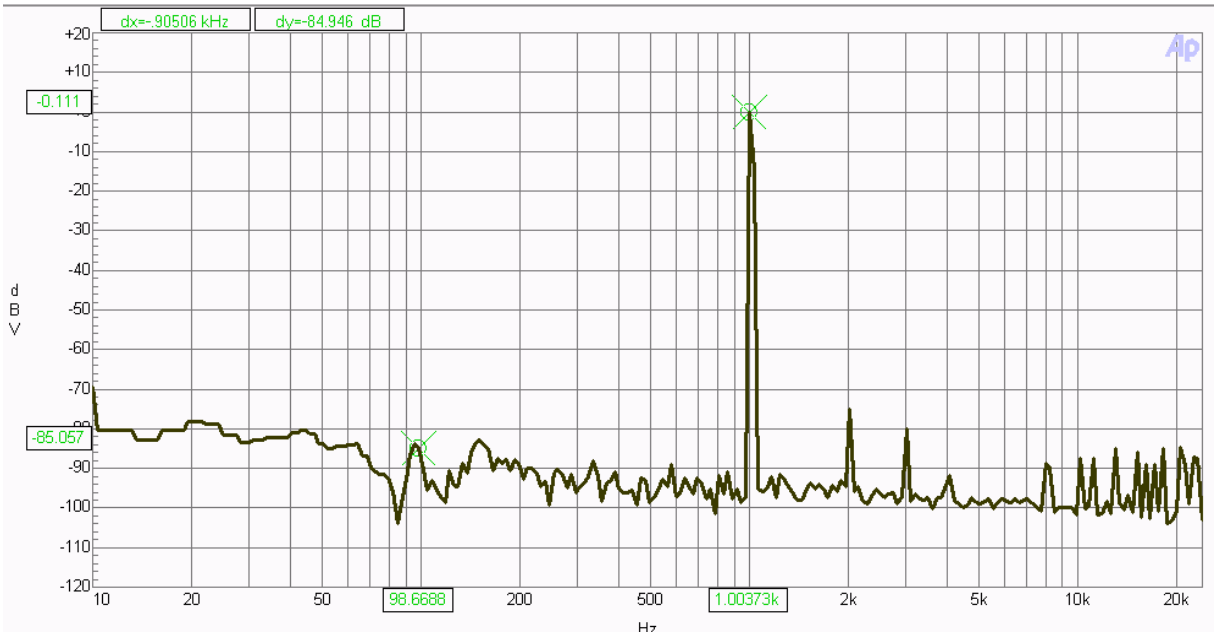


**Figure 6.** 1-$V_{RMS}$ **output Frequency Spectrum**

## IRAUDAMP9 Overview

The IRAUDAMP9 features a single-channel self-oscillating PWM modulator. This topology results in the lowest component count, highest performance and robust design. It represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of error correction.

The IRAUDAMP9 self-oscillating topology incorporates the following functional blocks.

- Front-end integrator
- PW Modulator and Level shifters
- Gate driver and buffer
- Power MOSFETs
- Output LPF

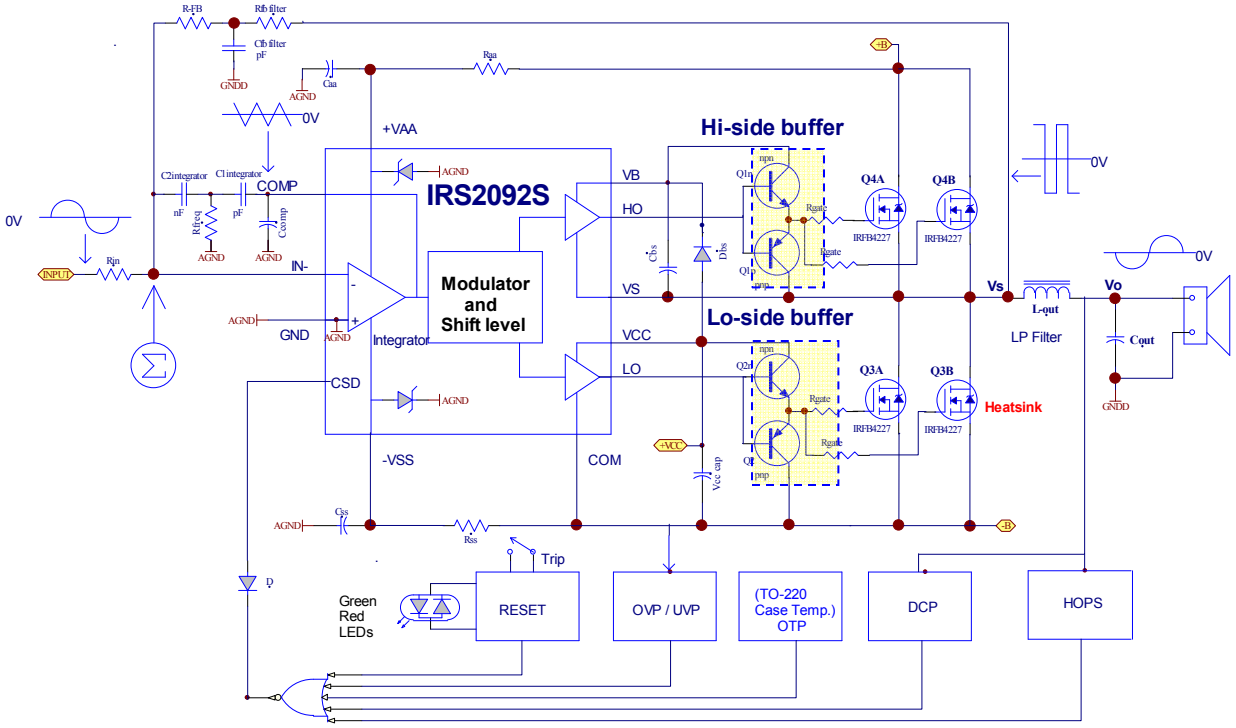


Fig. 7 Functional block diagram

# Functional Description

### Class-D Operation

The $C2_{integrator}$, $C_{1integrator}$, R21 + potentiometer P1 form a front-end second-order integrator. This integrator receives a rectangular feedback signal from the Class D switching stage and outputs a quadratic oscillatory waveform as a carrier signal. To create the modulated PWM signal, the input

signal shifts the average value of this quadratic waveform (through gain relationship between [(R38+R39) / (R154+R40)] ratio) so that the duty varies according to the instantaneous value of the analog input signal. The IRS2092S input comparator processes the signal to create the required PWM signal. This PWM signal is internally level-shifted down to the negative supply rail where it is split into two signals, with opposite polarity and added dead time, for high-side and low-side MOSFET gate signals, respectively. The IRS2092S drives 2 pairs of IRFB4227 TO-220 MOSFETs in the power stage to provide the amplified PWM waveform. The amplified analog output is re-created by demodulating the amplified PWM. This is done by means of the LC low-pass filter (LPF) formed by L4 and C34, which filters out the switching carrier signal.

## Gate Driver Buffer Stage

High power designs such as IRAUDAMP9 that use multiple mosfets in parallel connection to handle large amount of switching current often require far more than +/-1A drive current even for a brief moment due to mosfets' gate drive requirement (high total gate charge, Qg). In order to facilitate this high drive current, a buffer stage is devised to source and sink this high gate charge. This stage consists of NPN-PNP BJT transistors in totem pole configuration. It serves as a high-speed buffer amplifier that receives input from IRS2092S HO / LO to drive the power mosfet stage through Rg (1A,1B,2A,2B) for low side mosfets Q4(A,B) and for high-side Q3 (A,B) mosfets. Theoretically, the switching time is reduced by such amount (hfe) as compared to that high-Qg design that uses the divided output current capacity of the driver IC. This buffering action is very necessary to speed-up the switching times of each mosfets in order not to exceed the OCP voltage monitor time. The IC commences drain-to-source voltage monitoring as soon as the HO / LO go to high state but after the leading edge blanking time.

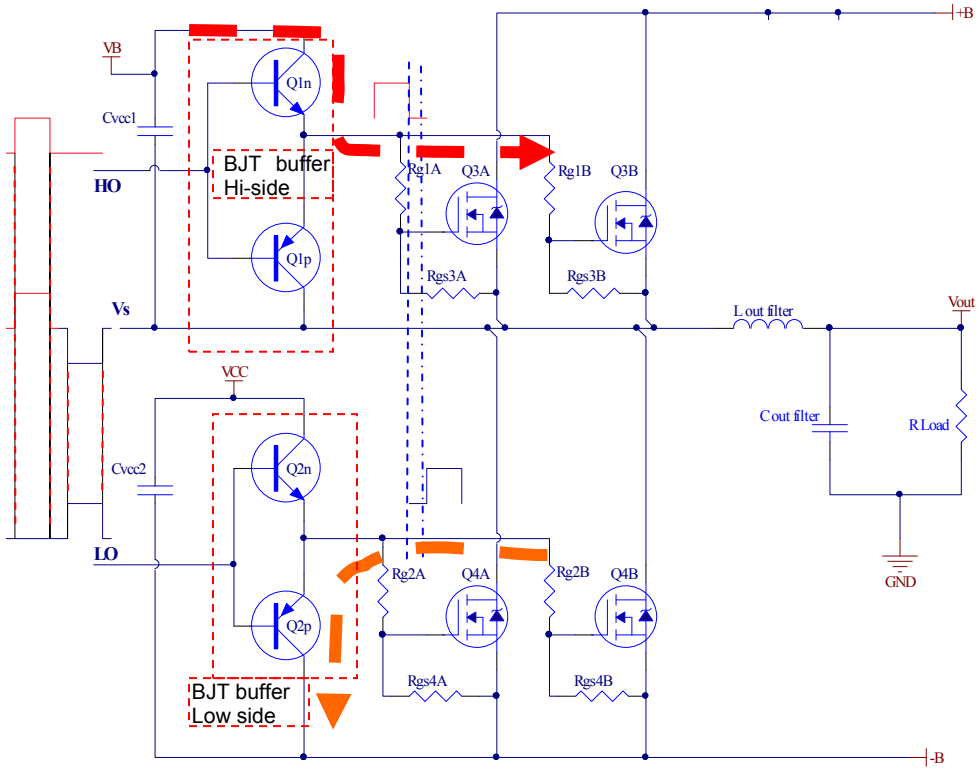


Fig. 8 Simplified diagram for gate-buffering of 2 x IRFB4227 mosfets

## Power Supplies

The IRAUDAMP9 has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies ranging from ±38 V to ±82 V (+B, GND, -B) for operation. The internally-generated housekeeping power supplies include a ±5 V supply for analog signal processing (preamp, etc.), and a +12 V supply (Vcc), referenced to –B, to supply the Class D gate-driver stage.

For the externally-applied power, a regulated power supply is preferable for performance measurements, but not always necessary. The bus capacitors, C45 ~ C48 on the motherboard, along with high-frequency bypass-capacitors C19 ~ C26 on daughter board, address the high-frequency ripple current that result from switching action. In designs involving unregulated power supplies, the designer should place a set of bus capacitors, having enough capacitance to handle the audio-ripple current, externally. Overall regulation and output voltage ripple for the power supply design are not critical when using the IRAUDAMP9 Class D amplifier as the power supply rejection ratio (PSRR) of the IRAUDAMP9 is excellent as shown in Figure 9 below.

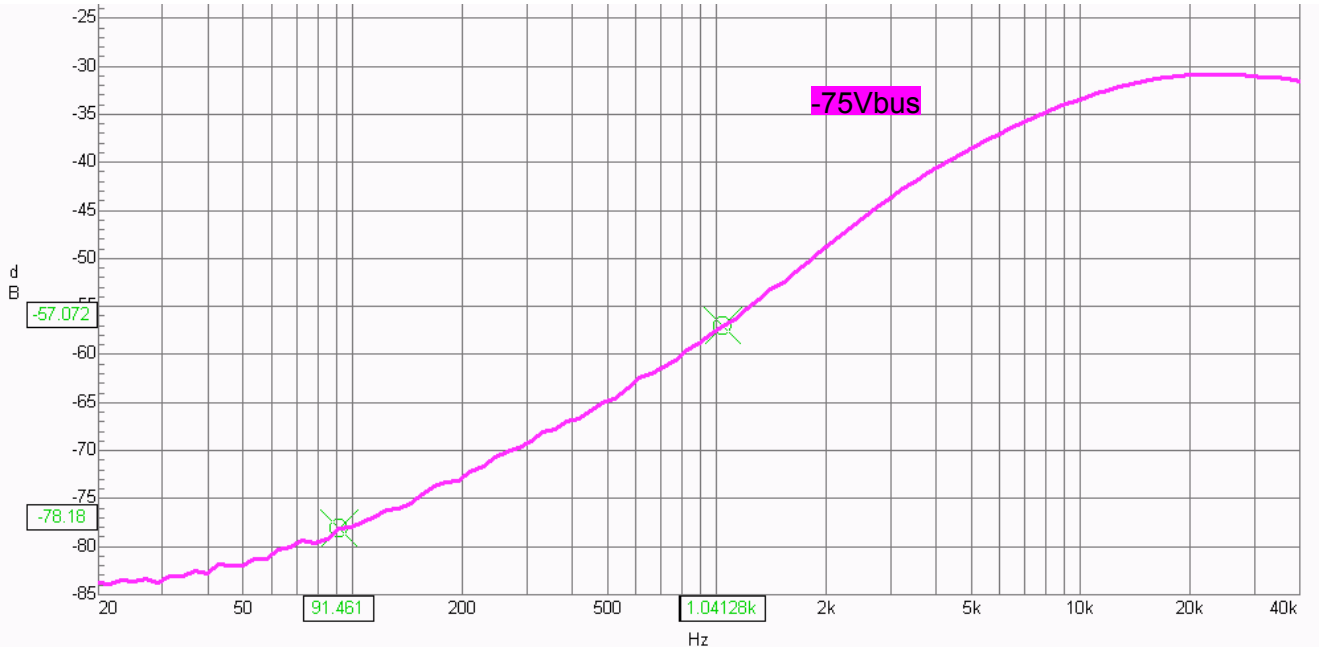


**Fig. 9 IRAUDAMP9 Power Supply Rejection Ratio (PSRR)**

## Bus Pumping

Since the IRAUDAMP9 is a half-bridge configuration, bus pumping does occur. Under normal operation during the first half of the cycle, energy flows from one supply through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage of the receiving power supply. In the second half of the cycle, this condition is reversed, resulting in bus pumping of the other supply.

The following conditions worsen bus pumping:

- Lower frequencies (bus-pumping duration is longer per half cycle)
- Higher power output voltage and/or lower load impedance (more energy transfers between supplies)
- Smaller bus capacitors (the same energy will cause a larger voltage increase)

The IRAUDAMP9 has protection features that will shutdown the switching operation if the bus voltage becomes too high (>82 V) or too low (<38 V). One brute countermeasure is to put a large electrolytic-capacitors between the power supply and the input terminals. Bus voltage detection is only done on the –B supply as the effect of the bus pumping on the supplies is assumed to be symmetrical in amplitude (although opposite in phase).

## House Keeping Power Supplies

The internally-generated power supplies include ±5V for analog signal processing, and +12V supply (Vcc) referred to the negative supply rail -B for TO-220 gate drive. The gate driver section of the IRS2092S uses Vcc to drive gates of the TO-220s. Vcc is referenced to –B (negative power supply). The D6, R26 and C5 form a bootstrap floating supply for the HO gate driver.

## Input

Input signal is an analog signal ranging from 20Hz to 20kHz with up to 2 $V_{RMS}$ amplitude with a source impedance of no more than 600 Ω. Input signal with frequencies around 20kHz may cause LC resonance in the output LPF and may result to a large reactive current flow through the switching stage, especially if the amplifier is not connected to any load - this can activate OC protection.

## Output

The IRAUDAMP9 has single output and therefore have terminals labeled (+) and (-) with the (-) terminal connected to power ground. Each channel is optimized for a 2 Ω speaker load for a rated output power of 1200 W @ 1% THD+N.

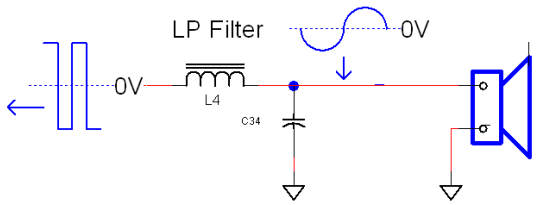


**Figure 10 Output Low Pass Filter**

## High Output Peak Shutdown (HOPS) circuit

It is common in amplifier design to have a RC snubber called Zobel network that is used to damp the resonance and prevent peaking frequency response with high load impedance. Instead, the IRAUDAMP9 has a simple detection circuit in placed, which consist of a NPN transistor, blocking diode and a current limiting resistor to detect the output peak status from exceeding –B supply during resonance of the output LC filter. This circuit pulls the Cstart capacitor (C66) down to output (+) that sends a signal to IRS2092S to inhibit the power stage from switching. As the output returns to unclipped level, the base-to-emitter voltage is reduced and releases the CSD cap to start charging. This would allow the IRS2092S to resume driving operation of the power stage.

The HOPS function is not expected to be triggered in normal operating conditions. It is use to halt the output going too negative ( < -B rail) during the natural resonance of output LC filter. The HOPS circuit is intended for higher than nominal impedance or open load conditions.

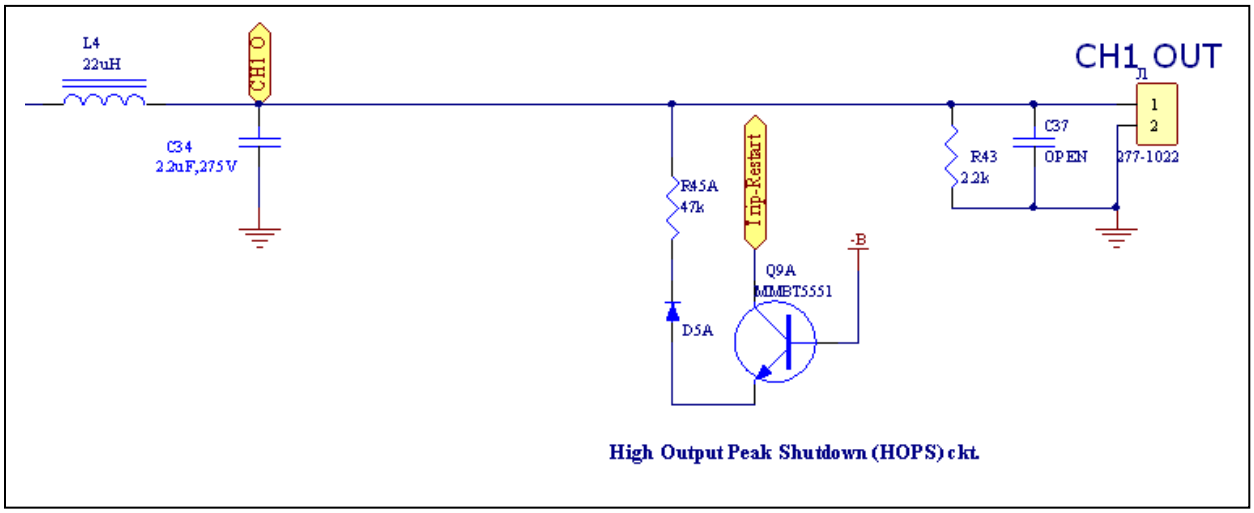


Fig. 11 Shutdown circuit diagram when output goes lower than negative rail.

## Gain Setting / Volume Control

The IRAUDAMP9 has an internal volume control (potentiometer R130 labeled, “VOLUME”) for gain adjustment. Gain setting is tracked and controlled by the volume control IC (U_2) setting the gain from the microcontroller IC (U_3). The total gain is a product of the power-stage gain, which is constant (+33 dB), and the input-stage gain that is directly-controlled by the volume adjustment. The volume range is about 100 dB with minimum volume setting to mute the system with an overall gain of less than -60 dB. For best performance in testing, the internal volume control should be set to 1 Vrms which results in rated output power (1 kW into 2 Ω).

## Efficiency

Figure 12 shows efficiency characteristics of the IRAUDAMP9. The high efficiency is achieved by the following major factors:

1) Low conduction loss due to the low $R_{DS(ON)}$ of the IRFB4227 mosfets
2) Low switching loss due to the high gate drive output for fast rise and fall times
3) Secure dead-time provided by the IRS2092S, avoiding cross-conduction

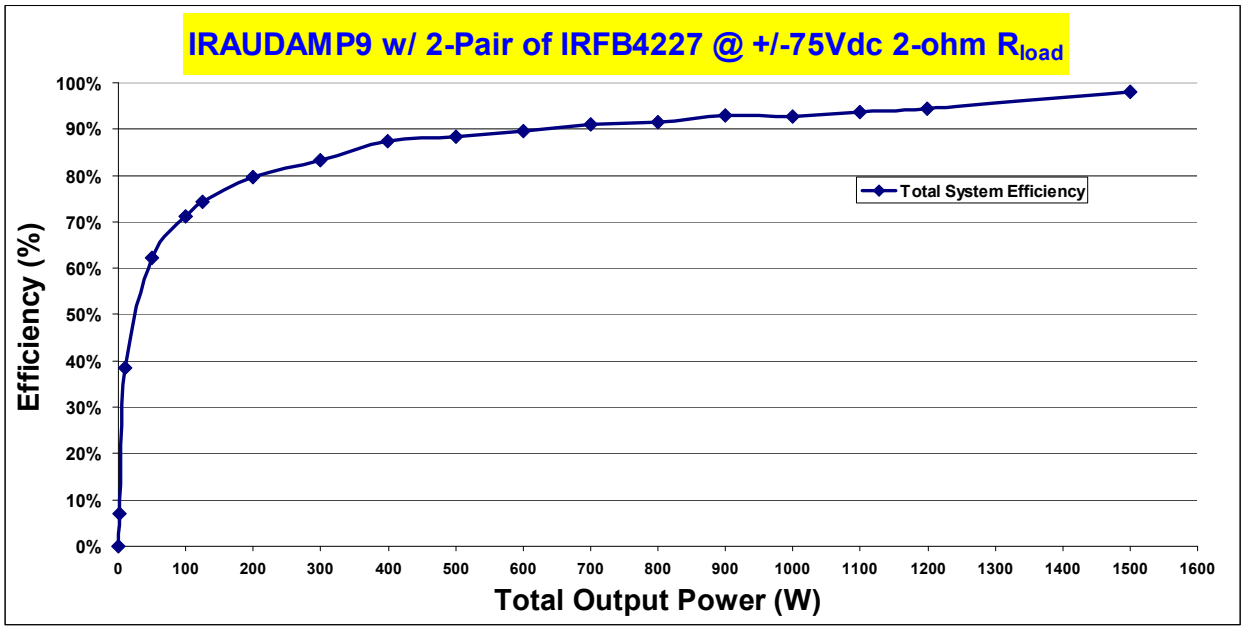


**Fig.12 Efficiency plots.**

## Output Filter and Preamplifier

### Output filter:

The amplified PWM output is reconstructed back to an analog signal by the output LC LPF.
This LPF is formed by L4 and C34, provides pass band for the audio frequencies while filtering out the switching carrier signal. A single stage output filter can be used with switching frequencies of around 300 kHz ; a design with a lower switching frequency may require an additional stage of filtering.

Since the output filter is not included in the control loop of the IRAUDAMP9, the reference design cannot compensate for performance deterioration due to the output filter. Therefore, it is important to select filter components with the following characteristics in mind.

1) The DC resistance of the inductor should be minimized to 6 mΩ or less.
2) The linearity of the output inductor and capacitor should be high with respect to load current and voltage.

**Preamplifier**

The preamp allows partial gain of the input signal. It is possible to evaluate the performance without the preamp and volume control, by removing R154 and feeding the input signal directly through R46 resistors (IN-1). This effectively bypasses the preamp and connects the RCA inputs directly to the Class D power stage input. Improving the preamp noise performance and the output filter, will improve the overall system performance approaching that of the stand-alone Class D power stage.

## Self-Oscillating PWM Modulator

The IRAUDAMP9 features a self-oscillating type PWM modulator for the lowest component count and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of correction.

The self-oscillating frequency is determined by the total delay time inside the control loop of the system. The delay of the logic circuits, propagation delay of IRS2092S gate-driver, delay caused by the external buffer, IRFB4227 (x 2 pairs) switching speed, time-constant of front-end integrator and variations in the supply voltages are critical factors of the self-oscillating frequency. Under normal conditions, the switching-frequency is around 300 kHz with no audio input signal and a +/-75 V supply.

### *Adjustments of Self-Oscillating Frequency*

The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute frequency and frequency relative to the other channels. In absolute terms, at higher frequencies, distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. Most importantly, higher switching frequency results in higher switching loss of the power stage, hence the thermal performance degrades, especially with those that having a limited-size heatsink design.

Potentiometers for adjusting self-oscillating frequency
P1 potentiometer + R21 Switching frequency for CH1*
*Adjustments have to be done in idle condition with no input signal.

## Switches and Indicators

There are two different indicators on the reference design:

- A red LED, signifying a fault / shutdown condition when lit.
- A green LED on the motherboard, signifying conditions are normal and no fault condition is present.

There are three switches on the reference design:

Switch S1 is an oscillator selector. This three-position switch is selectable for internal self-oscillator (middle position – “SELF”), or either internal (“INT”) or external (“EXT”) clock synchronization.

– Switch S3 is a trip and reset push-button. Pushing this button has the same effect of a fault condition. The circuit will restart about three seconds after the shutdown button is released.

## Startup and Shutdown

One of the most important aspects of any audio amplifier is the startup and shutdown procedures. Typically, transients occurring during these intervals can result in audible pop- or click-noise on the output speaker. Traditionally, these transients have been kept away from the speaker through the use of a series relay that connects the speaker to the audio amplifier only after the startup transients have passed and disconnects the speaker prior to shutting down the amplifier. It is interesting to note that the audible noise of the relay opening and closing is not considered "click noise", although in some cases, it can be louder than the click noise of non-relay-based solutions.

The IRAUDAMP9 does not use any series relay to disconnect the speaker from the audible transient noise, but rather depends on IRS2092S's on-chip noise reduction circuit that yields audible noise levels that are far less than those generated by the relays they replace. This results in a more reliable, superior performance system.

## Startup and Shutdown Sequencing

The IRAUDAMP9 sequencing is achieved through the charging and discharging of the $C_{Start}$ capacitor C66. This, coupled to the charging and discharging of the voltage of CSD (C10 on daughter board for CH1) of the IRS2092S, is all that is required for complete sequencing. The conceptual startup and shutdown timing diagrams are show in Figure 13.

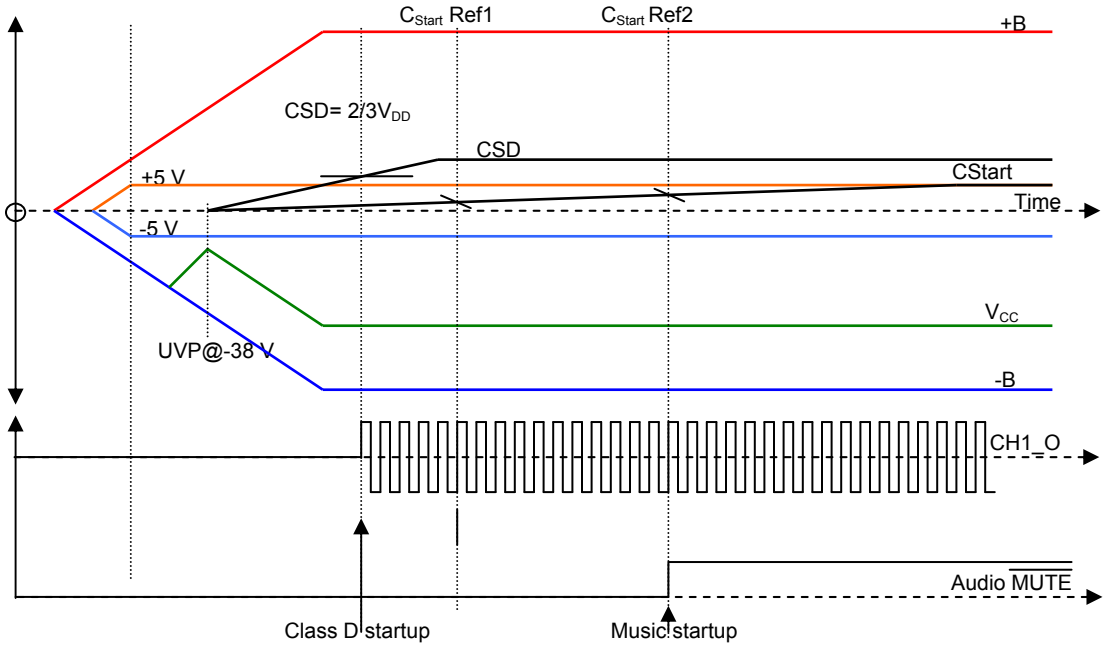


**Figure 13, Conceptual Startup Sequencing of Power Supplies and Audio Section Timing**

For startup sequencing, +/-B supplies startup at different intervals. As +/-B supplies reach +5 V (Vaa) and -5 V (Vss) respectively, the analog supplies (Vaa, Vss) start charging and, once +B

reaches ~16 V, Vcc charges. Once –B reaches -38 V, the UVP is released and CSD and $C_{Start}$ start charging. As CSD reaches two-thirds $V_{aa}$, the Class D stage starts oscillating. The Class D amplifier is now operational, but the preamp output remains muted until $C_{Start}$ reaches Ref2. At this point, normal operation begins. The entire process takes less than three seconds.

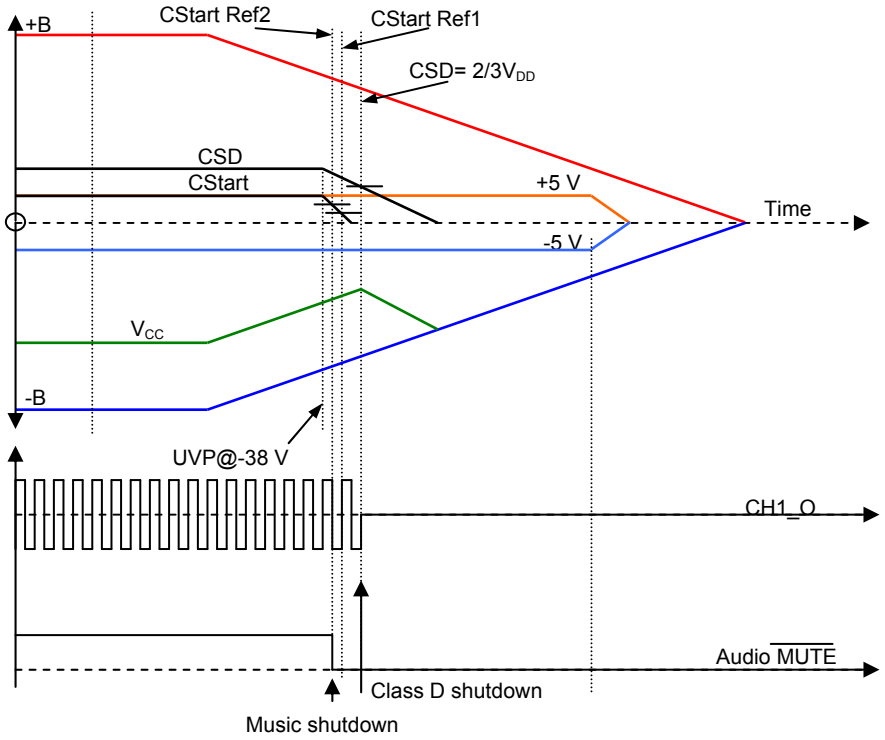


**Figure 14. Conceptual Shutdown Sequencing of Power Supplies and Audio Section Timing.**

Shutdown sequencing is initiated once UVP is activated. As long as the supplies do not discharge too quickly, the shutdown sequence can be completed before the IRS2092S trips UVP. Once UVP is activated, CSD and $C_{start}$ are discharged at different rates. In this case, threshold Ref2 is reached first and the preamp audio output is muted. Once $C_{Start}$ reaches threshold Ref1, the click-noise reduction circuit is activated. It is then possible to shutdown the Class D stage (CSD reaches two-thirds $V_{DD}$). This process takes less than 200 ms.

For any external fault condition (OTP, OVP, UVP or DCP – see “Protection”) that does not lead to power supply shutdown, the system will trip in a similar manner as described above. Once the fault is cleared, the system will reset (similar sequence as startup).

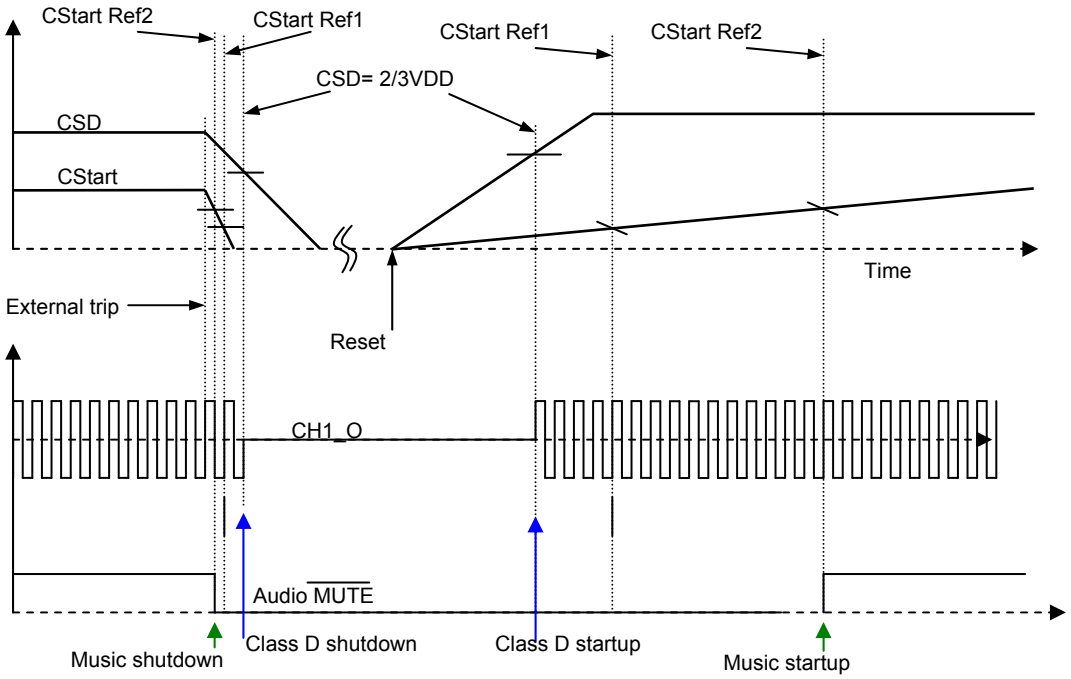


**Figure 15. Conceptual Click Noise Reduction Sequencing at Trip and Reset**

## Protection System Overview

The IRS2092S integrates over current protection (OCP) inside the IC. The rest of the protections, such as over-voltage protection (OVP), under-voltage protection (UVP), and over temperature protection (OTP), are detected externally to the IRS2092S.

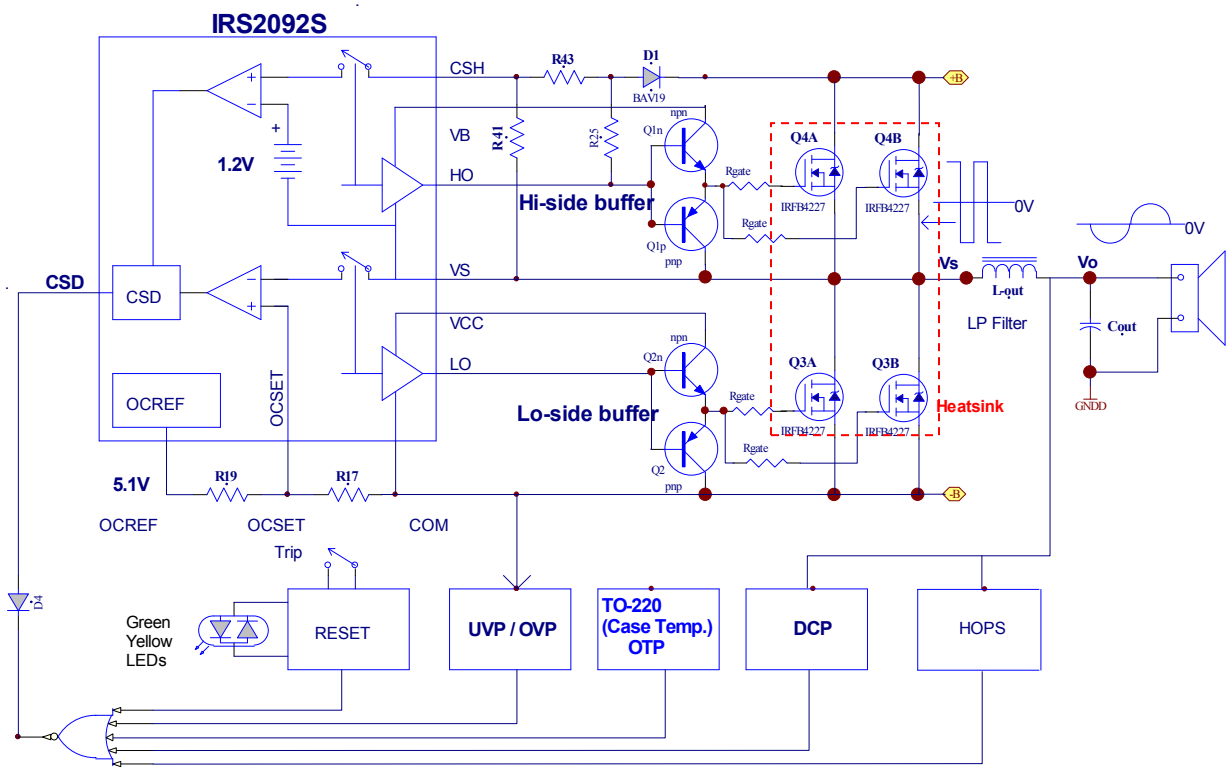


**Figure 16. Functional Block Diagram of Protection Circuit Implementation**

The external shutdown circuit will disable the output by pulling down CSD pins . If the fault condition persists, the protection circuit stays in shutdown until the fault is removed.

## Over-Current Protection (OCP)

The OCP internal to the IRS2092S shuts down the IC if an OCP is sensed in either of the output MOSFETs. For a complete description of the OCP circuitry, please refer to the application note AN1138. Here is a brief description:

### Low-Side Current Sensing

The low-side current sensing feature protects the low side MOSFET from an overload condition from negative load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level. An external resistive divider R17 and R19 on the daughter board are used to program the low-side OCP trip point.

The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. When the VS voltage becomes higher than the OCSET voltage during low-side conduction, the IRS2092S turns the outputs OFF and pulls CSD down to -VSS.

### High-Side Current Sensing

The high-side current sensing protects the high side MOSFET from an overload condition from positive load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

High-side over-current sensing monitors drain-to-source voltage of the high-side MOSFET during the on state through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side MOSFET. In contrast to the low-side current sensing, the threshold of the CSH pin to trigger OC protection is internally fixed at 1.2V. An external resistive divider, R41 and R43 are used to program a hi-side OCP trip point. An external reverse blocking diode D8 is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D1, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source.

## Input Bus Over-Voltage Protection (OVP)

OVP is provided externally to the IRS2092S. OVP shuts down the amplifier if the bus voltage between GND and -B exceeds 82V. The threshold is determined by a Zener diode Z9. OVP protects the board from harmful excessive supply voltages, such as due to bus pumping at very low frequency-continuous output in stereo mode.

## Input Bus Under-Voltage Protection (UVP)

UVP is provided externally to the IRS2092S. UVP prevents unwanted audible noise output from unstable PWM operation during power up and down. UVP shuts down the amplifier if the bus voltage between GND and -B falls below a voltage set by Zener diode Z8.

## Speaker DC-offset Protection (DCP)

DCP protects speakers against DC output current feeding to its voice coil. DC offset detection detects abnormal DC offset and shuts down PWM. If this abnormal condition is caused by a MOSFET failure because one of the high-side or low-side MOSFETs short circuited and remained in the on state, the power supply needs to be cut off in order to protect the speakers. Output DC offset greater than ±2.1V triggers DCP.

## Offset Null (DC Offset) Adjustment

The IRAUDAMP9 is designed such that no output-offset nullification is required. DC offsets are tested to be less than ±50 mV.

## Over-Temperature Protection (OTP)

An external NTC resistor is placed in close proximity to the low-side Q5A IRFB4227 TO-220 MOSFET. If the thermistor temperature rises above 100 °C, the OTP is activated. The OTP protection will shut down switching by pulling the CSD pin low and will recover once the temperature at the NTC has dropped sufficiently. This temperature protection limit yields a PCB temperature at the MOSFET of about 100 °C. This setting is limited by the PCB material and not by the operating range of the MOSFET.

## Thermal Considerations

Due to limited heat sink size, the IRAUDAMP9 is designed for high efficiency to deliver 1 kW rated power for 1 minute at open-air room temperature ( starting w/ Tamb: ~22 - 25C)
However, the IRAUDAMP9 requires larger heatsink design to handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards. If the user decides to increase the size of the heatsink or have a minimum forced air-cooling, the daughter board can handle continuous rated power.

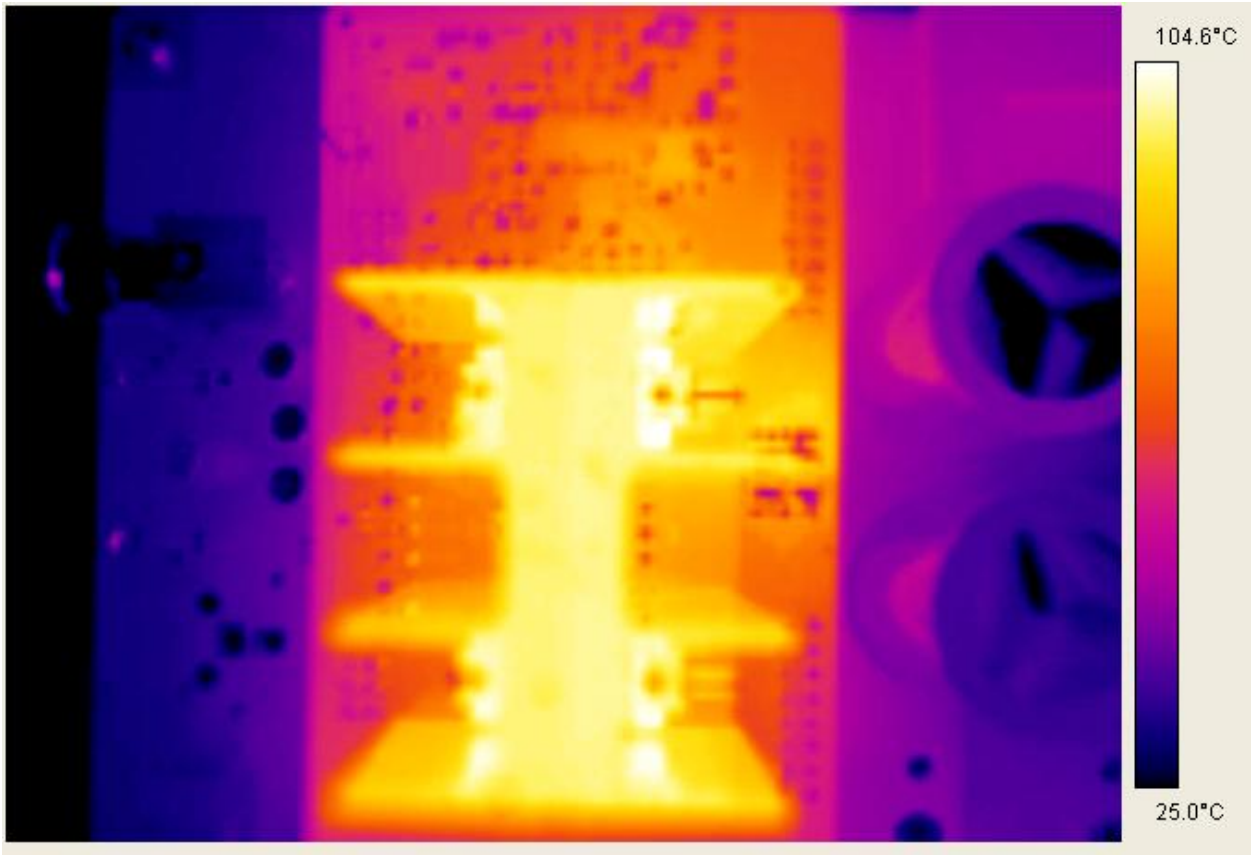


**Figure 17. Thermal image of the heatsink assembly during 1/8 rated power burn-in test.**

## Short Circuit Protection Response

Figures 18-19 show over current protection reaction time of the IRAUDAMP9 in a short circuit event. As soon as the IRS2092S detects an over current condition, it shuts down PWM. After one second, the IRS2092S tries to resume the PWM. If the short circuit persists, the IRS2092S repeats try and fail sequences until the short circuit is removed.

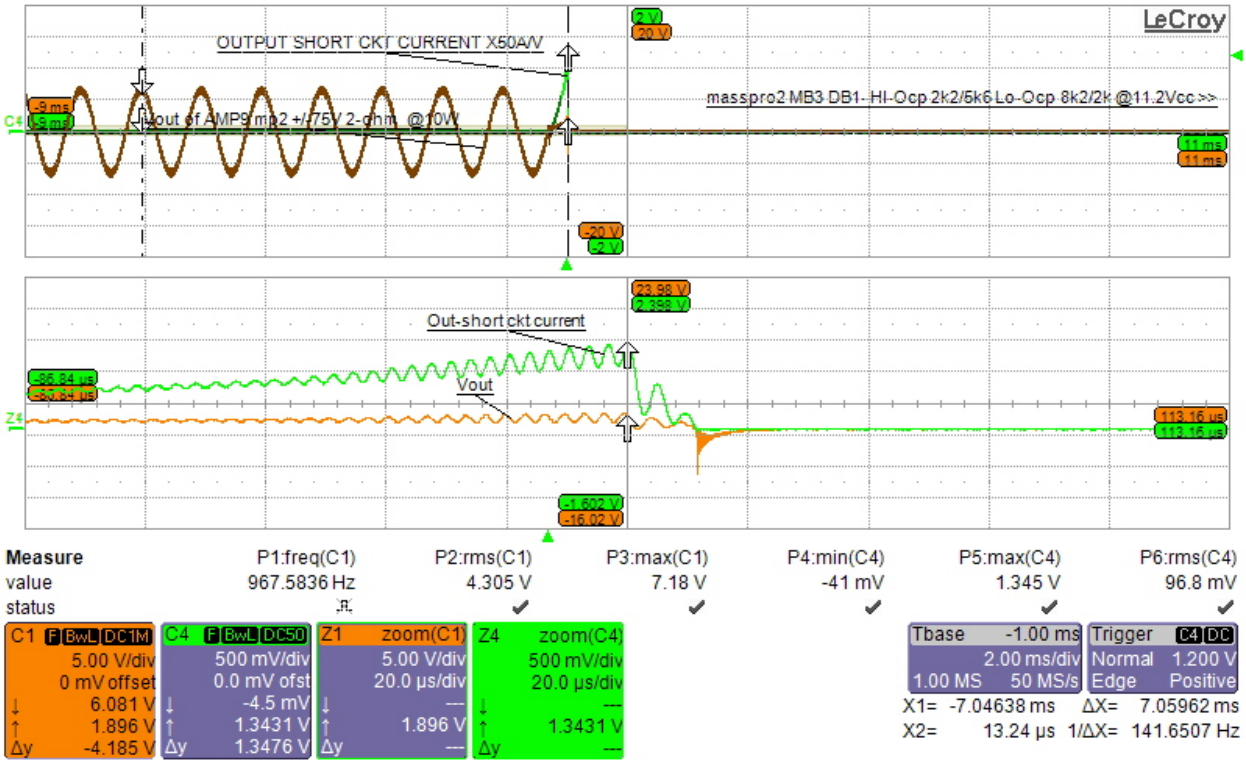


*Figure 18. Positive-side OCP waveforms during short circuit test at 10W load condition.*

## High side OCP Calculation :

## Given:

**Vf = 0.7V, $R_{dsON}$ : 9.85 mohm : 2 // IRFB4227**

**$V_{dsON}$ = Idtrip * $R_{dsON}$ = 0.985 V**

**Let R43 = 2.2 kohm, R41 = 5.6 kohm**

$$I_{dtrip\_Hi-side} = \frac{(\frac{V_{thOCH} * (R41 + R43)}{R41}) - V_f)}{R_{dsON}}$$ **= Calculated OCP current limit: ~99 Apk**

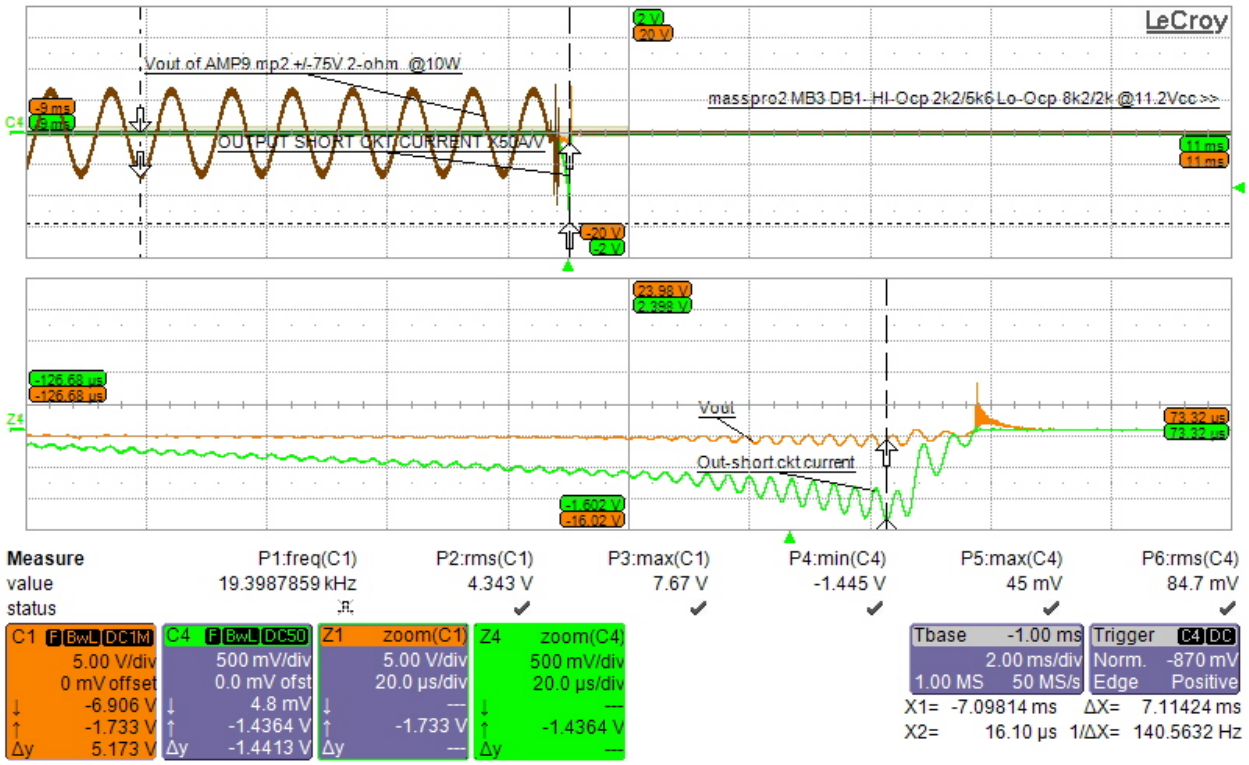


*Figure 19 Negative-side OCP waveforms during short circuit test at clipping condition.*

**Lo- side OCP Calculation :**

**Given: Vref = 5.1V**

**$R_{dsON}$ ( for 2 // IRFB4227) : 9.85 mohm**

**Let R19 = 8.2 kohm, R17 = 2.0 kohm**

$$V_{OCset} = Vref * R17 / (R17+R19)$$

$$I_{dtrip\_Lo\text{-}side} * R_{dsON} = V_{OCset}$$

$$I_{dtrip\_Lo-side} = \frac{Vref * (\frac{R17}{(R17+R19)})}{R_{dsON}}$$ **= Calculated OCP current limit: ~101 Apk**

# Schematic Diagrams

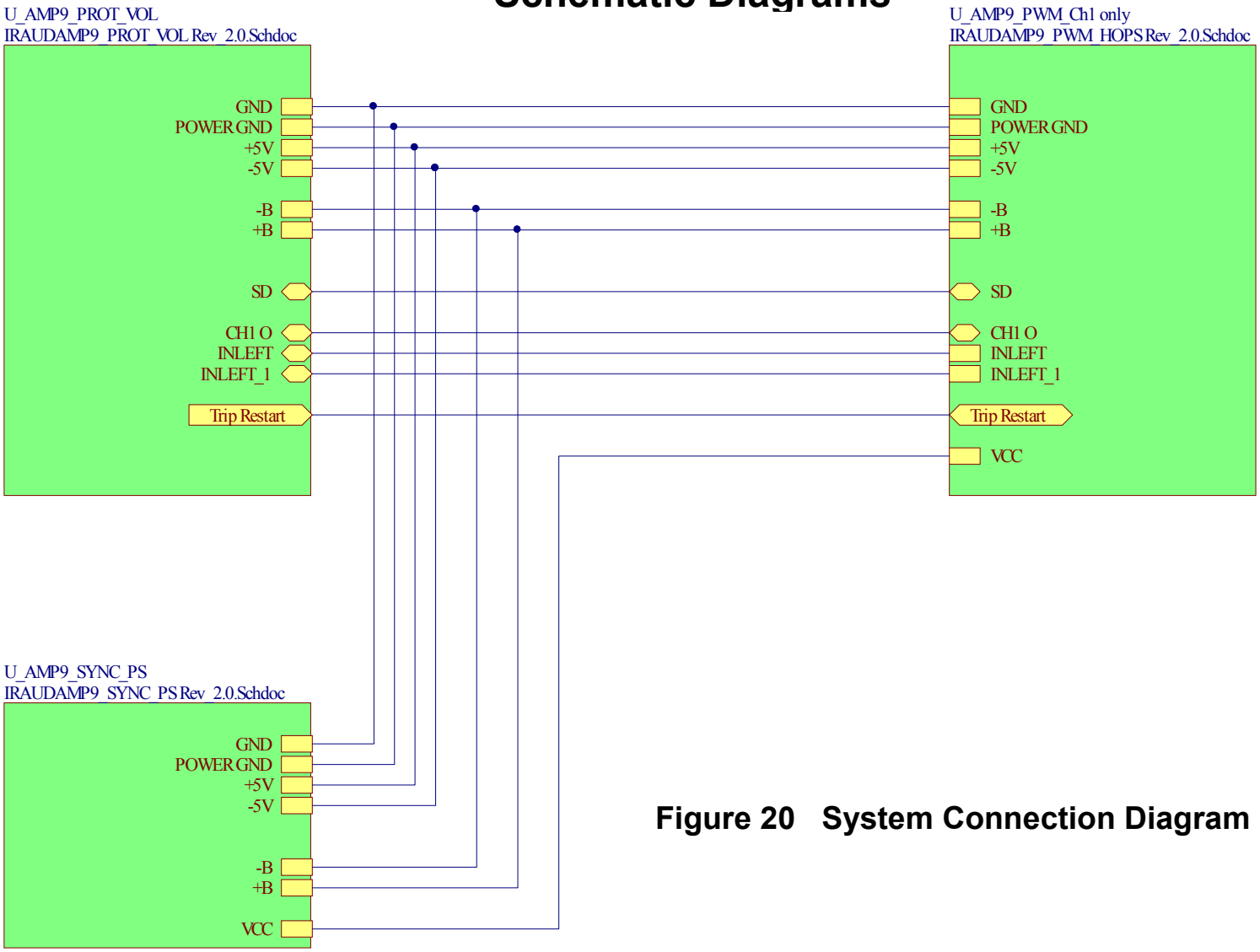


**Figure 20 System Connection Diagram**