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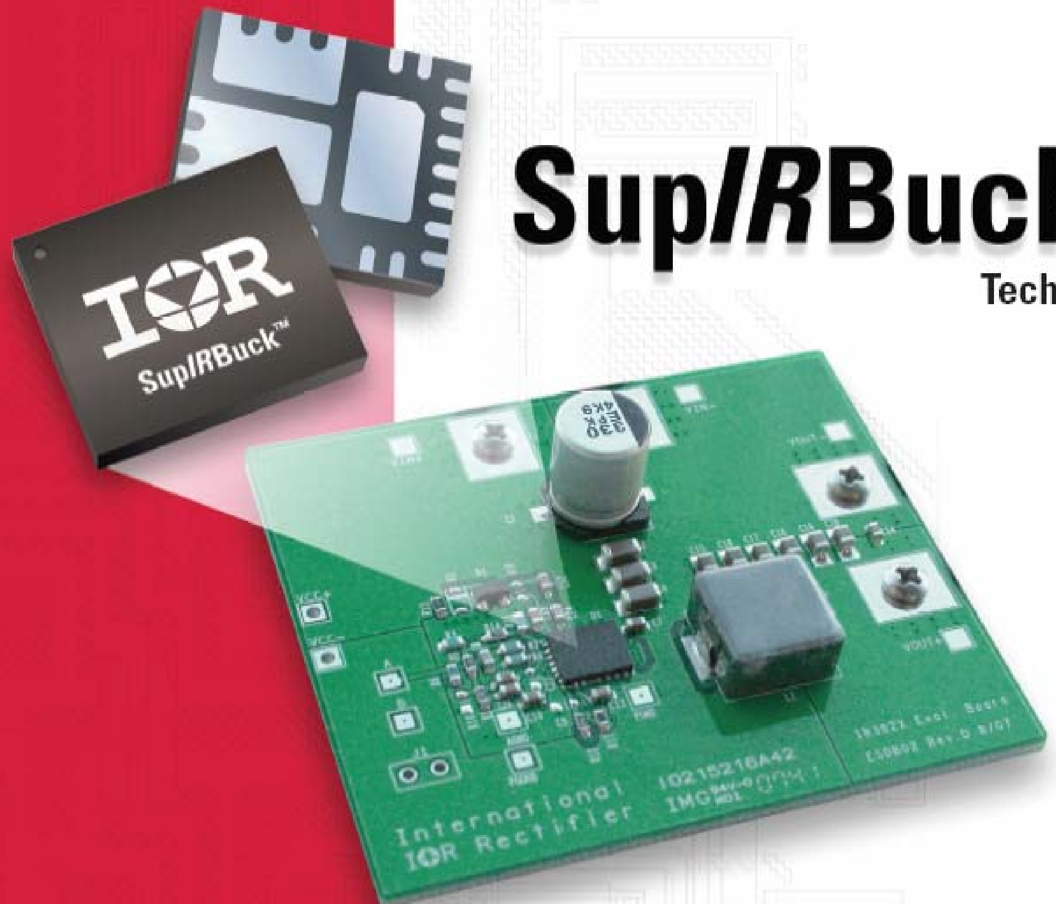


SupIRBuck™
Technology

IRDC3822A – Integrated Point of Load DC-DC Voltage Regulator

Featuring IR3822A Voltage Regulator

Programmable Soft Start; Programmable Power Good; Programmable Over Current Protection; Pre-Bias Start Up

300kHz Switching Frequency

$12V_{IN}$ to $1.8V_{OUT}$ @ 6A

International
IOR Rectifier

SupIRBuck™

USER GUIDE FOR IR3822A EVALUATION BOARD

DESCRIPTION

The IR3822A is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 5mmx6mm Power QFN package.

Key features offered by the IR3822A include programmable soft-start ramp, precision 0.6V reference voltage, programmable Power Good, thermal protection, fixed 300kHz switching frequency requiring no external component, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3822A evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3822A is available in the IR3822A data sheet.

BOARD FEATURES

- V_{in} = +12V (13.2V Max)
- V_{out} = +1.8V @ 0- 6A
- L= 2.2uH
- C_{in}= 3x10uF (ceramic 1206) + 330uF (electrolytic)
- C_{out}= 6x22uF (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 6A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3822A has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). These inputs are connected on the board with a zero ohm resistor (R15). Separate supplies can be applied to these inputs. Vcc input cannot be connected unless R15 is removed. Vcc input should be a well regulated 5V-12V supply and it would be connected to Vcc+ and Vcc-.

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
Vcc+	Optional Vcc input
Vcc-	Ground for Optional Vcc input
VOUT-	Ground of V_{out}
VOUT+	V_{out} (+1.8V)
P_Good	Power Good Signal

LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. The IR3822A SupIRBuck and all of the passive components are mounted on the top side of the board.

Power supply decoupling capacitors, the charge-pump capacitor and feedback components are located close to IR3822A. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the SupIRBuck.

To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

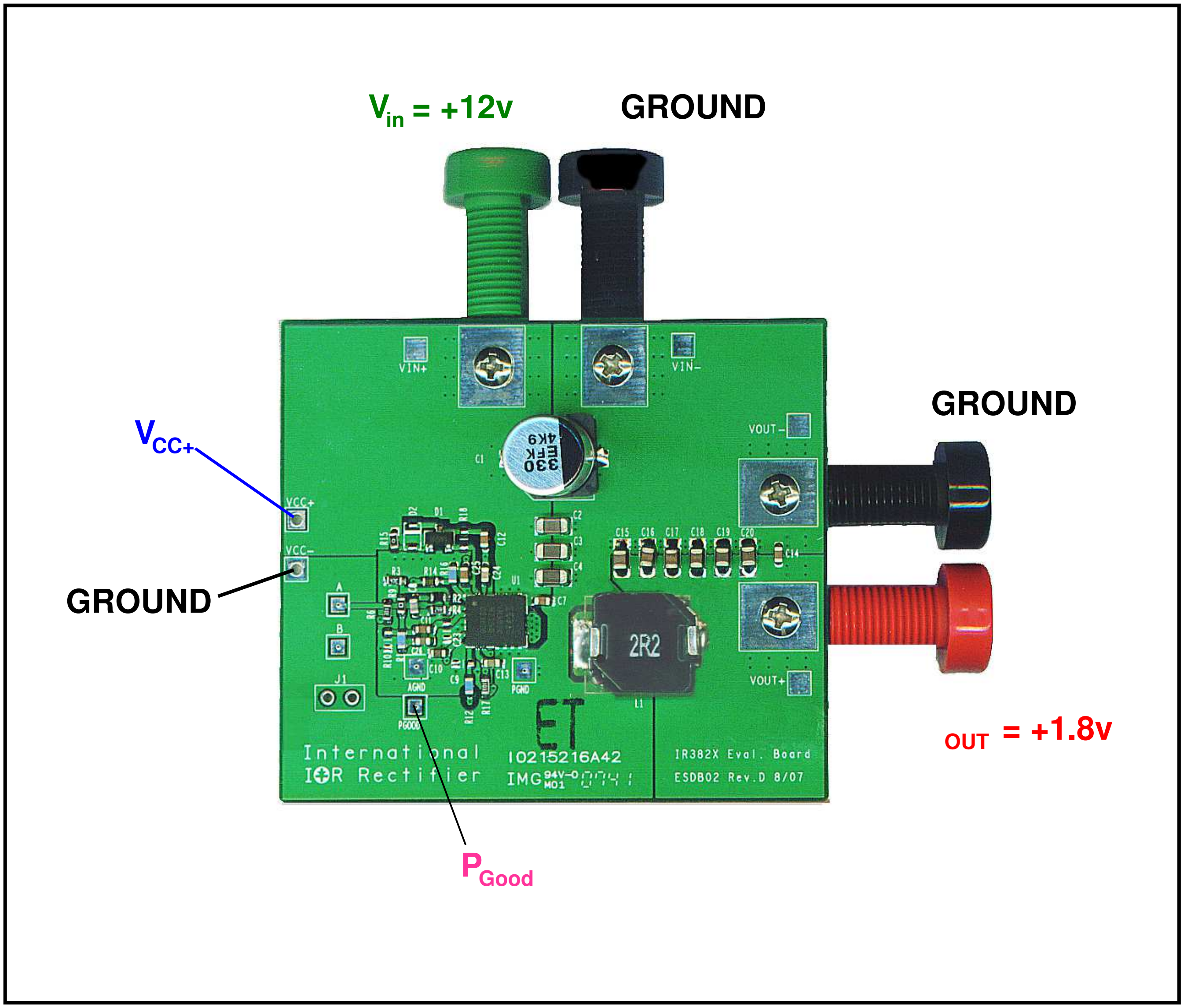


Fig. 1: Connection diagram of IR3822A evaluation board

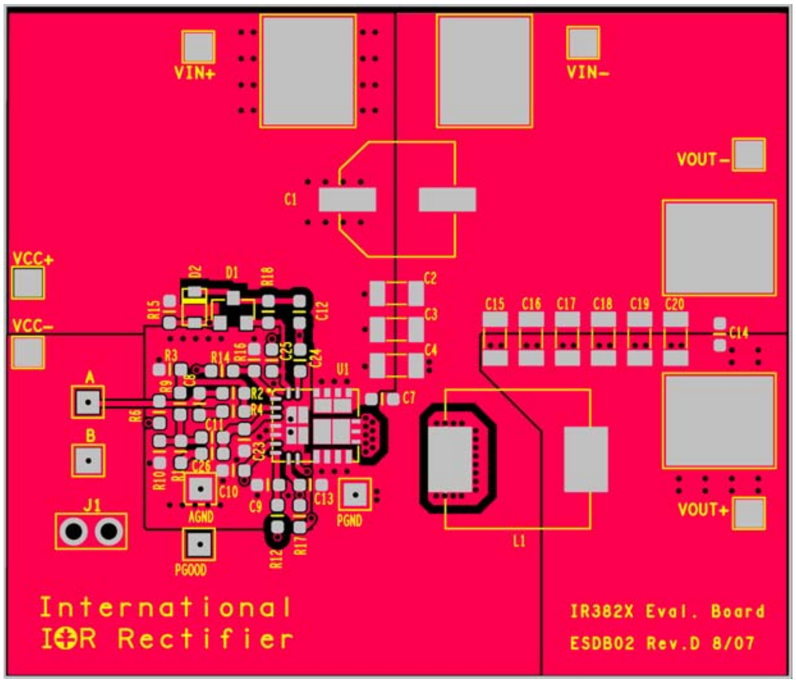


Fig. 2: Board layout, top overlay

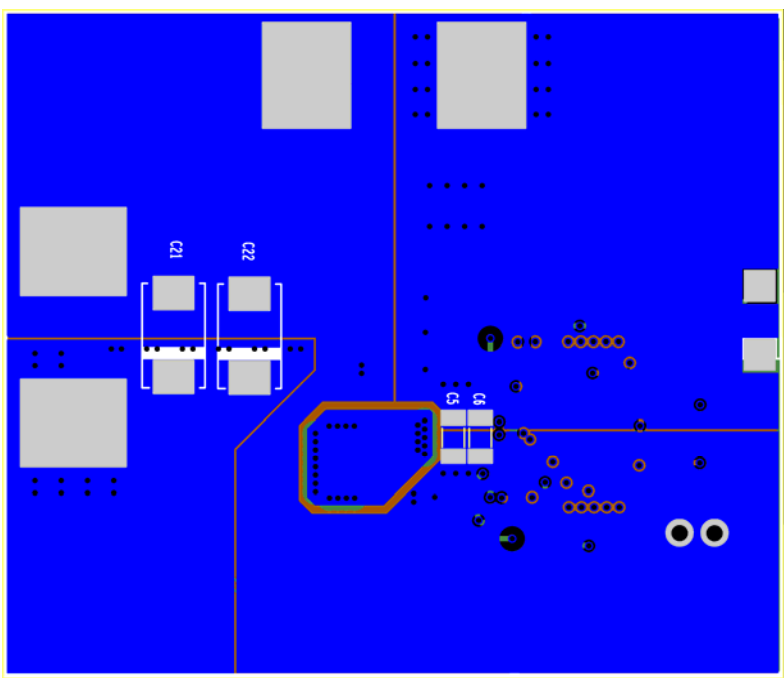


Fig. 3: Board layout, bottom overlay (rear view)

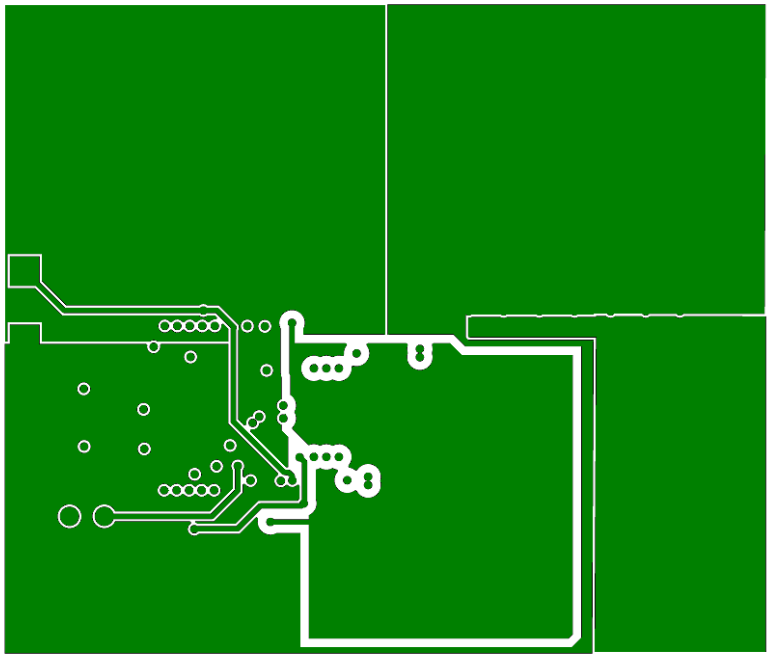


Fig. 4: Board layout, mid-layer I.

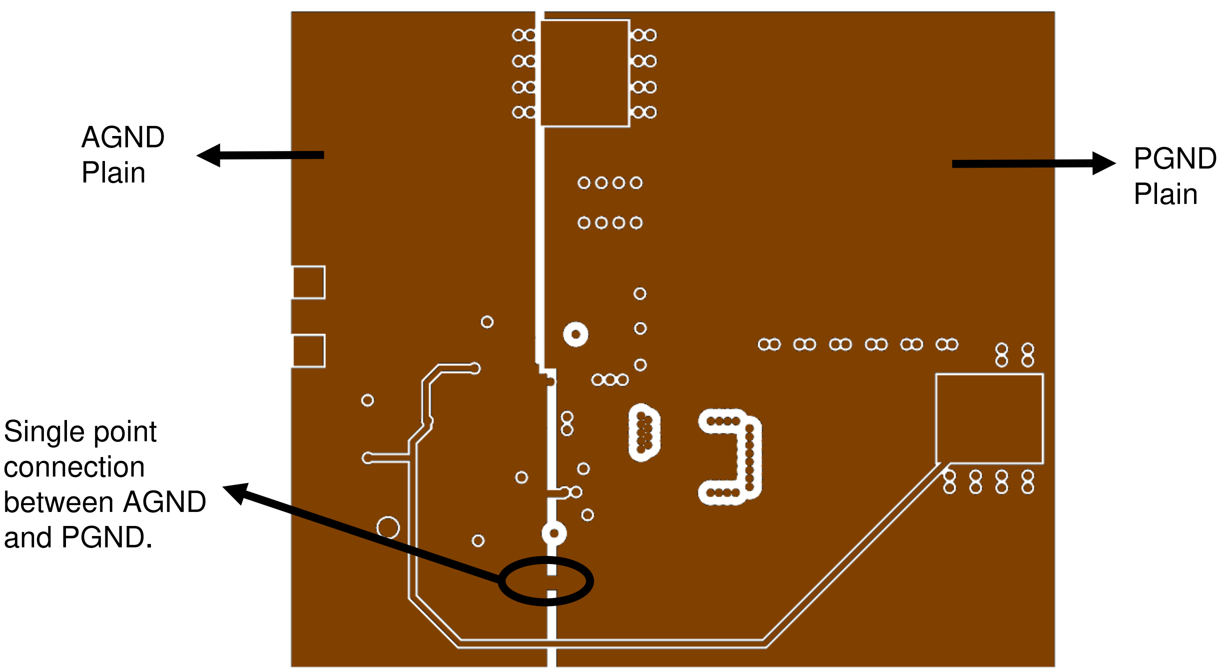
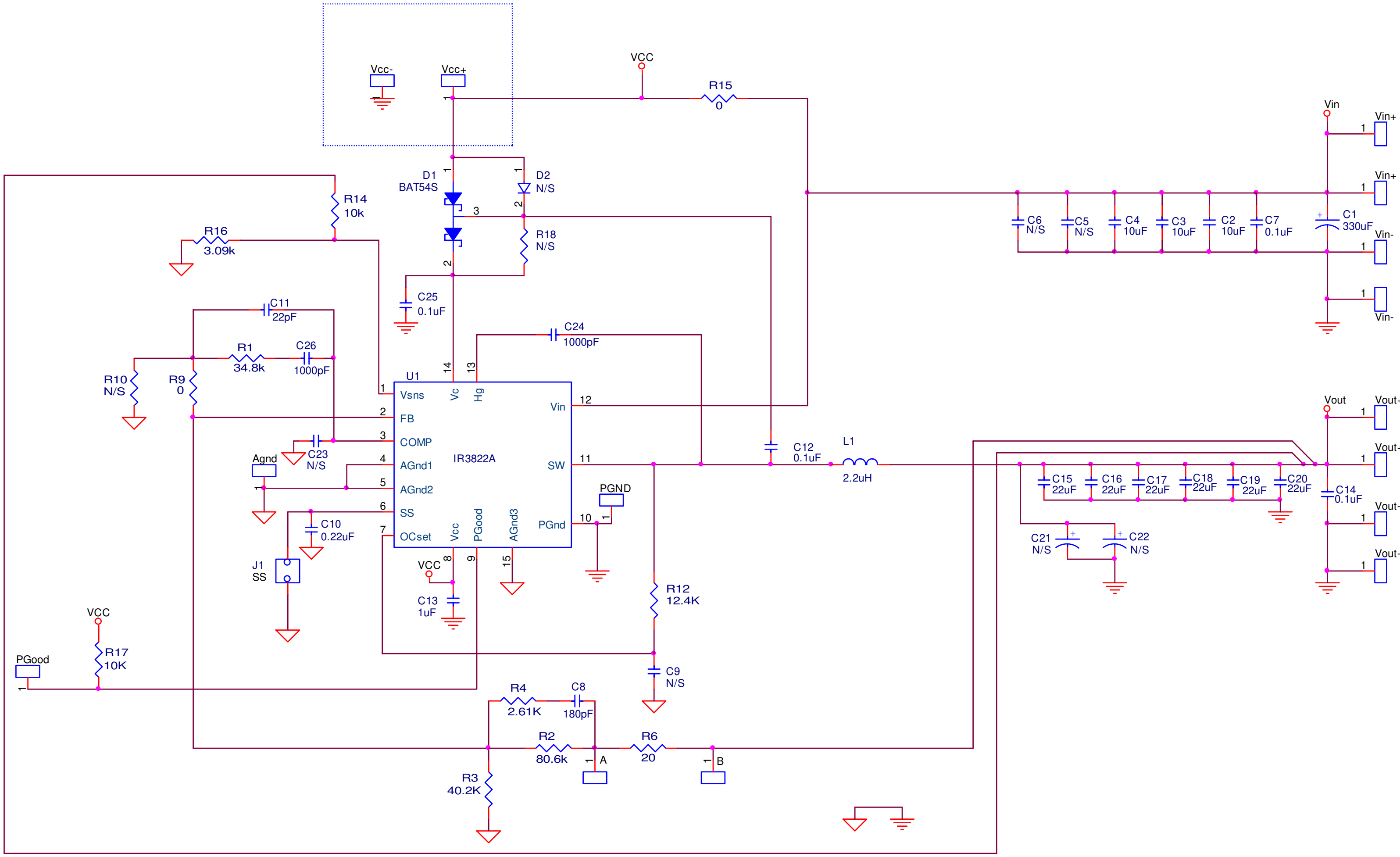


Fig. 5: Board layout, mid-layer II.



Single point of connection between Power Ground and Signal ("analog") Ground

Fig. 6: Schematic of the IR3822A evaluation board

Bill of Materials

Item	Quantity	Designator	Value	Description	Size	Manufacturer	Mfr. Part Number
1	1	C1	330uF	SMD Electrolytic, 25V, 20%	SMD	Panasonic	EEV-FK1E331P
2	3	C2 C3 C4	10uF	Ceramic, 16V, X7R, 10%	1206	Panasonic	ECJ-3YX1C106K
3	4	C7 C12 C14 C25	0.1uF	Ceramic, 50V, X7R, 10%	0603	Panasonic	ECJ-1VB1H104K
4	1	C10	0.22uF	Ceramic, 10V, X5R, 10%	0603	Panasonic	ECJ-1VB1A224K
5	1	C8	180pF	Ceramic, 50V, NPO, 5%	0603	Murata	GRM1885C1H181JA01
6	1	C11	22pF	Ceramic, 50V, NPO, 5%	0603	Murata	GRM1885C1H220JA01
7	1	C13	1uF	Ceramic, 16V, X5R, 10%	0603	Panasonic	ECJ-1VB1C105K
8	6	C15 C16 C17 C18 C19 C20	22uF	Ceramic, 6.3V, X5R, 20%	0805	Panasonic	ECJ-2FB0J226M
9	2	C24, C26	1000pF	Ceramic, 50V, NPO, 5%	0603	Murata	GRM1885C1H102JA01
10	1	D1	BAT54S	Diode Schottky ,40V, 200mA	SOT-23	Fairchild	BAT54S
11	1	L1	2.2uH	SMT Inductor, 4.2mOhm, 20%	11.8x 10.5mm	ACT	STS1205-2R2
12	1	R1	34.8K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW060334K8FKEA
13	1	R3	40.2K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW060340K2FKEA
14	1	R2	80.6K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW060380K6FKEA
15	1	R4	2.61K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW06032K61FKEA
16	1	R6	20	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW060320R0FKEA
17	2	R9 R15	0	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW06030000Z0EA
18	1	R12	12.4K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW060312K4FKEA
19	2	R14, R17	10K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW060310K0FKEA
20	1	R16	3.09K	Thick film, 1/10W, 1%	0603	Vishey/Dale	CRCW06033K09FKEA
21	1	U1	IR3822A	300kHz, 6A, SupIRBuck Module	5x6mm	International Rectifier	IR3822A
22	2	-	-	Banana Jack, Insulated Solder Terminal, Black	-	Johnson Components	105-0853-001
23	1	-	-	Banana Jack- Insulated Solder Terminal, Red	-	Johnson Components	105-0852-001
24	1	-	-	Banana Jack- Insulated Solder Terminal, Green	-	Johnson Components	105-0854-001

TYPICAL OPERATING WAVEFORMS

Vin=Vcc=12.0V, Vo=1.8V, Io=0- 6A, Room Temperature, No Air Flow

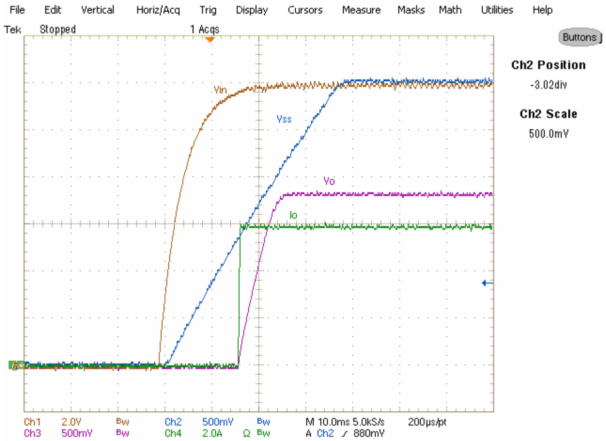


Fig. 7: Start up at 6A Load
Ch_1:V_{in}, Ch_2:V_{SS}, Ch_3:V_{out}, Ch_4:I_{out}

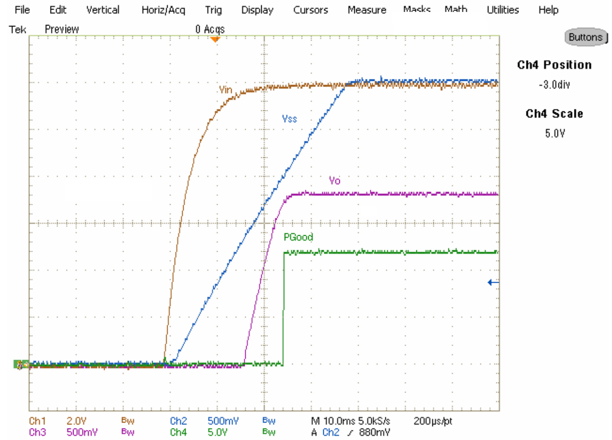


Fig. 8: Start up at 6A Load,
Ch_1:V_{in}, Ch_2:V_{SS}, Ch_3:V_{out}, Ch_4:V_{PGood}

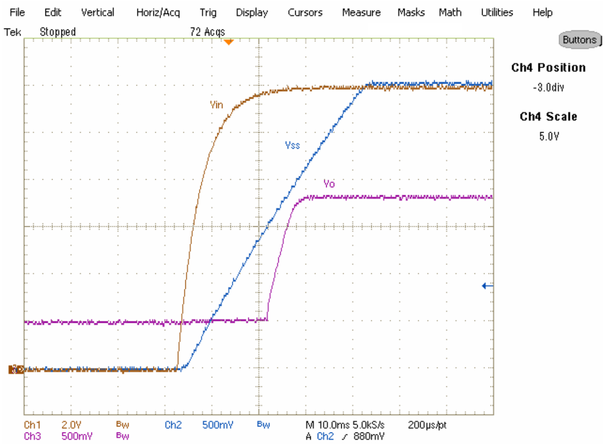


Fig. 9: Start up with 0.5V Pre Bias, 0A
Load, Ch_1:V_{in}, Ch_2:V_{SS}, Ch_3:V_{out}

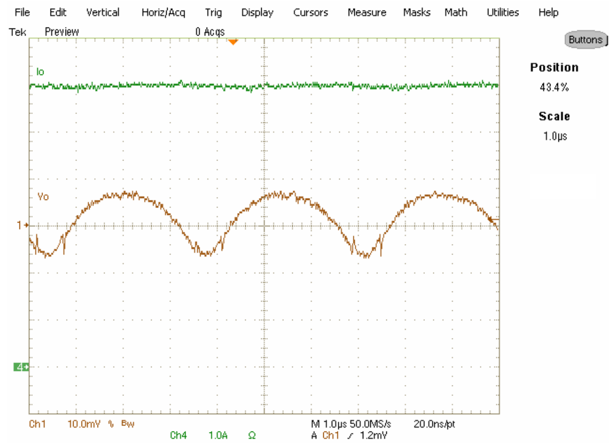


Fig. 10: Output Voltage Ripple, 6A load
Ch_1: V_{out} , Ch_4: I_{out}

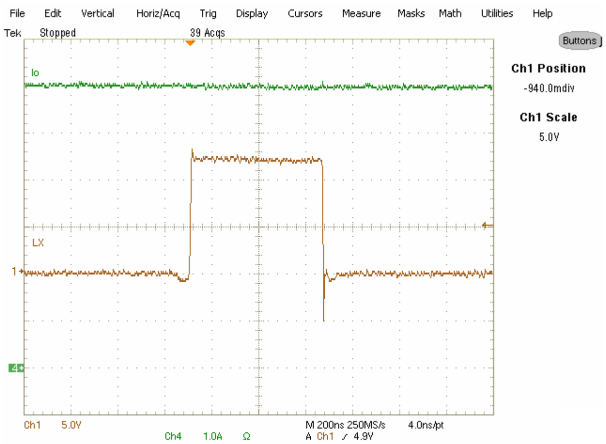


Fig. 11: Inductor node at 6A load
Ch_1:LX, Ch_4:I_{out}

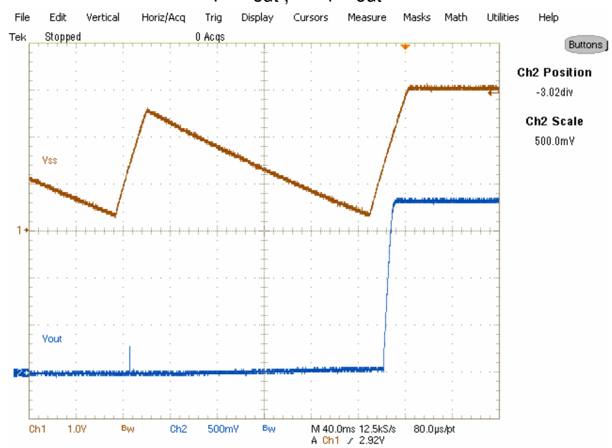


Fig. 12: Short (Hiccup) Recovery
Ch_1:V_{SS} , Ch_2:V_{out}

TYPICAL OPERATING WAVEFORMS

Vin=Vcc=12V, Vo=1.8V, Io=3A- 6A, Room Temperature, No Air Flow

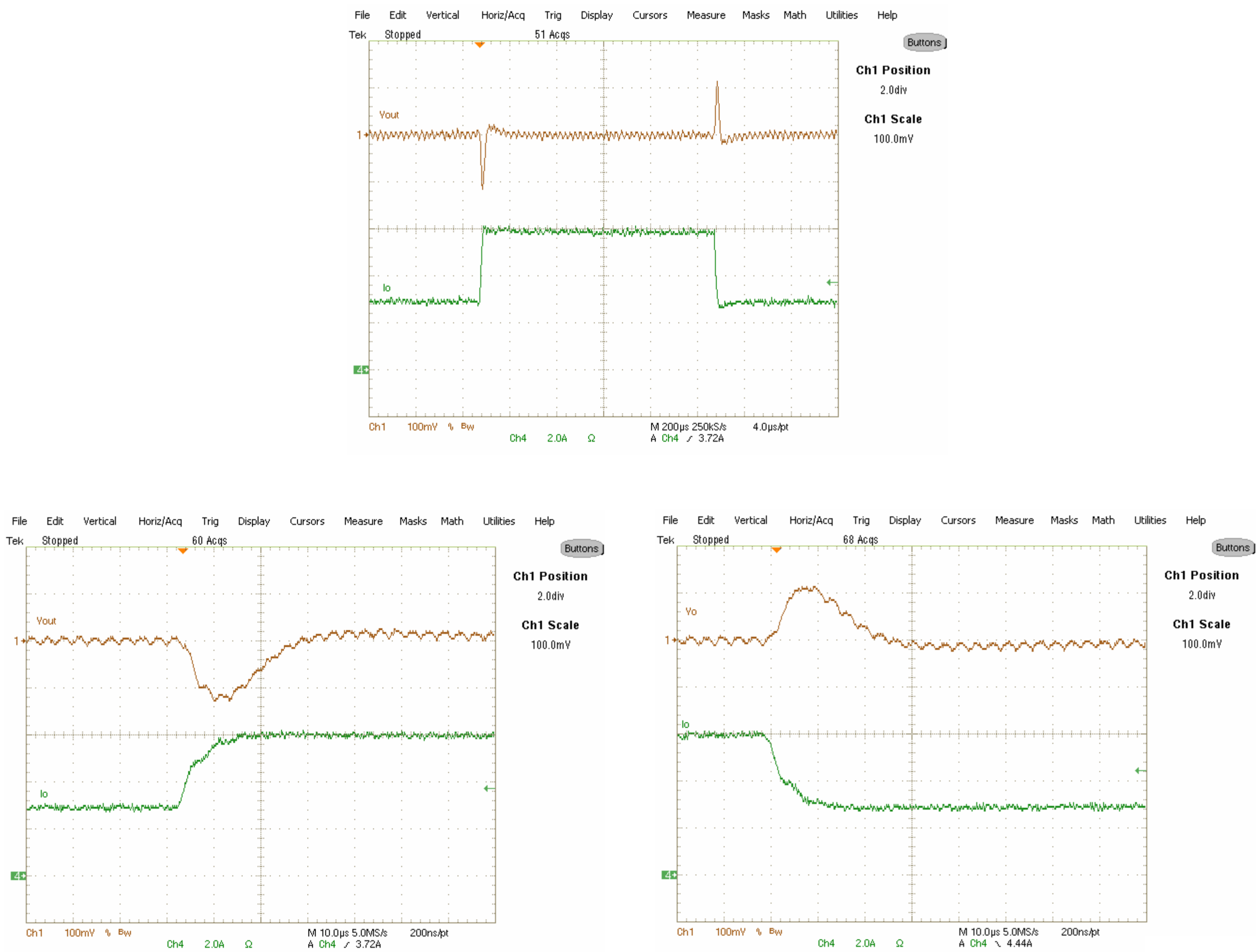


Fig. 13: Transient Response, 3A to 6A step

Ch_1:V_{out}, Ch_4:I_{out}

TYPICAL OPERATING WAVEFORMS
Vin=Vcc=12V, Vo=1.8V, Io=6A, Room Temperature, No Air Flow

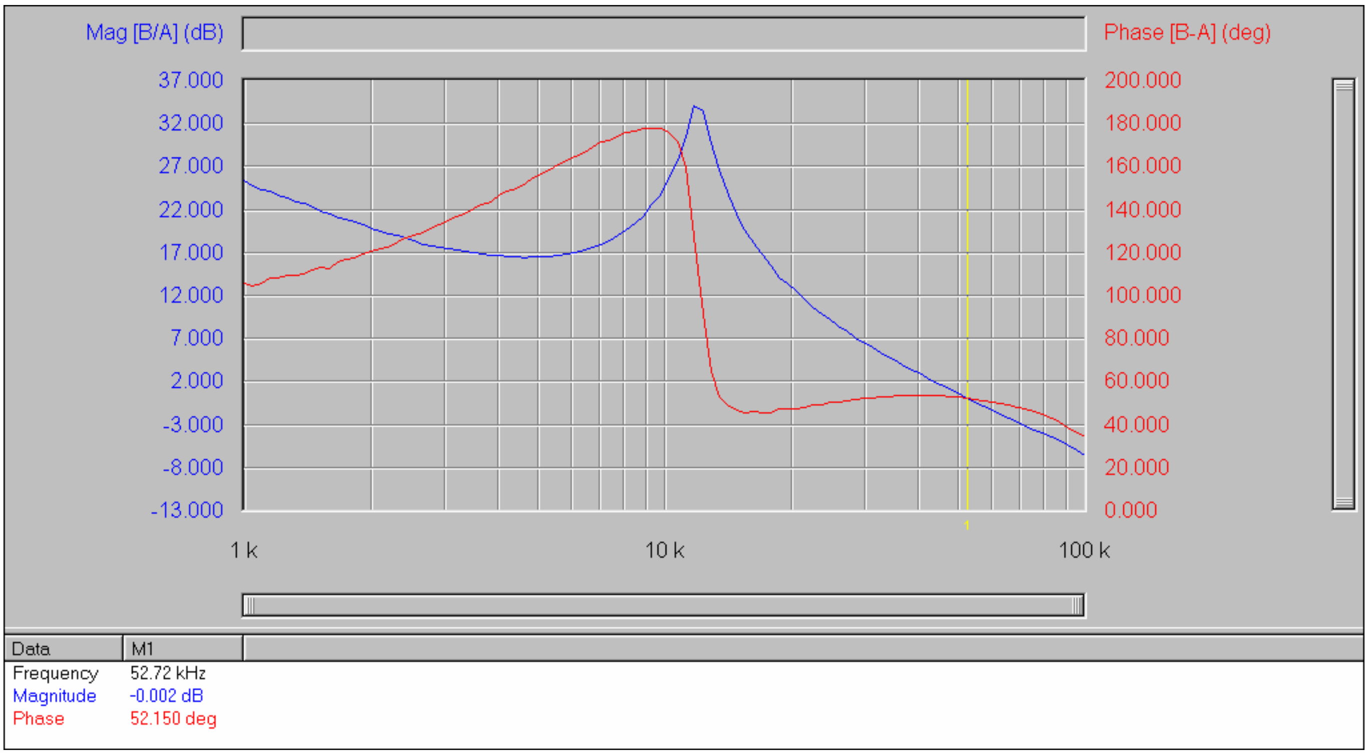


Fig. 14: Bode Plot at 6A load shows a bandwidth of 52.7kHz and phase margin of 52 degrees

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vo=1.8V, Io=0- 6A, Room Temperature, No Air Flow

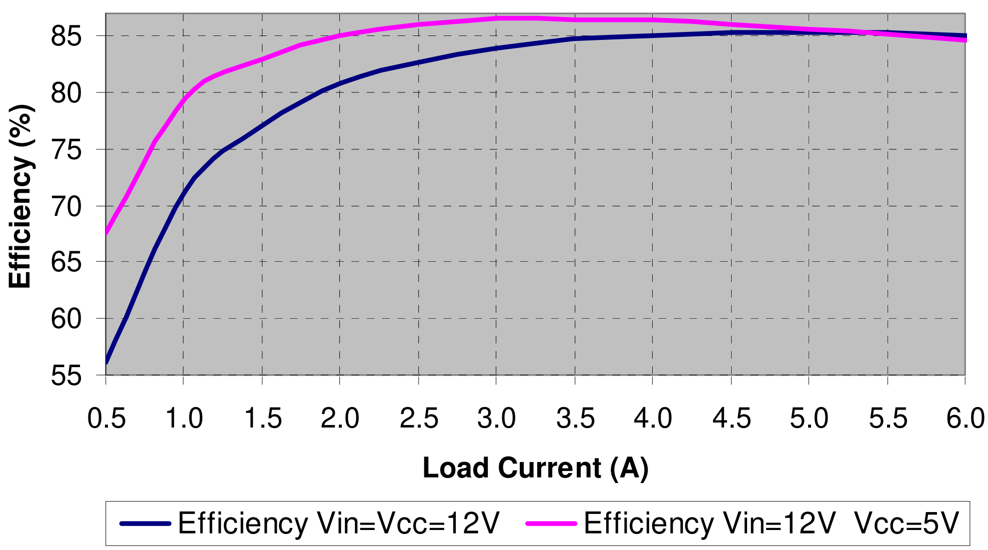


Fig.15: Efficiency versus load current

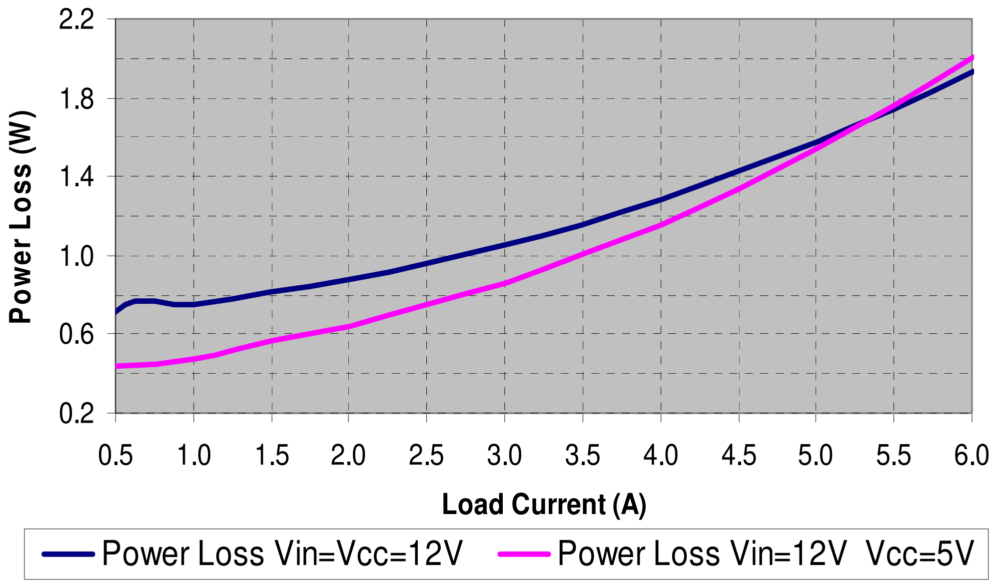


Fig.16: Power loss versus load current

THERMAL IMAGES
Vin=12V, Vo=1.8V, Io=6A, Room Temperature, No Air Flow

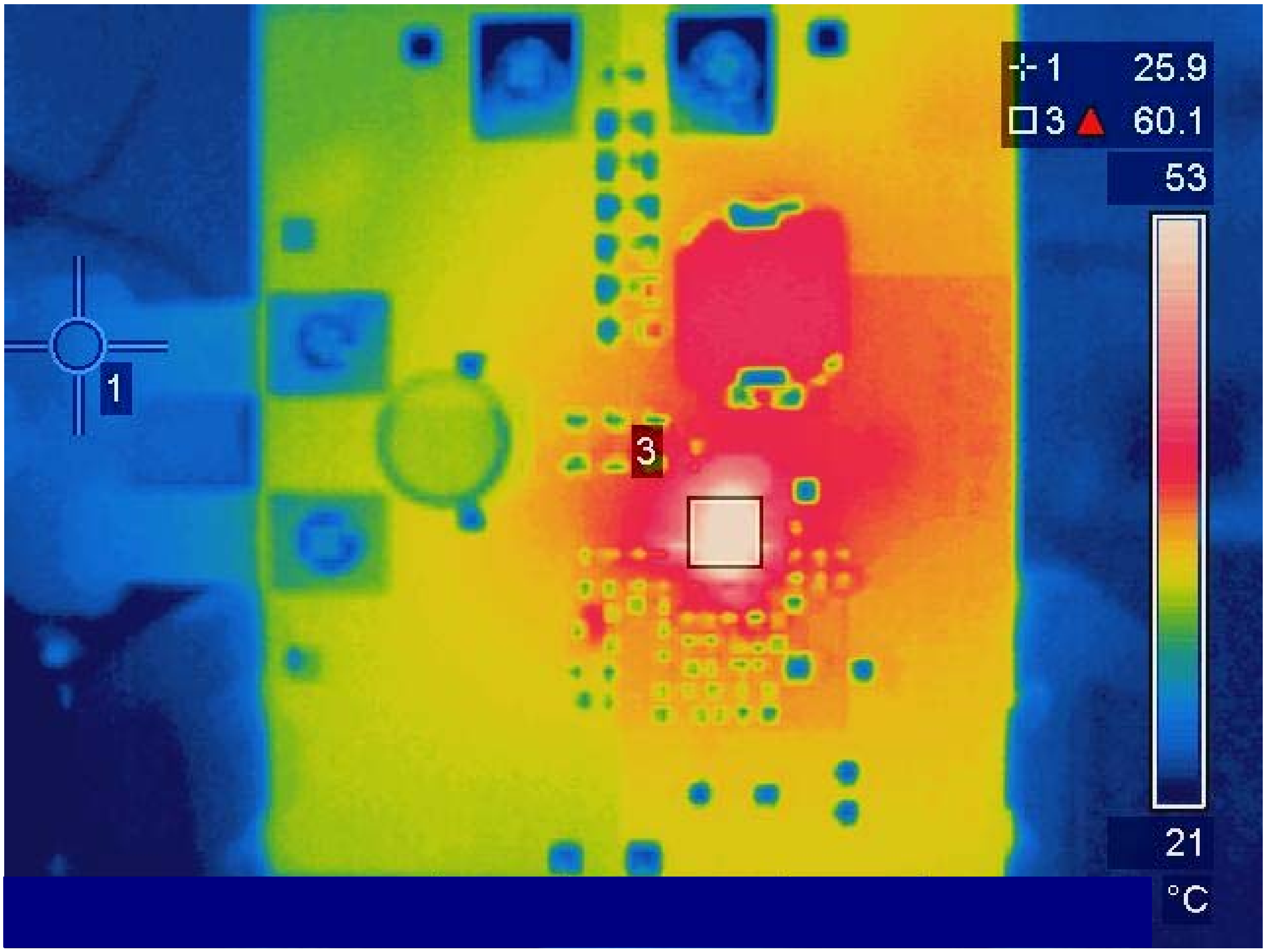


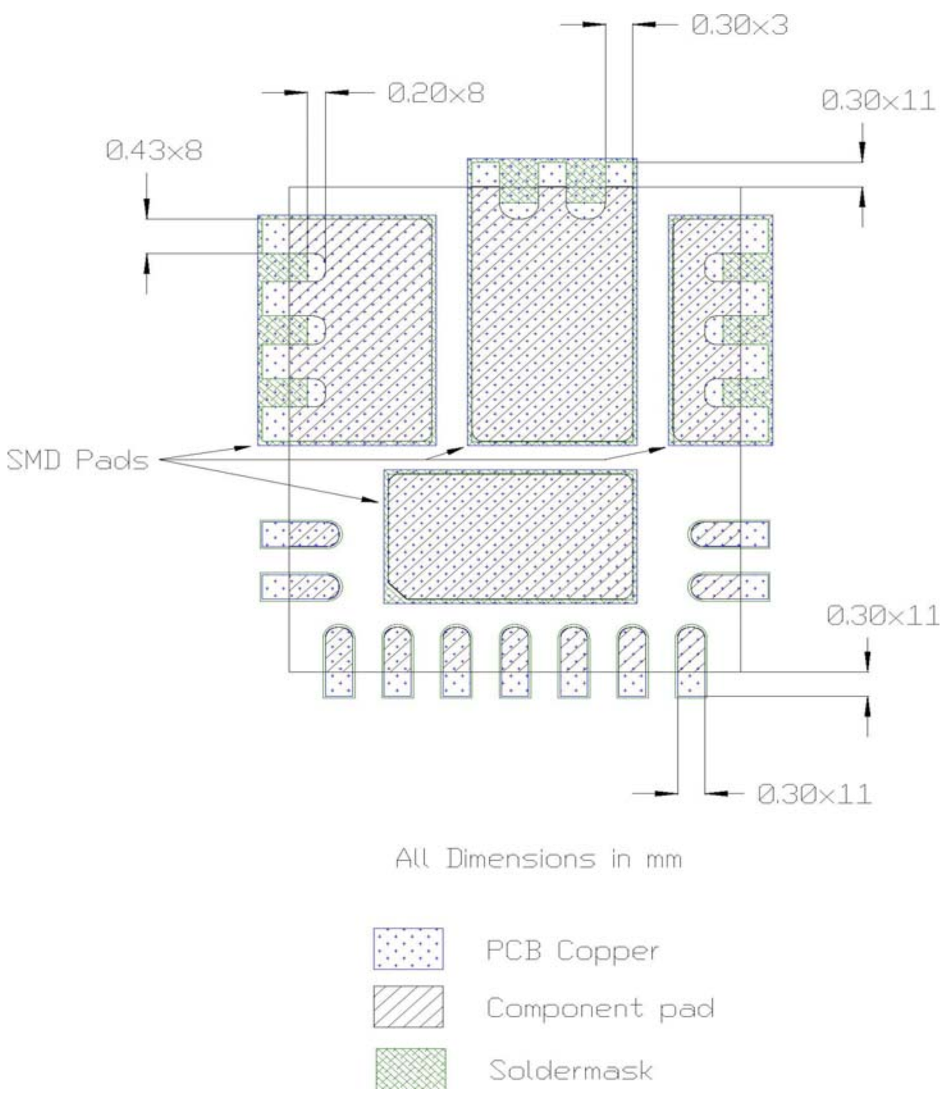
Fig. 17: Thermal Image at 6A load
Test point 3 is IR3822A

PCB Metal and Components Placement

The lead lands (the 11 IC pins) width should be equal to the nominal part lead width. The minimum lead to lead spacing should be ⩾ 0.2mm to minimize shorting.

Lead land length should be equal to the maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

The pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.

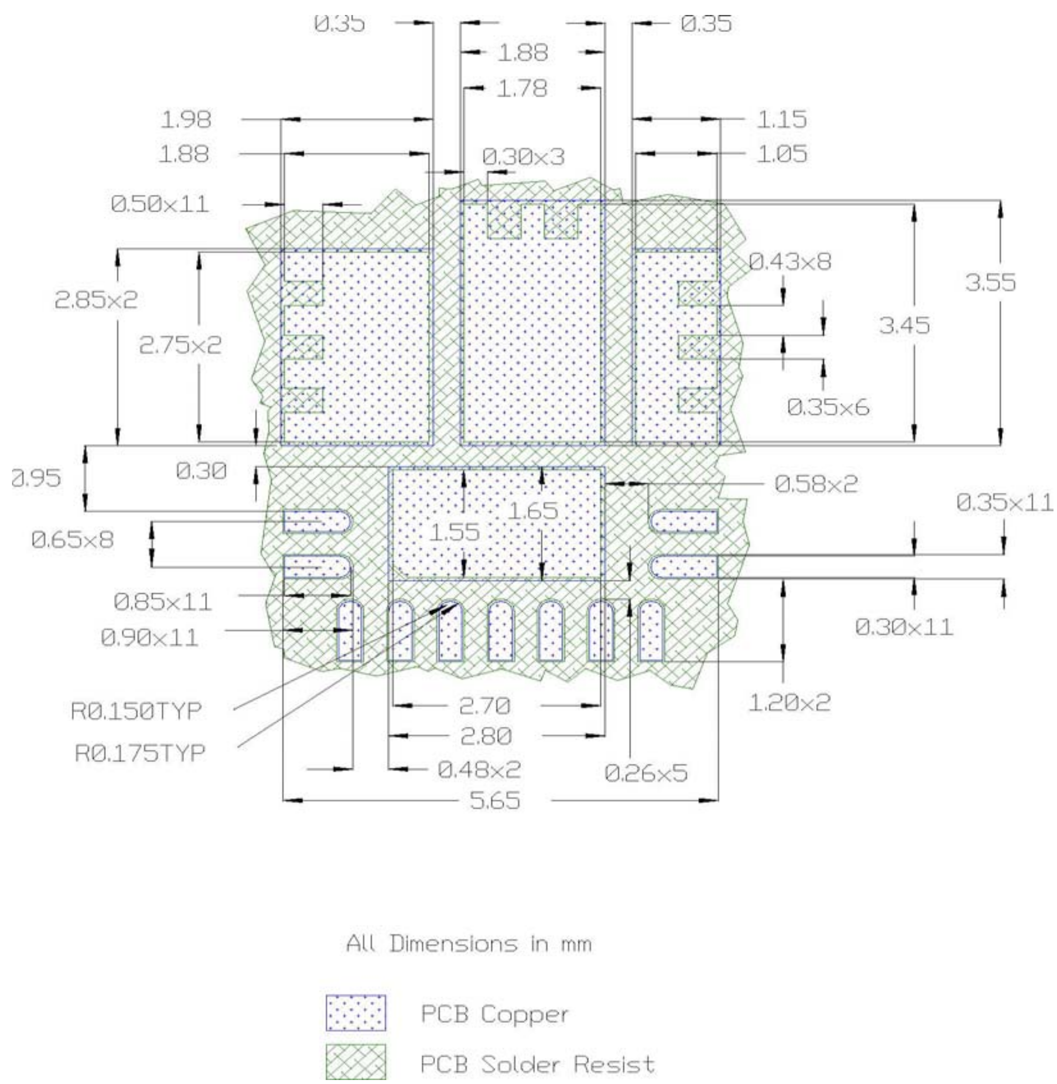


Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

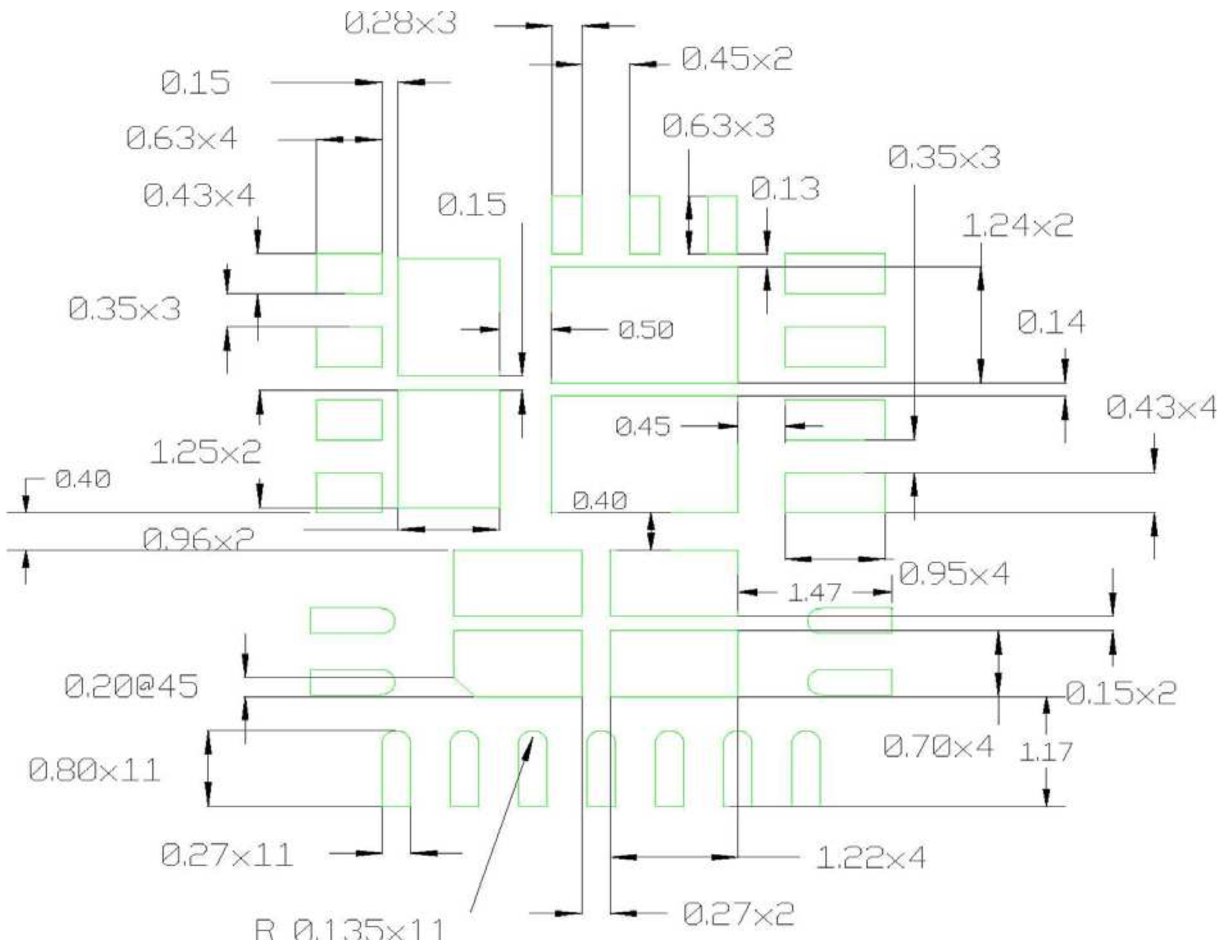
The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in between the lead lands and the pad land is ⩾ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

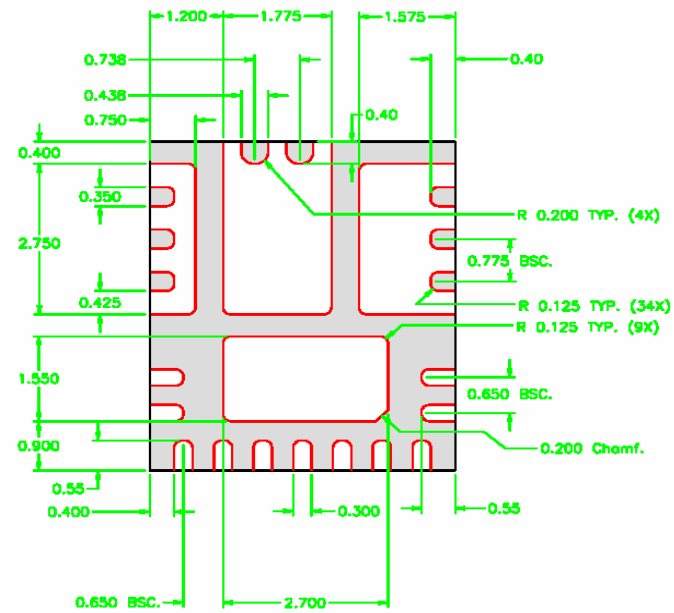


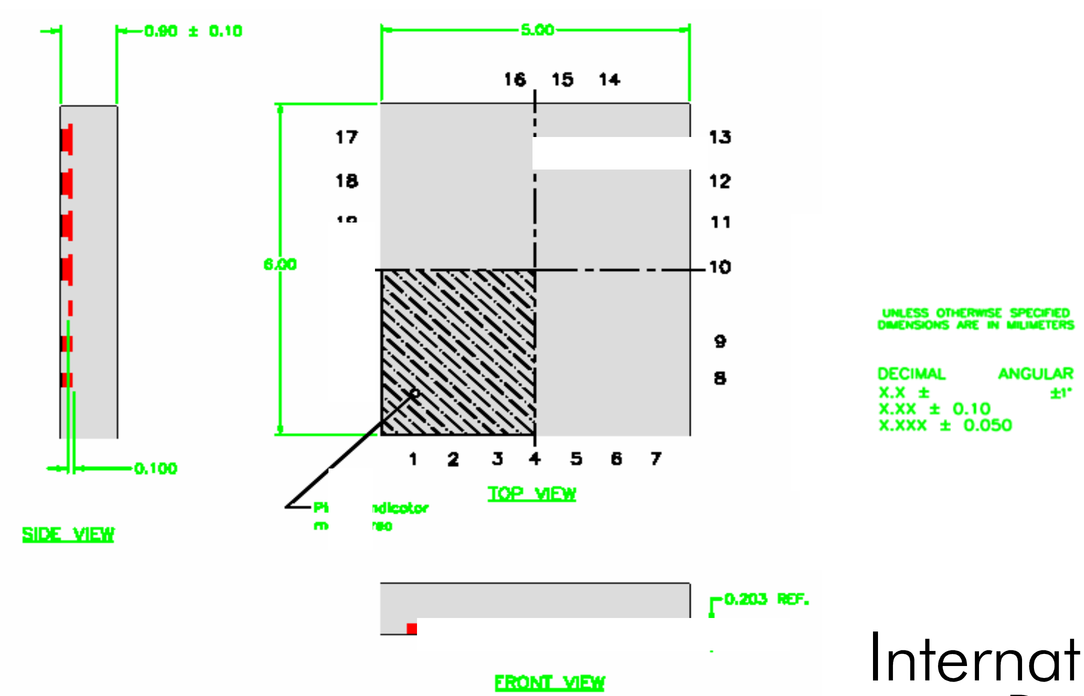
Stencil Design

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm





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