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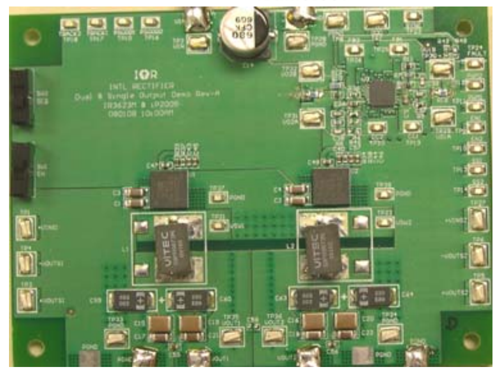
REFERENCE DESIGN IRDCiP2005C-2

International Rectifier • 233 Kansas Street, El Segundo, CA 90245 USA

IRDCiP2005C-2: 500kHz, 30A, Dual Output, 180° Out of Phase Synchronous Buck Converter Featuring iP2005C and IR3623M



Overview

This reference design is capable of delivering a continuous current of 30A per channel without heatsink at an ambient temperature of 45ºC and airflow of 200LFM. Fig. 4 - Fig. 25 provide performance graphs, thermal images, and waveforms. Fig. 1 - Fig. 3 are provided to engineers as design references for implementing an IR3623+iP2005C solution.

The components installed on this demoboard were selected based on operation at an input voltage of 12V (+/-10%), a switching frequency of 500kHz (+/-15%), and an output voltage of 1.5V at channel-1 and 2.5V at channel-2. Major changes from these set points may require optimizing the control loop and/or adjusting the values of input/output filters in order to meet the user's specific application requirements. Refer to iP2005C and IR3623 datasheets for more information.

IRDCiP2005C-2 Recommended Operating Conditions

(refer to the iP2005C datasheet for maximum operating conditions)

Input voltage:	8.5V – 14.5V
Output voltage:	0.8 – 5V
Switching Freq:	500kHz
Output current:	This reference design is capable of delivering a continuous current of 30A per channel without heatsink at an ambient temperature of 45ºC and airflow of 200LFM.

Demoboard Quick Start Guide

Initial Settings:

VOUT1 is set to 1.5V, but can be adjusted from 0.8V to 5V by changing the values of R11 and R15 according to the following formula:

$$R11 = R15 = (10k * 0.8) / (VOUT1 - 0.8)$$

VOUT2 is set to 2.5V, but can be adjusted from 0.8V to 5V by changing the values of R12 and R16 according to the following formula:

$$R12 = R16 = (10k * 0.8) / (VOUT2 - 0.8)$$

The switching frequency is set to 500kHz, but can be adjusted by changing the value of R26. See Fig. 4 for the relationship between R26 and the switching frequency.

Power Up Procedure:

1. Apply input voltage across VIN and PGND.
2. If R45 is not installed, apply bias voltage across VDD and PGND.
3. Apply load across VOUT pads and PGND pads.
4. Toggle the SEQ (SW1) and EN (SW2) switches to the ON position.
5. Adjust load to desired level. See recommendations above.

Demoboard Schematic

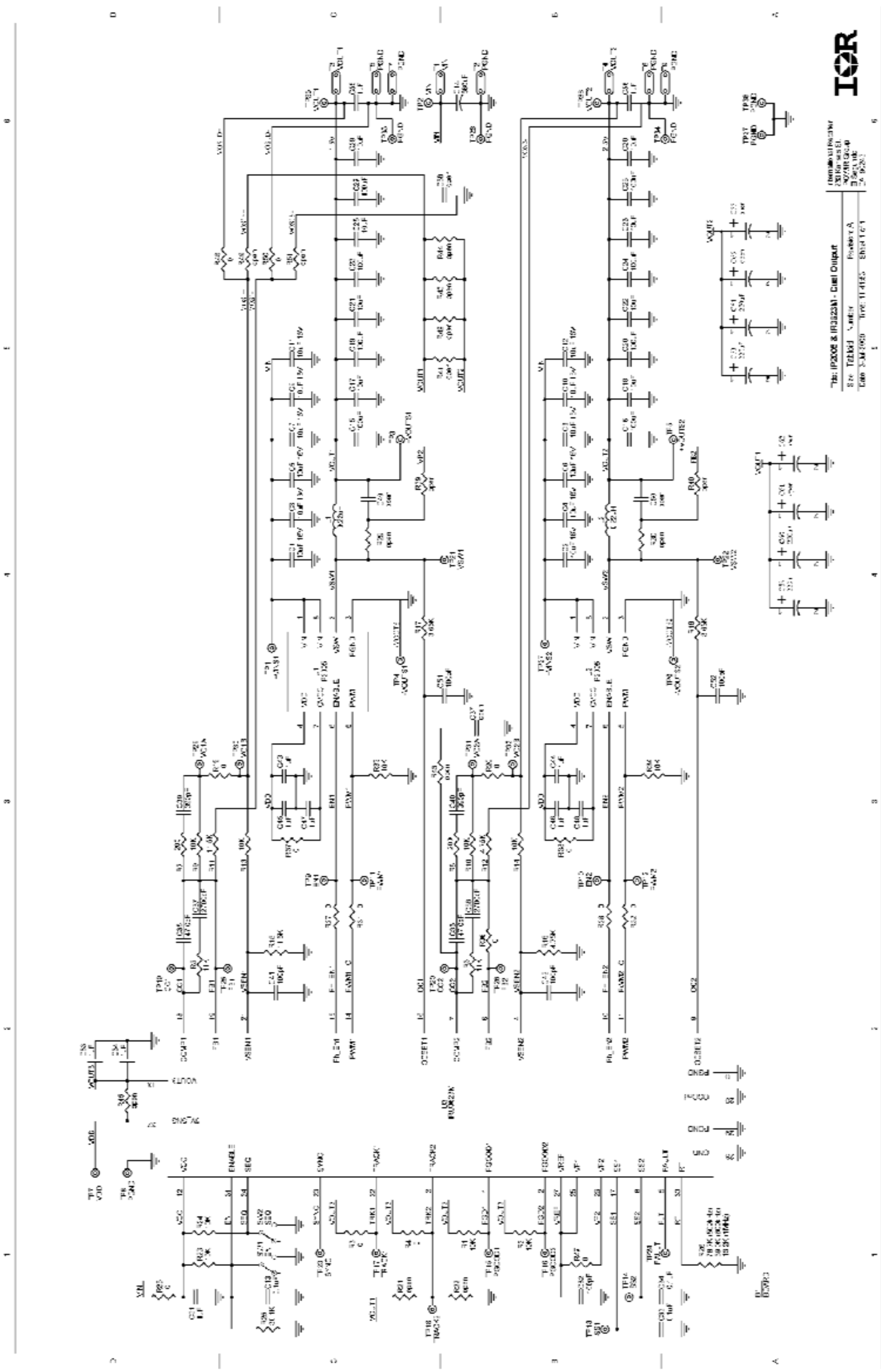


Fig. 1 Schematic

Bill of Material

Quantity	Designator	Type 1	Type 2	Value 1	Value 2	Tolerance	Package	Manufac 1	Manufac 1No
20	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C17, C18, C21, C22, C25, C26, C29, C30	capacitor	X7R	10.0uF	16V	10%	1206	TDK	C3216X7R1C106KT
3	C13, C33, C34	capacitor	X7R	0.100uF	50V	10%	0603	TDK	C1608X7R1H104K
1	C14	capacitor	electrolytic	680uF	16V	20%	SMD	Panasonic	EEV-FK1C681GP
8	C15, C16, C19, C20, C23, C24, C27, C28	capacitor	X5R	100uF	6.3V	20%	1210	TDK	C3225X5R0J107M
11	C31, C43, C44, C45, C46, C47, C48, C53, C54, C55, C56	capacitor	X7R	1.00uF	16V	10%	0603	TDK	C1608X7R1C105KT
5	C32, C41, C42, C51, C52	capacitor	NPO	100pF	50V	5%	0603	Phycomp	0603CG101J9B20
2	C35, C36	capacitor	NPO	47.0pF	50V	5%	0603	KOA	NPO0603HTTD470J
2	C37, C38	capacitor	X7R	2700pF	50V	10%	0603	KOA	X7R0603HTTD272K
2	C39, C40	capacitor	NPO	390pF	50V	5%	0603	KOA	NPO0603HTTD391J
4	C59, C60, C63, C64	capacitor	tantalum polymer	220uF	2.5V	20%	7343	Sanyo	2R5TPC220M
2	L1, L2	inductor	ferrite	0.22uH	47A	10%	SMT	Vitec	59PR9873N
10	R1, R2, R9, R10, R13, R14, R23, R24, R33, R34	resistor	thick film	10.0K	1/10W	1%	0603	KOA	RK73H1J1002F
2	R11, R15	resistor	thick film	11.5K	1/10W	1%	0603	KOA	RK73H1JLTD1152F
2	R12, R16	resistor	thick film	4.75K	1/10W	1%	0603	KOA	RK73H1JLTD4751F
2	R17, R18	resistor	thick film	3.65K	1/10W	1%	0603	KOA	RK73H1JLTD3651F
2	R19, R20	resistor	thick film	0	1/8W	<50m	0805	ROHM	MCR10EZHJ000
1	R25	resistor	thick film	30.1K	1/10W	1%	0603	KOA	RK73H1J3012F
1	R26	resistor	thick film	78.7K	1/10W	1%	0603	KOA	RK73H1JLTD7872F
12	R3, R4, R27, R28, R31, R32, R36, R37, R38, R47, R48, R50	resistor	thick film	0	1/10W	1%	0603	KOA	RK73Z1JLTD
1	R35	resistor	thick film	0	1/8W	<50m	1206	Panasonic	ERJ-8GEY0R00
2	R5, R6	resistor	thick film	11.0K	1/10W	1%	0603	KOA	RK73H1JLTD1102F
2	R7, R8	resistor	thick film	200	1/10W	1%	0603	KOA	RK73H1J2000F
2	SW1, SW2	switch	slide	SPDT	30VDC	0.2A	pcb mount	E-Switch	EG1218
18	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36	hardware	test point	90 mils	112 x 150 mils	-	5016	Keystone	5016
20	TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP37, TP38	hardware	test point	60 mils	40 x 105 mils	-	5015	Keystone	5015
2	U1, U2	iP2005	LGA unit	rev e	-	-	7.65mm x 7.65mm	IRF	rev e
1	U3	IC analog	PWM controller	-0.5 - 16V	-0.5 - 16V	-40 - 120°C	MLPQ-32L	IRF	IR3623M

Demoboard Component Placement

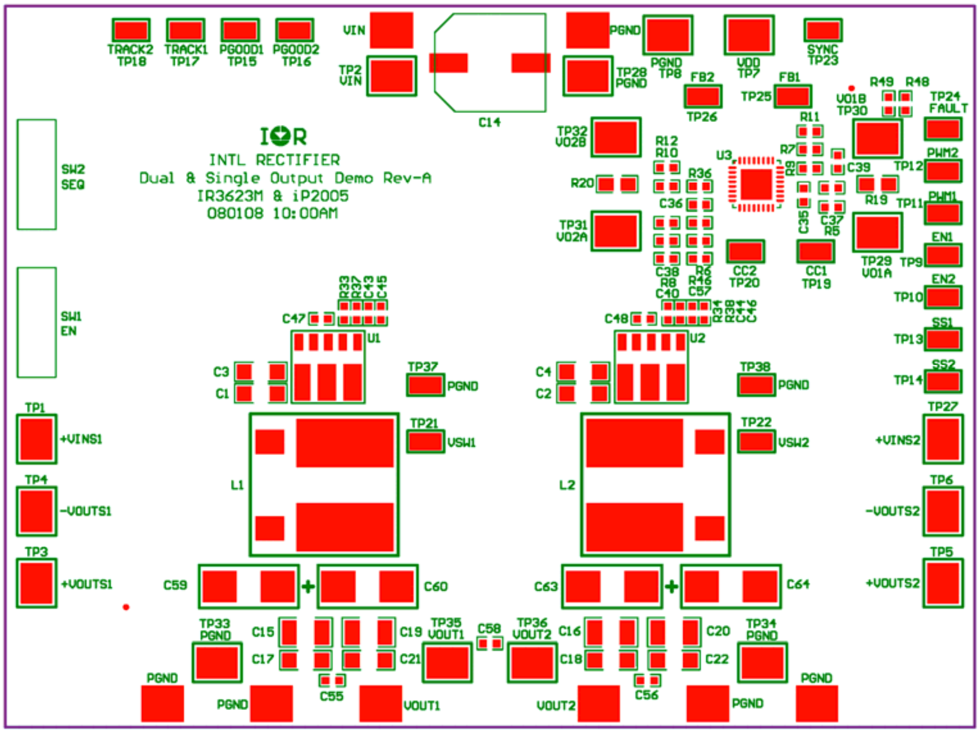


Fig. 2 Top Layer (Face View)

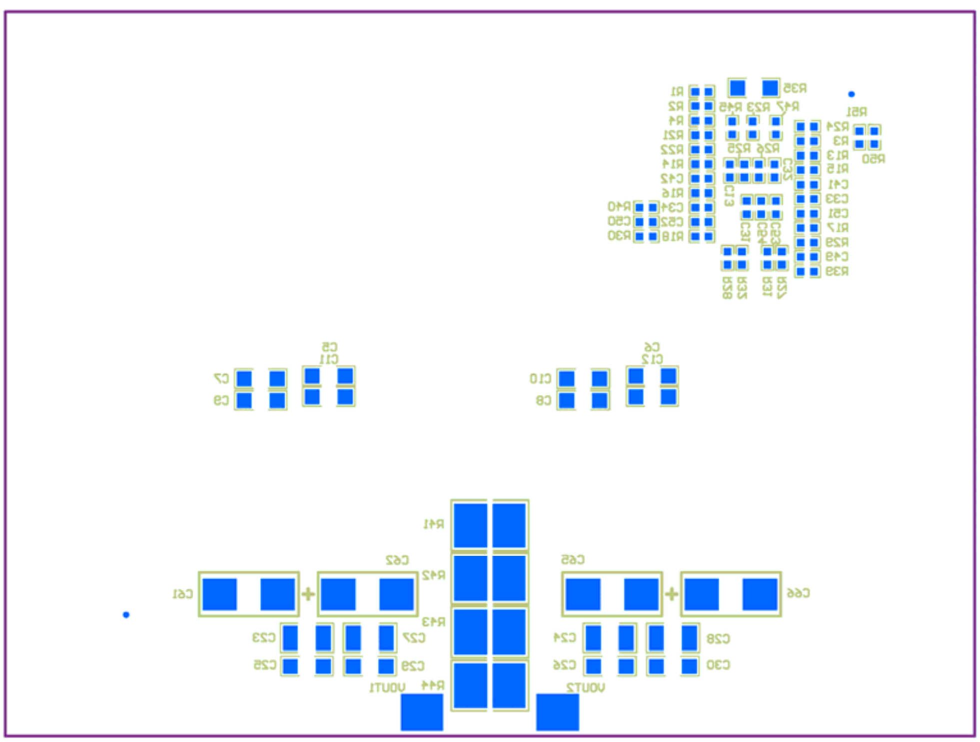


Fig. 3 Bottom Layer (Through View)

Description of Test Points and Connectors

1. Jumpers

Jumper	Pin Name	Description
SW1	EN	Board Enable (switch Up=Off, Down=On) - Vin pin on top
SW2	SEQ	Sequence (switch Up=Off, Down=On) - Vin pin on top

2. Test Points/Connectors

Test Point	Pin Name	Description
T1 / T2	VIN / PGND	Vin supply voltage
TP2 / TP28	VIN / PGND	Vin supply voltage sense
T3 / T5 / T7	VOUT1 / PGND / PGND	Channel 1 Output, connect to DC load
TP35 / TP33	VOUT1 / PGND	Channel 1 Output sense
TP21 / TP37	VSW1 / PGND	Channel 1 switch node / PGND test points
TP9	EN1	Channel 1 Enable test point
TP11	PWM1	Channel 1 PWM test point
TP19	CC1	Channel 1 error amplifier output
TP25	FB1	Channel 1 error amplifier non-inverting input
T4 / T6 / T9	VOUT2 / PGND / PGND	Channel 2 Output, connect to DC load
TP36 / TP34	VOUT2 / PGND	Channel 2 Output sense
TP22 / TP38	VSW2 / PGND	Channel 2 switch node / PGND test points
TP10	EN2	Channel 2 Enable test point
TP12	PWM2	Channel 2 PWM test point
TP20	CC2	Channel 2 error amplifier output
TP26	FB2	Channel 2 error amplifier non-inverting input
TP7 / TP8	VDD / PGND	iP2005C internal bias voltage test points
TP23	SYNC	External frequency synchronization input
TP17	TRACK1	Channel 1 tracking input, pull-up to Vout3 if not used
TP18	TRACK2	Track2 test point
TP15	PGOOD1	Channel 1 Power good test point
TP16	PGOOD2	Channel 2 Power good test point
TP13	SS1	Channel 1 Soft start test point
TP14	SS2	Channel 2 Soft start test point
TP24	FAULT	Fault monitor test point

3. Test points for Efficiency Measurement

Test Point	Pin Name	Description
TP1 / TP4	+VINS1 / -VOUTS1	Channel 1 Vin sense for efficiency measurement
TP3 / TP4	+VOUTS1 / -VOUTS1	Channel 1 Output sense for efficiency measurement
TP27 / TP6	+VINS2 / -VOUTS2	Channel 2 Vin sense for efficiency measurement
TP5 / TP6	+VOUTS2 / -VOUTS2	Channel 2 Output sense for efficiency measurement

Test Results

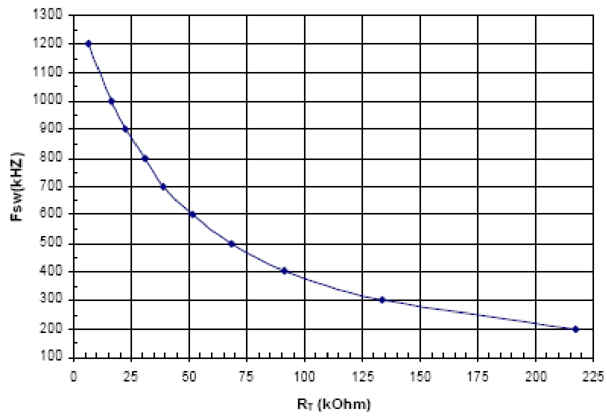


Fig. 4 Relationship Between Switching Frequency and R26

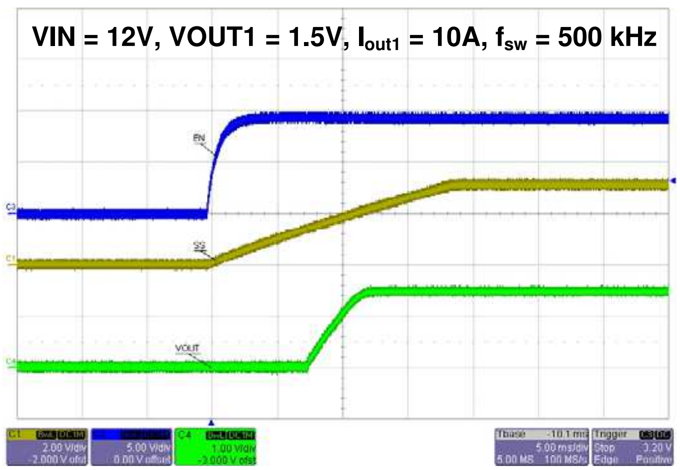


Fig. 5 Channel-1 Power Up Sequence (C3: EN, C1: SS1, C4: VOUT1)

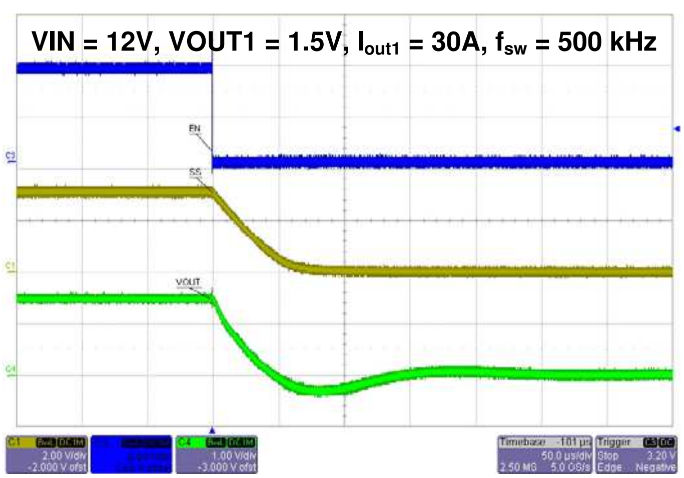


Fig. 6 Channel-1 Power Down Sequence (C3: EN, C1: SS1, C4: VOUT1)

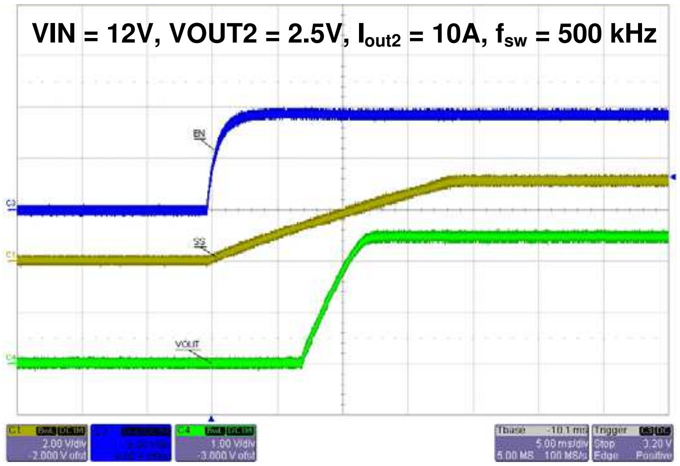


Fig. 7 Channel-2 Power Up Sequence (C3: EN, C1: SS2, C4: VOUT2)

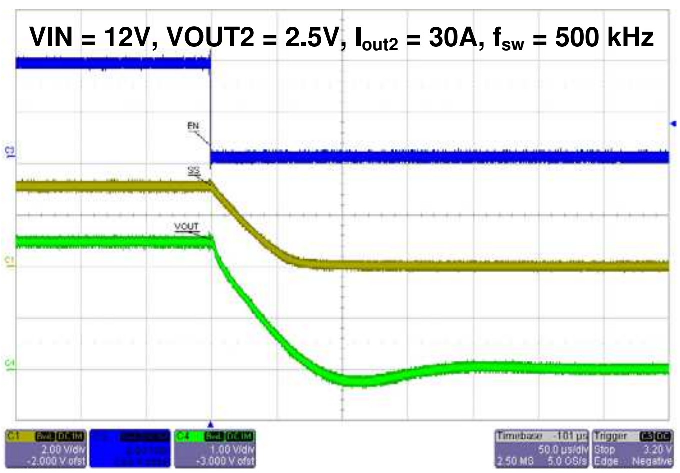


Fig. 8 Channel-2 Power Down Sequence (C3: EN, C1: SS2, C4: VOUT2)

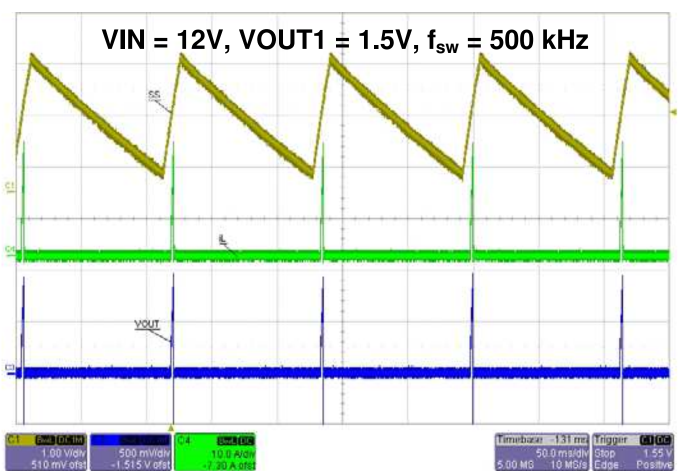


Fig. 9 Hiccup Mode Over Current Protection (C1: SS1, C4: I_{out1}, C3: VOUT1)

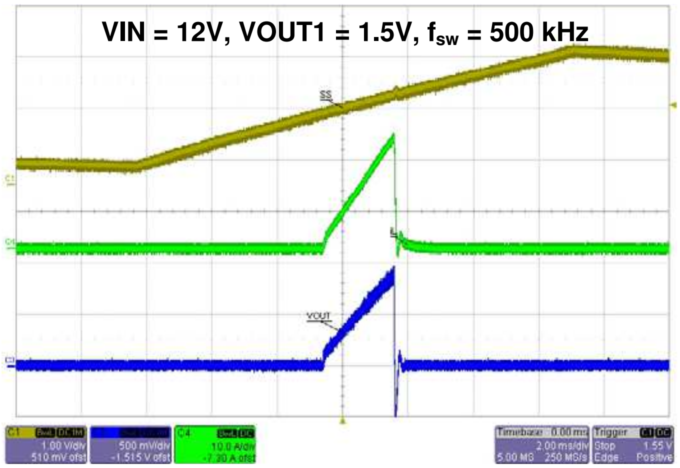


Fig. 10 Hiccup Mode Over Current Protection (C1: SS1, C4: I_{out1}, C3: VOUT1)

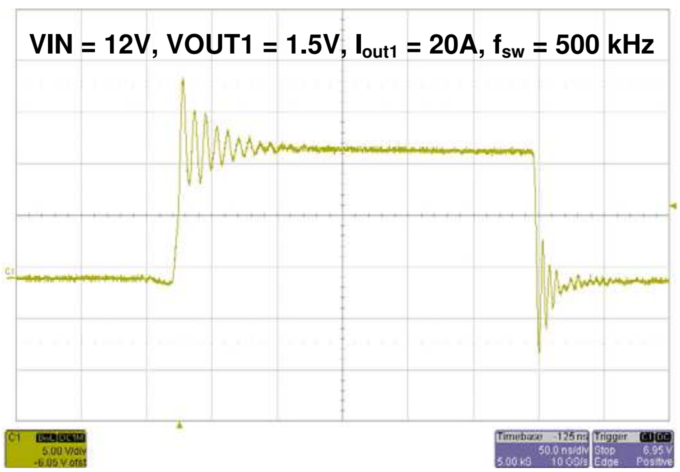


Fig. 11 Deadtime and Ringing at Switch Node

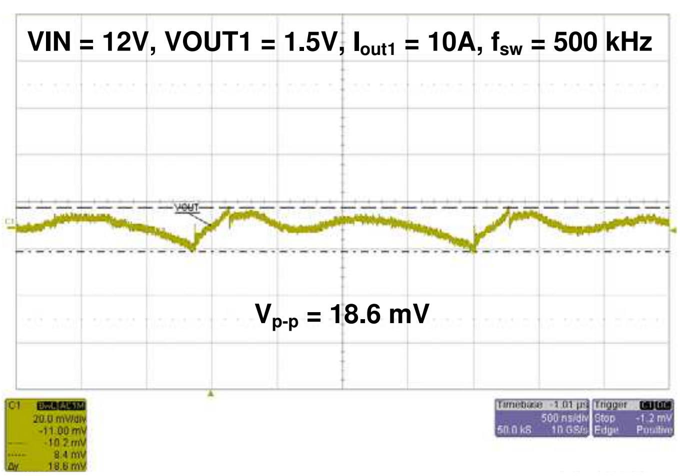


Fig. 12 Channel-1 Output Voltage DC Ripple

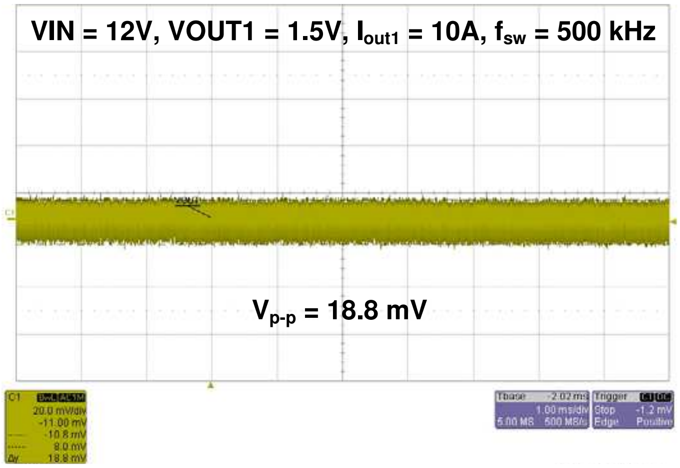


Fig. 13 Channel-1 Output Voltage DC Ripple

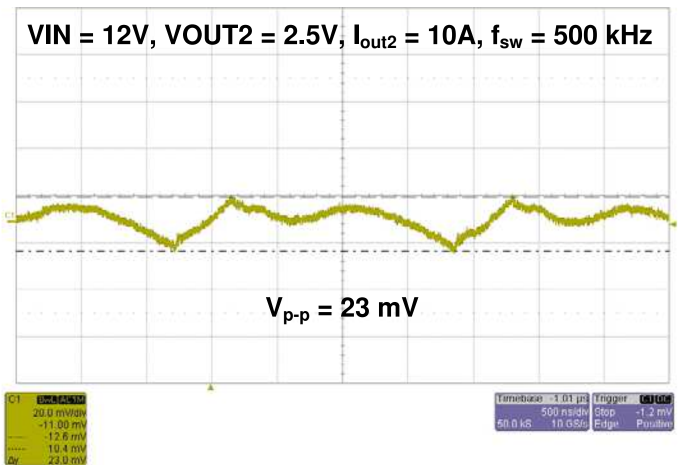


Fig. 14 Channel-2 Output Voltage DC Ripple

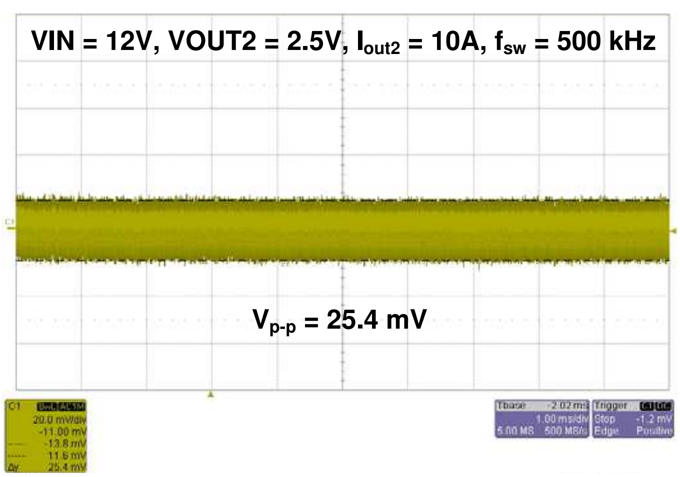


Fig. 15 Channel-2 Output Voltage DC Ripple

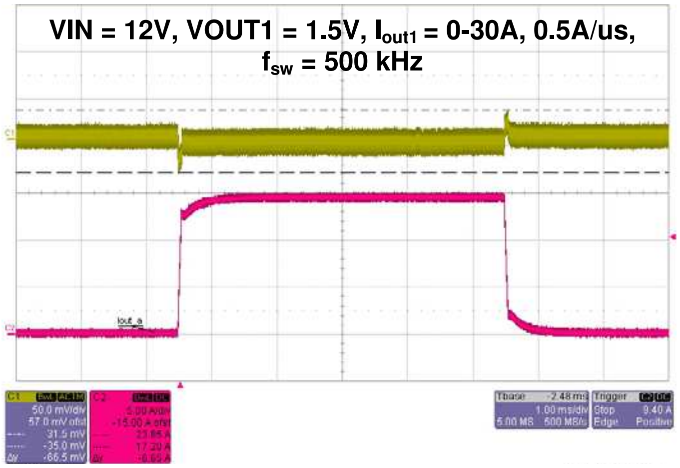


Fig. 16 Load Transient Response (C1: VOUT1 – AC, C2: I_{out1} divided by 2)

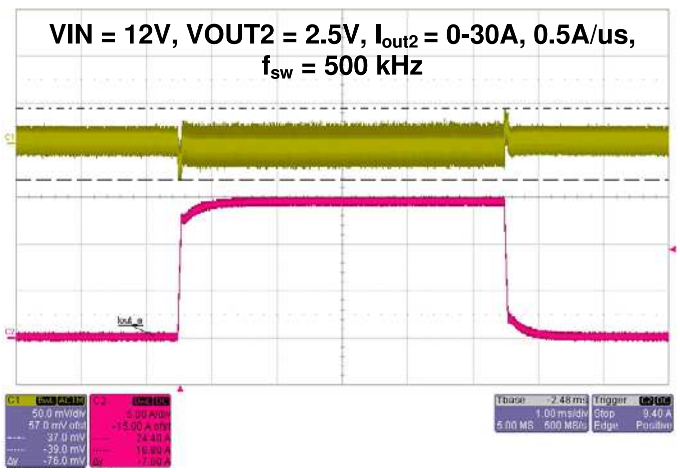


Fig. 17 Load Transient Response (C1: VOUT2 – AC, C2: I_{out2} divided by 2)

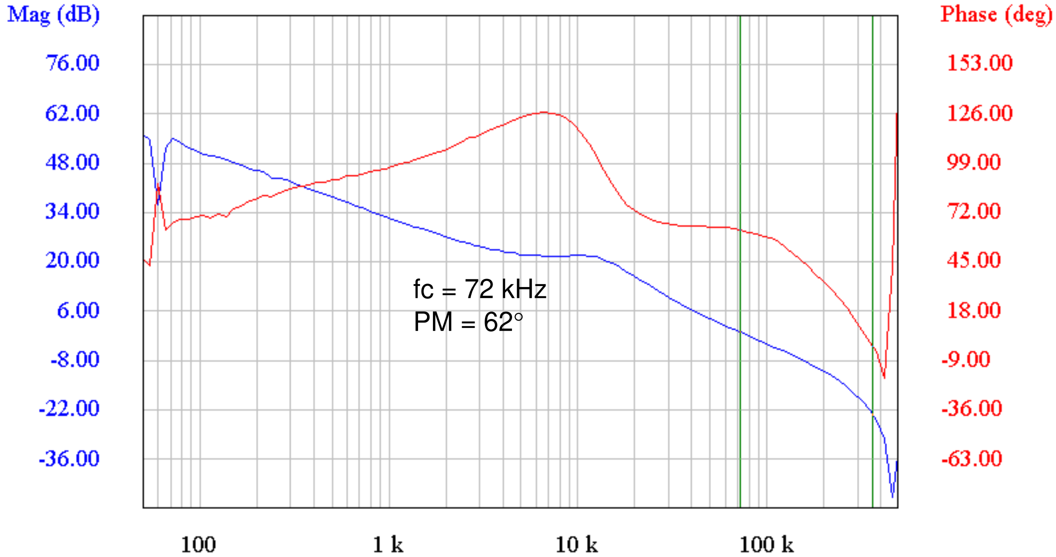


Fig. 18 Bode Plot (VIN = 12V, VOUT1 = 1.5V, I_{out1} = 20A)

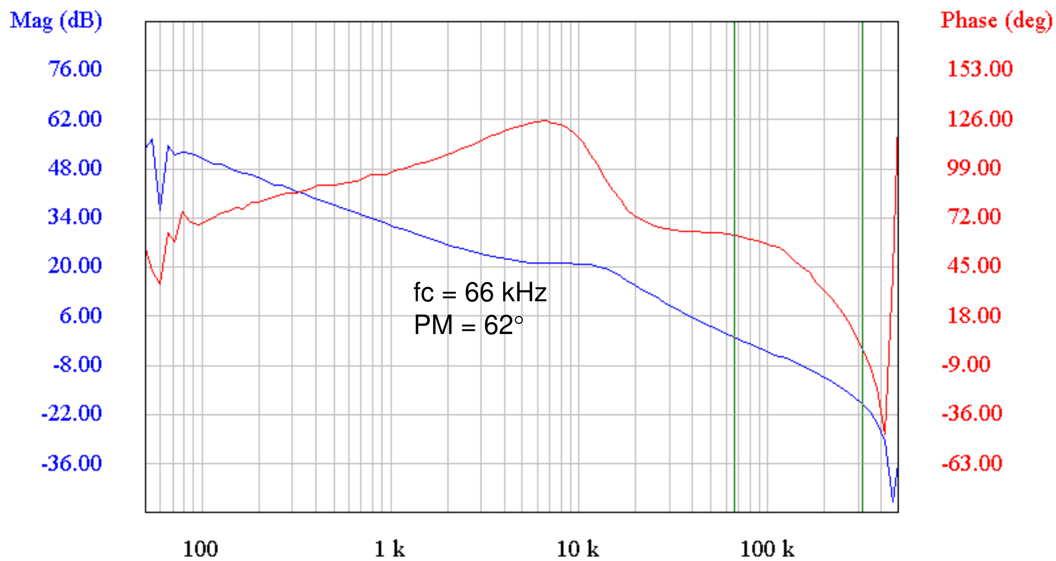


Fig. 19 Bode Plot (VIN = 12V, VOUT2 = 2.5V, I_{out2} = 20A)

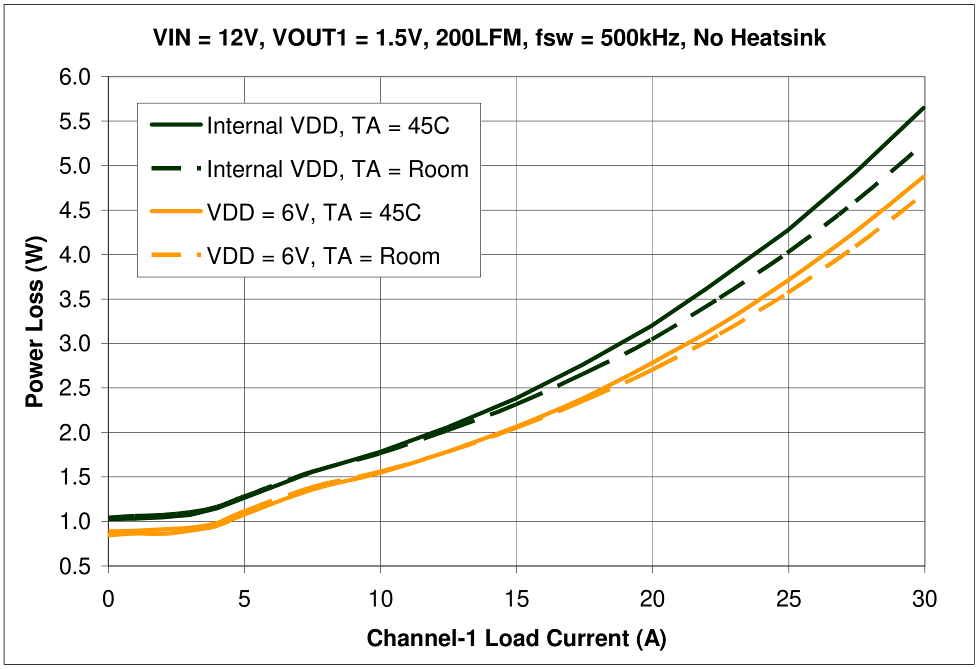


Fig. 20 Channel-1 Power Loss

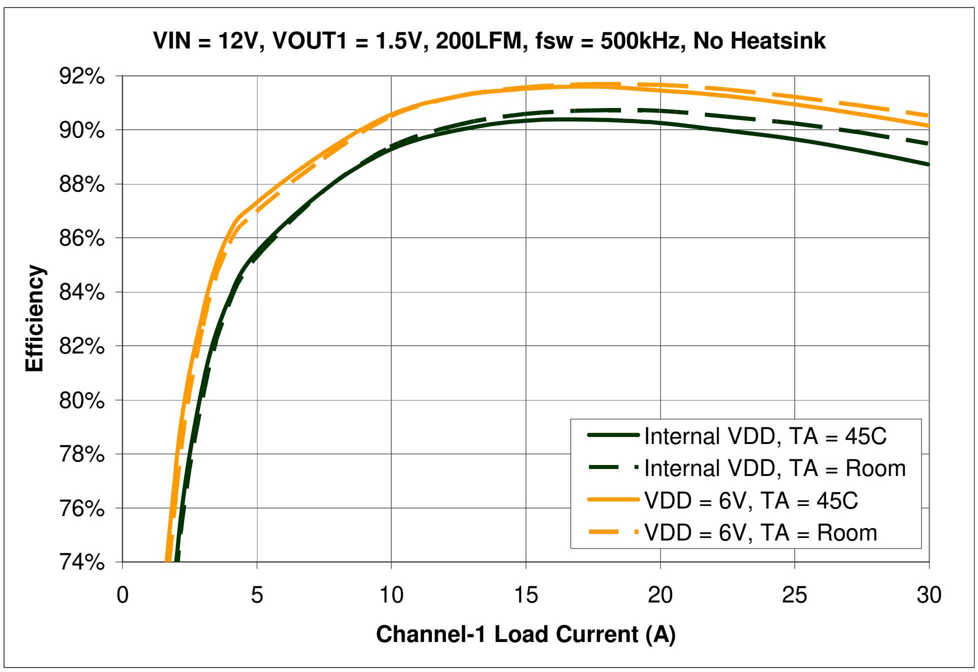


Fig. 21 Channel-1 Efficiency

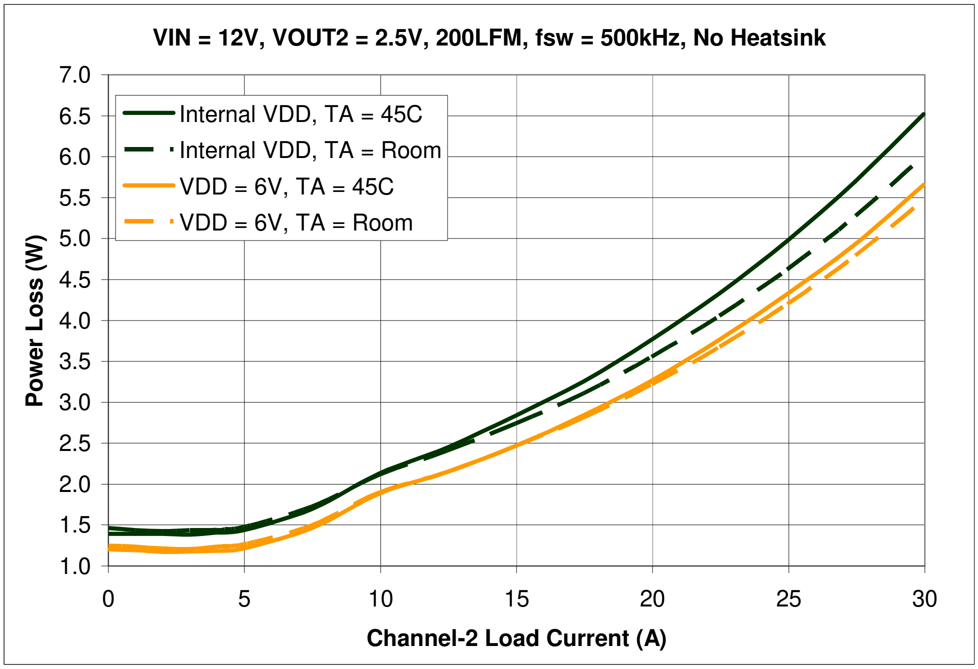


Fig. 22 Channel-2 Power Loss

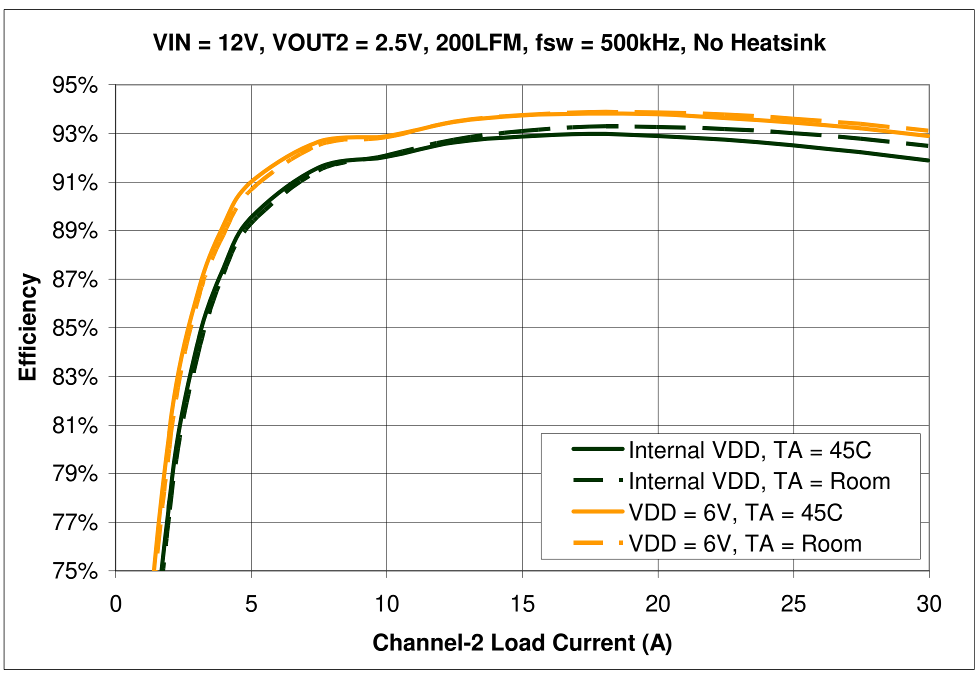


Fig. 23 Channel-2 Efficiency

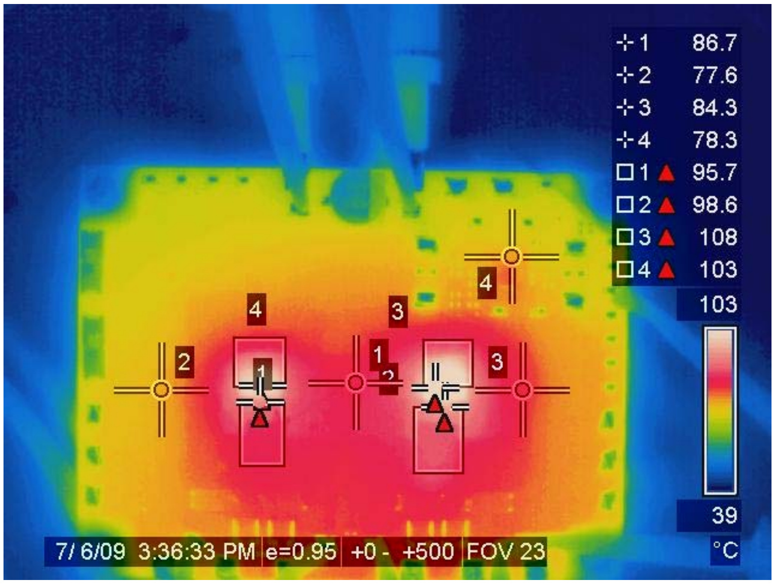


Fig. 24 Thermal Image: I_{out} = 30A per channel, VIN = 12V, with Internal VDD, VOUT1 = 1.5V, VOUT2 = 2.5V, TA = 45°C, f_{sw} = 500kHz, 200LFM, No Heatsink

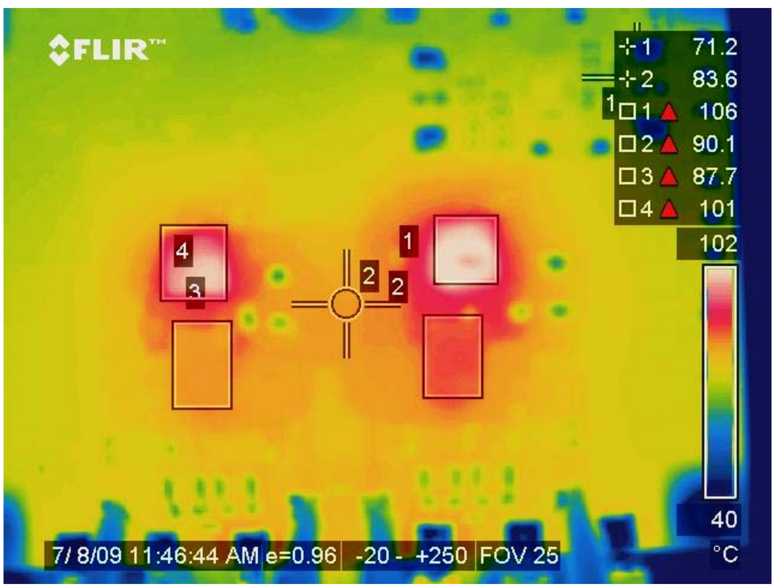


Fig. 25 Thermal Image: I_{out} = 30A per channel, VIN = 12V, VDD = 6V, VOUT1 = 1.5V, VOUT2 = 2.5V, TA = 45°C, f_{sw} = 500kHz, 200LFM, No Heatsink

Table 1 Maximum Temperature for iP2005C Dual Output Configuration

Bias Voltage	U1	U2
Internal VDD = 5.2V	103°C	108°C
External VDD = 6V	101°C	106°C

Refer to the following application notes for detailed guidelines and suggestions when implementing iPOWIR Technology products:

AN-1043: Stabilize the Buck Converter with Transconductance Amplifier
This paper explains how to design the voltage compensation network for Buck Converters with Transconductance Amplifier. The design methods and equations for Type II and Type III compensation are given.

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPowIR Technology BGA and LGA and Packages
This paper discusses optimization of the layout design for mounting iPowIR BGA and LGA packages on printed circuit boards, accounting for thermal and electrical performance and assembly considerations. Topics discussed include PCB layout placement, and via interconnect suggestions, as well as soldering, pick and place, reflow, inspection, cleaning and reworking recommendations.

AN-1030: Applying iPOWIR Products in Your Thermal Environment
This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

AN-1047: Graphical solution for two branch heatsinking Safe Operating Area
Detailed explanation of the dual axis SOA graph and how it is derived.

Use of this design for any application should be fully verified by the customer. International Rectifier cannot guarantee suitability for your applications, and is not liable for any result of usage for such applications including, without limitation, personal or property damage or violation of third party intellectual property rights.

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