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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# IRF1010NS

# IRF1010NL

HEXFET® Power MOSFET

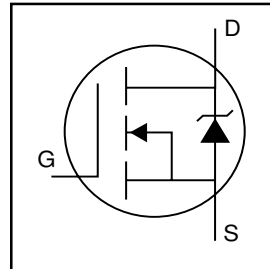
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

### Description

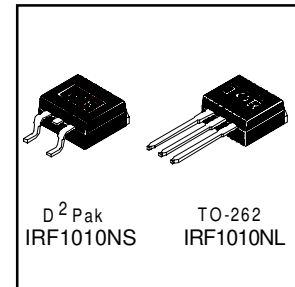
Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF1010NL) is available for low-profile applications.



|                          |
|--------------------------|
| $V_{DSS} = 55V$          |
| $R_{DS(on)} = 11m\Omega$ |
| $I_D = 85A \text{ (7)}$  |



### Absolute Maximum Ratings

|                           | Parameter  | Max.               | Units |
|---------------------------|--|--------------------|-------|
| $I_D @ T_C = 25^\circ C$  | Continuous Drain Current, $V_{GS} @ 10V \text{ (8)}$ | 85 (7)             | A     |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V \text{ (8)}$ | 60                 |       |
| $I_{DM}$                  | Pulsed Drain Current (1) (8)                         | 290                |       |
| $P_D @ T_C = 25^\circ C$  | Power Dissipation                                    | 180                | W     |
|                           | Linear Derating Factor                               | 1.2                | W/°C  |
| $V_{GS}$                  | Gate-to-Source Voltage                               | $\pm 20$           | V     |
| $I_{AR}$                  | Avalanche Current (1)                                | 43                 | A     |
| $E_{AR}$                  | Repetitive Avalanche Energy (1)                      | 18                 | mJ    |
| dv/dt                     | Peak Diode Recovery dv/dt (3) (8)                    | 3.6                | V/ns  |
| $T_J$                     | Operating Junction and                               | -55 to + 175       | °C    |
| $T_{STG}$                 | Storage Temperature Range                            |                    |       |
|                           | Soldering Temperature, for 10 seconds                |                    |       |
|                           | Mounting torque, 6-32 or M3 screw                    | 10 lbf•in (1.1N•m) |       |

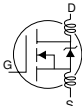
### Thermal Resistance

|                 | Parameter  | Typ. | Max. | Units |
|-----------------|--|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case                                   | —    | 0.85 | °C/W  |
| $R_{\theta JA}$ | Junction-to-Ambient ( PCB Mounted, steady-state)** | —    | 40   |       |

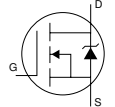
# IRF1010NS/IRF1010NL

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**IR** Rectifier

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

|  | Parameter                            | Min. | Typ.  | Max. | Units | Conditions   |
|--|--------------------------------------|------|-------|------|-------|--|
| V <sub>(BR)DSS</sub>                   | Drain-to-Source Breakdown Voltage    | 55   | —     | —    | V     | V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA   |
| ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub> | Breakdown Voltage Temp. Coefficient  | —    | 0.058 | —    | V/°C  | Reference to 25°C, I <sub>D</sub> = 1mA ⑧  |
| R <sub>DS(on)</sub>                    | Static Drain-to-Source On-Resistance | —    | —     | 11   | mΩ    | V <sub>GS</sub> = 10V, I <sub>D</sub> = 43A ④  |
| V <sub>GS(th)</sub>                    | Gate Threshold Voltage               | 2.0  | —     | 4.0  | V     | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA                           |
| g <sub>fs</sub>                        | Forward Transconductance             | 32   | —     | —    | S     | V <sub>DS</sub> = 25V, I <sub>D</sub> = 43A④⑧  |
| I <sub>DSS</sub>                       | Drain-to-Source Leakage Current      | —    | —     | 25   | μA    | V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V  |
|  |                                      | —    | —     | 250  |       | V <sub>DS</sub> = 44V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C                  |
| I <sub>GSS</sub>                       | Gate-to-Source Forward Leakage       | —    | —     | 100  | nA    | V <sub>GS</sub> = 20V  |
|  | Gate-to-Source Reverse Leakage       | —    | —     | -100 |       | V <sub>GS</sub> = -20V   |
| Q <sub>g</sub>                         | Total Gate Charge                    | —    | —     | 120  | nC    | I <sub>D</sub> = 43A   |
| Q <sub>gs</sub>                        | Gate-to-Source Charge                | —    | —     | 19   |       | V <sub>DS</sub> = 44V  |
| Q <sub>gd</sub>                        | Gate-to-Drain ("Miller") Charge      | —    | —     | 41   |       | V <sub>GS</sub> = 10V, See Fig. 6 and 13 ④⑧  |
| t <sub>d(on)</sub>                     | Turn-On Delay Time                   | —    | 13    | —    |       | V <sub>DD</sub> = 28V  |
| t <sub>r</sub>                         | Rise Time                            | —    | 76    | —    | ns    | I <sub>D</sub> = 43A   |
| t <sub>d(off)</sub>                    | Turn-Off Delay Time                  | —    | 39    | —    |       | R <sub>G</sub> = 3.6Ω  |
| t <sub>f</sub>                         | Fall Time                            | —    | 48    | —    |       | V <sub>GS</sub> = 10V, See Fig. 10 ④⑧  |
| L <sub>D</sub>                         | Internal Drain Inductance            | —    | 4.5   | —    | nH    | Between lead,<br>6mm (0.25in.)<br>from package<br>and center of die contact          |
| L <sub>S</sub>                         | Internal Source Inductance           | —    | 7.5   | —    |       |  |
| C <sub>iss</sub>                       | Input Capacitance                    | —    | 3210  | —    | pF    | V <sub>GS</sub> = 0V   |
| C <sub>oss</sub>                       | Output Capacitance                   | —    | 690   | —    |       | V <sub>DS</sub> = 25V  |
| C <sub>rss</sub>                       | Reverse Transfer Capacitance         | —    | 140   | —    |       | f = 1.0MHz, See Fig. 5 ⑧   |
| E <sub>AS</sub>                        | Single Pulse Avalanche Energy②⑧      | —    | 1030⑤ | 250⑥ |       | mJ   |

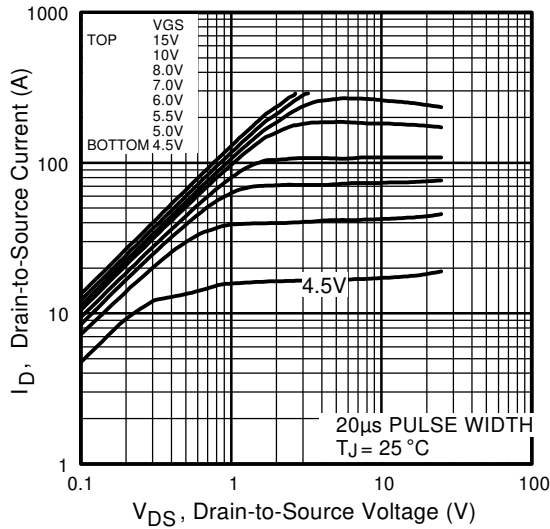
## Source-Drain Ratings and Characteristics

|                 | Parameter                                 | Min.   | Typ. | Max. | Units | Conditions  |
|-----------------|---|--|------|------|-------|---|
| I <sub>S</sub>  | Continuous Source Current<br>(Body Diode) | —  | —    | 85⑦  | A     | MOSFET symbol<br>showing the<br>integral reverse<br>p-n junction diode.               |
| I <sub>SM</sub> | Pulsed Source Current<br>(Body Diode)①    | —  | —    | 290  |       |  |
| V <sub>SD</sub> | Diode Forward Voltage                     | —  | —    | 1.3  | V     | T <sub>J</sub> = 25°C, I <sub>S</sub> = 43A, V <sub>GS</sub> = 0V ④                   |
| t <sub>rr</sub> | Reverse Recovery Time                     | —  | 69   | 100  | ns    | T <sub>J</sub> = 25°C, I <sub>F</sub> = 43A   |
| Q <sub>rr</sub> | Reverse Recovery Charge                   | —  | 220  | 230  | nC    | di/dt = 100A/μs ④⑧  |
| t <sub>on</sub> | Forward Turn-On Time                      | Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> ) |      |      |       |   |

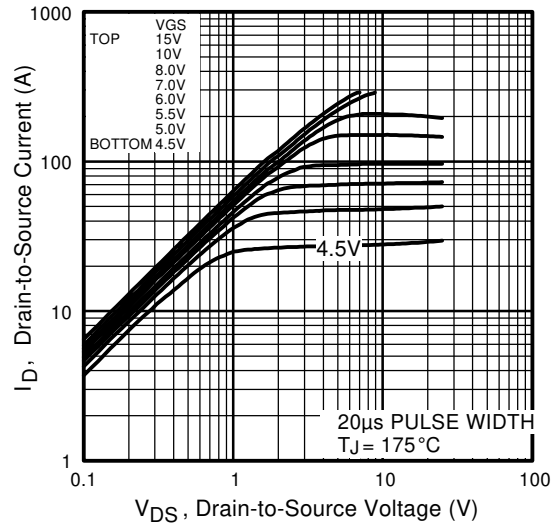
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting T<sub>J</sub> = 25°C, L = 270μH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 43A, V<sub>GS</sub> = 10V (See Figure 12)
- ③ I<sub>SD</sub> ≤ 43A, di/dt ≤ 210A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>.  
T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ This is a typical value at device destruction and represents operation outside rated limits.

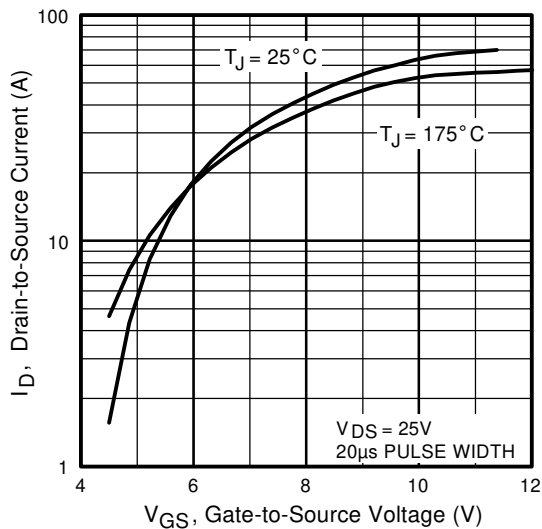
- ⑥ This is a calculated value limited to T<sub>J</sub> = 175°C .
  - ⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
  - ⑧ Uses IRF1010N data and test conditions.
- \*\* When mounted on 1" square PCB ( FR-4 or G-10 Material ).  
For recommended footprint and soldering techniques refer to application note #AN-994.



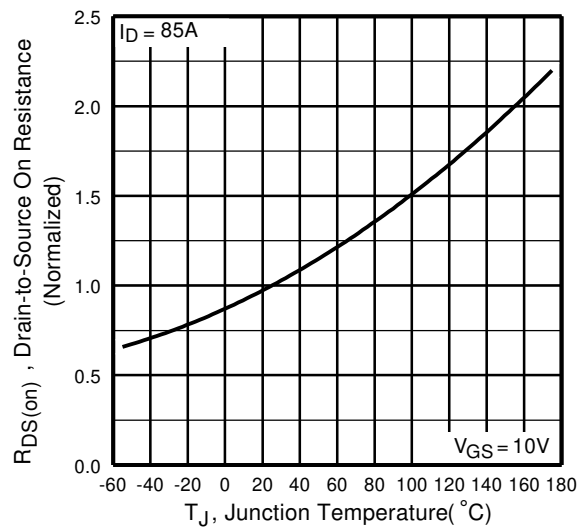
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



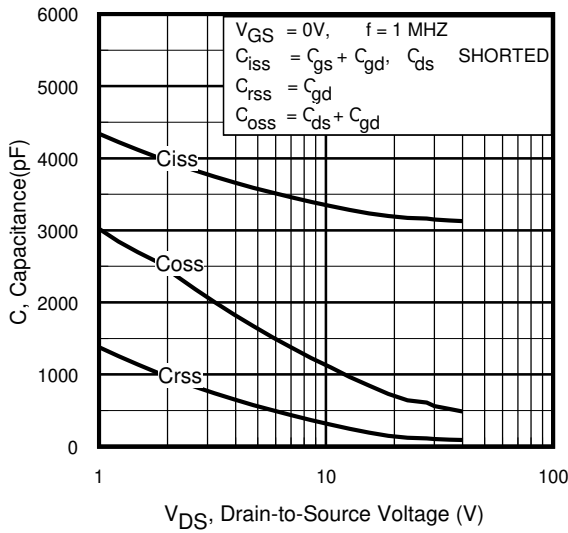
**Fig 3.** Typical Transfer Characteristics



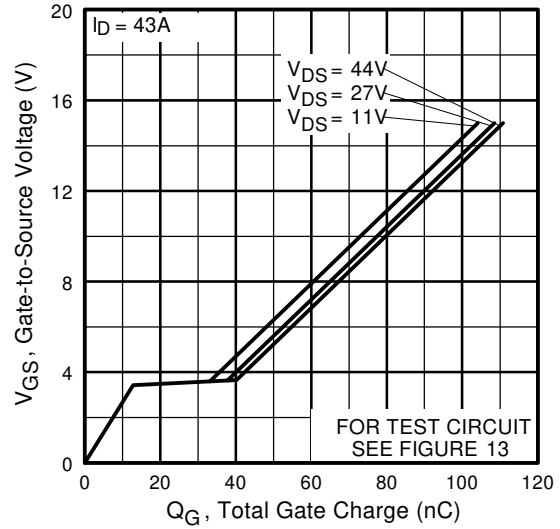
**Fig 4.** Normalized On-Resistance Vs. Temperature

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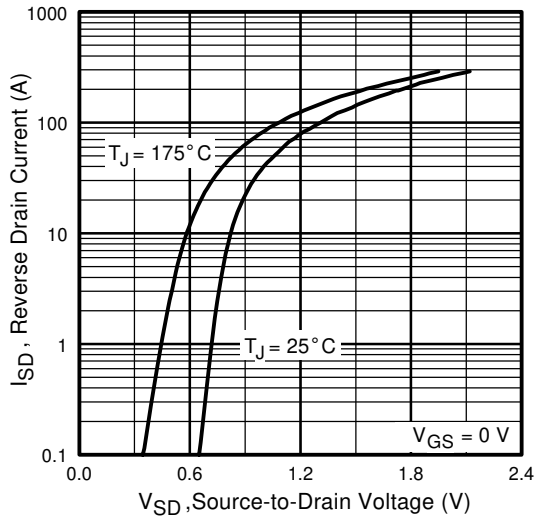
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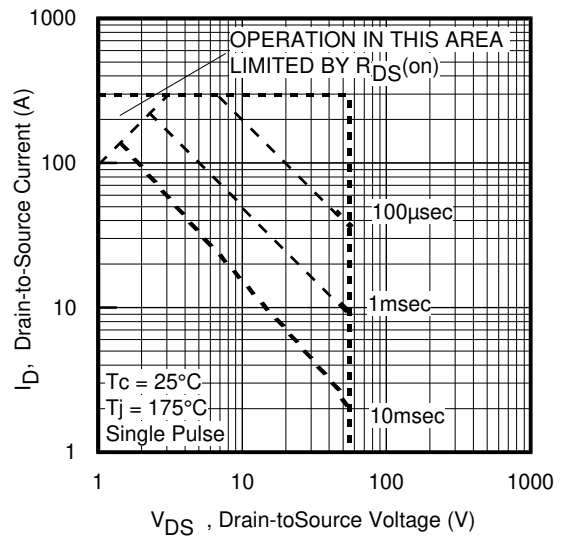
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



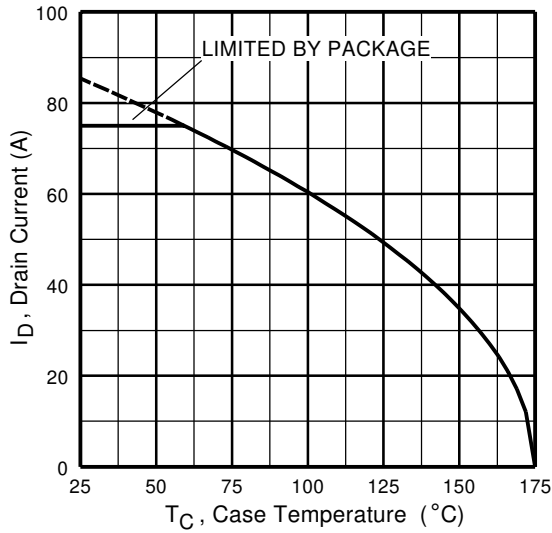
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



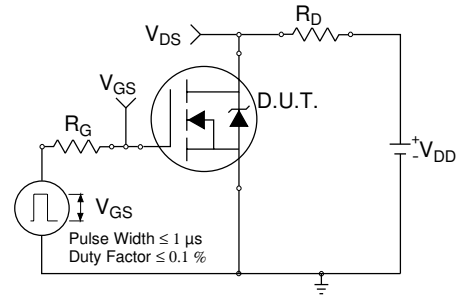
**Fig 7.** Typical Source-Drain Diode Forward Voltage



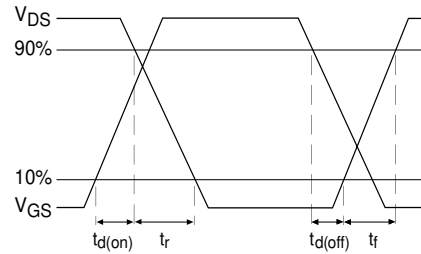
**Fig 8.** Maximum Safe Operating Area



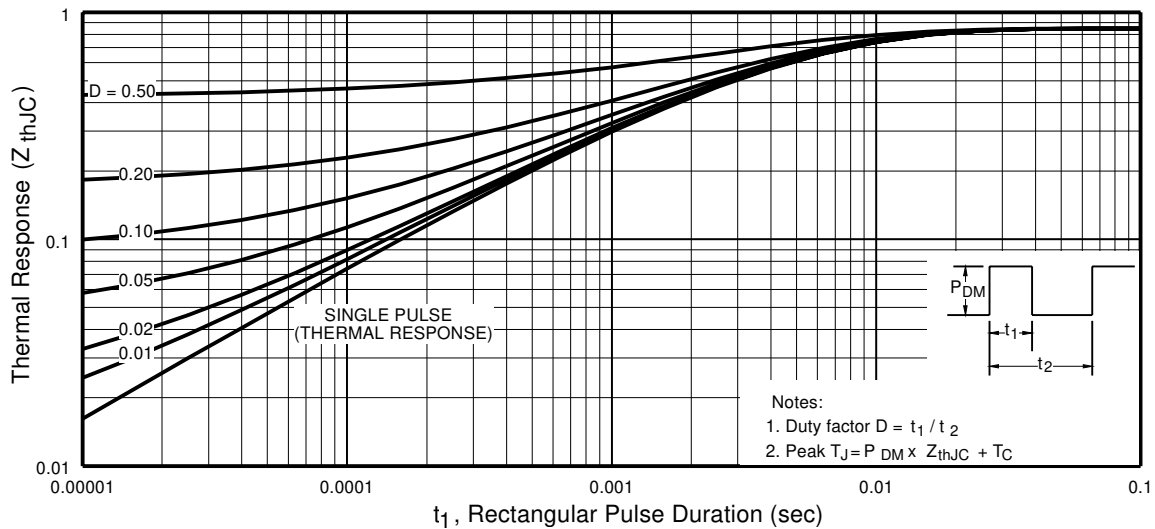
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



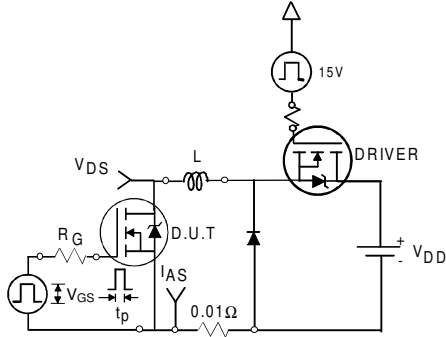
**Fig 10b.** Switching Time Waveforms



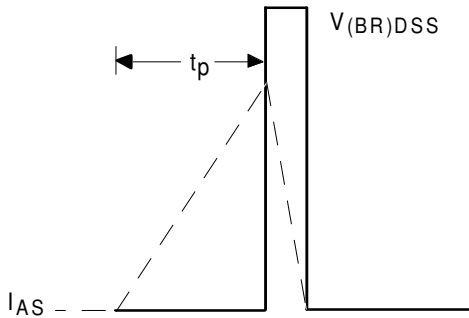
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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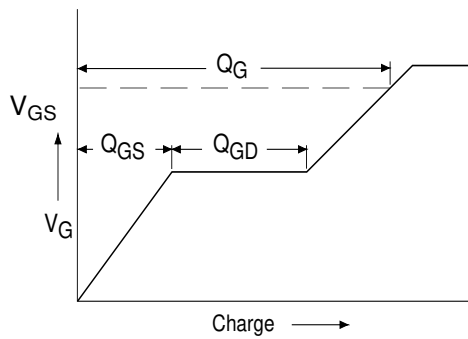
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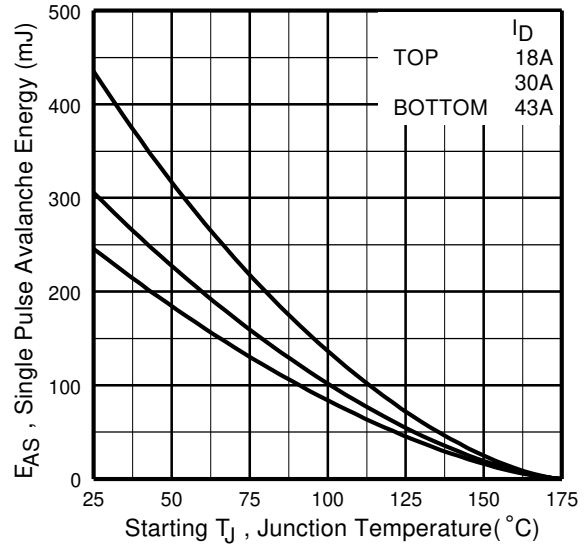
**Fig 12a.** Unclamped Inductive Test Circuit



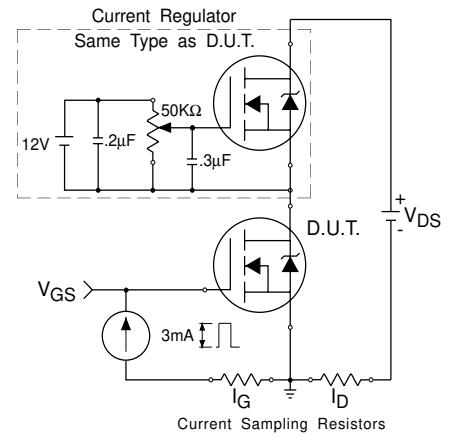
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

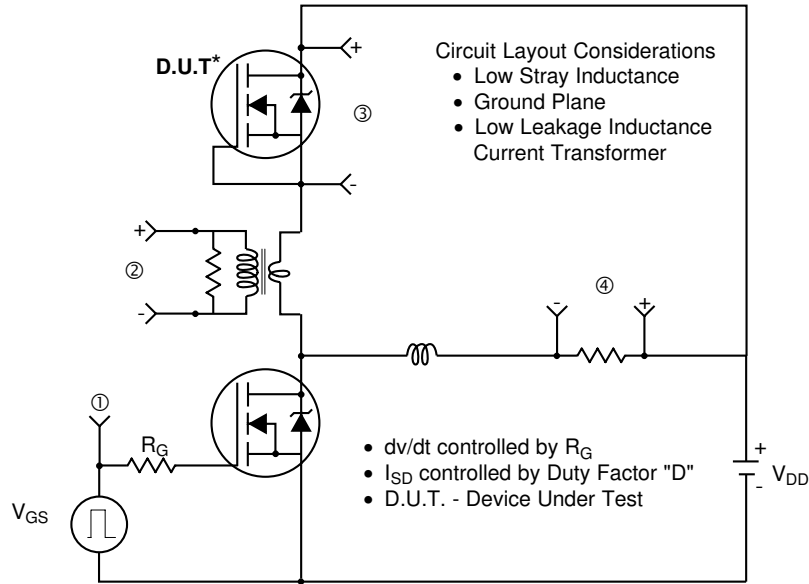


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

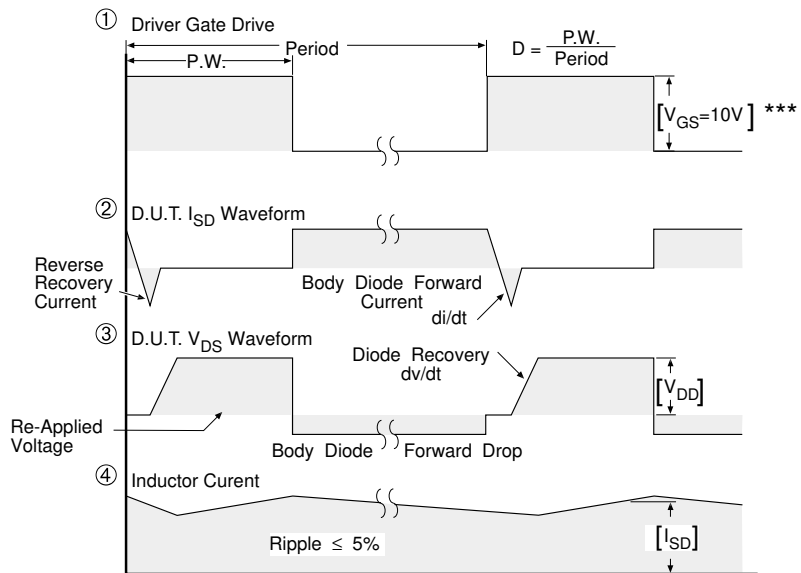


**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

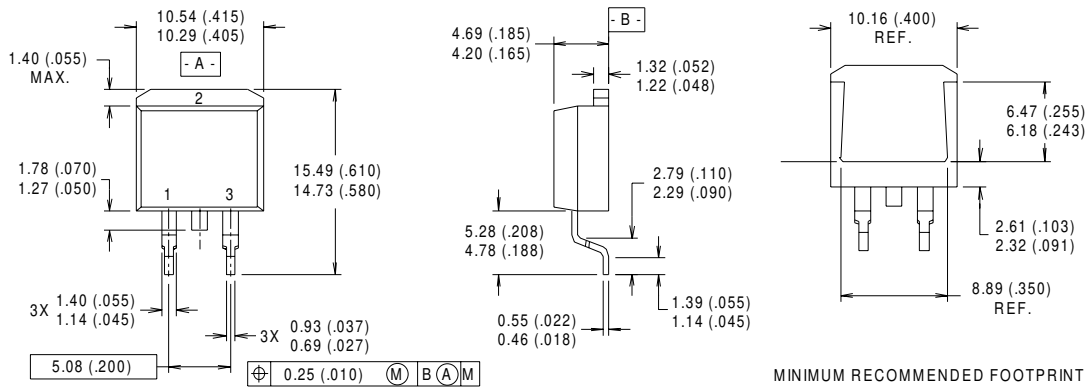
**Fig 14.** For N-channel HEXFET® power MOSFETs



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## D<sup>2</sup>Pak Package Outline



### NOTES:

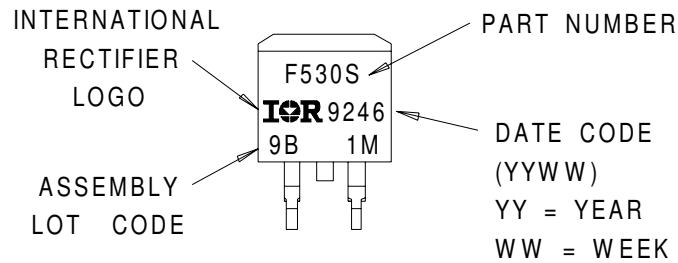
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

### LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

## Part Marking Information

D<sup>2</sup>Pak



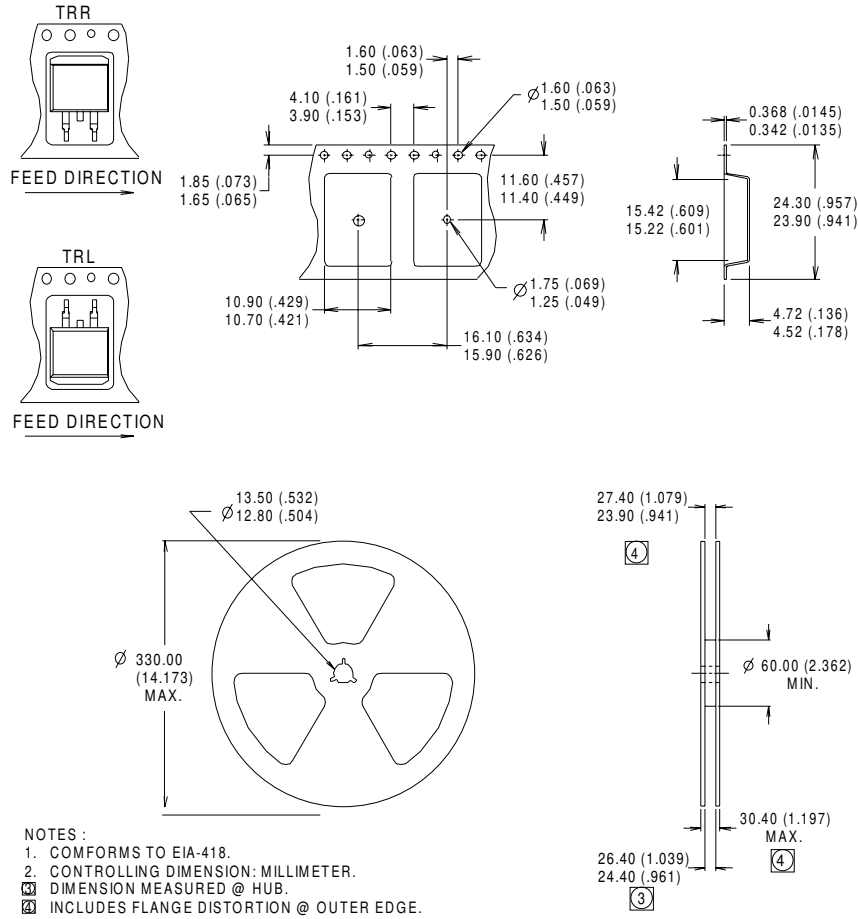


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## Tape & Reel Information

### D<sup>2</sup>Pak



Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
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<http://www.irf.com/package/>