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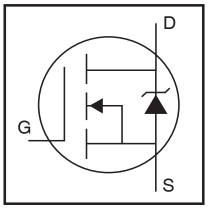
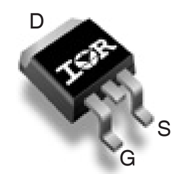
HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}		100V
$R_{DS(on)}$	typ.	9.3mΩ
	max.	11.6mΩ
I_D		103A

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



D^2Pak
IRF3610SPbF

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	103	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	73	
I_{DM}	Pulsed Drain Current ②	410	
P_D @T_C = 25°C	Maximum Power Dissipation	333	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	23	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Avalanche Characteristics

E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	460	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧⑨	——	0.50	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦	——	40	

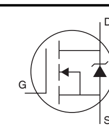
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.10	——	V/°C	Reference to 25°C, I_D = 1.0mA ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	9.3	11.6	mΩ	V_{GS} = 10V, I_D = 62A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Transconductance	110	——	——	S	V_{DS} = 25V, I_D = 62A
R_G	Internal Gate Resistance	——	2.2	——	Ω	
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 100V, V_{GS} = 0V
		——	——	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	——	100	150	nC	I_D = 62A
Q_{gs}	Gate-to-Source Charge	——	23	——		V_{DS} =50V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	42	——		V_{GS} = 10V ④
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	58	——		I_D = 62A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	——	15	——	ns	V_{DD} = 65V
t_r	Rise Time	——	55	——		I_D = 62A
$t_{d(off)}$	Turn-Off Delay Time	——	77	——		R_G = 2.7Ω
t_f	Fall Time	——	43	——		V_{GS} = 10V ④
C_{iss}	Input Capacitance	——	5380	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	690	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	100	——		ƒ = 1.0 MHz, See Fig. 5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	——	560	——		V_{GS} = 0V, V_{DS} = 0V to 80V ⑥, See Fig. 11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	——	750	——		V_{GS} = 0V, V_{DS} = 0V to 80V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	103	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	410	A	
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 62A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	110	——	ns	T_J = 25°C V_R = 85V,
		——	120	——		T_J = 125°C I_F = 62A
Q_{rr}	Reverse Recovery Charge	——	570	——	nC	T_J = 25°C di/dt = 100A/µs ④
		——	710	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	-9.5	——	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.24mH R_G = 50Ω, I_{AS} = 62A, V_{GS} =10V. Part not recommended for use above this value.

③ I_{SD} ≤ 62A, di/dt ≤ 1935A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑧ R_θ is measured at T_J approximately 90°C.

⑨ $R_{\theta JC}$ value shown is at time zero.

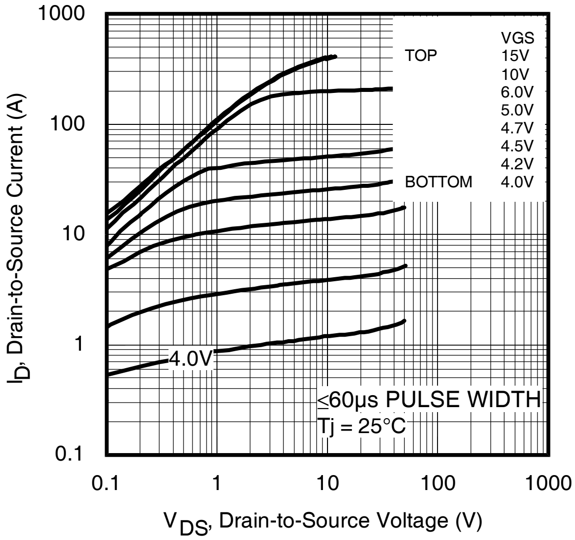


Fig 1. Typical Output Characteristics

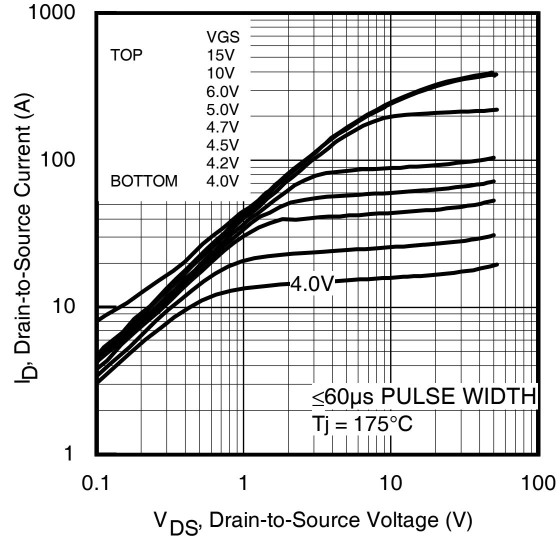


Fig 2. Typical Output Characteristics

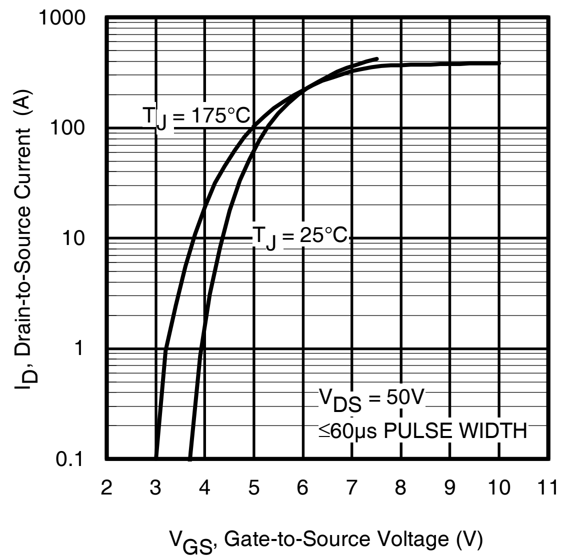


Fig 3. Typical Transfer Characteristics

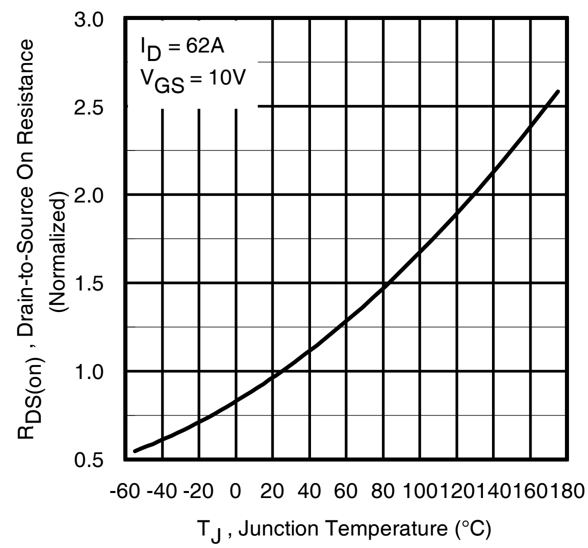


Fig 4. Normalized On-Resistance vs. Temperature

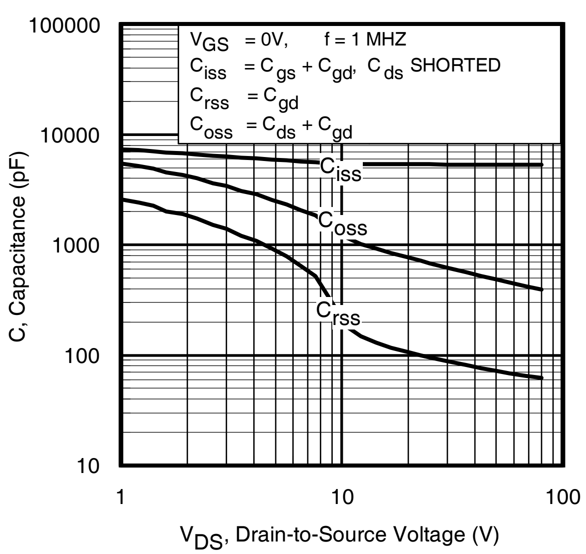


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

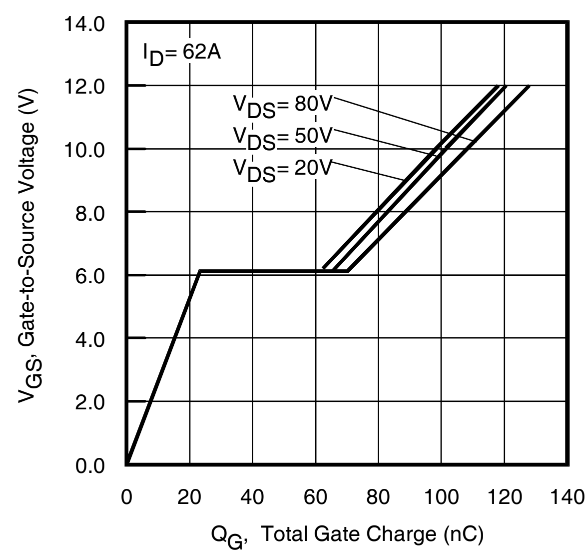


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

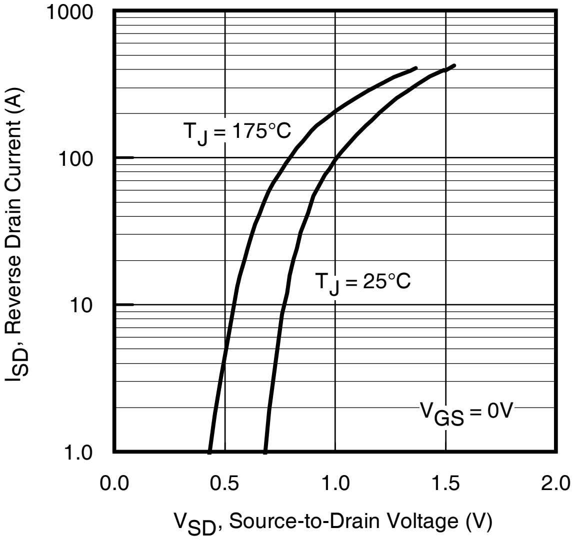


Fig 7. Typical Source-Drain Diode Forward Voltage

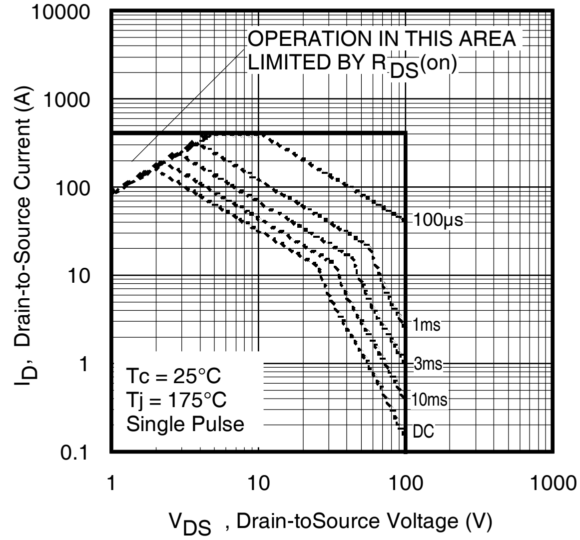


Fig 8. Maximum Safe Operating Area

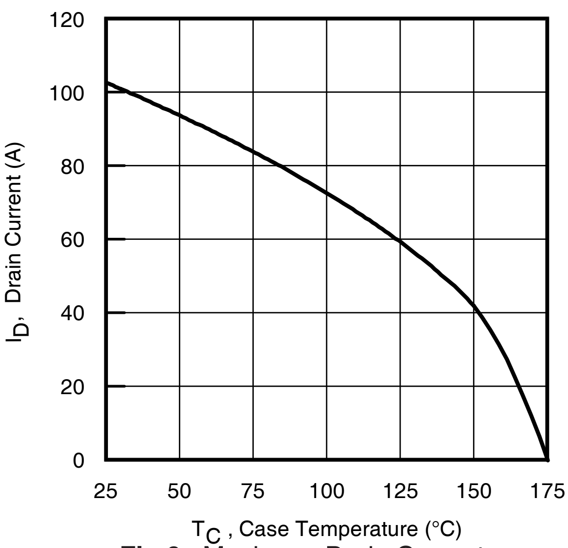


Fig 9. Maximum Drain Current vs. Case Temperature

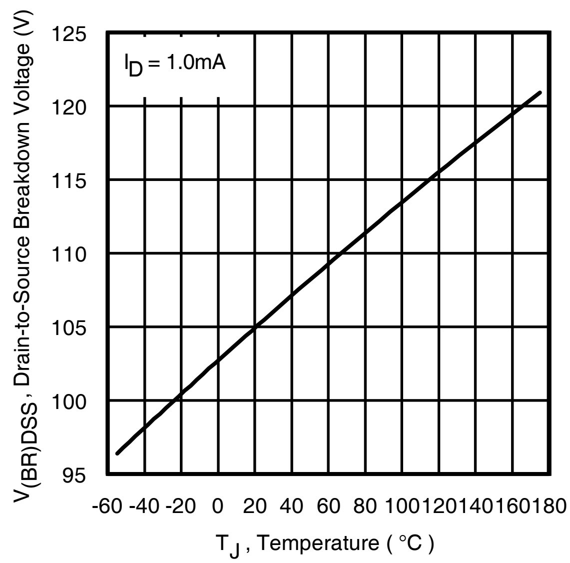


Fig 10. Drain-to-Source Breakdown Voltage

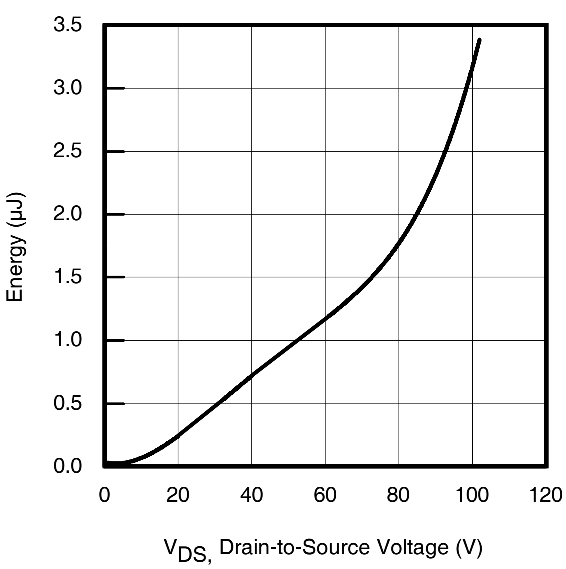


Fig 11. Typical C_{OSS} Stored Energy

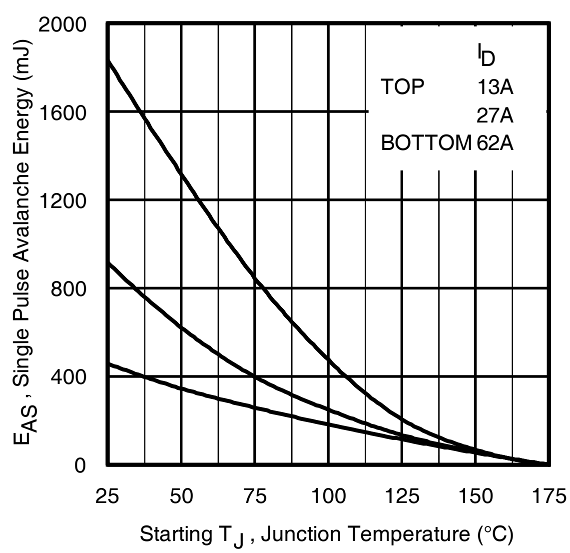


Fig 12. Maximum Avalanche Energy vs. DrainCurrent

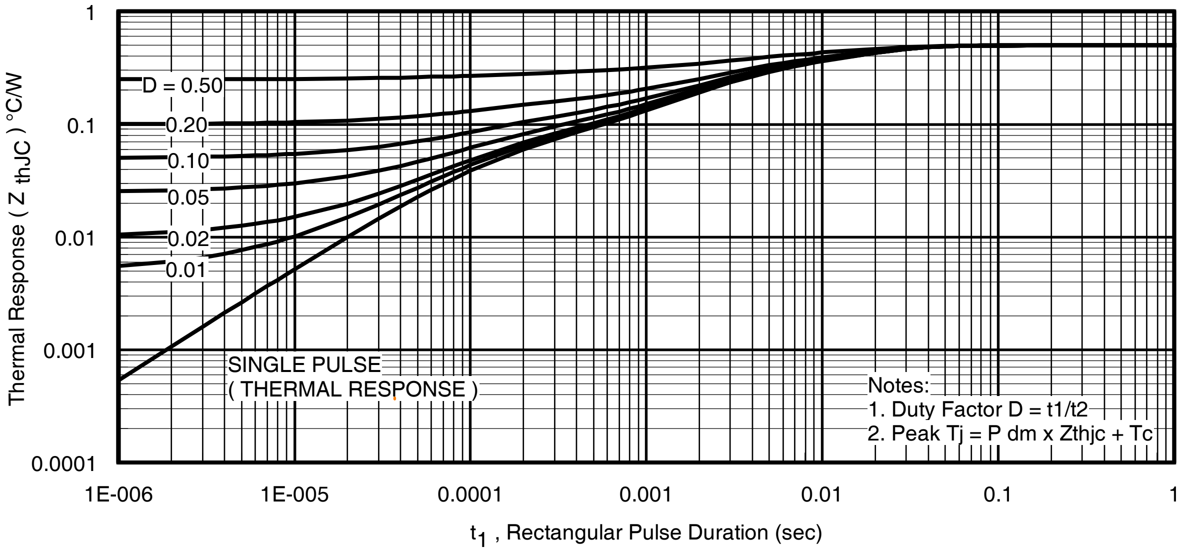


Fig 13. Maximum Effective Transient Thermal Impedance Junction-to-Case

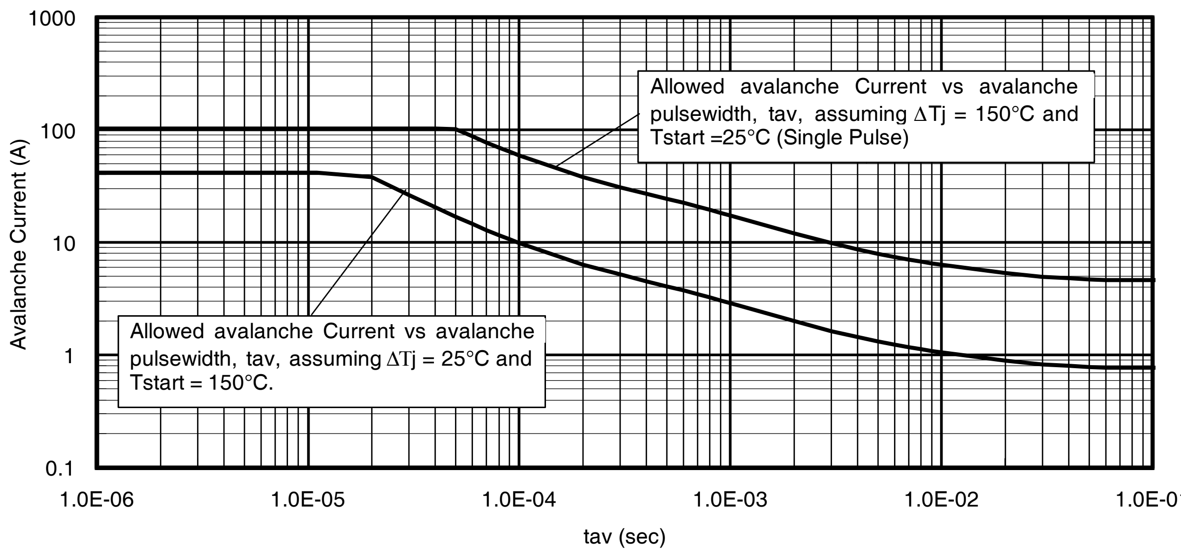


Fig 14. Typical Avalanche Current vs. Pulse Width

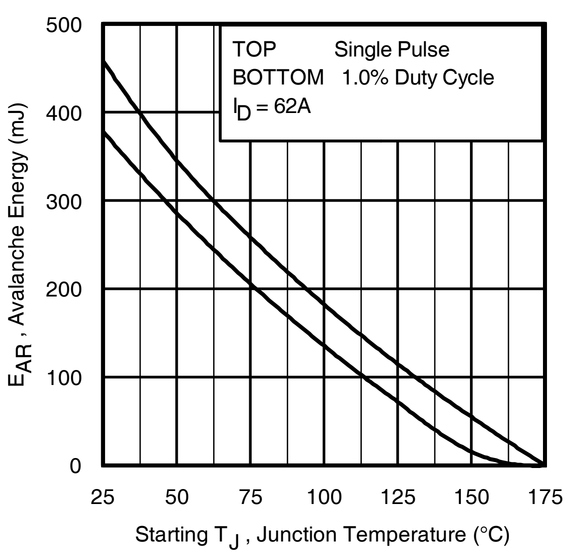


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

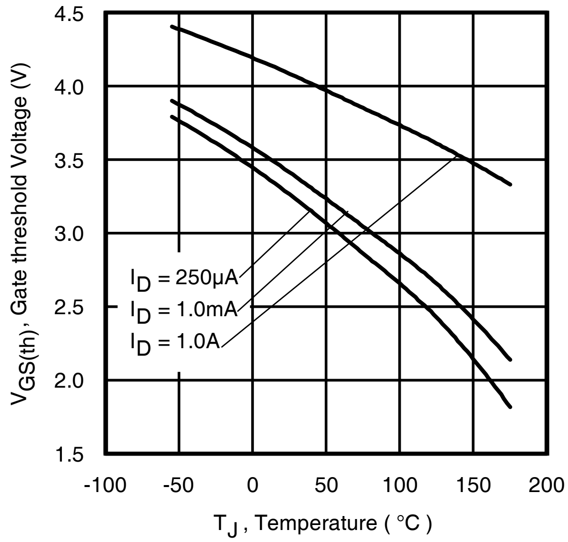


Fig 16. Threshold Voltage vs. Temperature

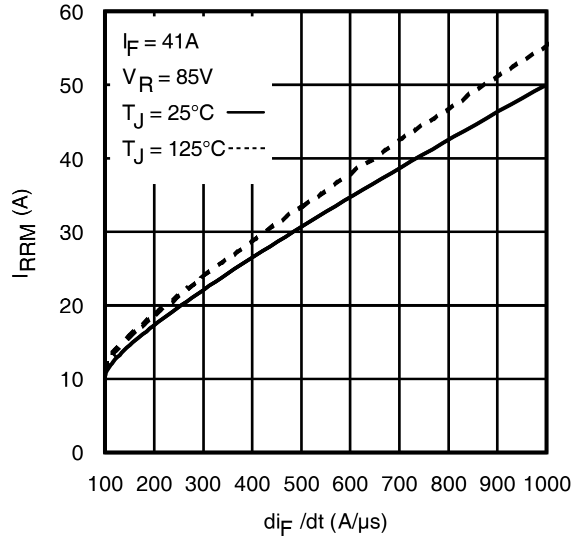


Fig. 17 - Typical Recovery Current vs. di_f/dt

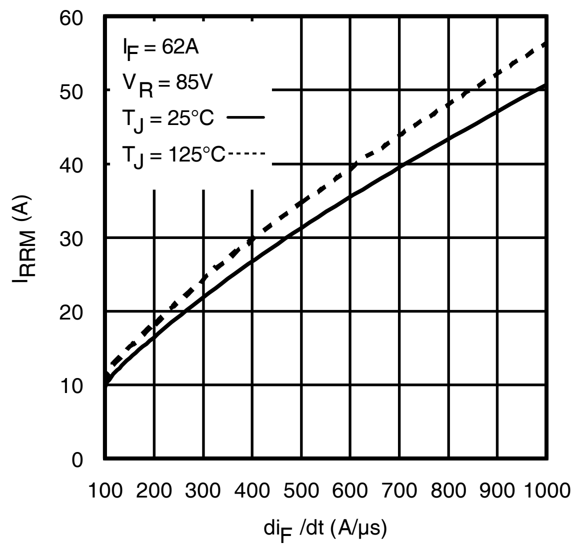


Fig. 18 - Typical Recovery Current vs. di_f/dt

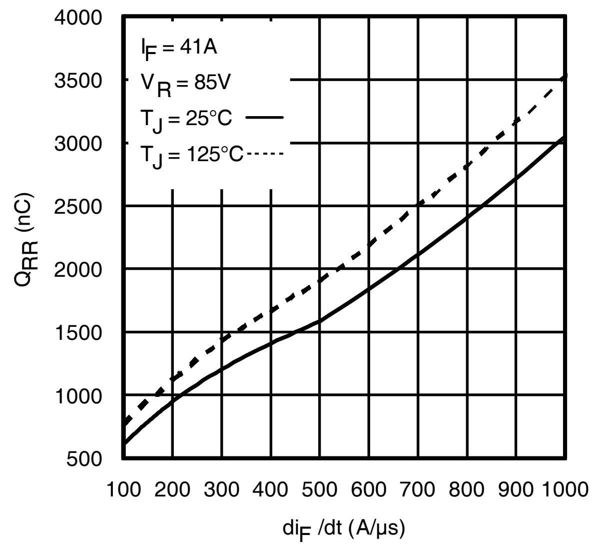


Fig. 19 - Typical Stored Charge vs. di_f/dt

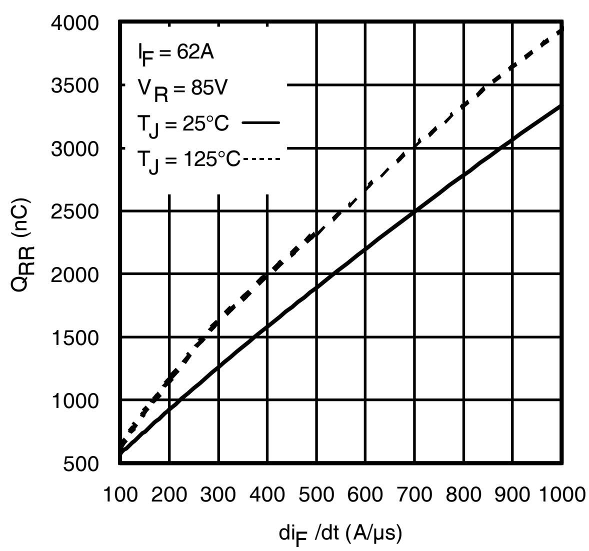
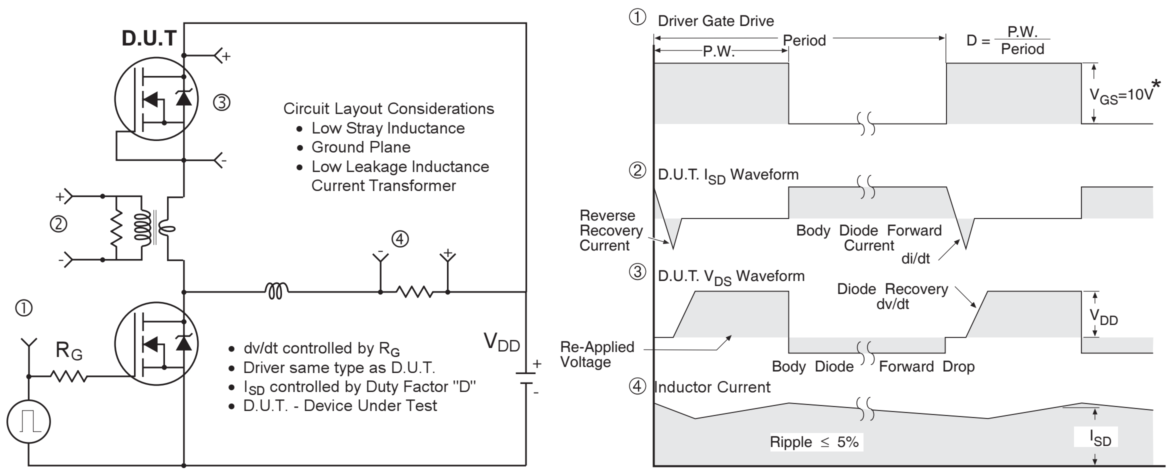


Fig. 20 - Typical Stored Charge vs. di_f/dt



* V_{GS} = 5V for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

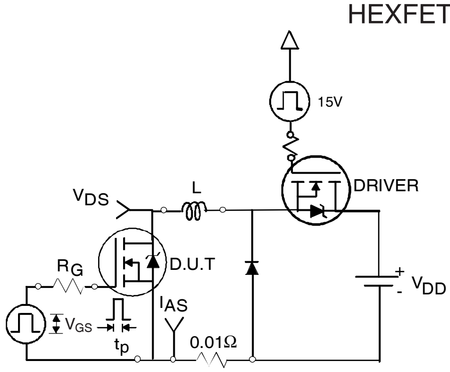


Fig 22a. Unclamped Inductive Test Circuit

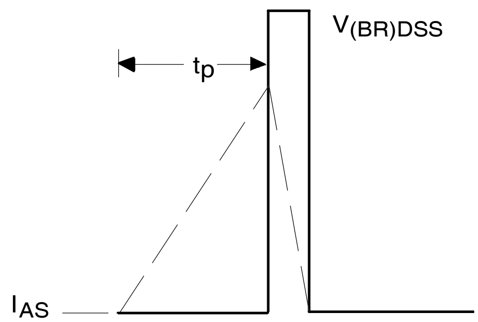


Fig 22b. Unclamped Inductive Waveforms

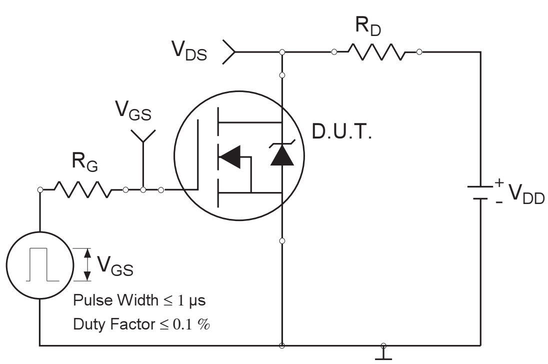


Fig 23a. Switching Time Test Circuit

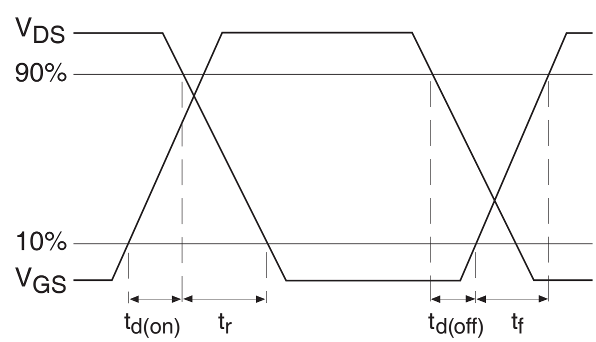


Fig 23b. Switching Time Waveforms

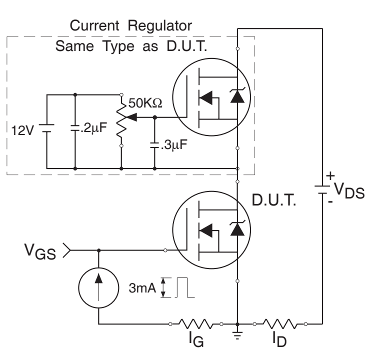


Fig 24a. Gate Charge Test Circuit

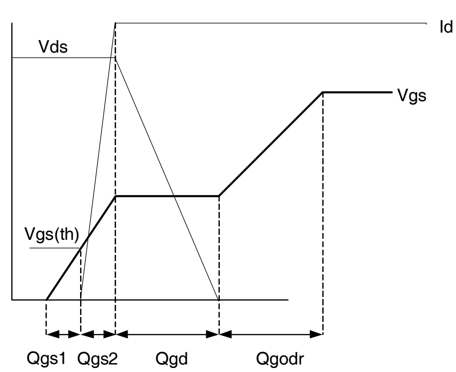
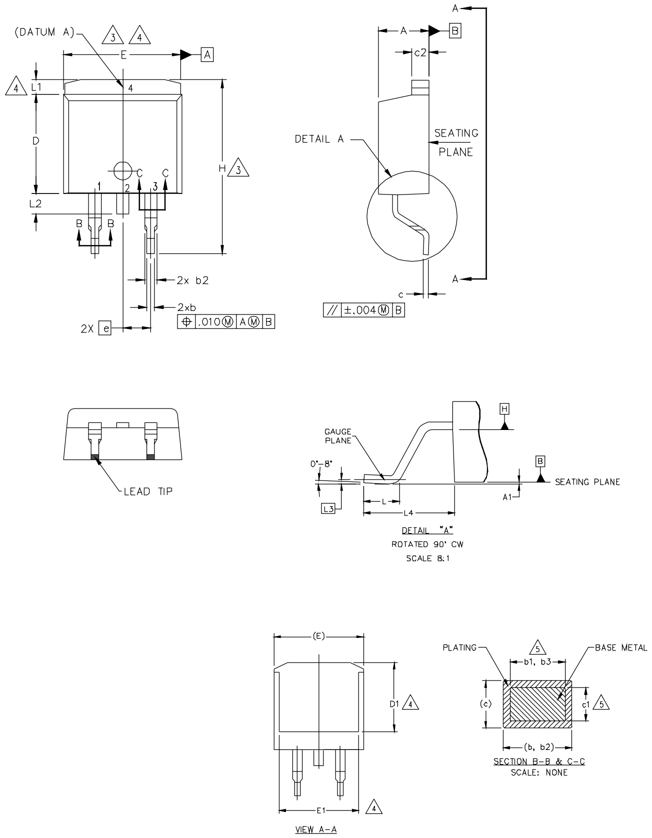


Fig 24b. Gate Charge Waveform

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. (△3) DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. (△4) THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. (△5) DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.65	–	.066	4
L2	1.27	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

IGBTs, CoPACK

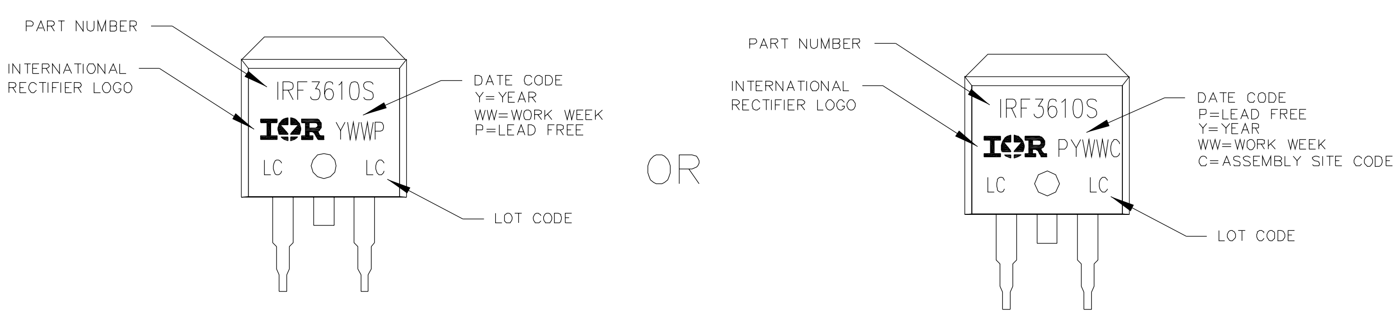
1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

DIODES

1.– ANODE *
2, 4.– CATHODE
3.– ANODE

* PART DEPENDENT.

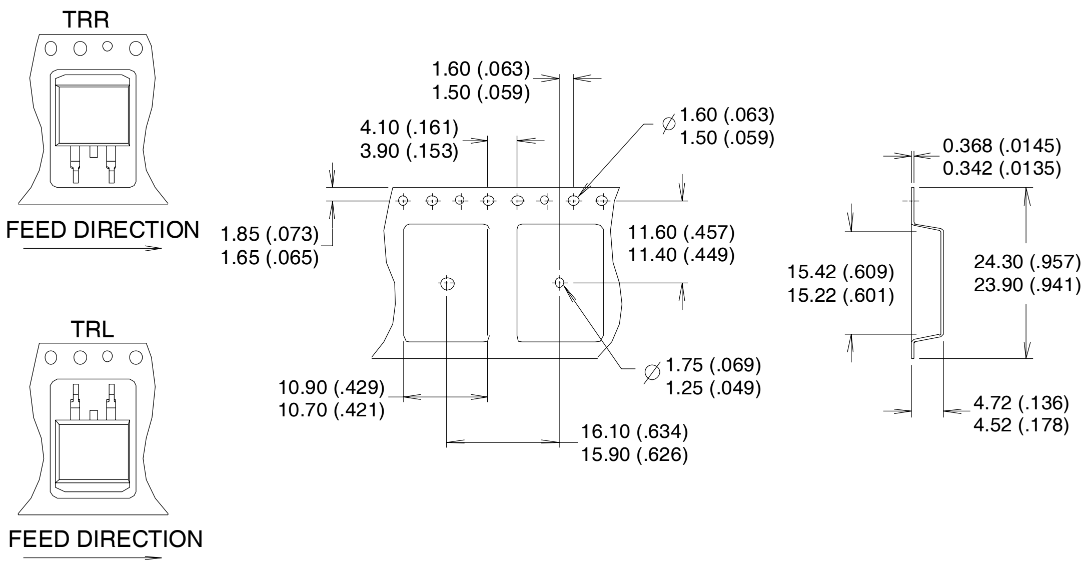
D²Pak (TO-263AB) Part Marking Information

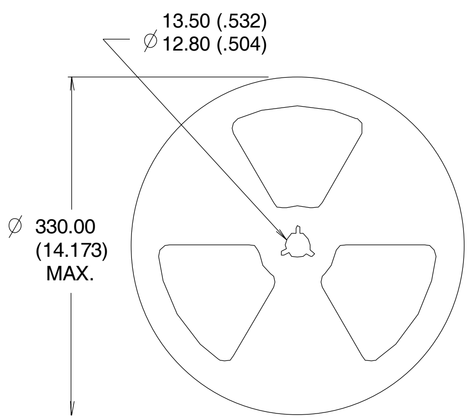


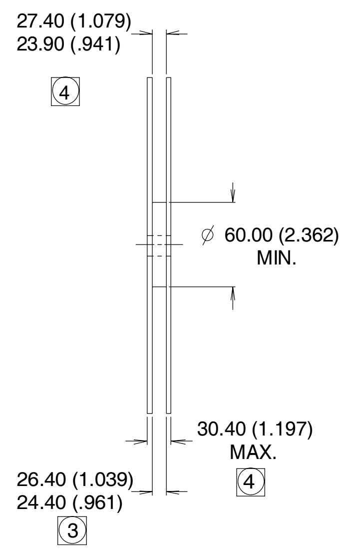
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D2Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

International
IOR Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
To contact International Rectifier, please visit http://www.irf.com/whoto-call/

