



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTORS THRU-HOLE (TO-204AA/AE)

IRF450 JANTX2N6770 JANTXV2N6770 500V, N-CHANNEL

Product Summary

Part Number	BVDSS	RDS(on)	ID
IRF450	500V	0.400Ω	12A

The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.



TO-3

Features:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements
- Ease of Paralleling

Absolute Maximum Ratings

	Parameter		Units
ID @ VGS = 0V, TC = 25°C	Continuous Drain Current	12	A
ID @ VGS = 0V, TC = 100°C	Continuous Drain Current	7.75	
IDM	Pulsed Drain Current ①	48	
PD @ TC = 25°C	Max. Power Dissipation	150	W
	Linear Derating Factor	1.2	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	8.0	mJ
IAR	Avalanche Current ①	12	A
EAR	Repetitive Avalanche Energy ①	-	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	11.5 (typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.78	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.400		V _{GS} = 10V, I _D = 7.75A④
		—	—	0.500		V _{GS} = 10V, I _D = 12A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	5.5	—	—	S (Ω)	V _{DS} > 15V, I _{DS} = 7.75A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 400V, V _{GS} = 0V
		—	—	250		V _{DS} = 400V V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	55	—	120	nC	V _{GS} = 10V, I _D = 12A
Q _{gs}	Gate-to-Source Charge	5.0	—	19		V _{DS} = 250V
Q _{gd}	Gate-to-Drain ('Miller') Charge	27	—	70		
t _{d(on)}	Turn-On Delay Time	—	—	35	ns	V _{DD} = 250V, I _D = 12A, R _G = 2.35Ω
t _r	Rise Time	—	—	190		
t _{d(off)}	Turn-Off Delay Time	—	—	170		
t _f	Fall Time	—	—	130		
L _S + L _D	Total Inductance	—	6.1	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C _{iss}	Input Capacitance	—	2700	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	600	—		
C _{rss}	Reverse Transfer Capacitance	—	240	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	12	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	48		
V _{SD}	Diode Forward Voltage	—	—	1.7	V	T _j = 25°C, I _S = 12A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	1600	nS	T _j = 25°C, I _F = 12A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	14	μC	V _{DD} ≤ 50V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction to Case	—	—	0.83	°C/W	Typical socket mount
R _{thJA}	Junction to Ambient	—	—	30		

For footnotes refer to the last page

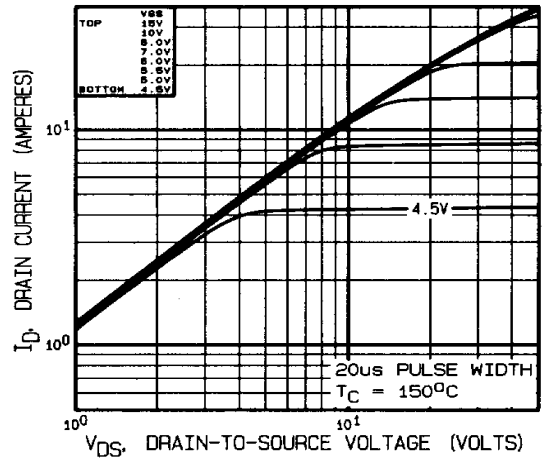
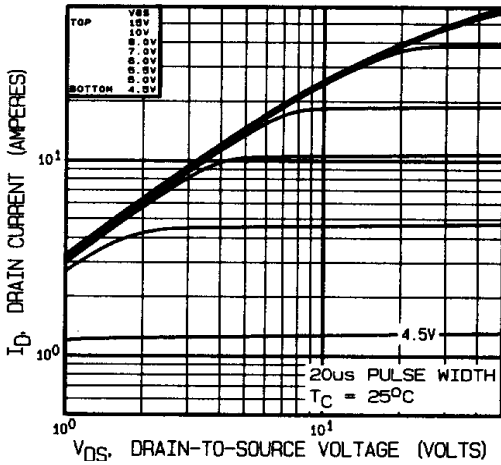


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

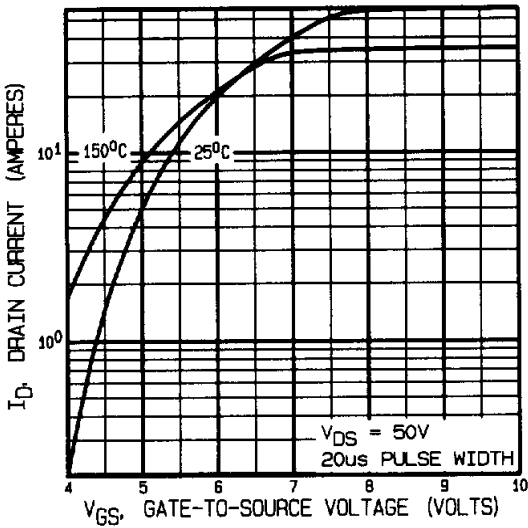


Fig 3. Typical Transfer Characteristics

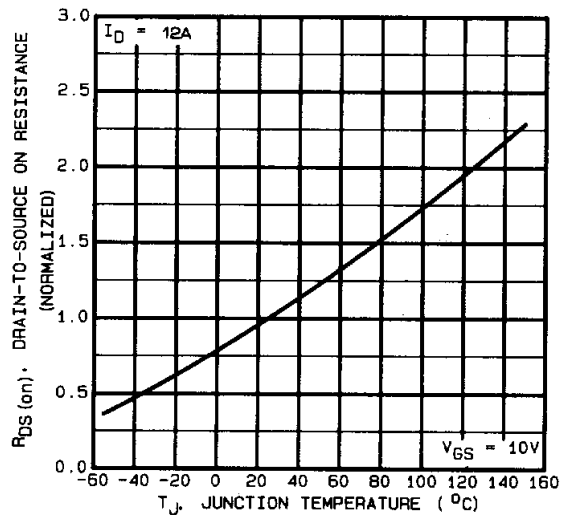


Fig 4. Normalized On-Resistance Vs. Temperature

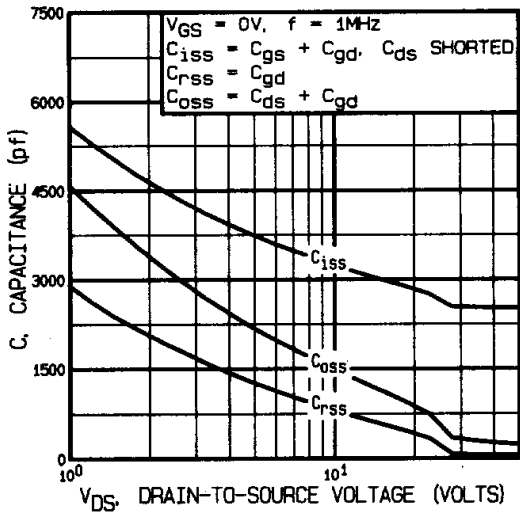


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

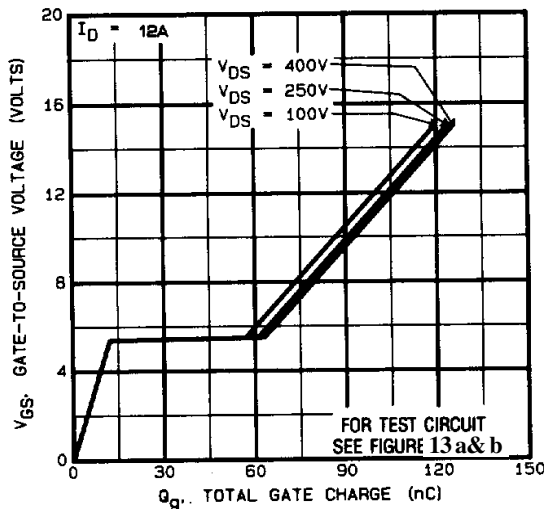


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

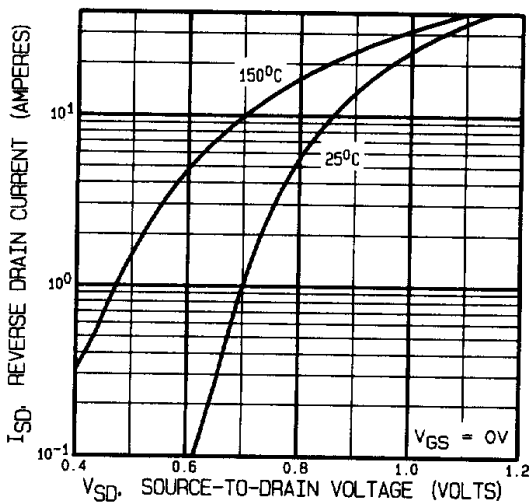


Fig 7. Typical Source-Drain Diode Forward Voltage

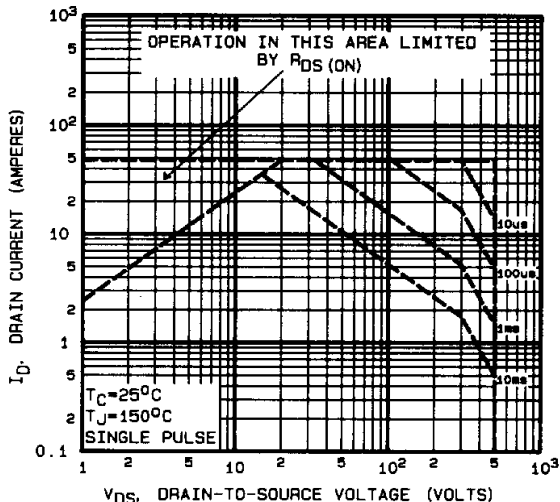


Fig 8. Maximum Safe Operating Area

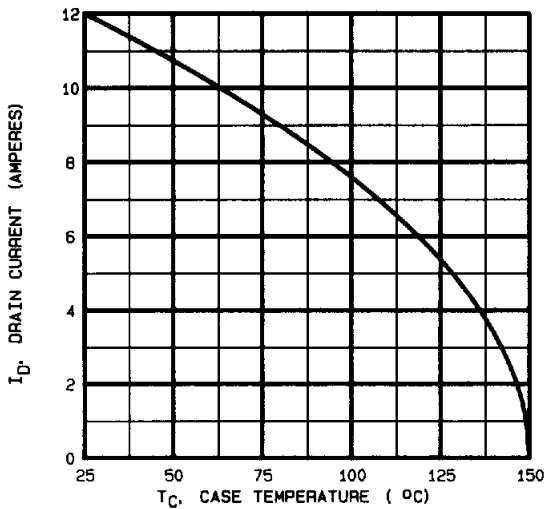


Fig 9. Maximum Drain Current Vs. Case Temperature

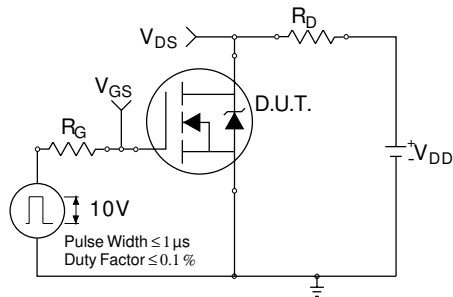


Fig 10a. Switching Time Test Circuit

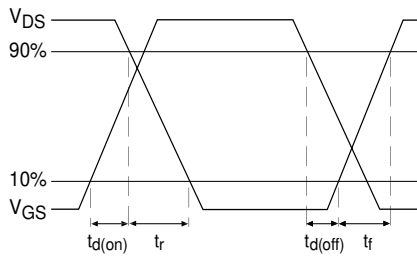


Fig 10b. Switching Time Waveforms

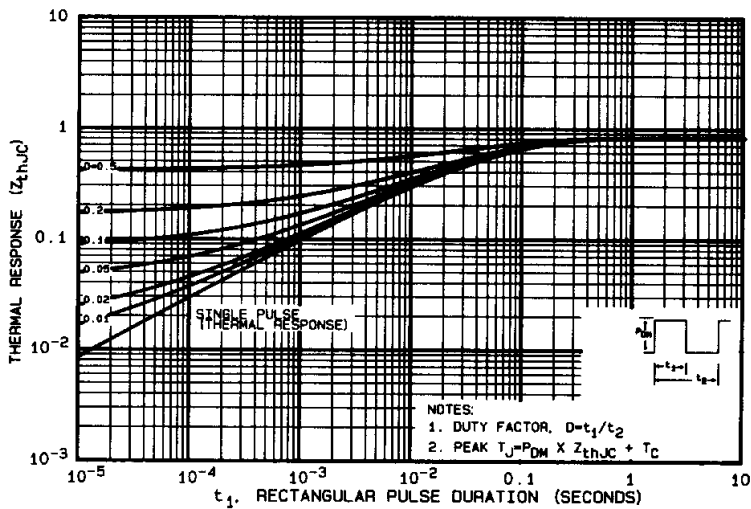


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

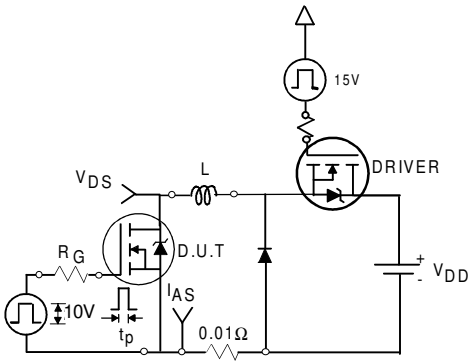


Fig 12a. Unclamped Inductive Test Circuit

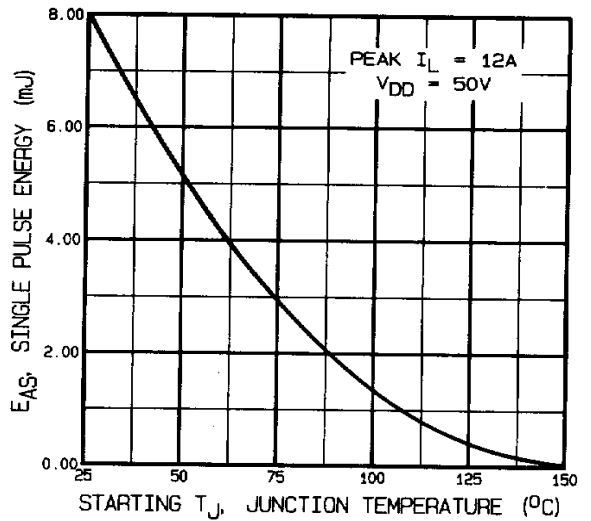


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

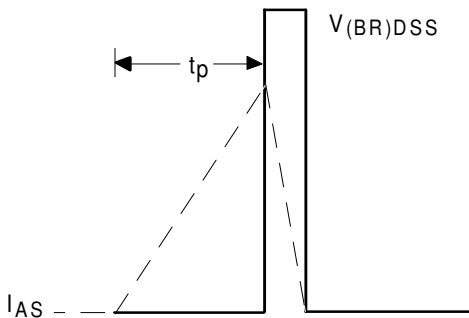


Fig 12b. Unclamped Inductive Waveforms

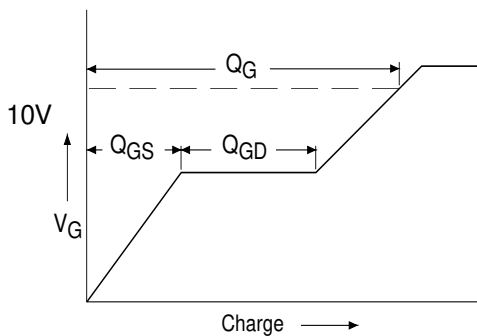


Fig 13a. Basic Gate Charge Waveform

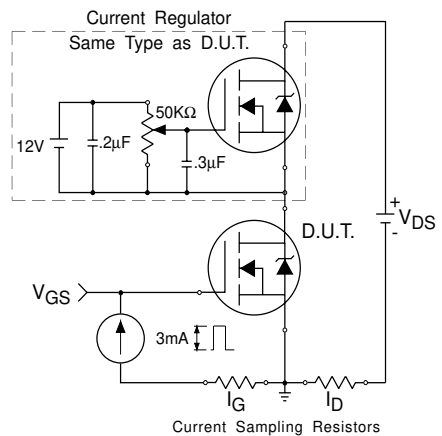
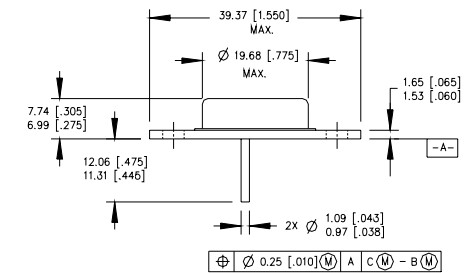


Fig 13b. Gate Charge Test Circuit

Foot Notes:

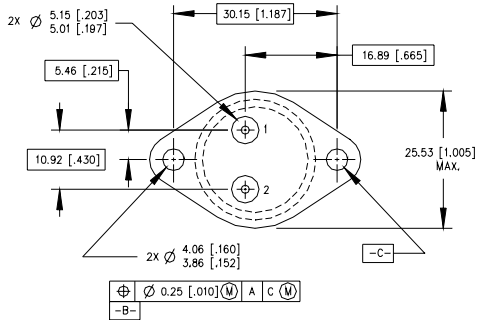
- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^{\circ}C$,
Peak $I_L = 12A$,
- ③ $I_{SD} \leq 12$, $di/dt \leq 130A/\mu s$,
 $V_{DD} \leq 500V$, $T_J \leq 150^{\circ}C$
Suggested $RG = 2.35 \Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions —TO-204AA (Modified TO-3)



PIN ASSIGNMENTS

HEXFET	SCHOTTKY	IGBT
1 - SOURCE	1 - ANODE 1	1 - GATE
2 - GATE	2 - ANODE 2	2 - EMITTER
3 - DRAIN (CASE)	3 - COMMON CATHODE (CASE)	3 - COLLECTOR (CASE)



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-204-AA.