Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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PD - 94592B

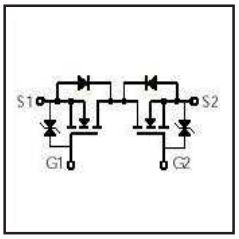
International
IOR Rectifier

IRF6156

FlipFET™ Power MOSFET

- Ultra Low $R_{SS(on)}$ per Footprint Area
- Low Thermal Resistance
- Bi-Directional N-Channel Switch
- Super Low Profile (<.8mm)
- Available Tested on Tape & Reel
- ESD Protection Diode ⑥

V_{SS}	$R_{SS(on)}$ max	I_S
20V	40mΩ@$V_{GS1,2}$ = 4.5V	±6.5
	60mΩ@$V_{GS1,2}$ = 2.5V	±5.2



Description

True chip-scale packaging is available from International Rectifier. Through the use of advanced processing techniques and a unique packaging concept, extremely low on-resistance and the highest power densities in the industry have been made available for battery and load management applications. These benefits, combined with the ruggedized device design that International Rectifier is well known for, provide the designer with an extremely efficient and reliable device.

The FlipFET™ package, is one-fifth the footprint of a comparable TSSOP-8 package and has a profile of less than .8mm. Combined with the low thermal resistance of the die level device, this makes the FlipFET™ the best device for applications where printed circuit board space is at a premium and in extremely thin application environments such as battery packs, mobile phones and PCMCIA cards.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{SS}	Source-to-Source Voltage	20	V
I_S @ T_A = 25°C	Continuous Current, V_{GS1} = V_{GS2} = 4.5V ③	±6.5	A
I_S @ T_A = 70°C	Continuous Current, V_{GS1} = V_{GS2} = 4.5V ③	±5.2	
I_{SM}	Pulsed Current ①	33	
P_D @T_A = 25°C	Power Dissipation ③	2.5	W
P_D @T_A = 70°C	Power Dissipation ③	1.6	
	Linear Derating Factor	20	mW/°C
V_{GS}	Gate-to-Source Voltage	±12	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	50	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-PCB	35	—	

06/15/06

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)SSS}$	Source-to-Source Breakdown Voltage	20	—	—	V	V_{GS}=0V, I_S=250µA,See Fig. 23a&b
$\Delta V_{(BR)SSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	16	—	mV/°C	Reference to 25°C,I_S=1mA,Fig.23a&b
$R_{SS(on)}$	Static Source-to-Source On-Resistanc	—	27	40	mΩ	$V_{GS1,2}$ = 4.5V, I_S = 6.5A ② Fig.11a&b
		—	43	60		$V_{GS1,2}$ = 2.5V, I_S = 5.2A ②
$V_{GS(th)}$	Gate Threshold Voltage	0.45	—	1.2	V	V_{SS} = V_{GS}, I_S = 250µA ② Fig. 10a&b
gfs	Forward Transconductance	18	—	—	S	V_{SS} = 10V, I_S = 6.5A, See Fig. 4
I_{SSS}	Zero Gate Voltage Source Current	—	—	1.0	µA	V_{SS} = 20V, V_{GS} = 0V,See Fig.23a&b
		—	—	25		V_{SS} = 16V, V_{GS} = 0V, T_J = 125°C
		—	50	—	nA	V_{SS} = 4.5V, V_{GS} = 0V, TJ = 25°C
		—	100	—		V_{SS} = 4.5V, V_{GS} = 0V, T_J = 60°C
I_{GSS}	Gate-to-Source Forward Leakage	—	8.0	20	µA	V_{GS} = 12V, See Fig. 22
	Gate-to-Source Reverse Leakage	—	-8.0	-20		V_{GS} = -12V
	Gate-to-Source Forward Leakage	—	0.20	0.5	µA	V_{GS} = 4.5V
	Gate-to-Source Reverse Leakage	—	-0.20	-0.5		V_{GS} = -4.5V
Q_g	Total Gate Charge	—	12	18		I_S = 6.5A
Q_{gs}	Gate-to-Source Charge	—	1.6	2.4	nC	V_{SS} = 16V
Q_{G1-S2}	Miller Charge	—	4.4	6.6		V_{GS} = 5.0V, See Fig. 14a,b&c
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—		V_{SS} = 10V
t_r	Rise Time	—	13	—	ns	I_S = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	33	—		R_G = 3.0Ω
t_f	Fall Time	—	26	—		V_{GS} = 5.0V, See Fig. 21a,b&c
C_{iss}	Input Capacitance	—	950	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	210	—	pF	V_{SS} = 15V
C_{rss}	Reverse Transfer Capacitance	—	150	—		f = 1.0KHz, See Fig. 13a,b,c,d,e&f
V_{ssf}	Source-to-Source Diode Forward Voltage, One Device On	—	—	1.2	V	See Fig. 17a&b I_{ss} = 2.5A

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 400µs; duty cycle ≤ 2%. Gate voltage applied to both gates.

③ When mounted on 1 inch square 2oz copper on FR-4.

④ Figures 1, 2 and 3: One Fet is biased with V_{GS} = 9.0V and curves show response of the second FET. See Fig.4.

⑤ Figures 5, 6 and 7: G1 and G2 are shorted. See Fig.9a&b.

⑥ The diode connected between the gate and source serves only as protection against ESD. No gate over voltage rating is implied.

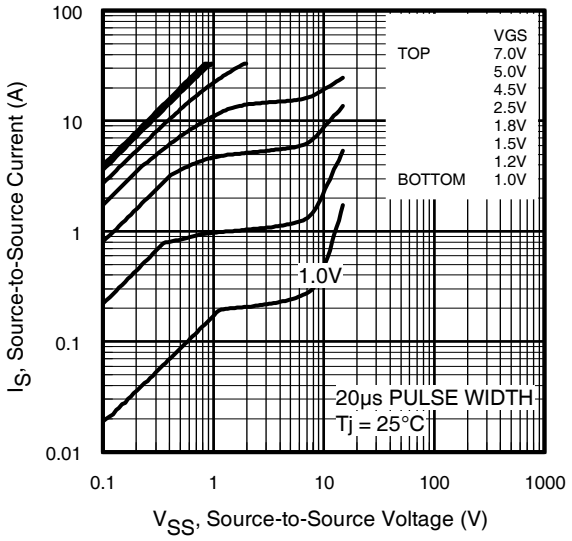


Fig 1. Typical Output Characteristics. ④

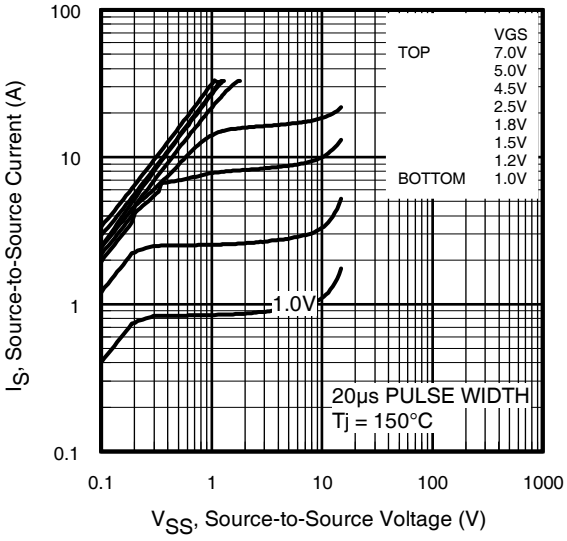


Fig 2. Typical Output Characteristics. ④

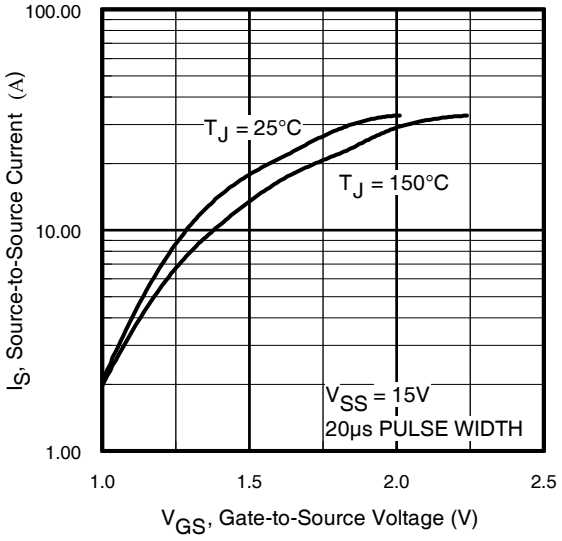


Fig 3. Typical Transfer Characteristics. ④

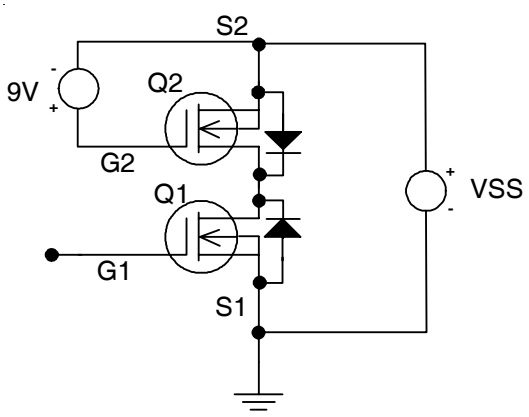


Fig 4. Output and Transfer Test Circuit.

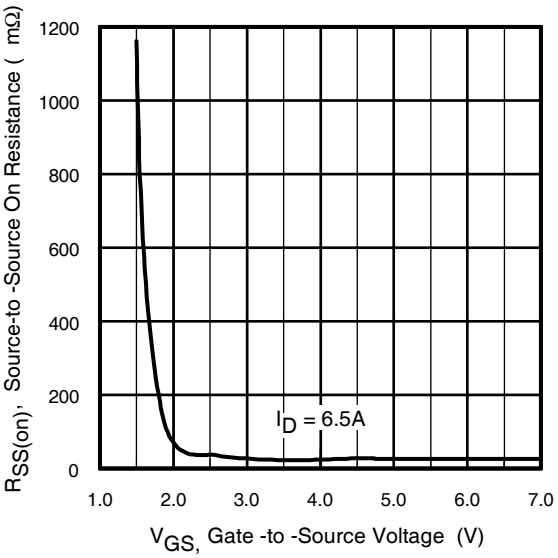


Fig 5. Typical On-Resistance vs. Gate Voltage. ⑤

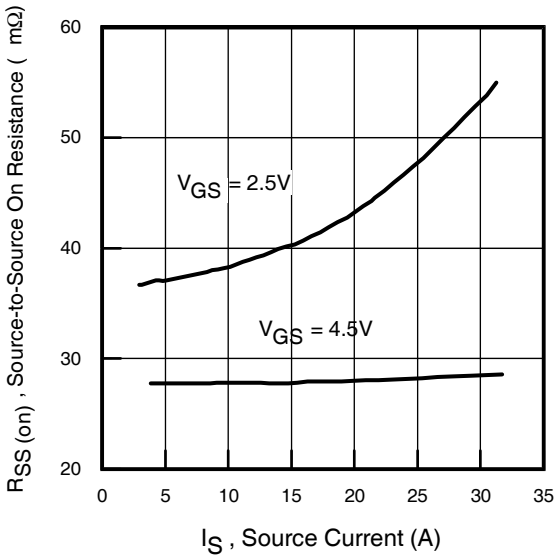


Fig 6. Typical On-Resistance vs. Source Current. ⑤

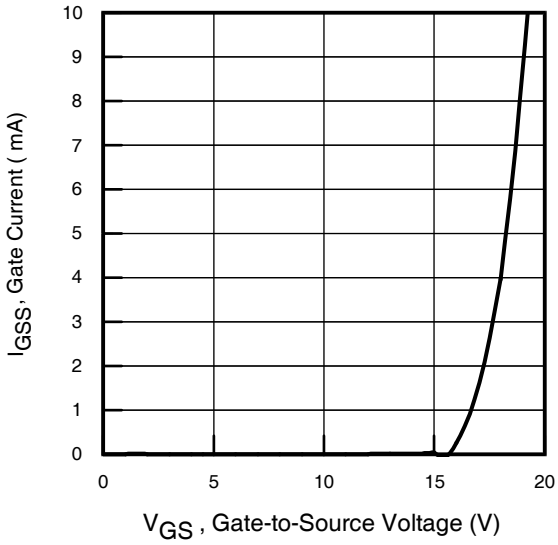


Fig 7a. Gate-Current vs. Gate-Source Voltage

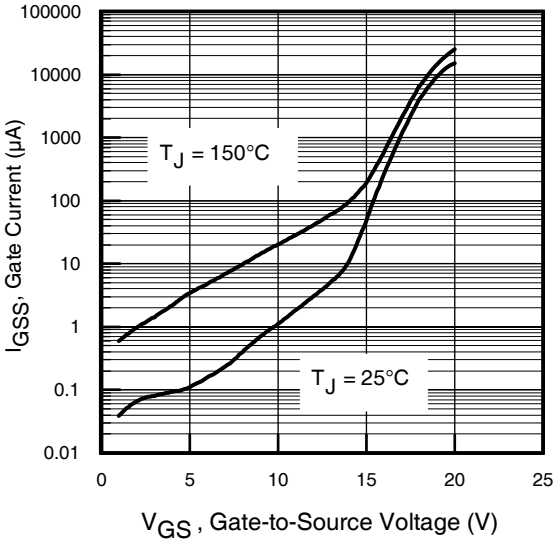


Fig 7b. Gate-Current vs. Gate-Source Voltage

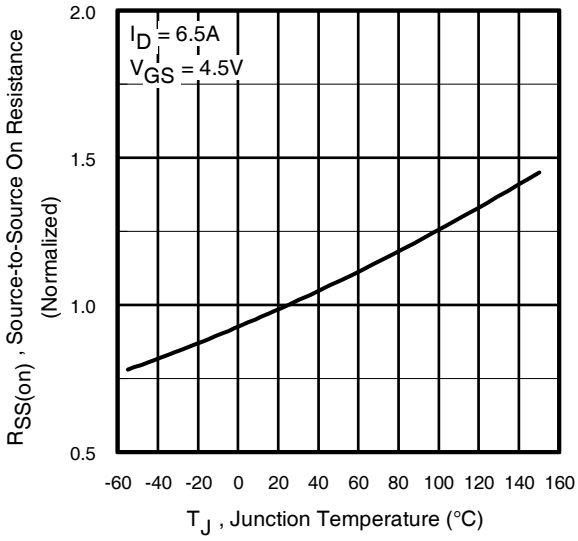


Fig 8. Normalized On-Resistance vs. Temperature. ⑤

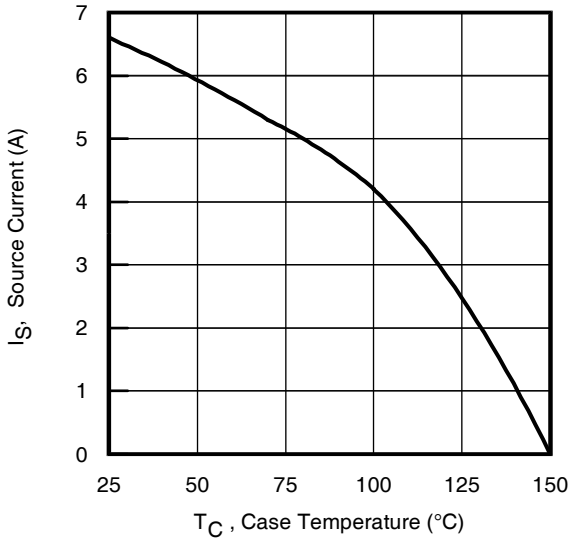


Fig 9. Maximum Source Current vs. Case Temperature.

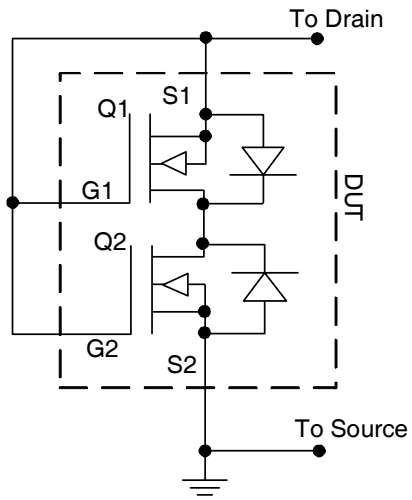


Fig 10a. $V_{GS(th)}$ is symmetrical and can be measured when connected as shown on figure 10a.

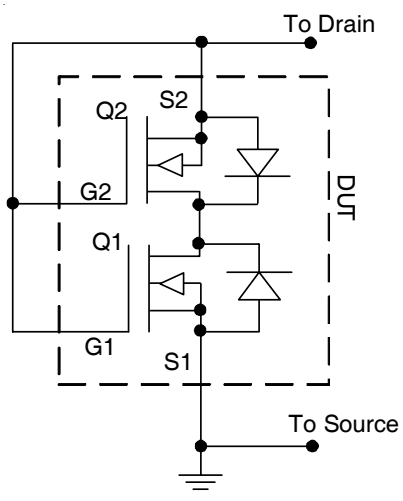


Fig 10b. $V_{GS(th)}$ is symmetrical and can be measured when connected as shown on figure 10b.

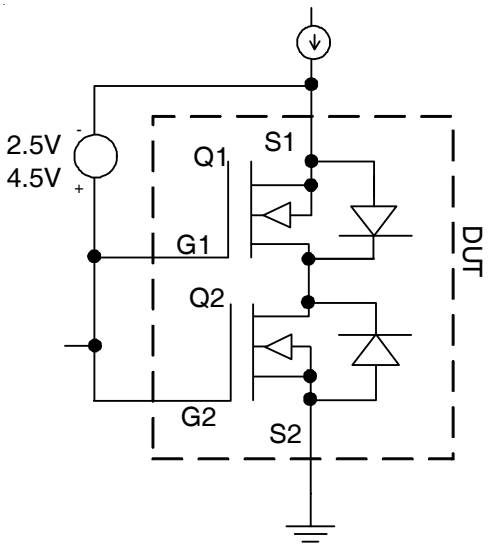


Fig 11a

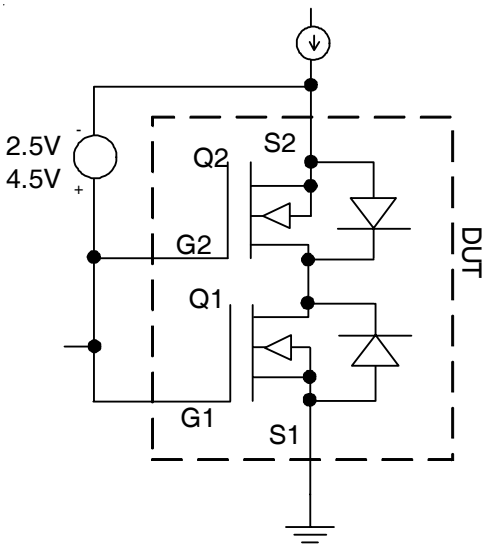


Fig 11b

$R_{SS(on)}$ is symmetrical and can be measured when connected as shown in either figures 11a or 11b.

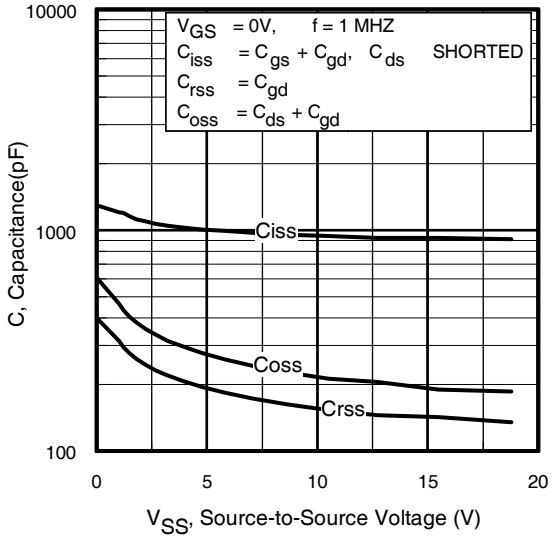


Fig 12. Typical Capacitance vs. Source-to-Source Voltage.

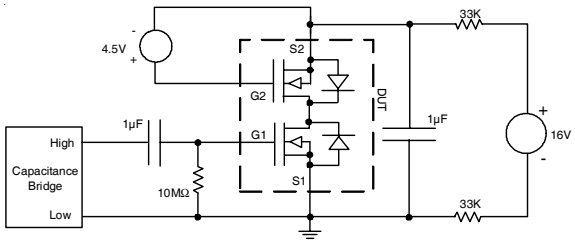


Fig 13a

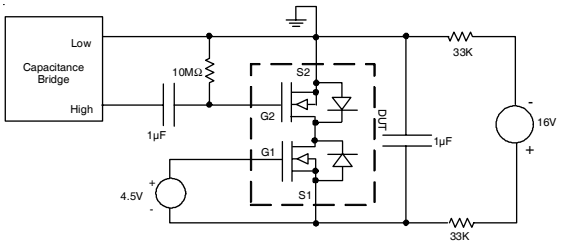


Fig 13b

Ciss capacitance is symmetrical and can be measured as shown either in figures 13a or 13b.

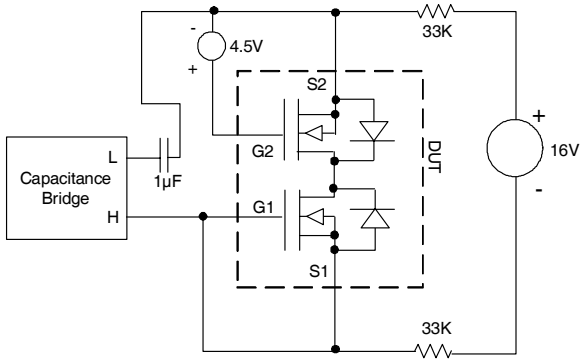


Fig 13c

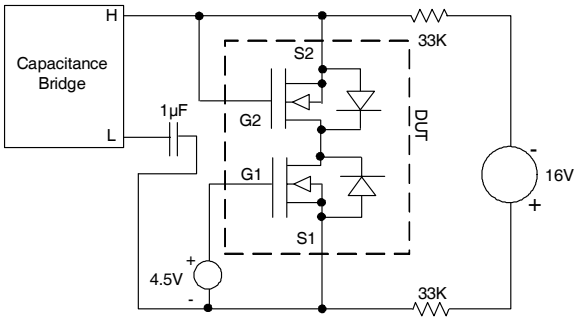


Fig 13d

Coss capacitance is symmetrical and can be measured as shown either in figures 13c or 13d.

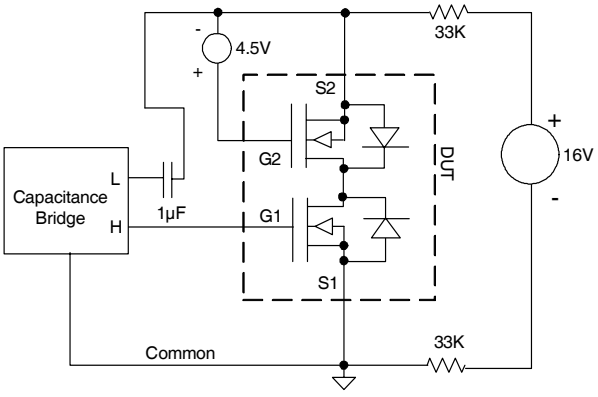


Fig 13e

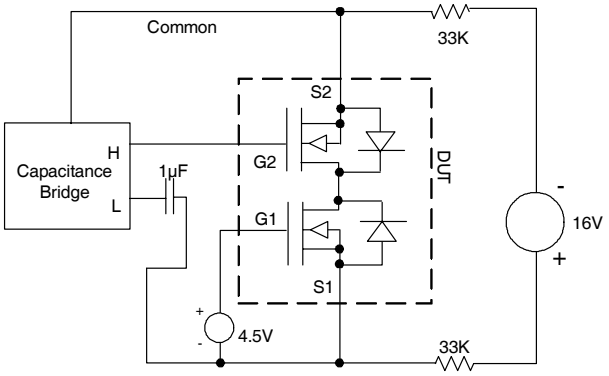


Fig 13f

Crss capacitance is symmetrical and can be measured as shown either in figures 13e or 13f.

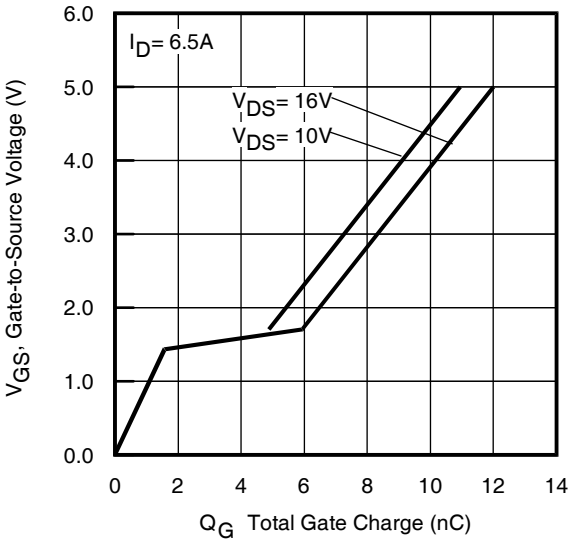


Fig 14. Typical Gate Charge vs. Gate-to-Source Voltage.

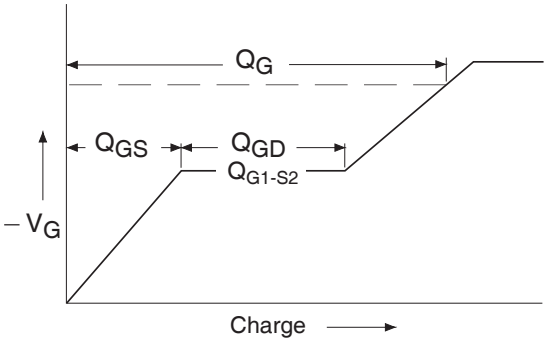


Fig 14a. Basic Gate Charge Waveform.

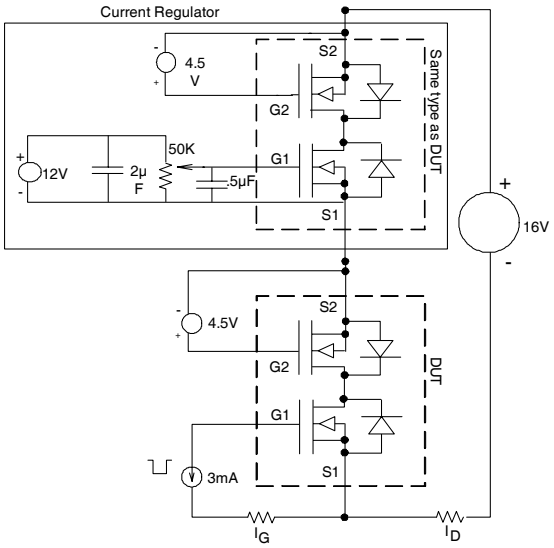


Fig 14b

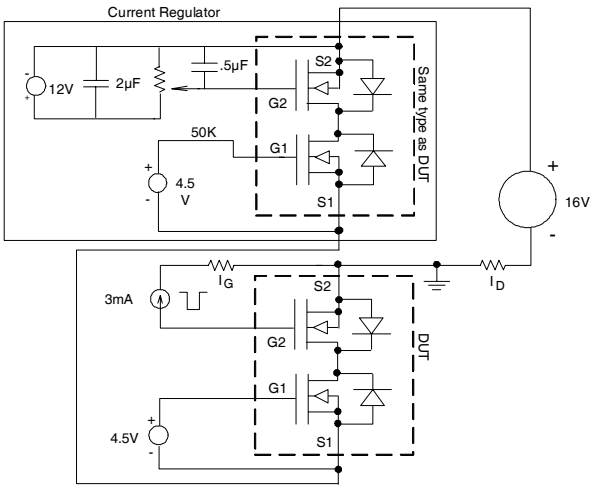


Fig 14c

Gate Charge is symmetrical and can be measured as shown in either figures 14b or 14c.

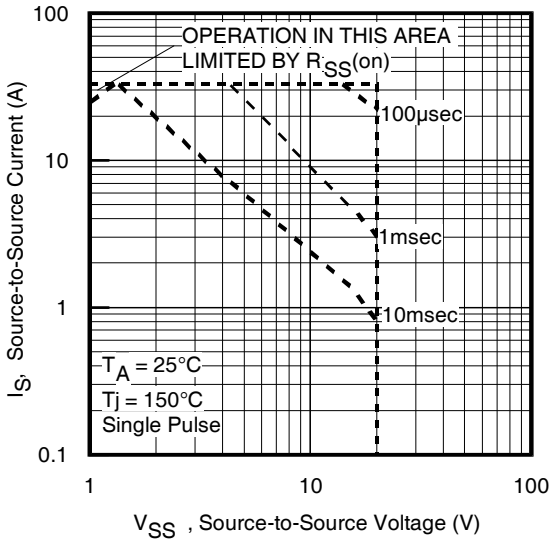


Fig 15. Maximum Safe Operating Area.

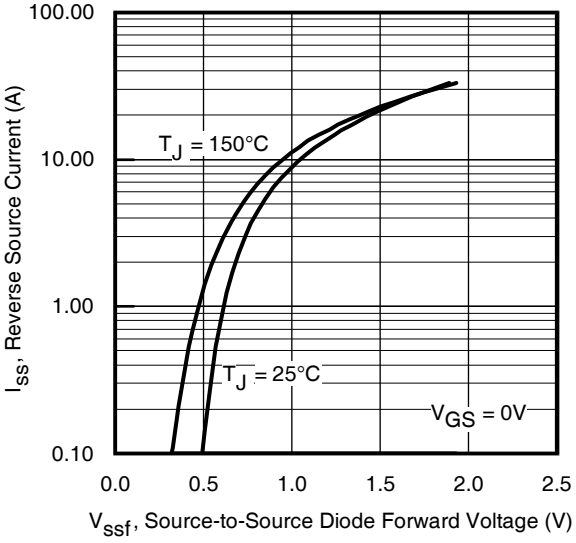


Fig 16. Typical Source-Source Diode Forward Voltage.
(See Fig.17a&b for Connection)

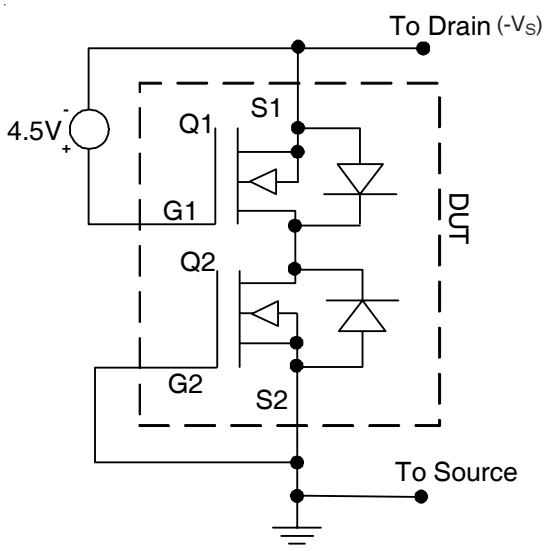


Fig 17a

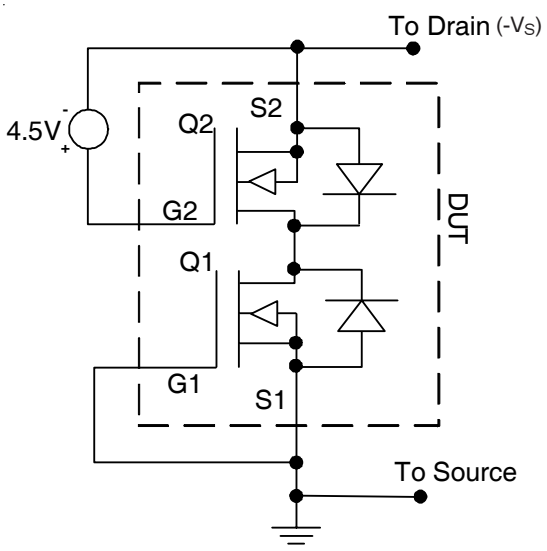


Fig 17b

V_{ssf} is symmetrical and can be measured when connected as shown either in figures 17a or 17b.

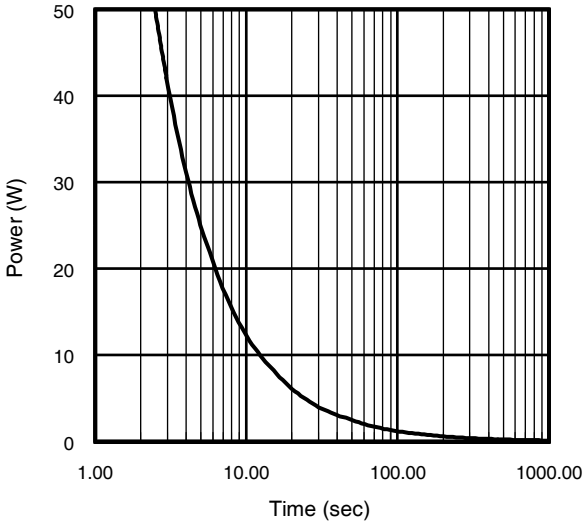


Fig 18. Typical Power vs. Time.

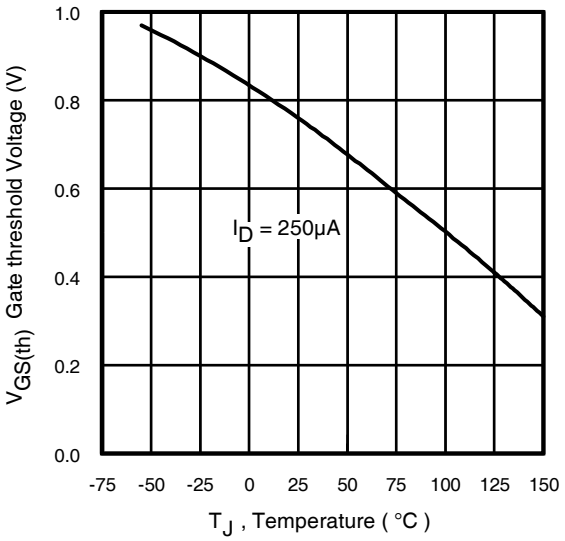


Fig 19. Threshold Voltage vs. Temperature.

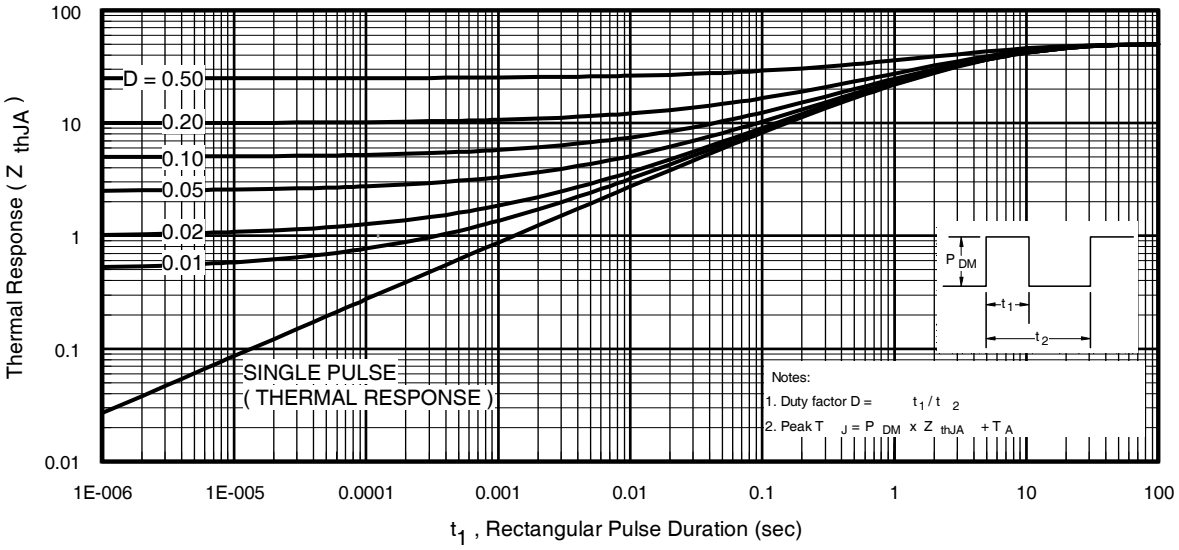


Fig 20. Typical Effective Transient Thermal Impedance, Junction-to-Ambient.

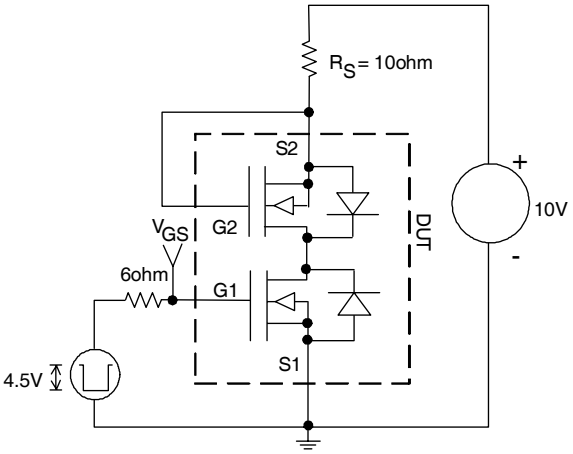


Fig 21a

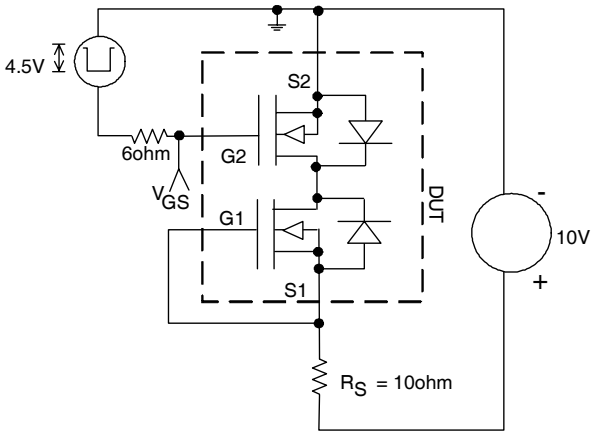


Fig 21b

Switching times are symmetrical and can be measured as shown in either figures 21a or 21b.

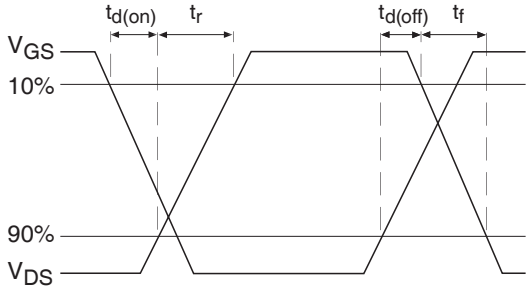


Fig 21c. Switching Time Waveforms.

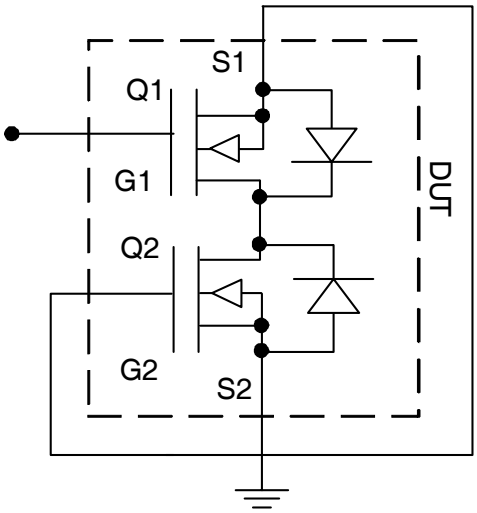


Fig 22a

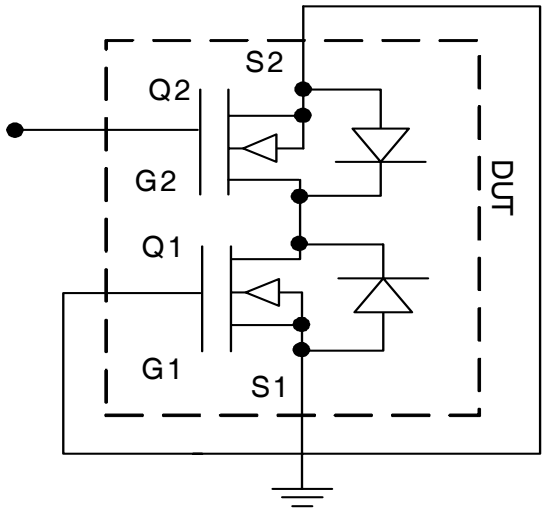


Fig 22b

I_{GSS} Test Connection

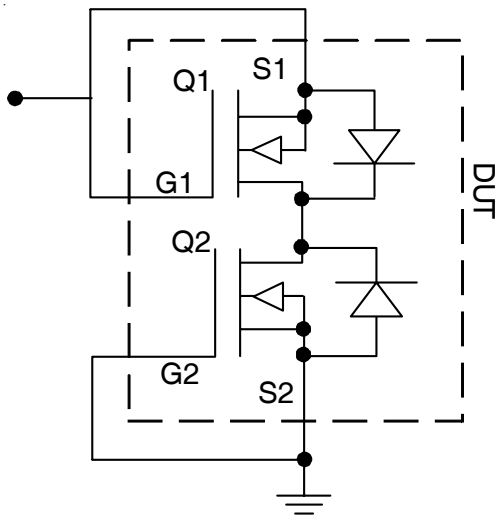


Fig 23a

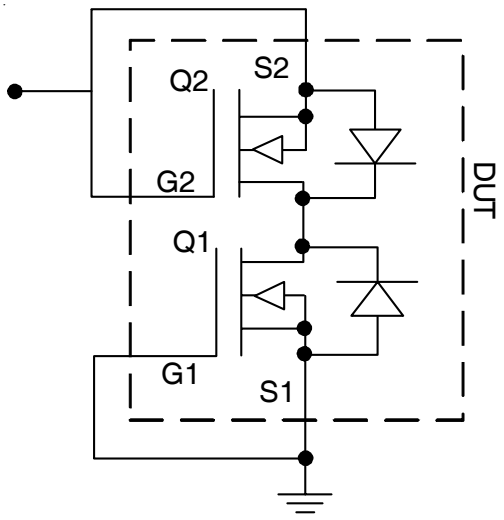
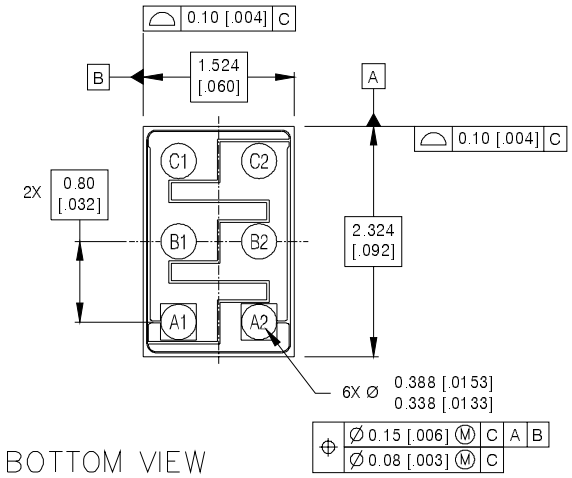


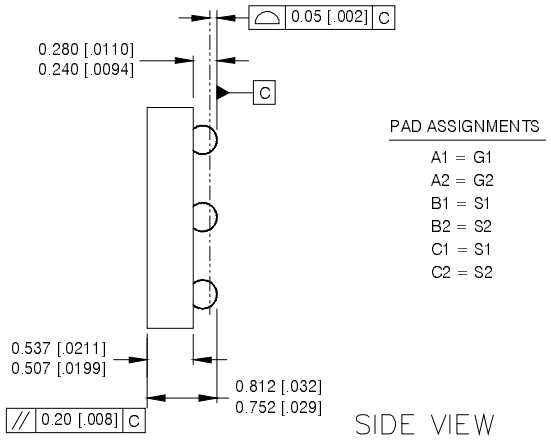
Fig 23b

I_{SSS} and $V_{(BR)SSS}$ are symmetrical and can be measured when connected either as figures 23a or 23b.

Bi-Directional MOSFET Pinout Outline Dimension and Tape and Reel Information
Drawing No. 01-0115



BOTTOM VIEW

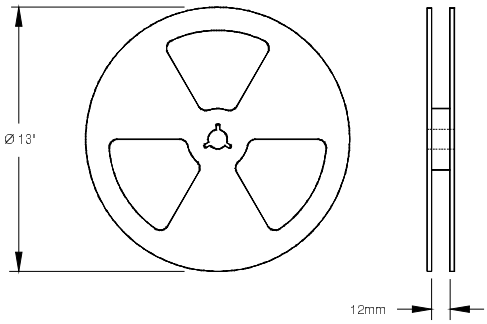


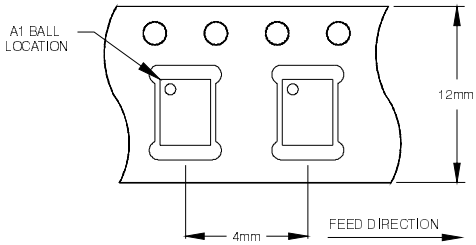
SIDE VIEW

PAD ASSIGNMENTS

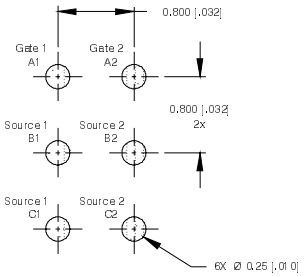
A1 = G1
A2 = G2
B1 = S1
B2 = S2
C1 = S1
C2 = S2

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].





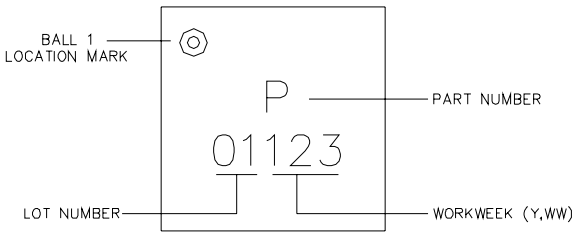
NOTES:
1. TAPE AND REEL OUTLINE CONFORMS TO EIA-481 & EIA-541.



RECOMMENDED FOOTPRINT

FlipFET™ Part Marking Information

LAYOUT MARKING A



Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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