PROVISIONAL

PD - 97204

IRF6691PbF
IRF6691TRPbF

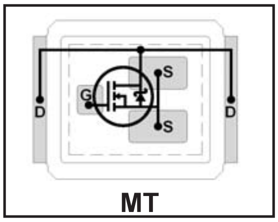
DirectFET™ Power MOSFET ②

- RoHs Compliant ①
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①

Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	$R_{DS(on)}$	$R_{DS(on)}$
20V max	±12V max	1.2mΩ@ 10V	1.8mΩ@ 4.5V

$Q_{g\ tot}$	Q_{gd}	Q_{gs2}	Q_{rr}	Q_{oss}	$V_{gs(th)}$
47nC	15nC	4.4nC	26nC	30nC	2.0V




DirectFET™ ISOMETRIC

Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST		MQ	MX	MT				

Description

The IRF6691PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. Application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6691PbF balances industry leading on-state resistance while minimizing gate charge along with ultra low package inductance to reduce both conduction and switching losses. This part contains an integrated Schottky diode to reduce the Qrr of the body drain diode further reducing the losses in a Synchronous Buck circuit. The reduced losses make this product ideal for high frequency/high efficiency DC-DC converters that power high current loads such as the latest generation of microprocessors. The IRF6691PbF has been optimized for parameters that are critical in synchronous buck converter's SyncFET sockets.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	±12	
I_D @ $T_A = 25°C$	Continuous Drain Current, V_{GS} @ 10V ③	32	A
I_D @ $T_A = 70°C$	Continuous Drain Current, VGS @ 10V ③	26	
I_D @ $T_C = 25°C$	Continuous Drain Current, V_{GS} @ 10V ④	180 ⑧	
I_{DM}	Pulsed Drain Current ⑤	260	
E_{AS}	Single Pulse Avalanche Energy⑥	230	mJ
I_{AR}	Avalanche Current ⑤	26	A

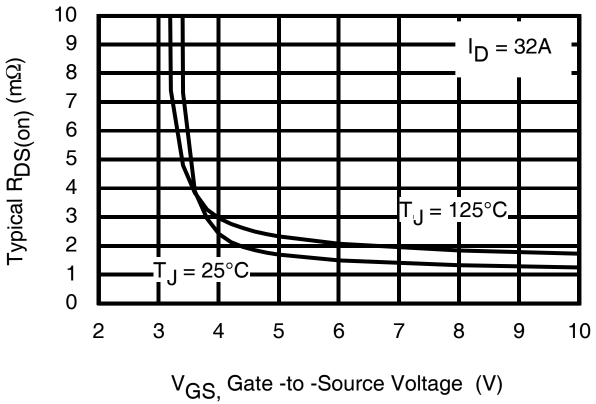


Fig 1. Typical On-Resistance vs. Gate-to-Source Voltage

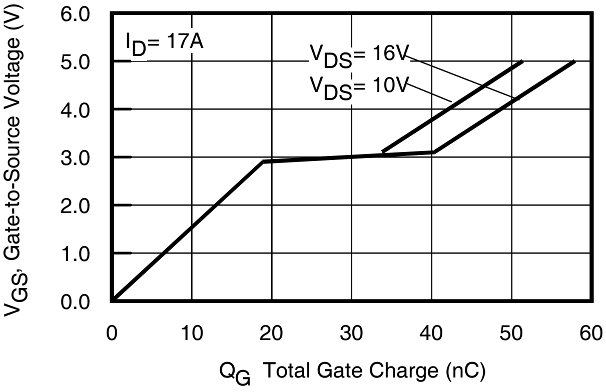


Fig 2. Total Gate Charge vs. Gate-to-Source Voltage

Notes:

① Click on this section to link to the appropriate technical paper.

② Click on this section to link to the DirectFET Website.

③ Surface mounted on 1 in. square Cu board, steady state.

④ T_C measured with thermocouple mounted to top (Drain) of part.

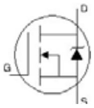
⑤ Repetitive rating; pulse width limited by max. junction temperature.

⑥ Starting $T_J = 25°C$, $L = 0.72mH$, $R_G = 25Ω$, $I_{AS} = 26A$.

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	12	—	mV/°C	Reference to 25°C, I_D = 10mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.8	2.5	mΩ	V_{GS} = 4.5V, I_D = 12A ⑦
		—	1.2	1.8		V_{GS} = 10V, I_D = 15A ⑦
$V_{GS(th)}$	Gate Threshold Voltage	1.6	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.1	—	mV/°C	I_D = 10mA, reference to 25°C
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.4	mA	V_{DS} = 20V, V_{GS} = 0V
		—	—	500	μA	V_{DS} = 16V, V_{GS} = 0V
		—	—	5	mA	V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 12V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -12V
gfs	Forward Transconductance	110	—	—	S	V_{DS} = 10V, I_D = 26A
Q_g	Total Gate Charge	—	47	71	nC	
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	14	—		V_{DS} = 10V
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	4.4	—		V_{GS} = 4.5V
Q_{gd}	Gate-to-Drain Charge	—	15	—		I_D = 17A
Q_{godr}	Gate Charge Overdrive	—	14	—		See Fig. 14
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	19	—		
Q_{oss}	Output Charge	—	30	—	nC	V_{DS} = 10V, V_{GS} = 0V
R_G	Gate Resistance	—	0.60	1.5	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	V_{DD} = 16V, V_{GS} = 4.5V ⑦
t_r	Rise Time	—	95	—		I_D = 26A
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		Clamped Inductive Load
t_f	Fall Time	—	10	—		See Fig. 15 & 16
C_{iss}	Input Capacitance	—	6580	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	2070	—		V_{DS} = 10V
C_{rss}	Reverse Transfer Capacitance	—	840	—		f = 1.0MHz

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	200⑧	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	260		
V_{SD}	Diode Forward Voltage	—	—	0.65	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V ⑦
t_{rr}	Reverse Recovery Time	—	32	48	ns	T_J = 25°C, I_F = 25A
Q_{rr}	Reverse Recovery Charge	—	26	39	nC	di/dt = 100A/μs ⑦ See Fig. 17

Notes:

⑤ Repetitive rating; pulse width limited by max. junction temperature.

⑦ Pulse width ≤ 400μs; duty cycle ≤ 2%.

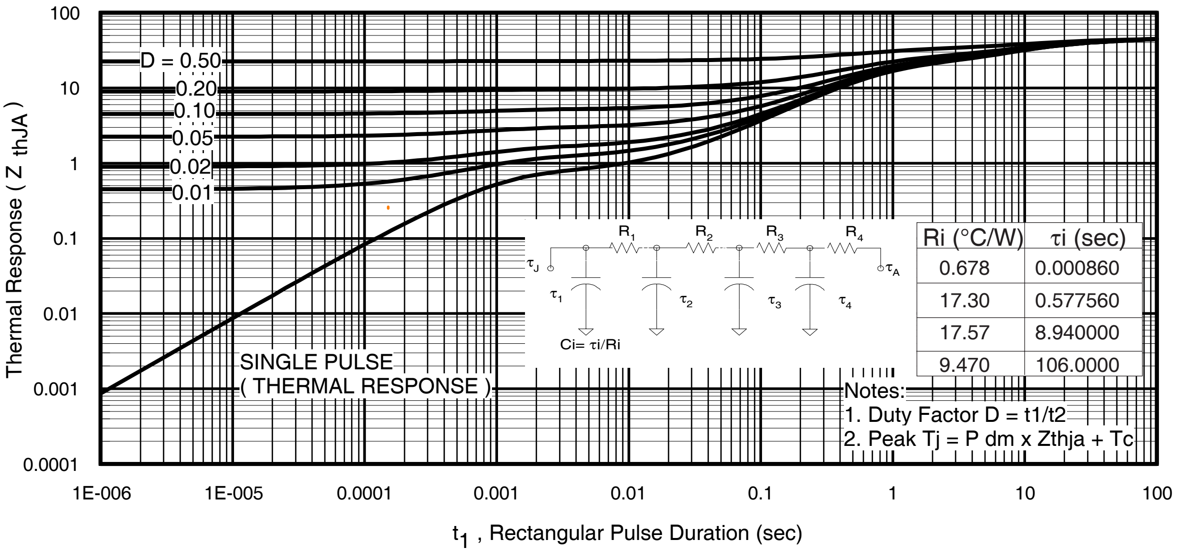
⑧ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 150A.

Absolute Maximum Ratings

P_D @T_A = 25°C	Power Dissipation ③	2.8	W
P_D @T_A = 70°C	Power Dissipation ③	1.8	
P_D @T_C = 25°C	Power Dissipation ④	89	
T_P	Peak Soldering Temperature	270	°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③ ⓫	–––	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑨ ⓫	12.5	–––	
$R_{\theta JA}$	Junction-to-Ambient ⑩ ⓫	20	–––	
$R_{\theta JC}$	Junction-to-Case ④ ⓫	–––	1.4	
$R_{\theta J\text{-}PCB}$	Junction-to-PCB Mounted	1.0	–––	
	Linear Derating Factor ③	0.022		W/°C



Ri (°C/W)	τi (sec)
0.678	0.000860
17.30	0.577560
17.57	8.940000
9.470	106.0000

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthja + Tc

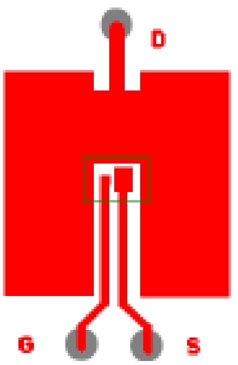
Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Notes:

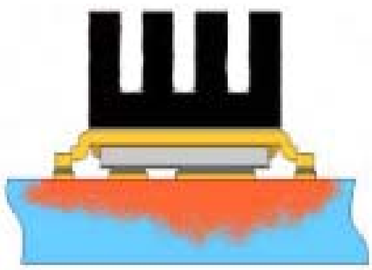
⑨ Used double sided cooling , mounting pad.

⑩ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

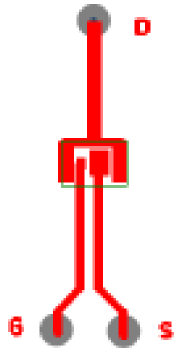
⓫ R_θ is measured at T_J of approximately 90°C.



③ Surface mounted on 1 in. square Cu (still air).



⑨ Mounted to a PCB with small clip heatsink (still air)



⑩ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

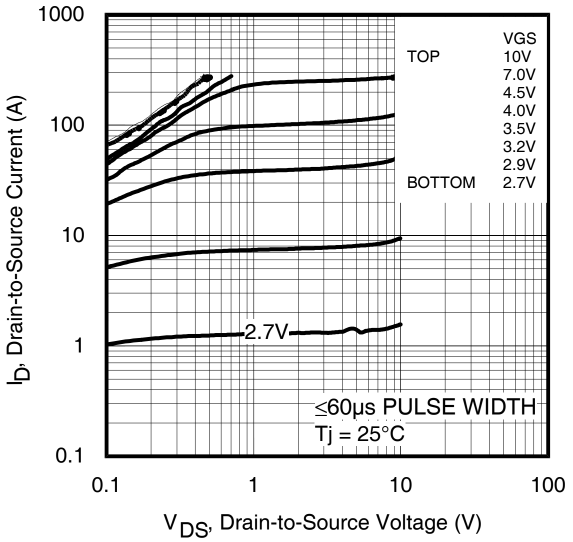


Fig 4. Typical Output Characteristics

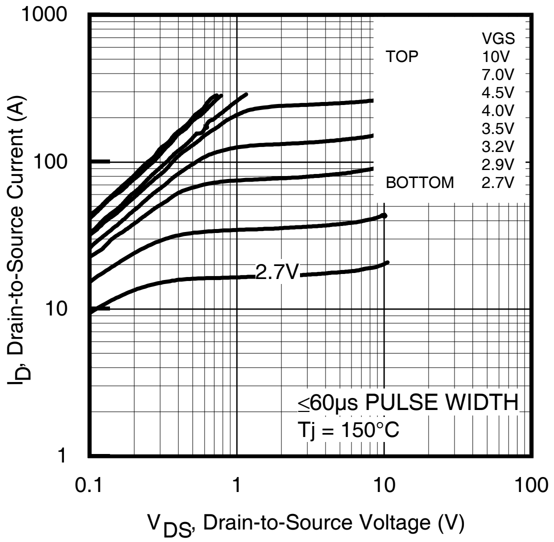


Fig 5. Typical Output Characteristics

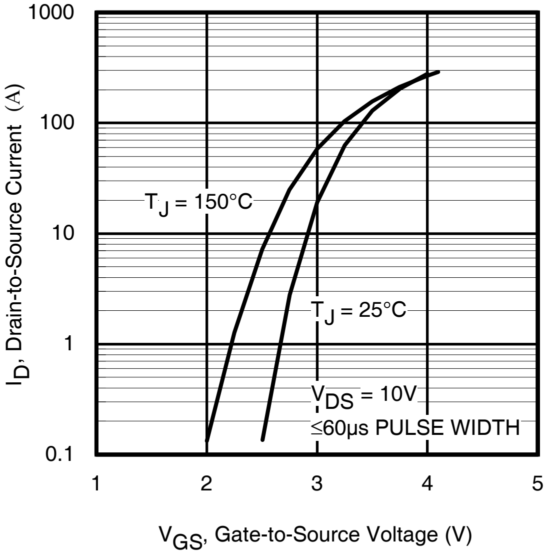


Fig 6. Typical Transfer Characteristics

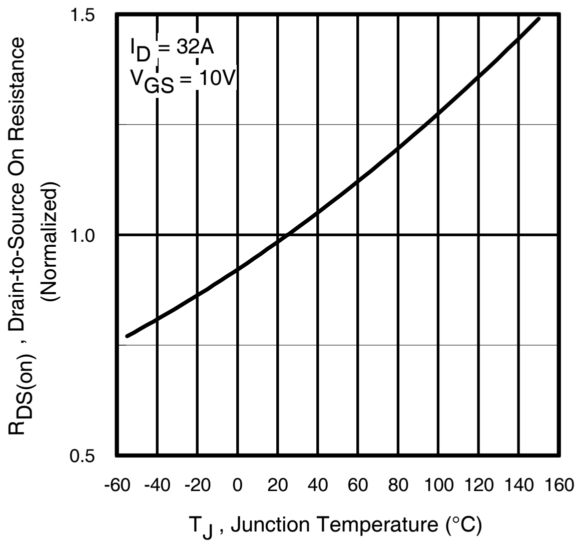


Fig 7. Normalized On-Resistance vs. Temperature

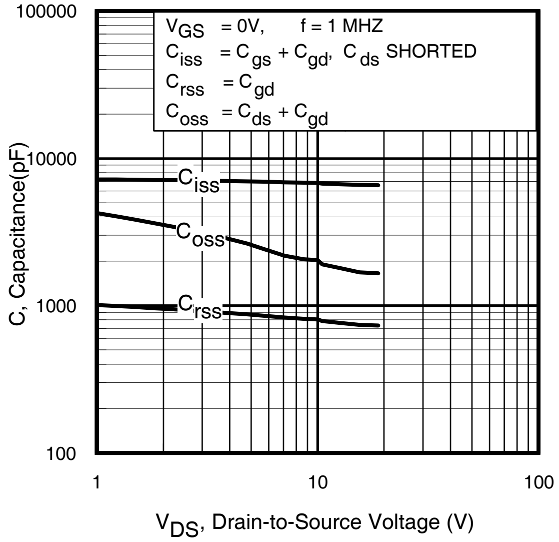


Fig 8. Typical Capacitance vs.Drain-to-Source Voltage

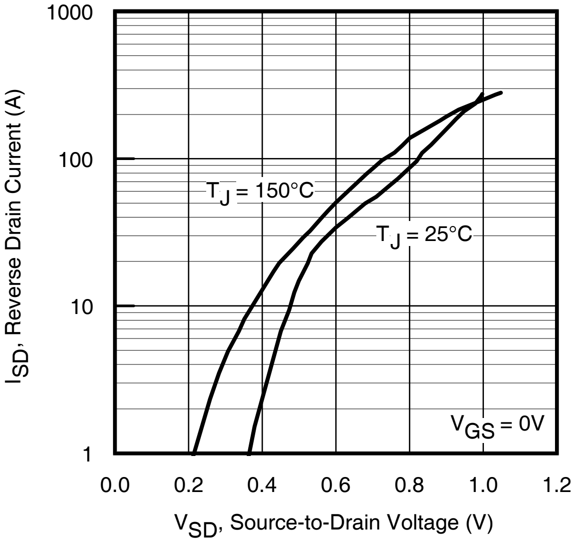


Fig 9. Typical Source-Drain Diode Forward Voltage

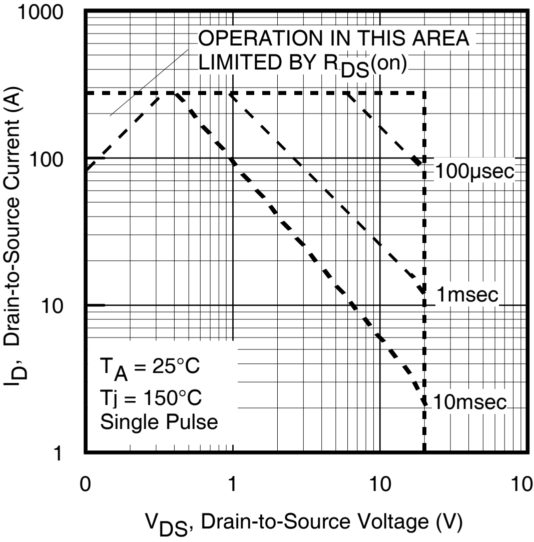


Fig10. Maximum Safe Operating Area

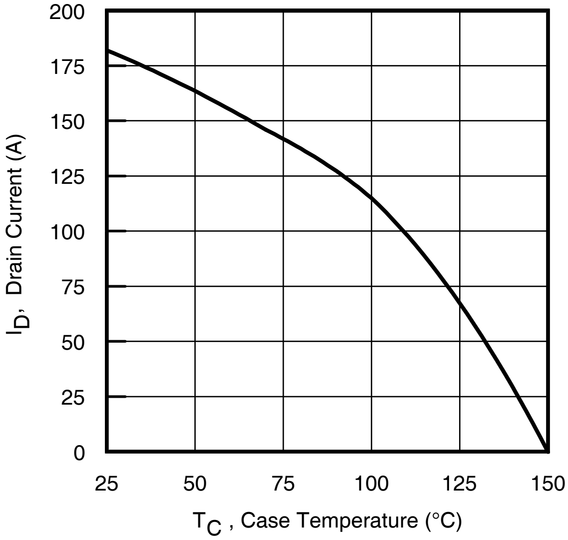


Fig 11. Maximum Drain Current vs. Case Temperature

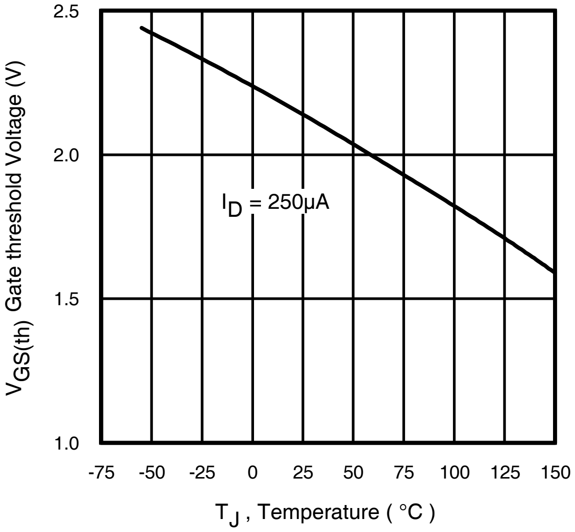


Fig 12. Threshold Voltage vs. Temperature

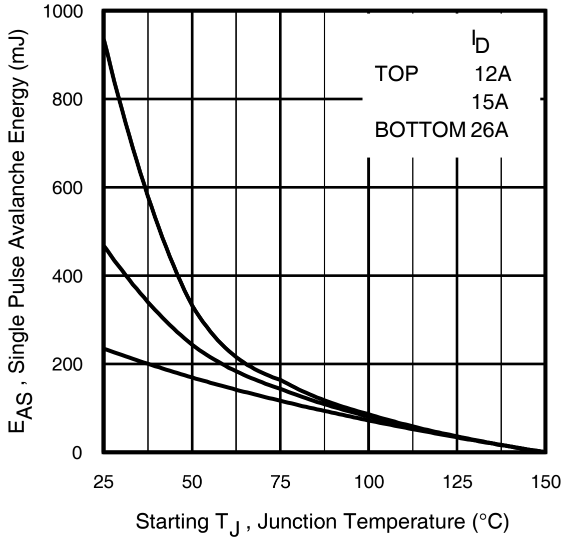


Fig 13. Maximum Avalanche Energy vs. Drain Current

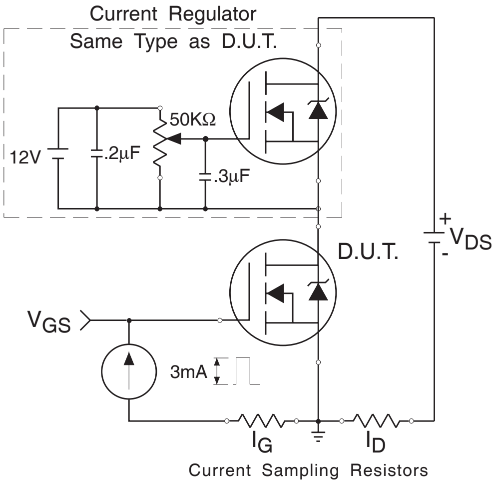


Fig 14a. Gate Charge Test Circuit

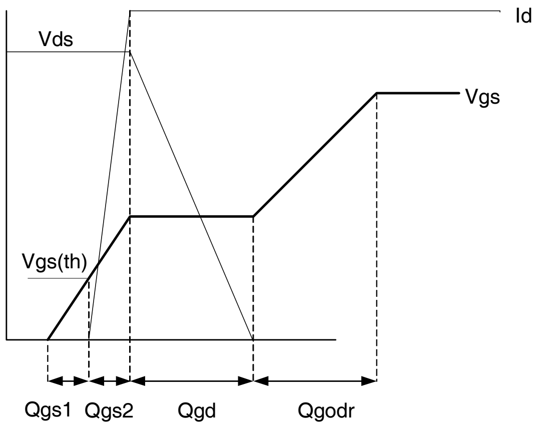


Fig 14b. Gate Charge Waveform

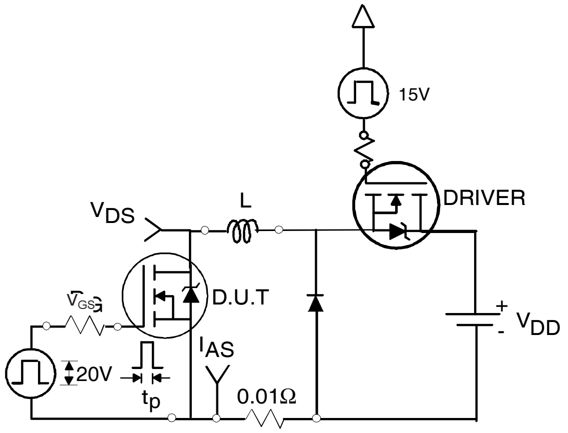


Fig 15a. Unclamped Inductive Test Circuit

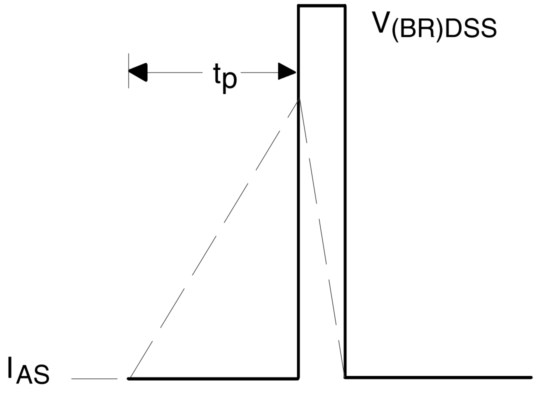


Fig 15b. Unclamped Inductive Waveforms

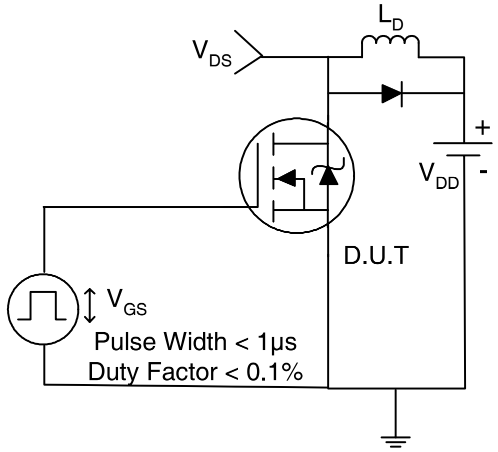


Fig 16a. Switching Time Test Circuit

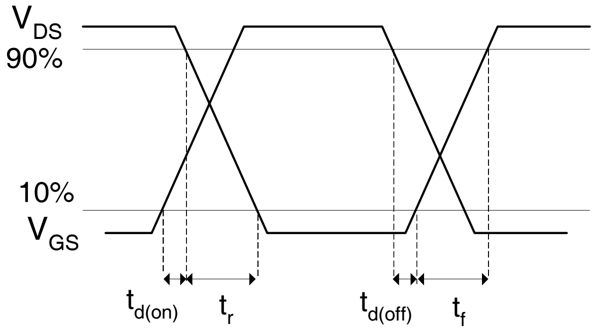


Fig 16b. Switching Time Waveforms

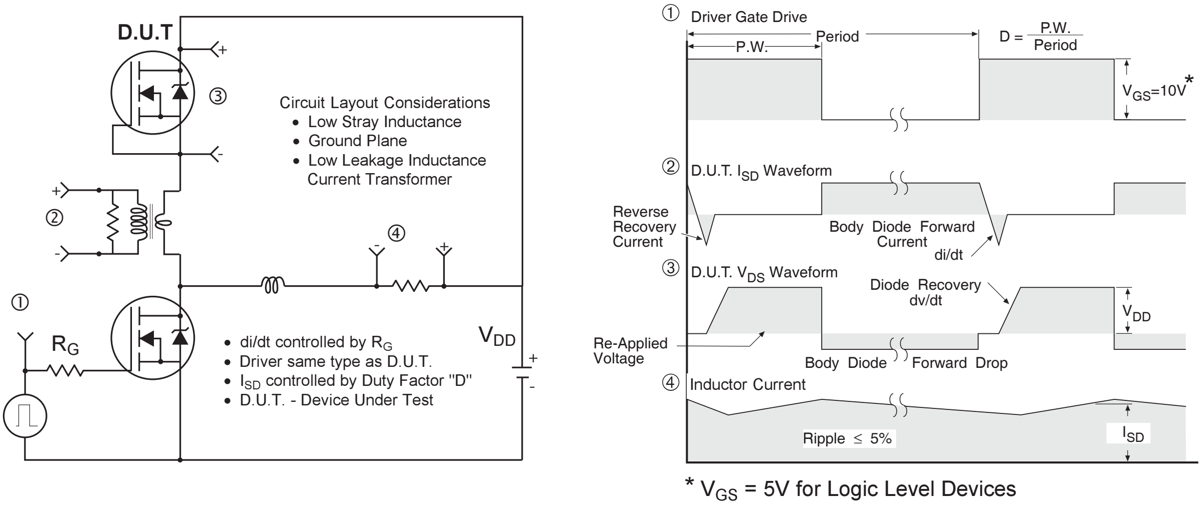
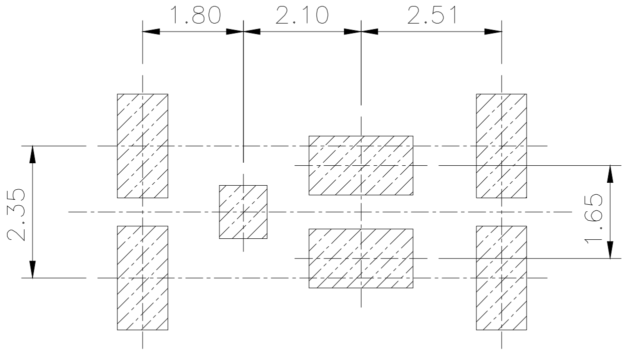


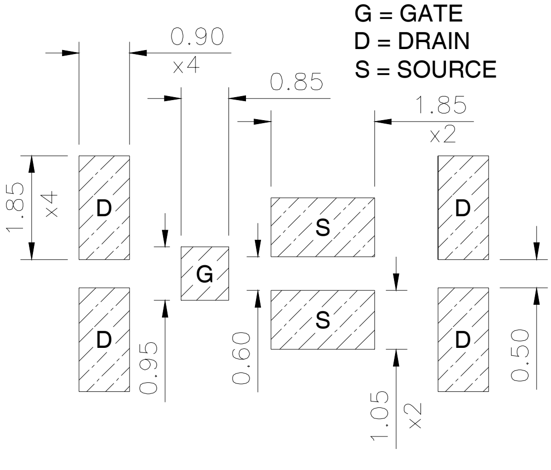
Fig 17. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

DirectFET™ Board Footprint, MT Outline ③ (Medium Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

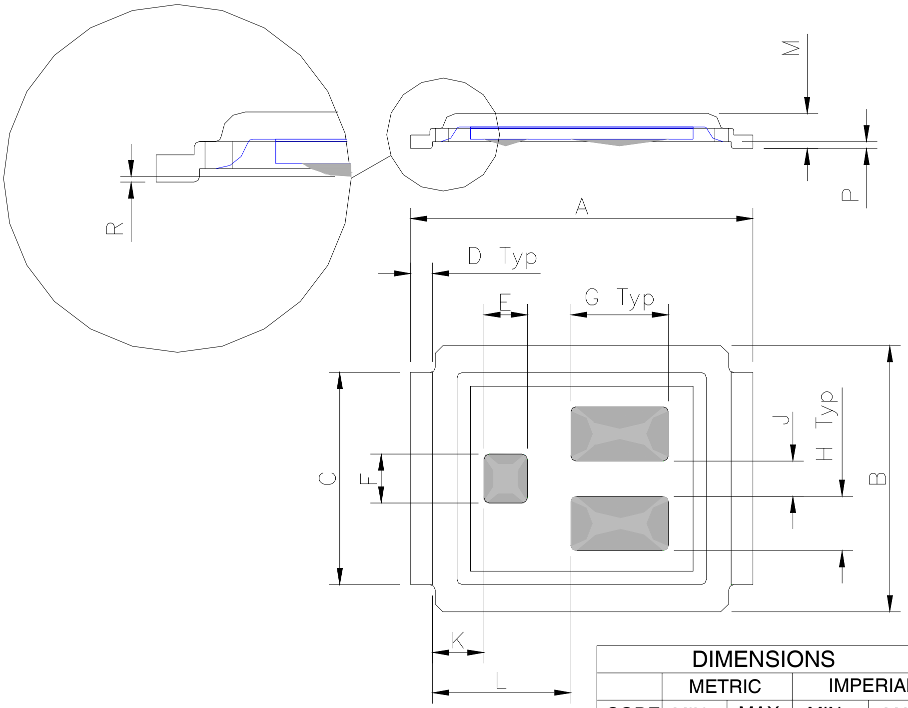
This includes all recommendations for stencil and substrate designs.





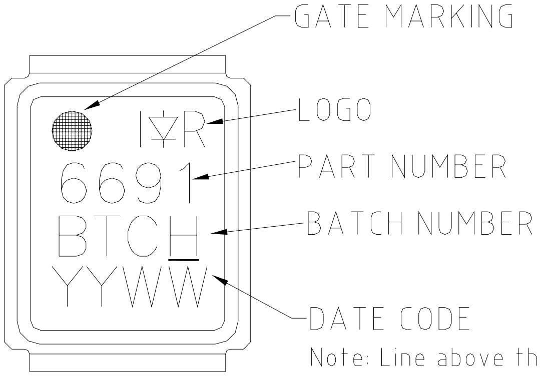
DirectFET™ Outline Dimension, MT Outline (Medium Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



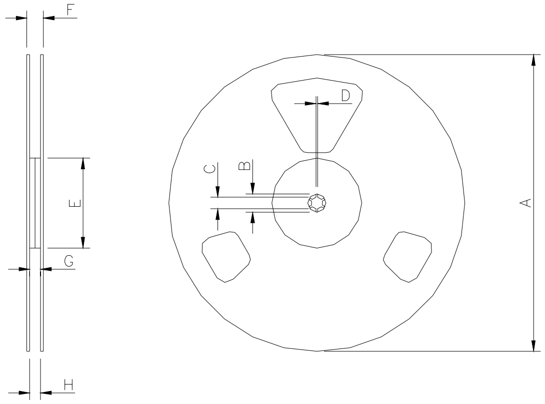
DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.78	0.82	0.031	0.032
F	0.88	0.92	0.035	0.036
G	1.78	1.82	0.070	0.072
H	0.98	1.02	0.039	0.040
J	0.63	0.67	0.025	0.026
K	0.88	1.01	0.035	0.039
L	2.46	2.63	0.097	0.104
M	0.616	0.676	0.0235	0.0274
R	0.020	0.080	0.0008	0.0031
P	0.08	0.17	0.003	0.007

DirectFET™ Part Marking



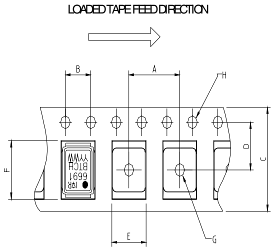
Note: Line above the last character of the date-code indicates "Lead-Free".

DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6691TRPBF). For 1000 parts on 7" reel, order IRF6691TR1PBF

REEL DIMENSIONS								
	STANDARD OPTION **(QTY 4800)**				TR1 OPTION **(QTY 1000)**			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C



NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

International Rectifier

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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/