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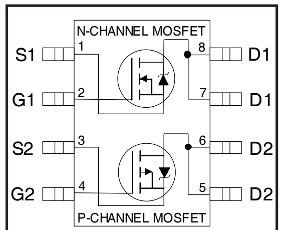
PD - 96102B

International
IOR Rectifier

IRF7105QPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- 150°C Operating Temperature
- Lead-Free

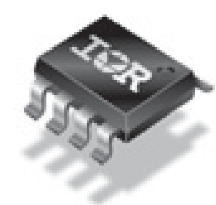


Top View

	N-Ch	P-Ch
V_{DSS}	25V	-25V
$R_{DS(on)}$	0.10Ω	0.25Ω
I_D	3.5A	-2.3A

Description

These HEXFET® Power MOSFET's in a Dual SO-8 package utilize the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of these HEXFET Power MOSFET's are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.
The efficient SO-8 package provides enhanced thermal characteristics and dual MOSFET die capability making it ideal in a variety of power applications. This dual, surface mount SO-8 can dramatically reduce board space and is also available in Tape & Reel.



SO-8

Base part number	Orderable part number	Package Type	Standard Pack		EOL Notice	Replacement Part Number
			Form	Quantity		
IRF7105QPbF	IRF7105QTRPbF	SO-8	Tape and Reel	4000	EOL 527	Please search the EOL part number on IR's website for guidance
	IRF7105QPbF	SO-8	Tube	95	EOL 529	

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	3.5	-2.3	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	2.8	-1.8	
I_{DM}	Pulsed Drain Current ①	14	-10	
P_D @T_C = 25°C	Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	3.0	-3.0	V/nS
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	——	——	62.5	°C/W

05/20/14

END OF LIFE

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	25	—	—	V	V_{GS} = 0V, I_D = 250μA
		P-Ch	-25	—	—		V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.030	—	V/°C	Reference to 25°C, I_D = 1mA
		P-Ch	—	-0.015	—		Reference to 25°C, I_D = -1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	0.083	0.10	Ω	V_{GS} = 10V, I_D = 1.0A ③
			—	0.14	0.16		V_{GS} = 4.5V, I_D = 0.50A ③
		P-Ch	—	0.16	0.25		V_{GS} = -10V, I_D = -1.0A ③
			—	0.30	0.40		V_{GS} = -4.5V, I_D = -0.50A ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	3.0	V	V_{DS} = V_{GS}, I_D = 250μA
		P-Ch	-1.0	—	-3.0		V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	N-Ch	—	4.3	—	S	V_{DS} = 15V, I_D = 3.5A ③
		P-Ch	—	3.1	—		V_{DS} = -15V, I_D = -3.5A ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	2.0	μA	V_{DS} = 20V, V_{GS} = 0V
		P-Ch	—	—	-2.0		V_{DS} = -20V, V_{GS} = 0V,
		N-Ch	—	—	25		V_{DS} = 20V, V_{GS} = 0V, T_J = 55°C
		P-Ch	—	—	-25		V_{DS} = -20V, V_{GS} = 0V, T_J = 55°C
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	±100		V_{GS} = ± 20V
Q_g	Total GateCharge	N-Ch	—	9.4	27	nC	N-Channel
		P-Ch	—	10	25		I_D = 2.3A, V_{DS} = 12.5V, V_{GS} = 10V
Q_{gs}	Gate-to-Source Charge	N-Ch	—	1.7	—		③
		P-Ch	—	1.9	—		P-Channel
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	3.1	—		I_D = -2.3A, V_{DS} = -12.5V, V_{GS} = -10V
		P-Ch	—	2.8	—		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	7.0	20	ns	N-Channel
		P-Ch	—	12	40		V_{DD} = 25V, I_D = 1.0A, R_G = 6.0Ω,
t_r	Rise Time	N-Ch	—	9.0	20		R_D = 25Ω
		P-Ch	—	13	40		③
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	45	90		P-Channel
		P-Ch	—	45	90		V_{DD} = -25V, I_D = -1.0A, R_G = 6.0Ω,
t_f	Fall Time	N-Ch	—	25	50		R_D = 25Ω
		P-Ch	—	37	50		
L_D	Internal Drain Inductace	N-P	—	4.0	—	nH	Between lead , 6mm (0.25in.)from
L_S	Internal Source Inductance	N-P	—	6.0	—		package and center of die contact
C_{iss}	Input Capacitance	N-Ch	—	330	—	pF	N-Channel
		P-Ch	—	290	—		V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz
C_{oss}	Output Capacitance	N-Ch	—	250	—		
		P-Ch	—	210	—		P-Channel
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	61	—		V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz
		P-Ch	—	67	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	2.0	A	
		P-Ch	—	—	-2.0		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	14		
		P-Ch	—	—	-9.2		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.2	V	T_J = 25°C, I_S = 1.3A, V_{GS} = 0V ③
		P-Ch	—	—	-1.2		T_J = 25°C, I_S = -1.3A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	N-Ch	—	36	54	ns	N-Channel
		P-Ch	—	69	100		T_J = 25°C, I_F = 1.3A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	N-Ch	—	41	75	nC	P-Channel ③
		P-Ch	—	90	180		T_J = 25°C, I_F = -1.3A, di/dt = 100A/μs
t_{on}	Forward Turn-On Time	N-P	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② N-Channel $I_{SD} \le$ 3.5A, di/dt ≤ 90A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C
P-Channel $I_{SD} \le$ -2.3A, di/dt ≤ 90A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t ≤ 10sec.

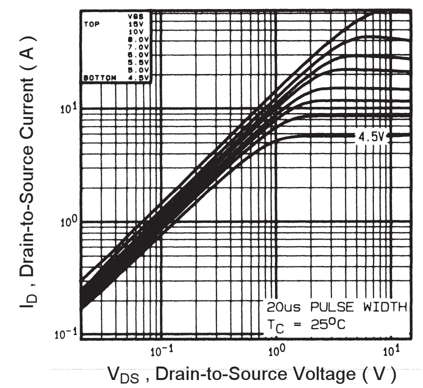


Fig 1. Typical Output Characteristics

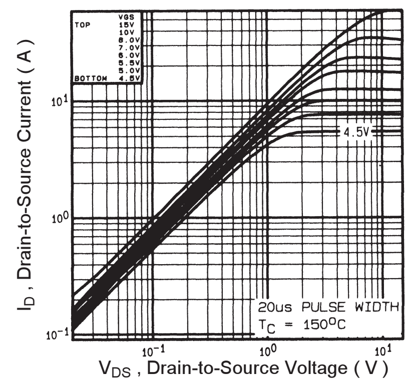


Fig 2. Typical Output Characteristics

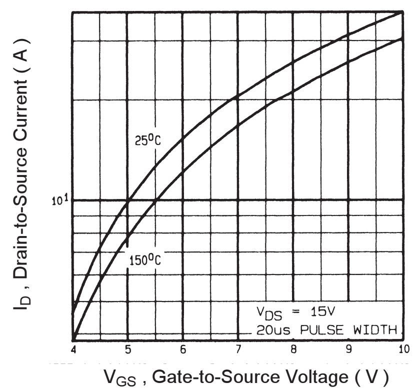


Fig 3. Typical Transfer Characteristics

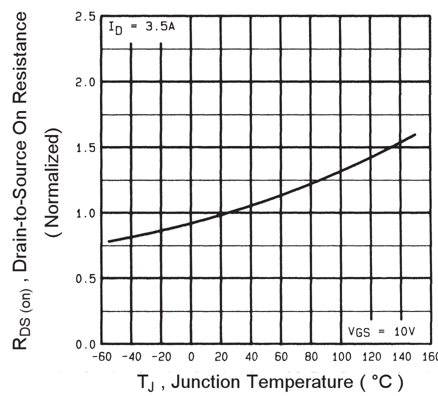


Fig 4. Normalized On-Resistance Vs. Temperature

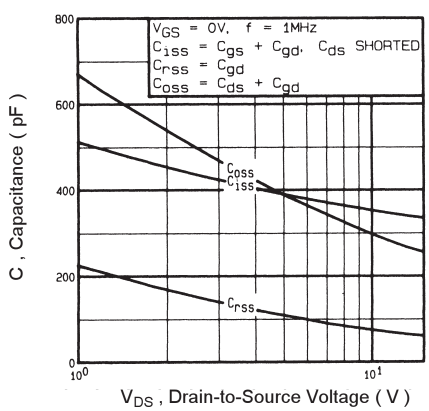


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

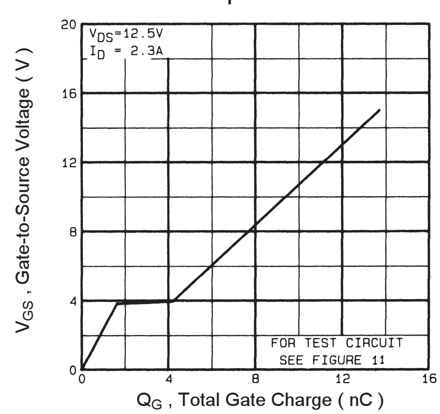


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

N-Channel

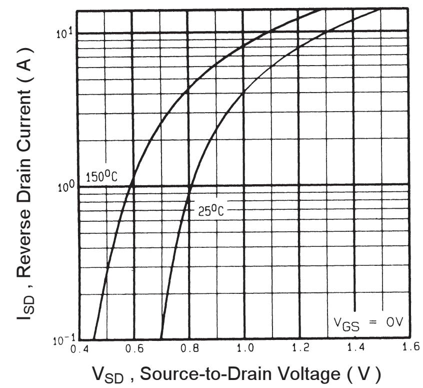


Fig 7. Typical Source-Drain Diode Forward Voltage

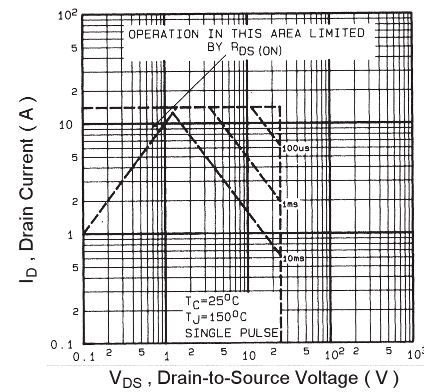


Fig 8. Maximum Safe Operating Area

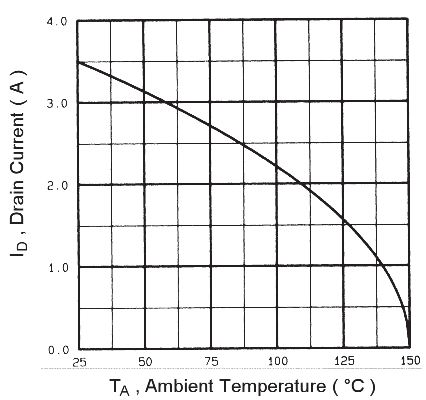


Fig 9. Maximum Drain Current Vs. Ambient Temperature

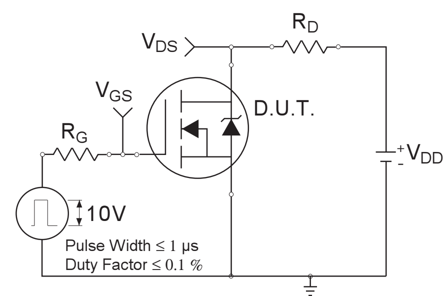


Fig 10a. Switching Time Test Circuit

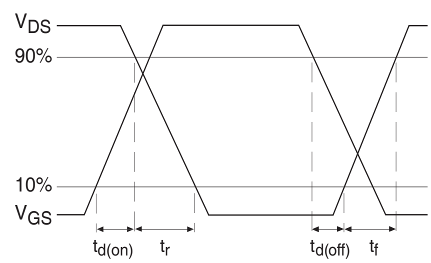


Fig 10b. Switching Time Waveforms

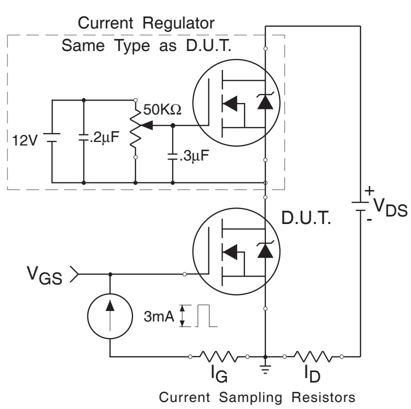


Fig 11a. Gate Charge Test Circuit

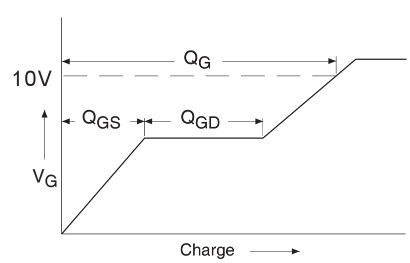


Fig 11b. Basic Gate Charge Waveform

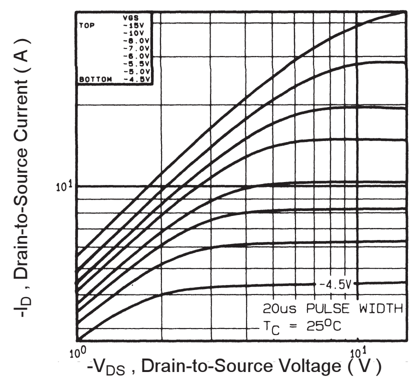


Fig 12. Typical Output Characteristics

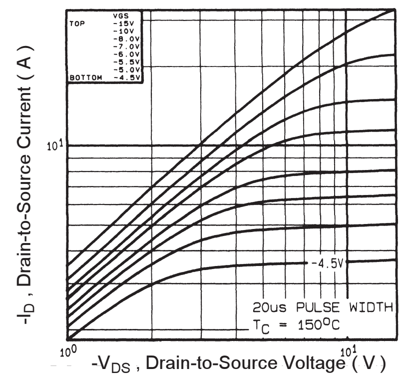


Fig 13. Typical Output Characteristics

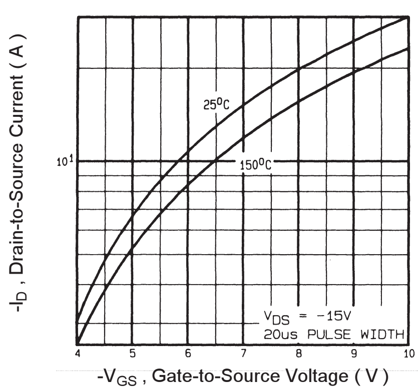


Fig 14. Typical Transfer Characteristics

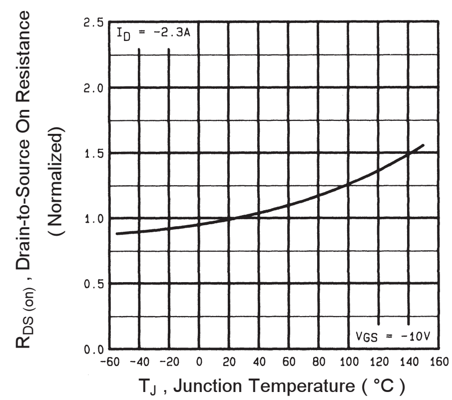


Fig 15. Normalized On-Resistance Vs. Temperature

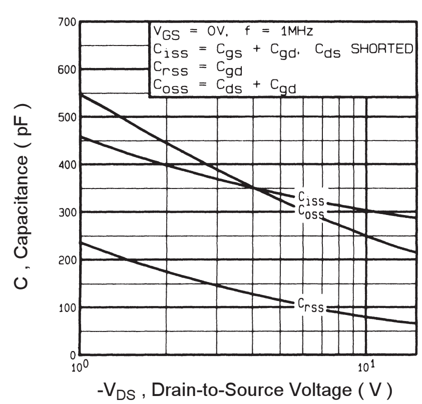


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

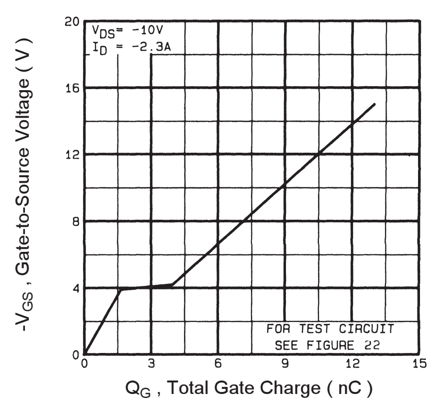


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

P-Channel

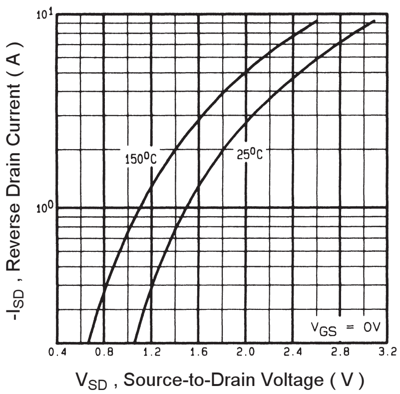


Fig 18. Typical Source-Drain Diode Forward Voltage

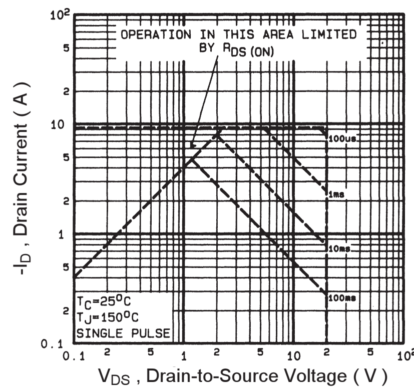


Fig 19. Maximum Safe Operating Area

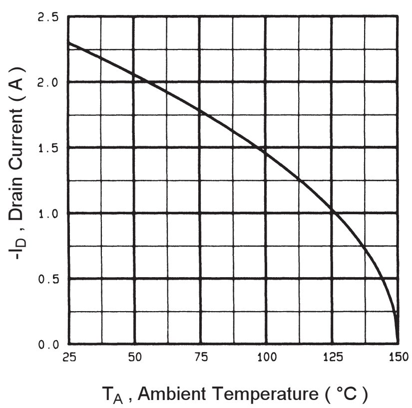


Fig 20. Maximum Drain Current Vs. Ambient Temperature

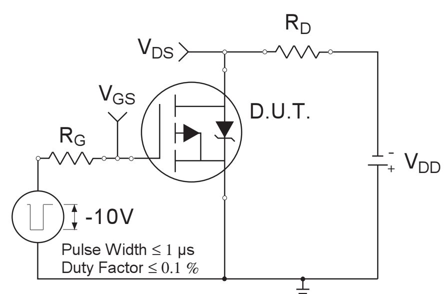


Fig 21a. Switching Time Test Circuit

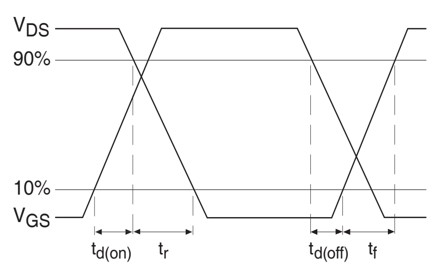


Fig 21b. Switching Time Waveforms

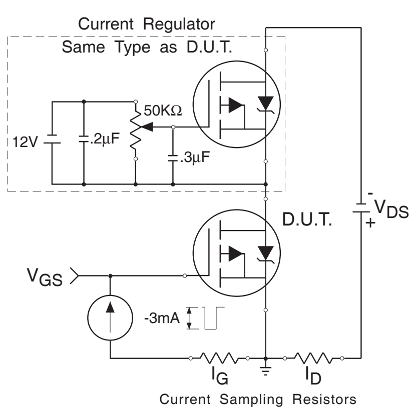


Fig 22a. Gate Charge Test Circuit

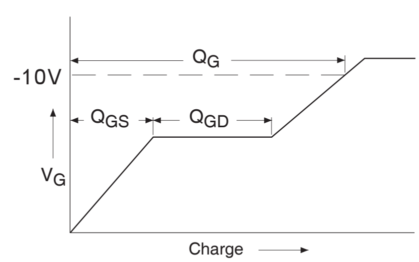


Fig 22b. Basic Gate Charge Waveform

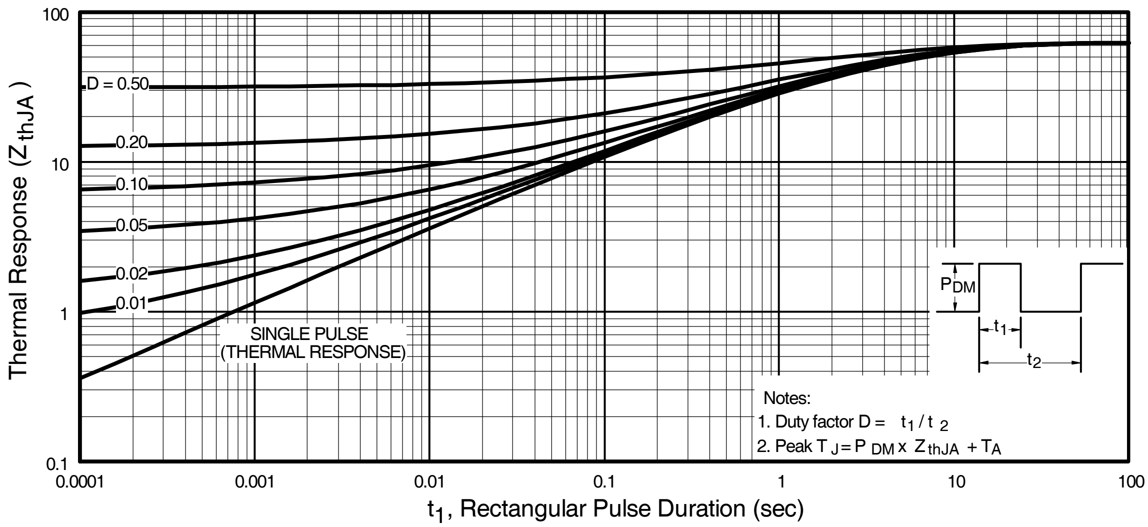


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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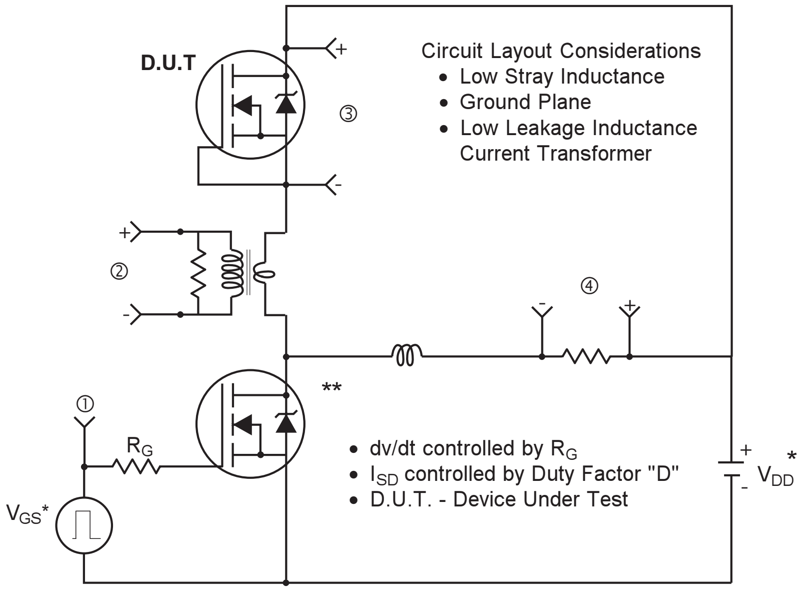
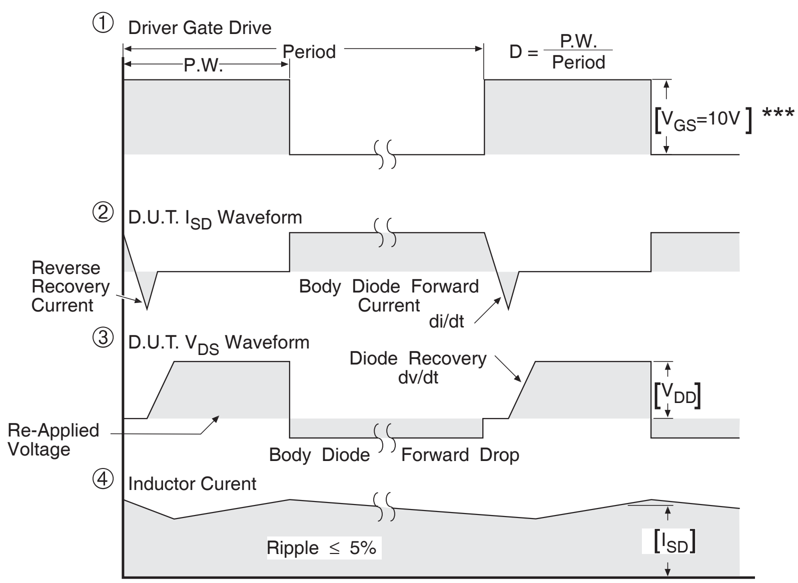
Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements

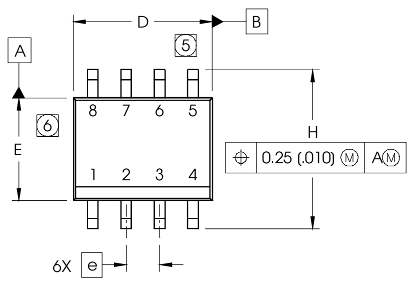


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

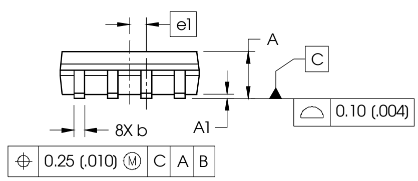
Fig 24. For N and P Channel HEXFETS

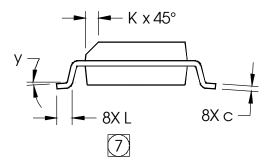
SO-8 Package Outline

Dimensions are shown in millimeters (inches)



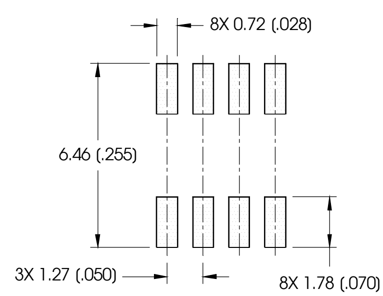
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°





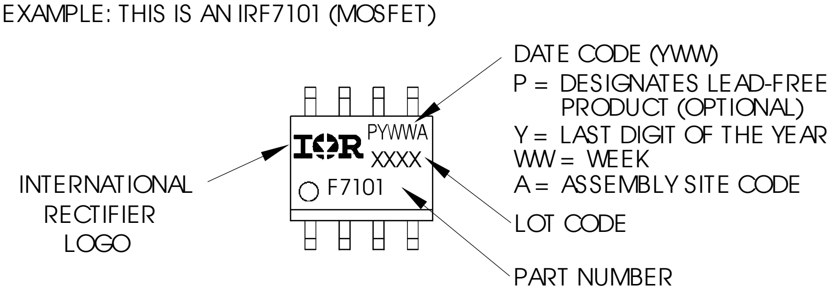
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)



Notes:

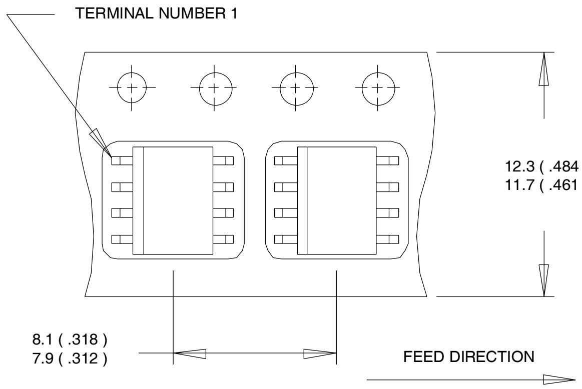
1. For an Automotive Qualified version of this part please see http://www.irf.com/product-info/auto/

2. For the most current drawing please refer to IR website at http://www.irf.com/package/

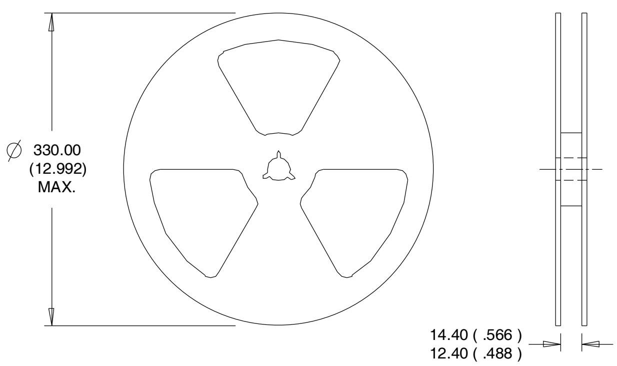
END OF LIFE

SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification level	Industrial †	
	(per JEDEC JESD47F†† guidelines)	
Moisture Sensitivity Level	SO-8	MSL1 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site
http://www.irf.com/product-info/reliability

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
5/8/2014	• Added ordering information to reflect the End-Of-life

International
IOR Rectifier

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